Updates on the strip front-end

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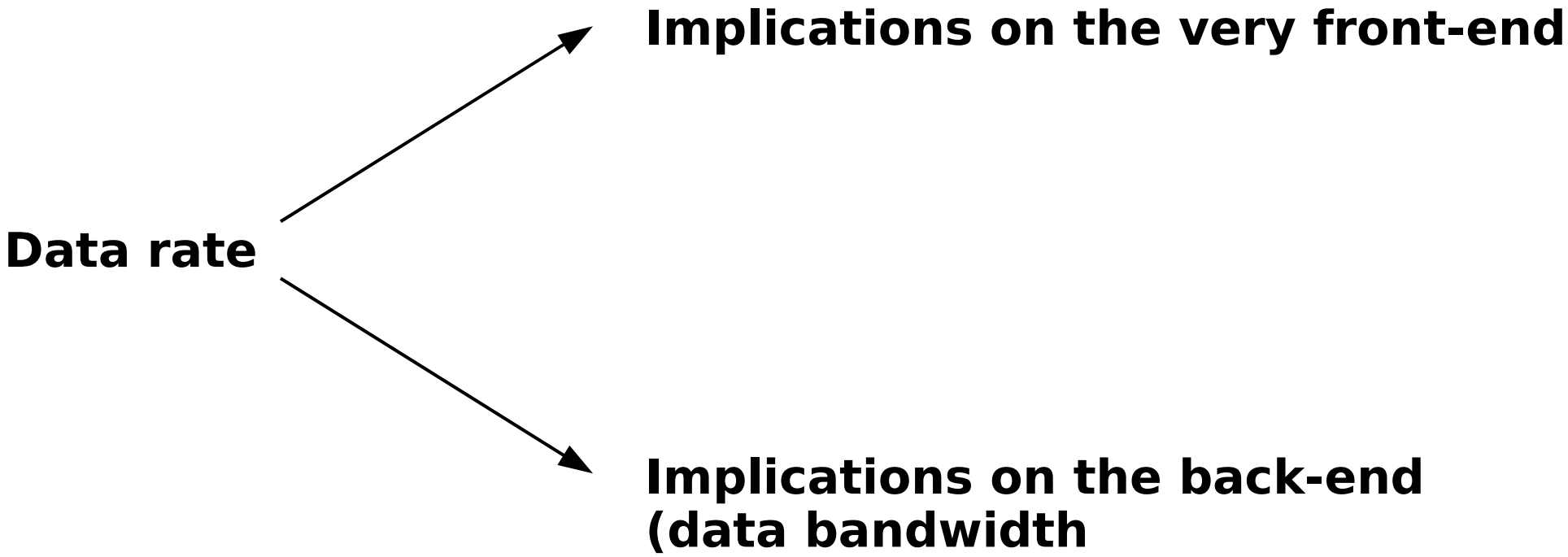
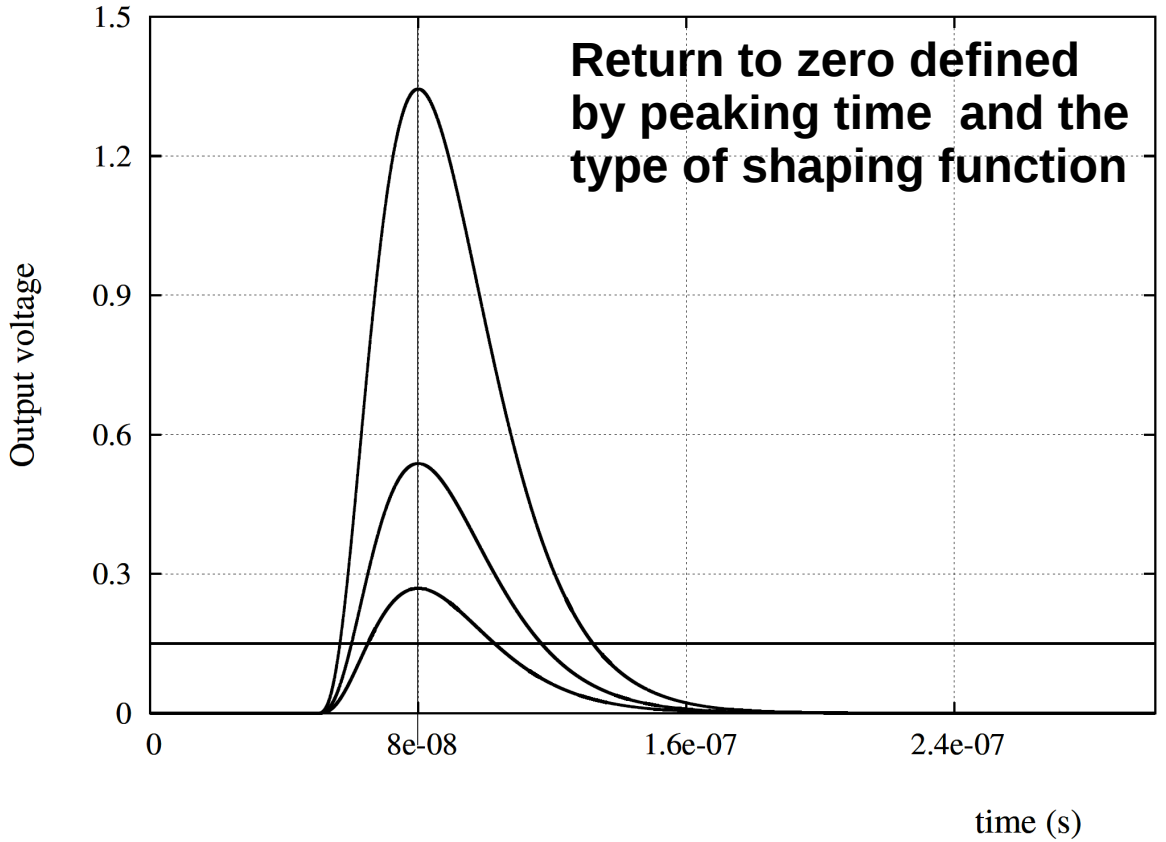
Specifications: rate

- Max rate per strip: 40~kHz (average of a Poisson distribution) .
- Max average distance between events: 25 us.



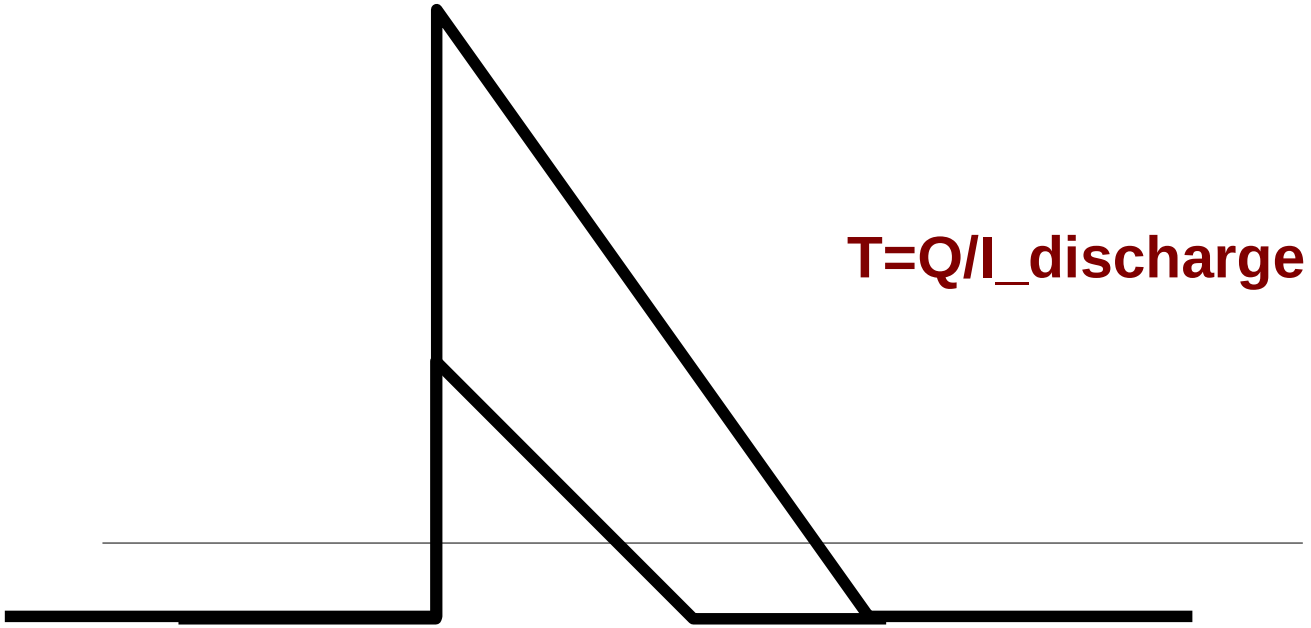
Rate impact on the front-end

- **Max average distance between events: 25 us.**
- **Average pulse duration in the front-end for 0.5% pile-up probability: 125 ns.**
  - **For CR-RC-like linear signal processing: all hits have the same duration regardless of the amplitude.**



Rate impact on the front-end

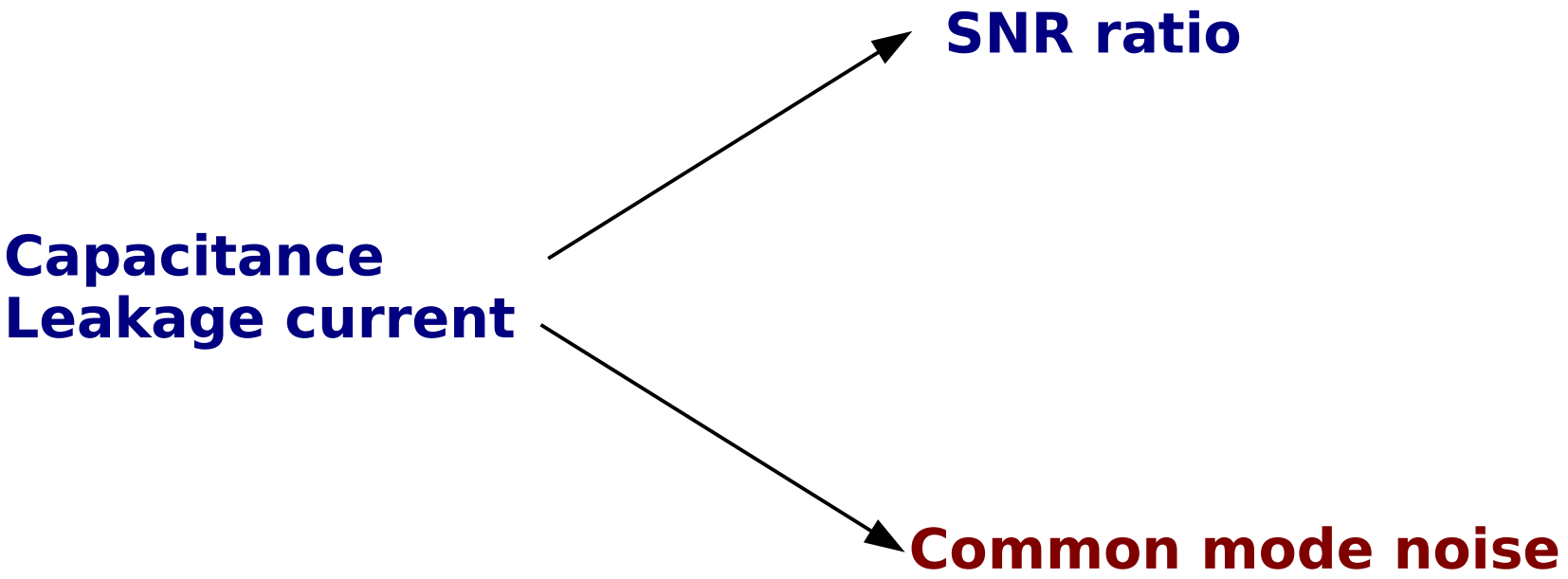
- Max average distance between events: 25 us.
- Average pulse duration in the front-end for 0.5% pile-up probability: 125 ns.
  - For ToT-like signal processing: correlation between amplitude and signal duration.



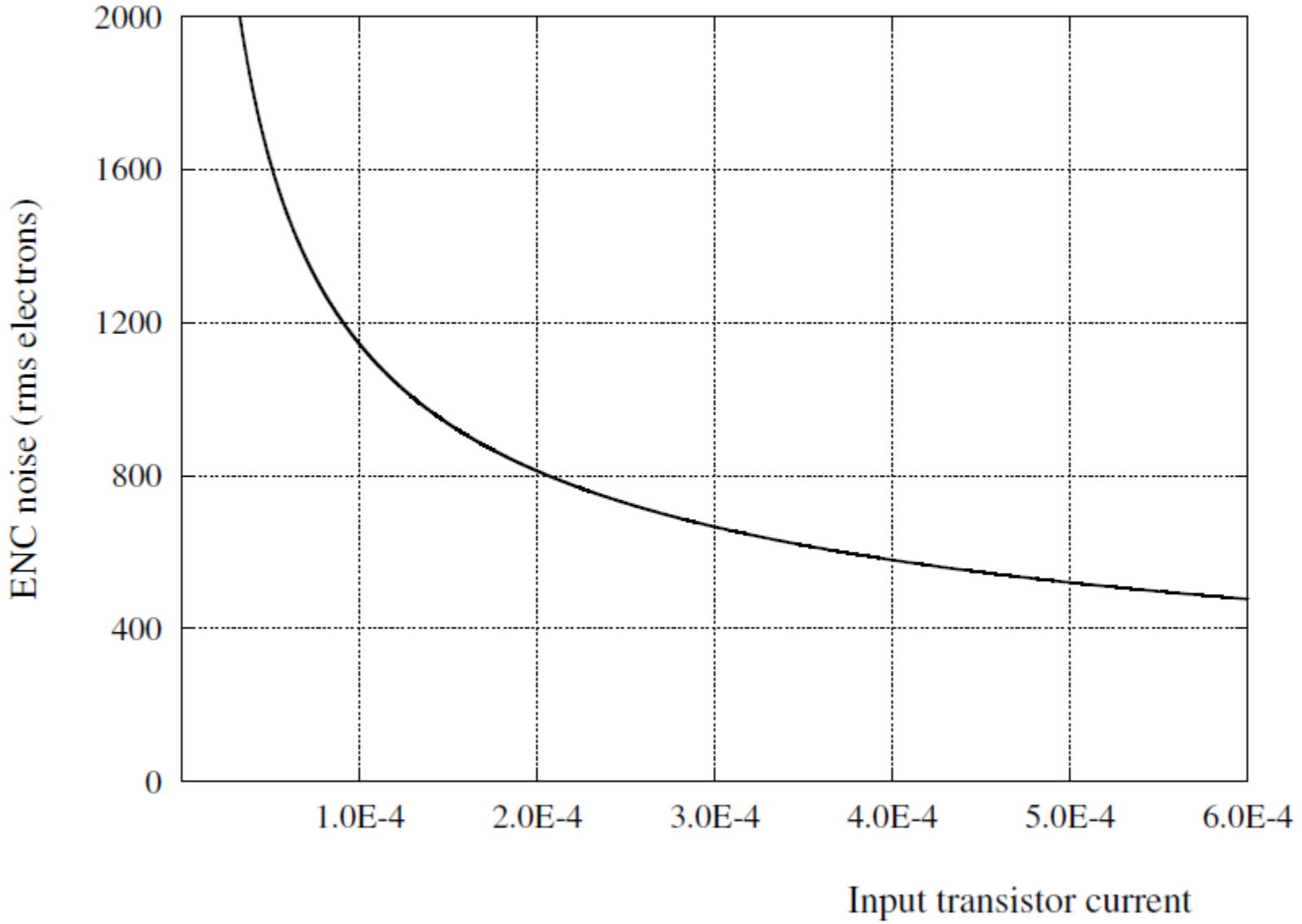
Important to reconsider the charge distribution. Long charges can be tolerated easily if they occur rarely.

Strip capacitance

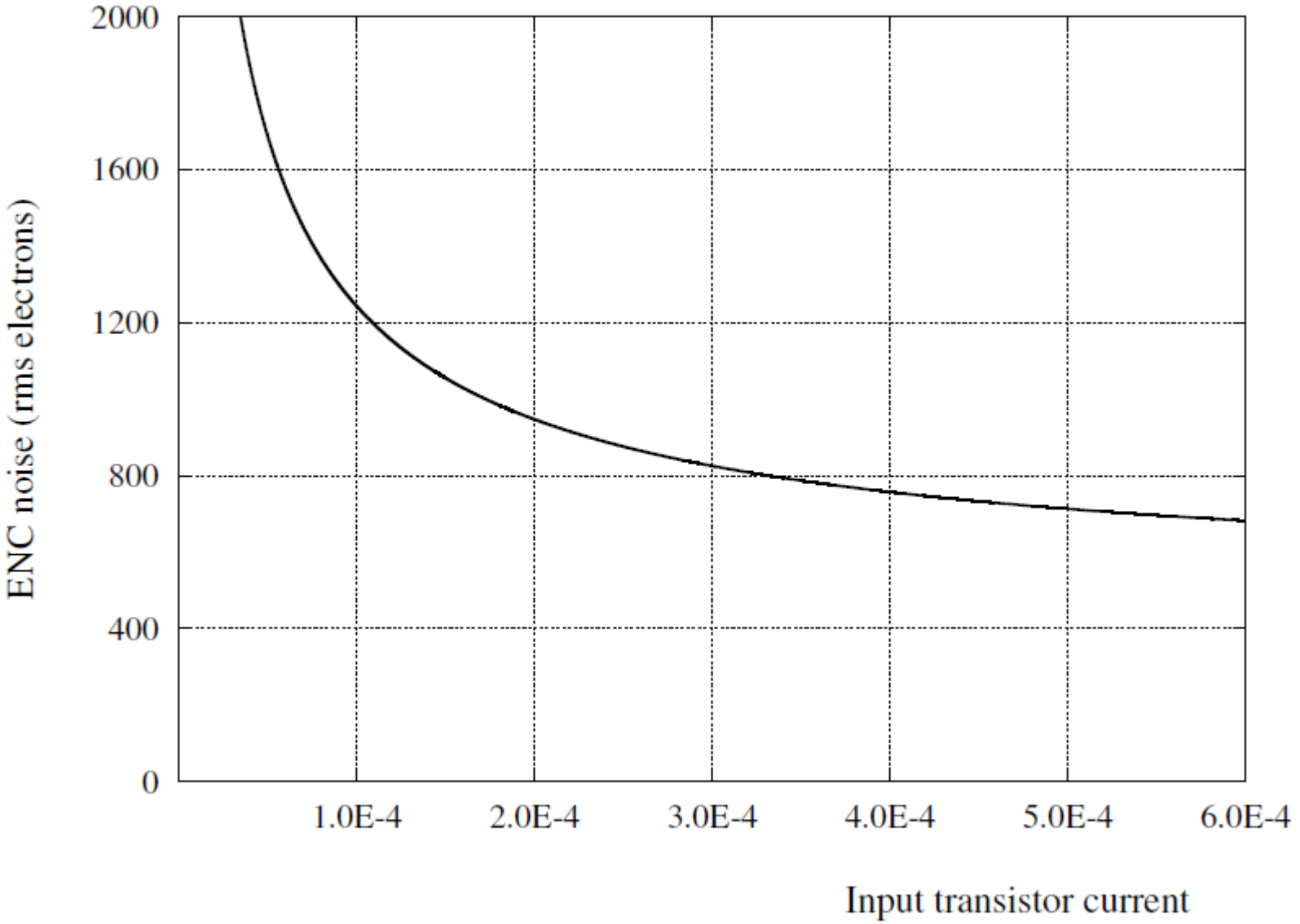
- Barrel strips: sensor capacitance 10 pF (50 pF with ganging)
- Disk strip: sensor capacitance: 20 pF
- Leakage at the detector end-life?



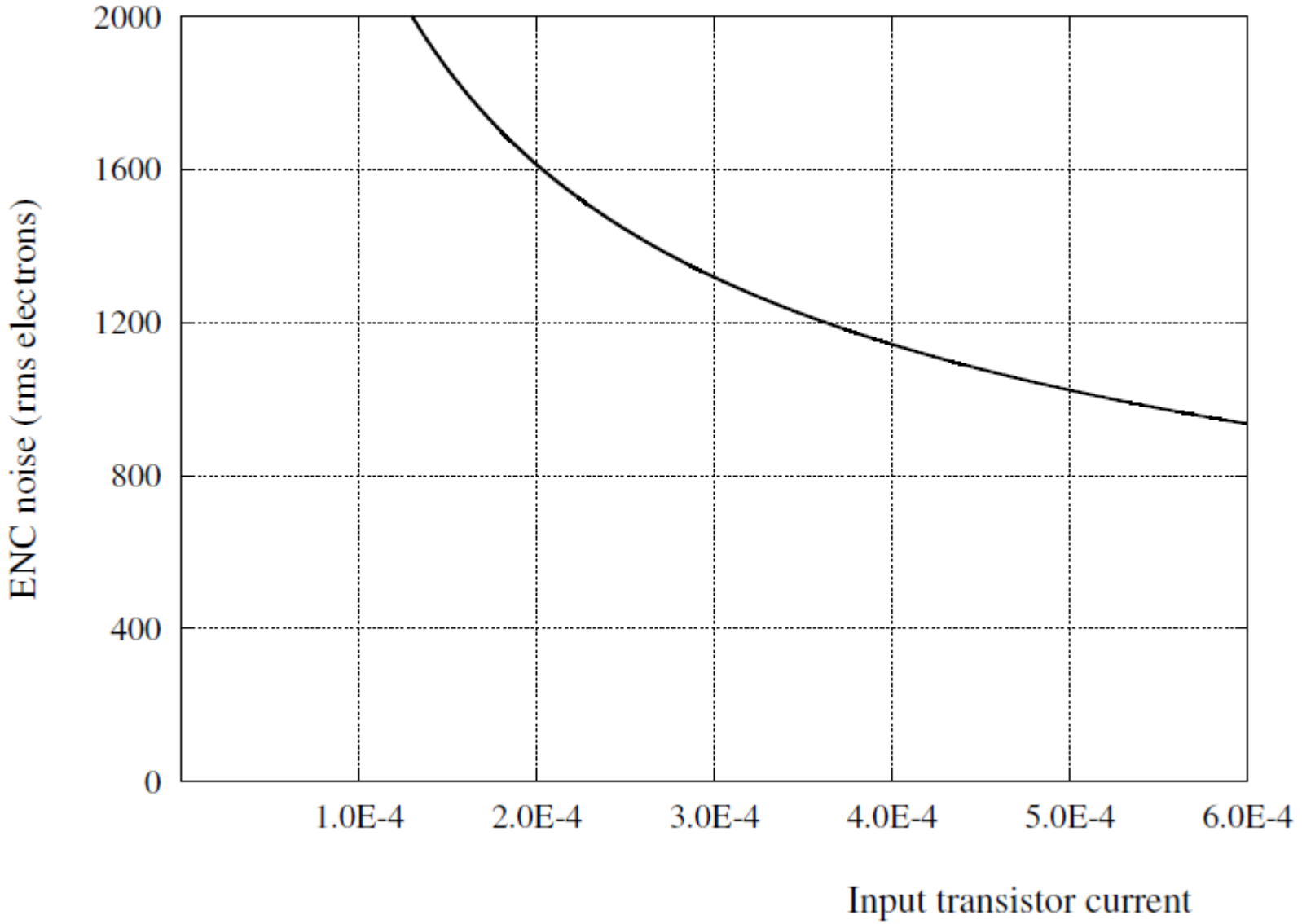
Noise@10pF 50nA



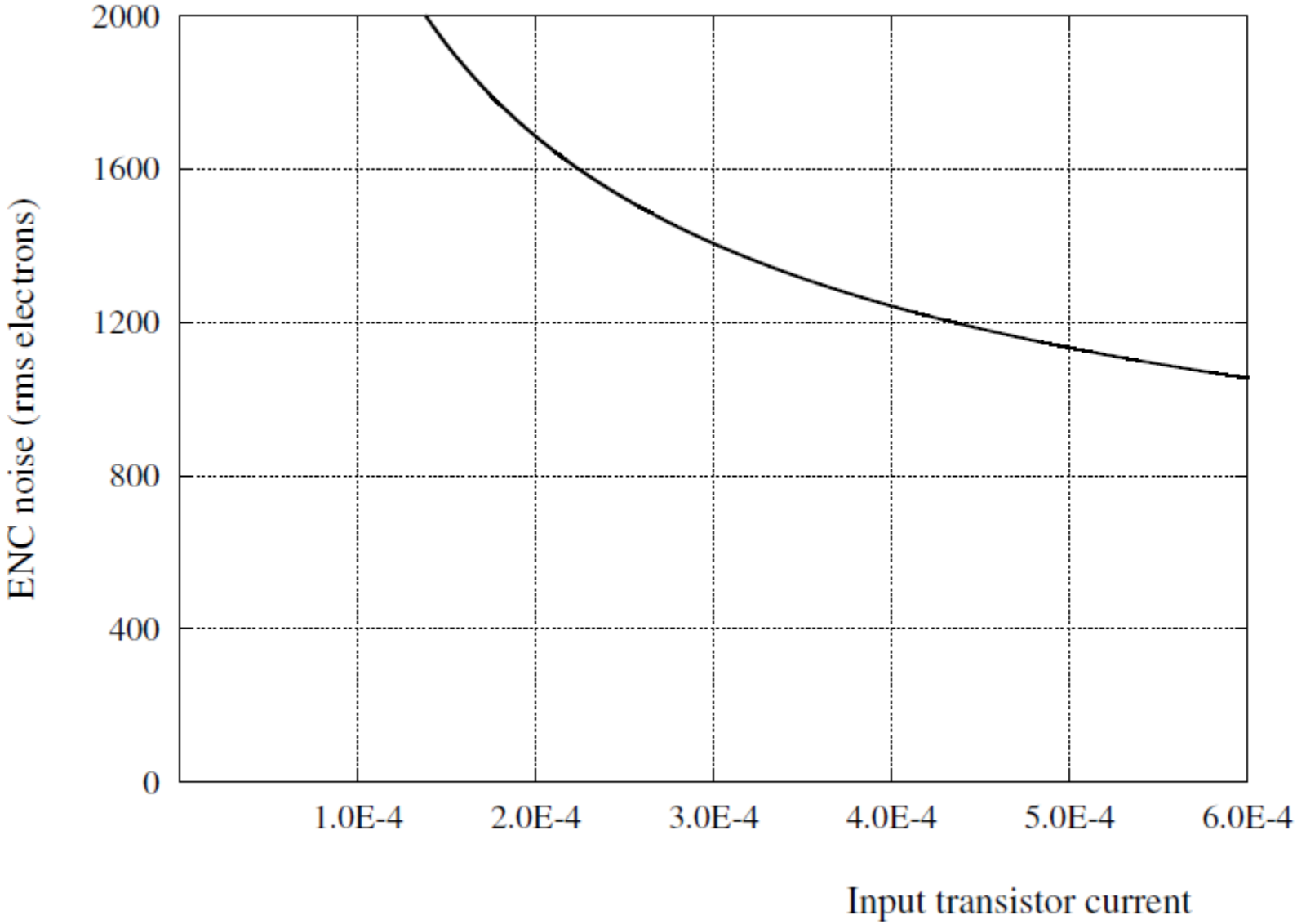
Noise@10pF 1uA



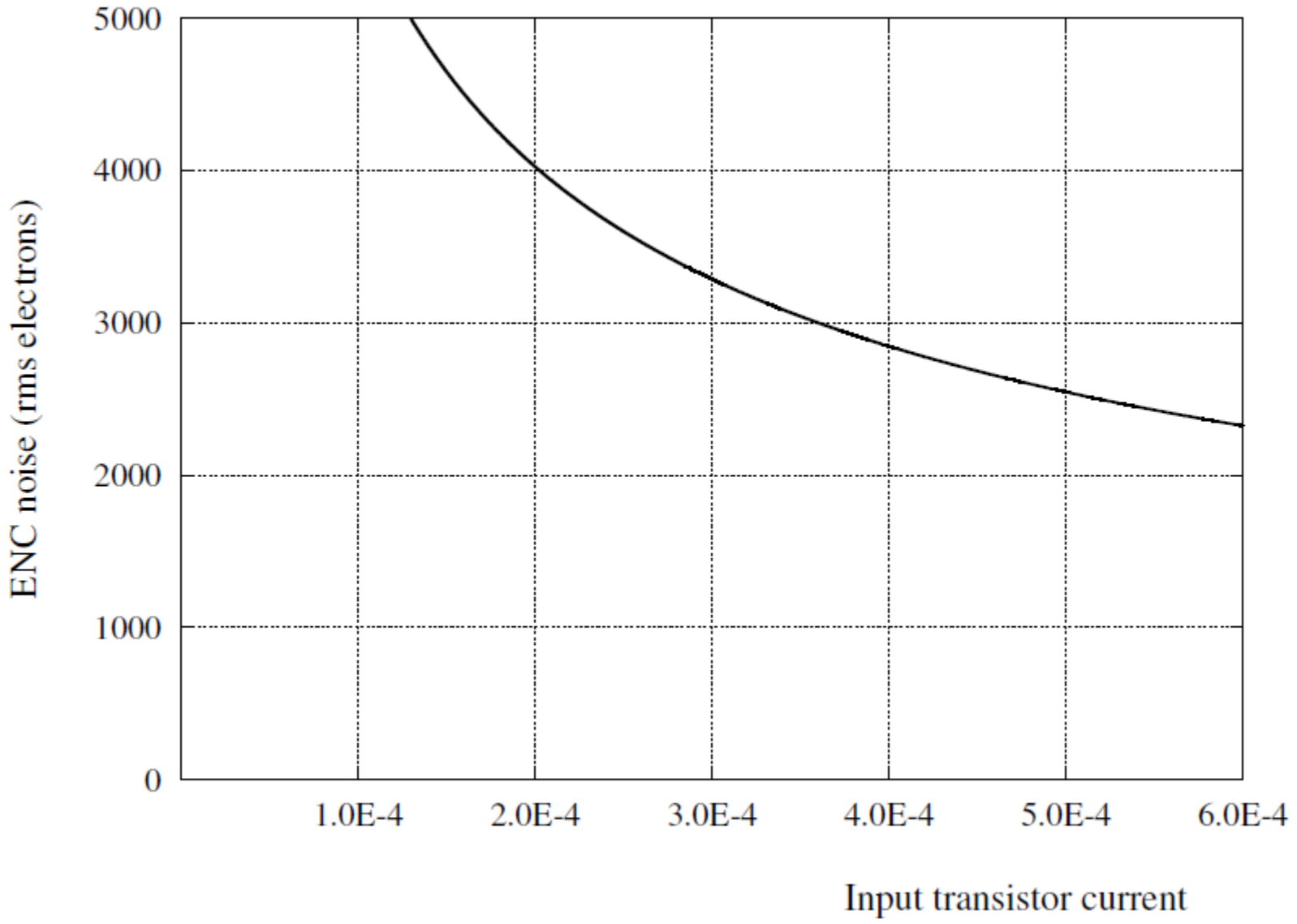
Noise@20pF 50nA



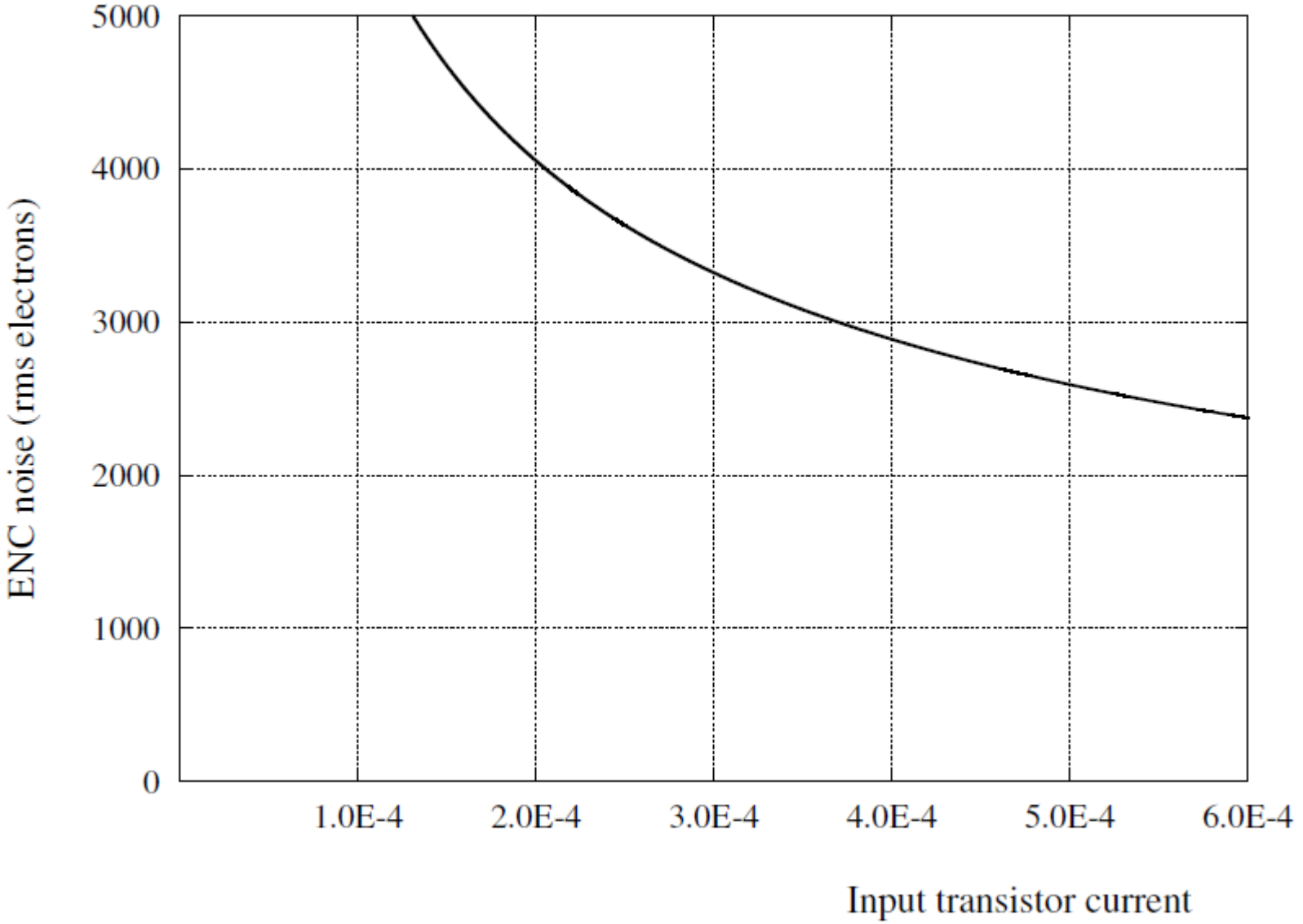
Noise@20pF 1uA



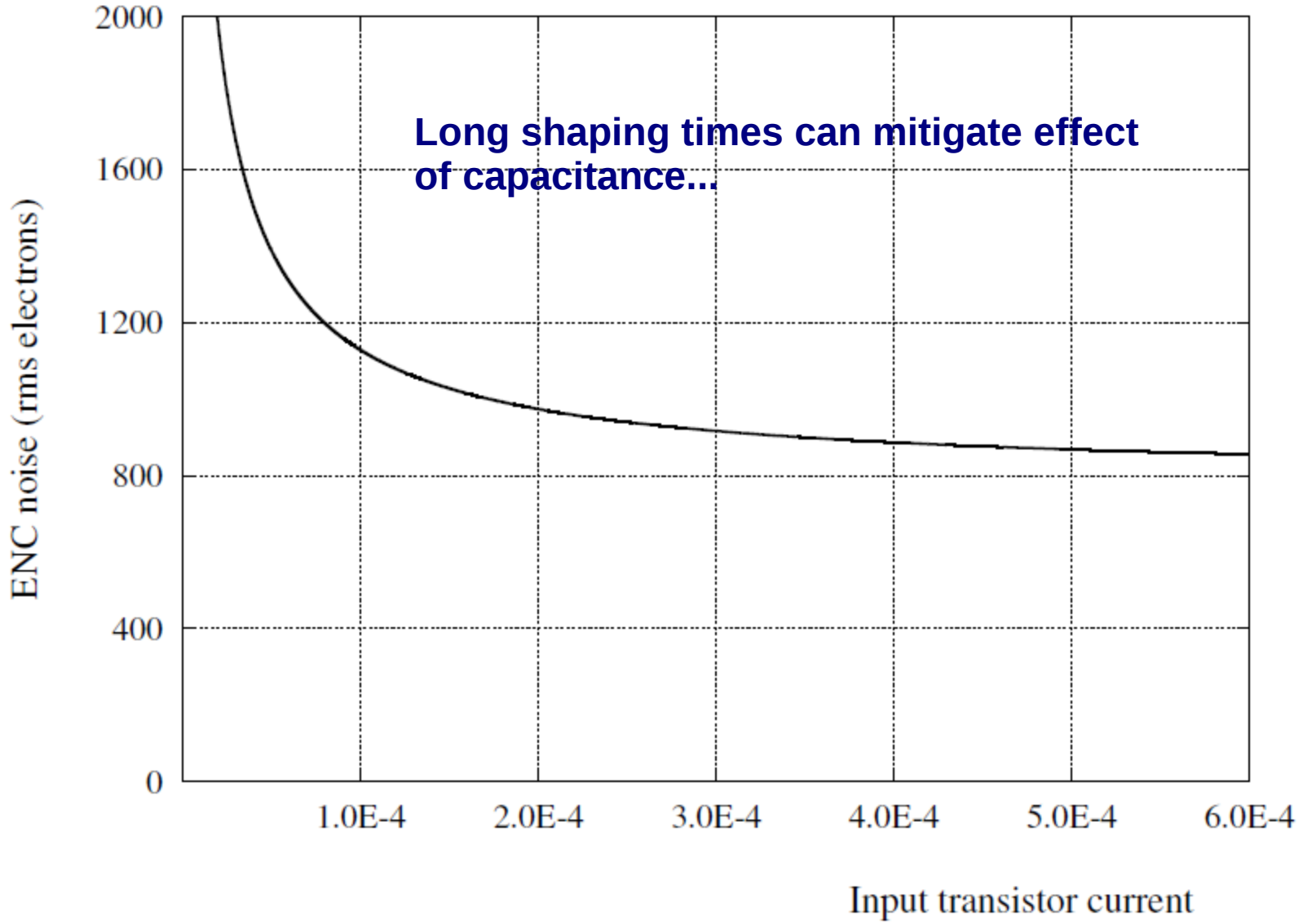
Noise@50pF 50nA



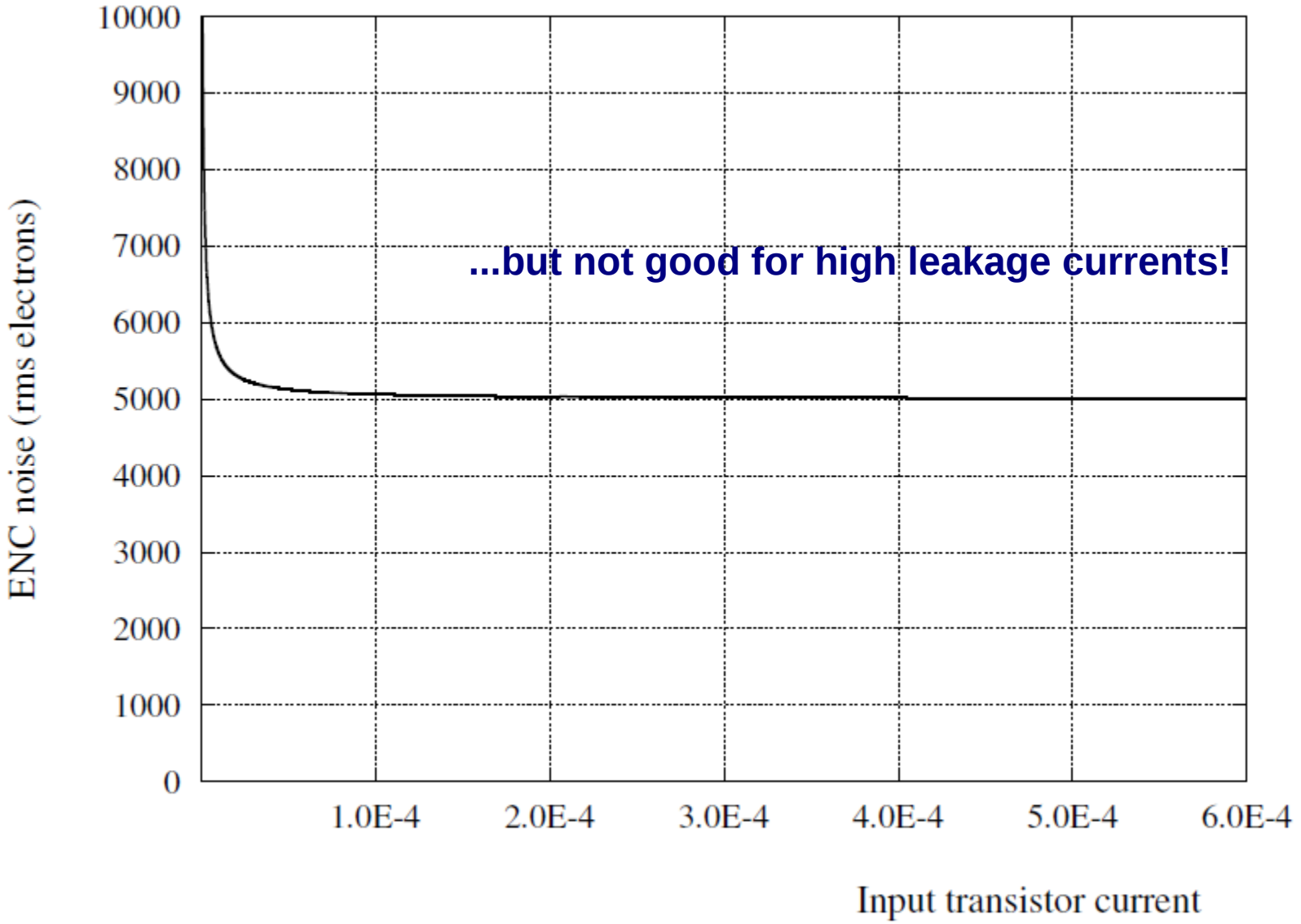
Noise@50pF 1uA



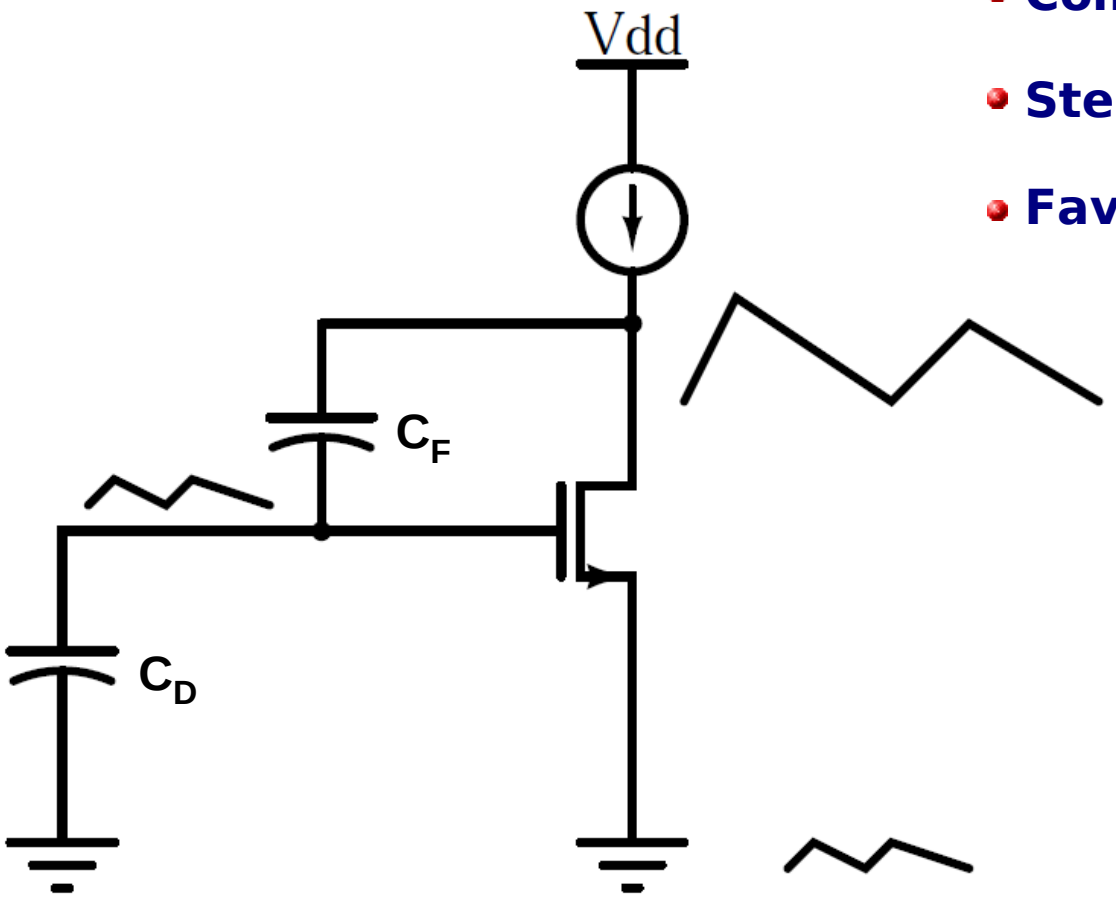
Noise@50pF 1us, 50 nA



Noise@50pF 1us, 2 uA



A word on common mode



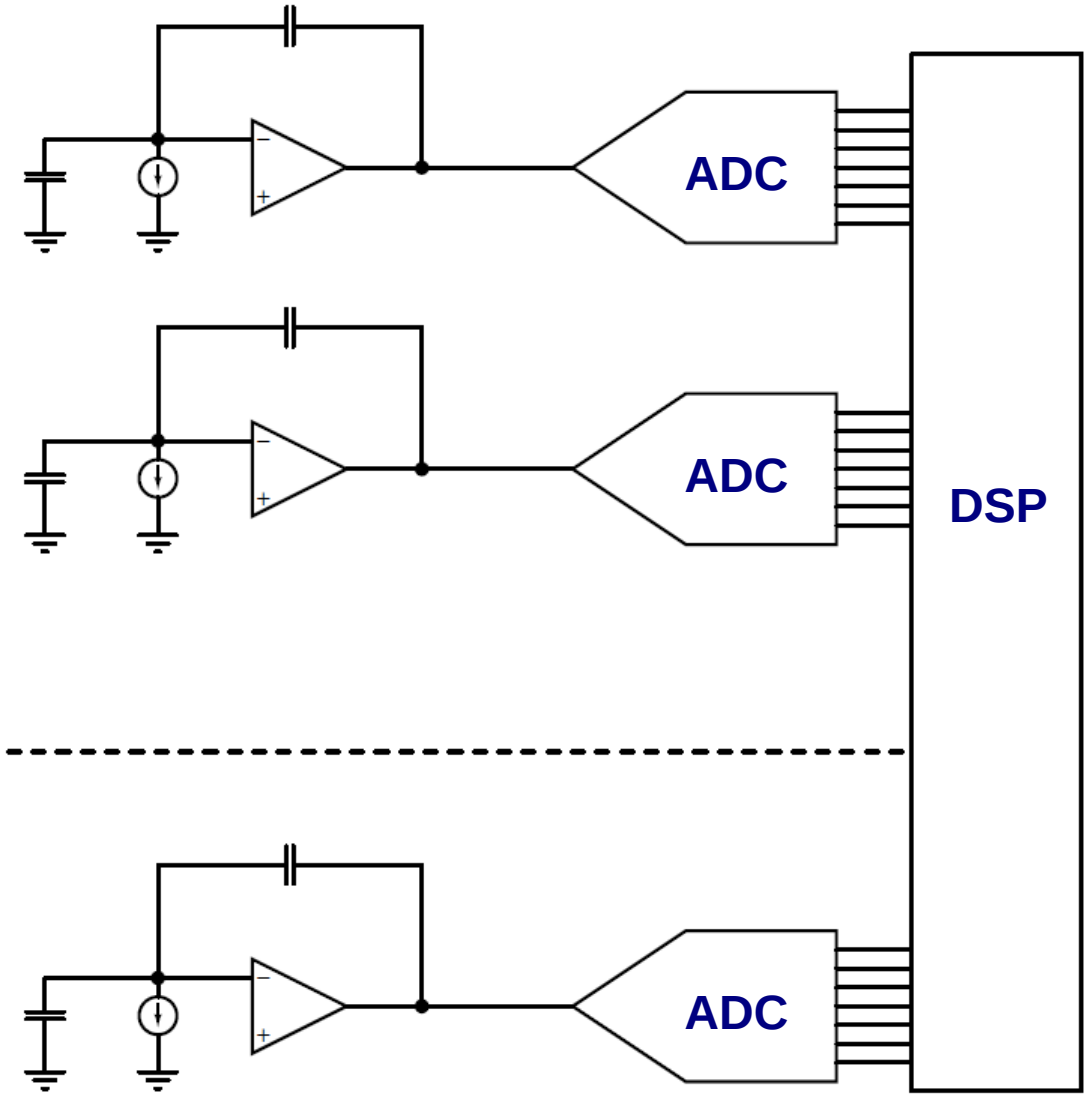
- **Common mode is a system issue.**
- **Stems from poor decoupling.**
- **Favored by large C_D/C_F ratios**

Architecture considerations

Before starting the design phase we need to be convinced of what we are doing….

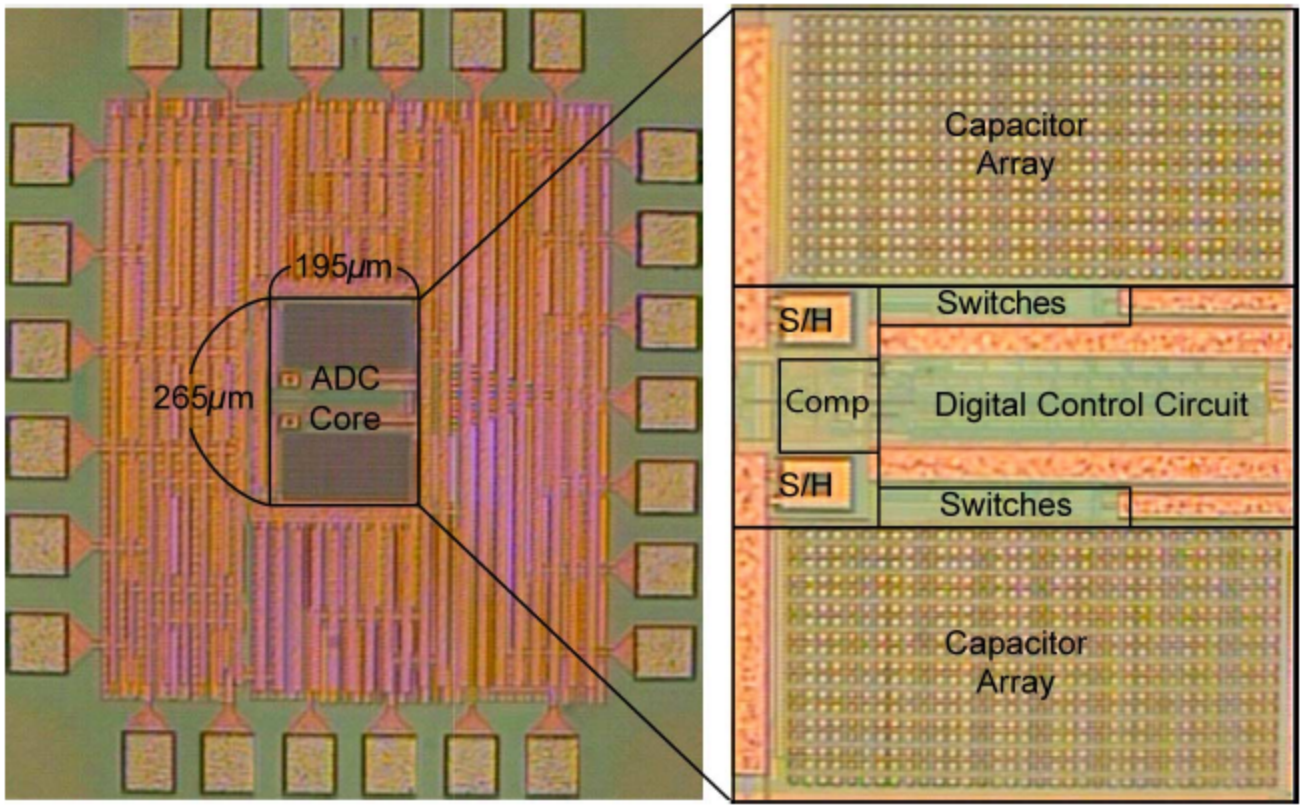
- **Full sampling**
- **ToT based**

Full sampling



- Retains the maximum information
- Allows for common mode correction
- Everything must be started from scratch.
- DSP power to be understood.
- SEE protected logic is cumbersome

ADC today



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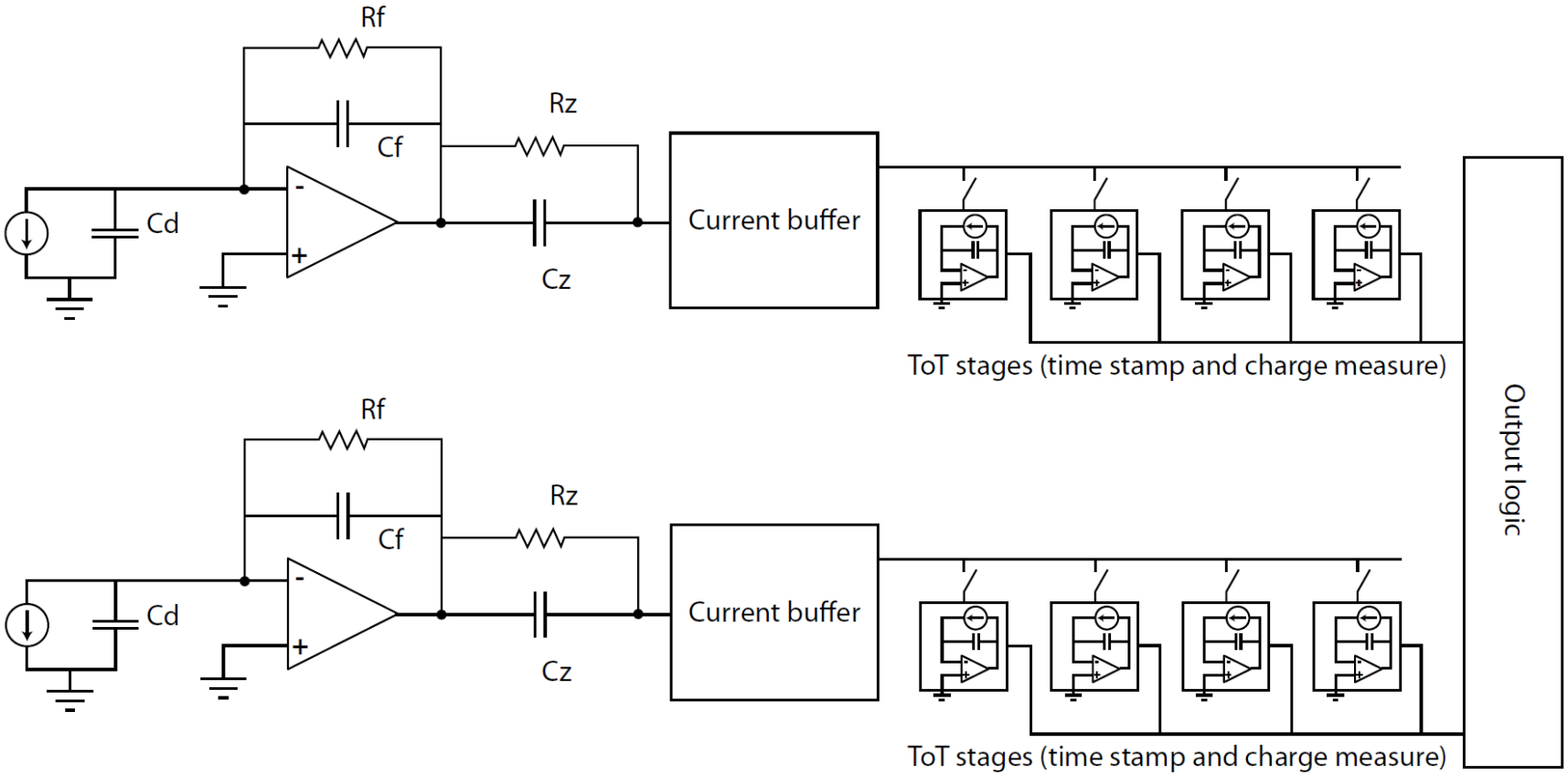
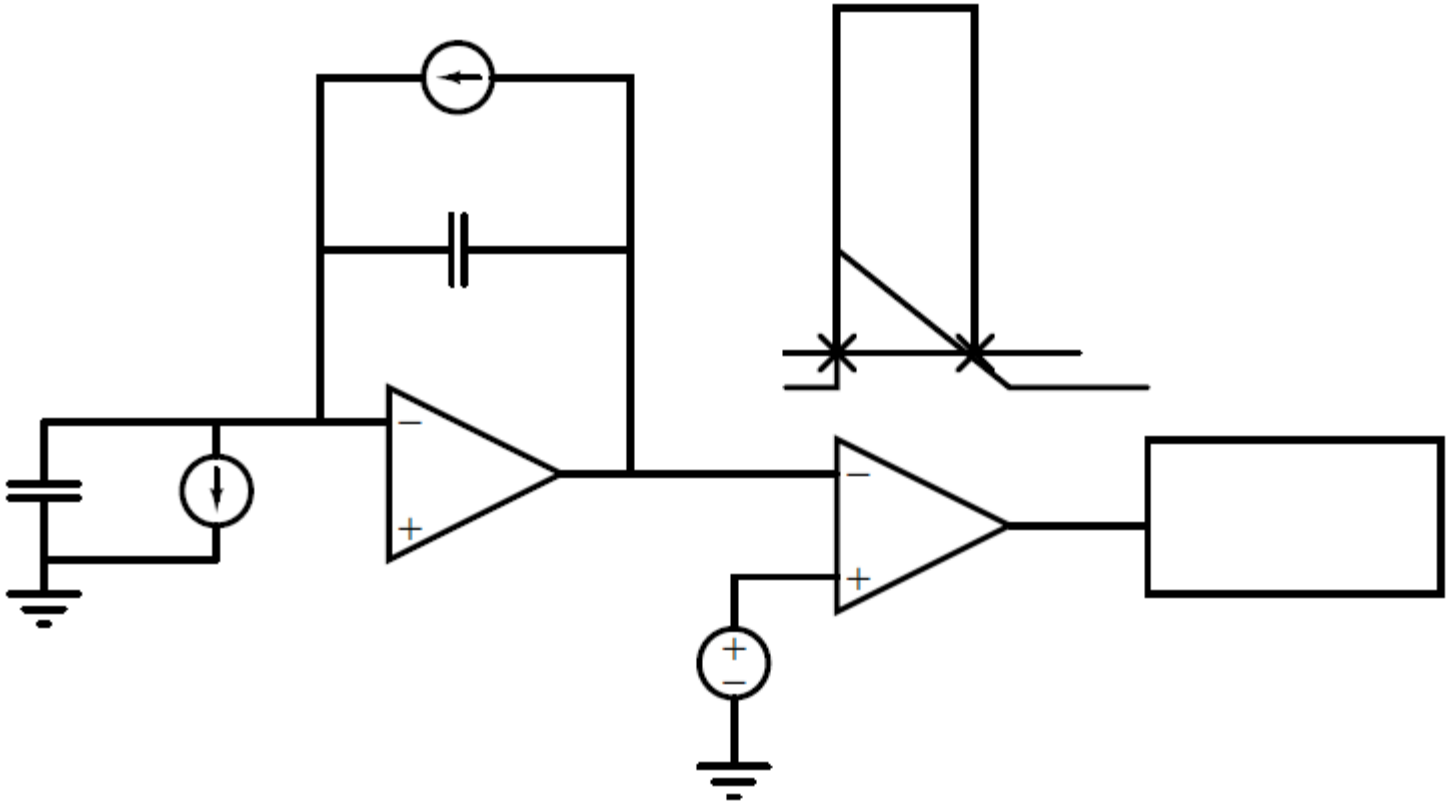
10 bit, 50 Msamples, 0.9 mW in 0.13 um CMOS

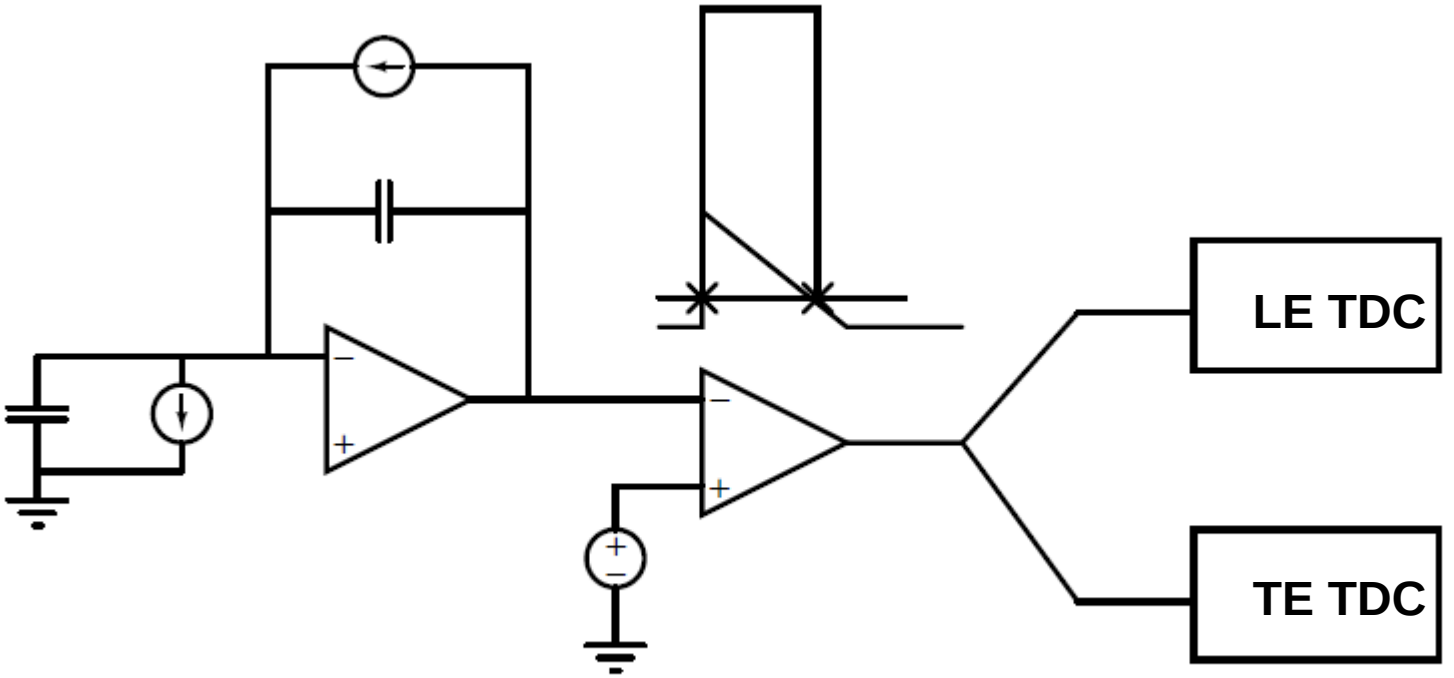
ToT-based readout



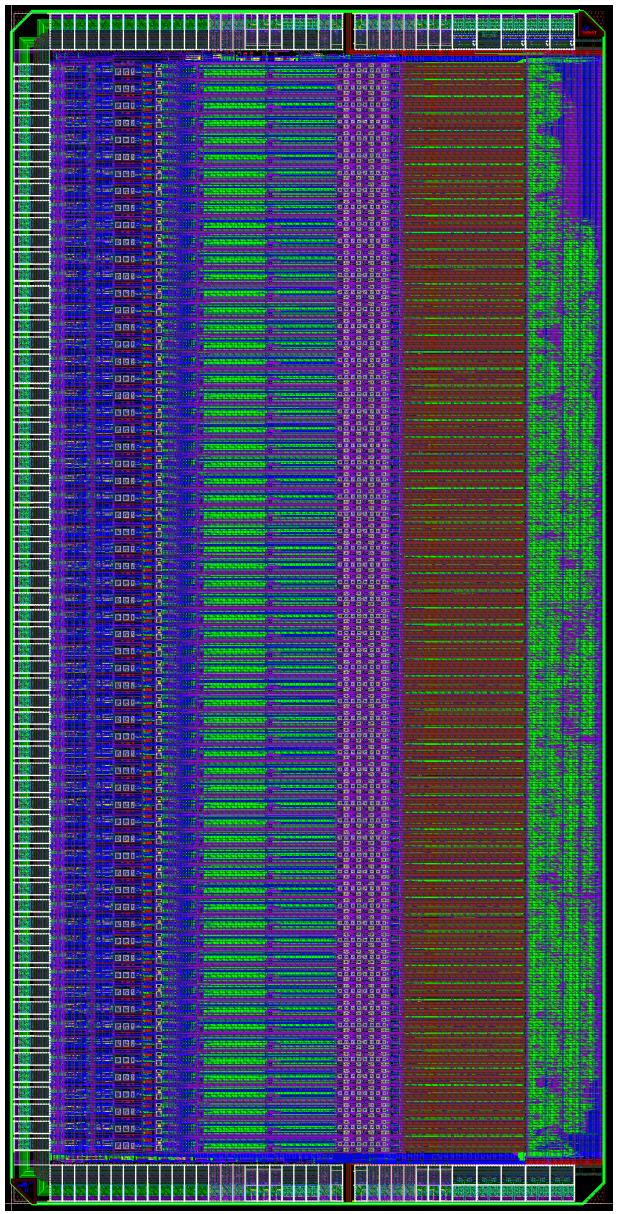
Time-based readout (1)



Time-based readout (2)



Starting point



ASIC develop in Torino and LIP (Lisbon) by people supported by a medical physics project (EndoTOF/US)

64 channels for time based readout of silicon PM
ToT done by measuring directly the duration
of the pulse shape of a fast amplifier with high resolution TDC (50-100 ps binning)

Good point: The chip is using TDC with analog interpolators
Analog interpolator=Wilkinson ADC. Very similar problem with efficiency=>Derandomization with 4 buffers

The logic controlling the buffer could be very similar, if not Identical to the one that we need.

ASIC already produced in an engineering run, expected back end of the year...

Starting from this would be the fastest approach

Front-end with fast ToT

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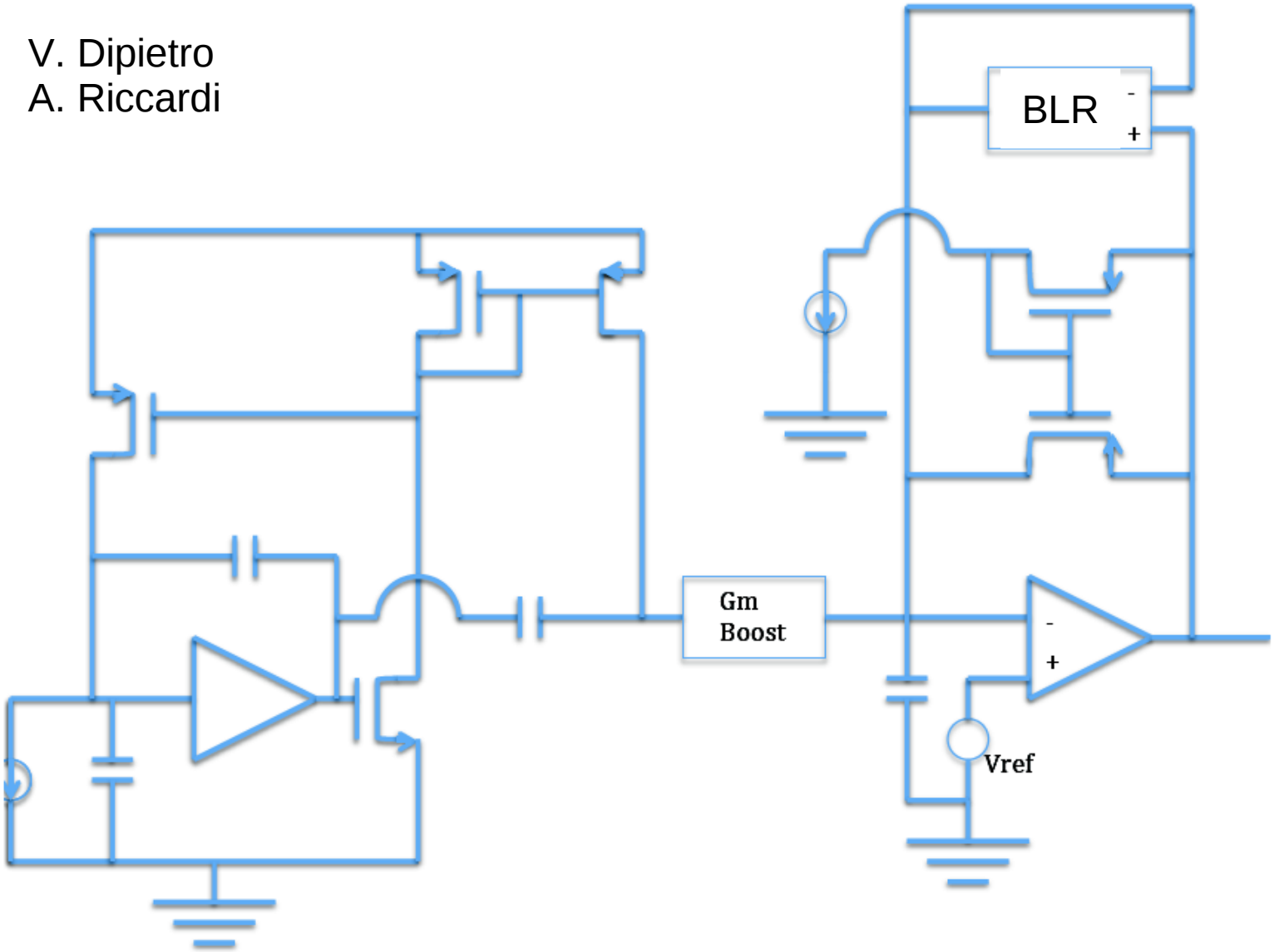
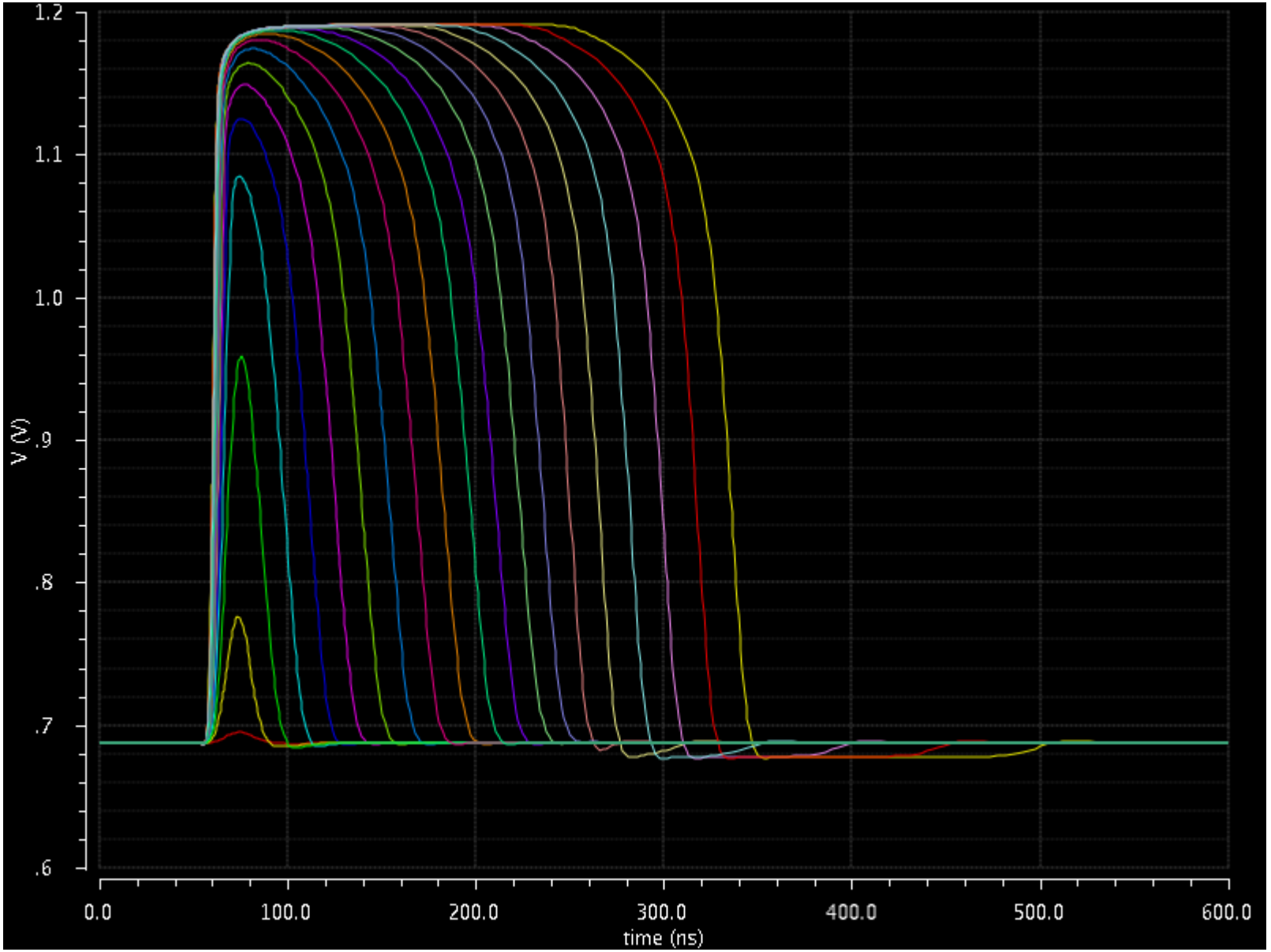
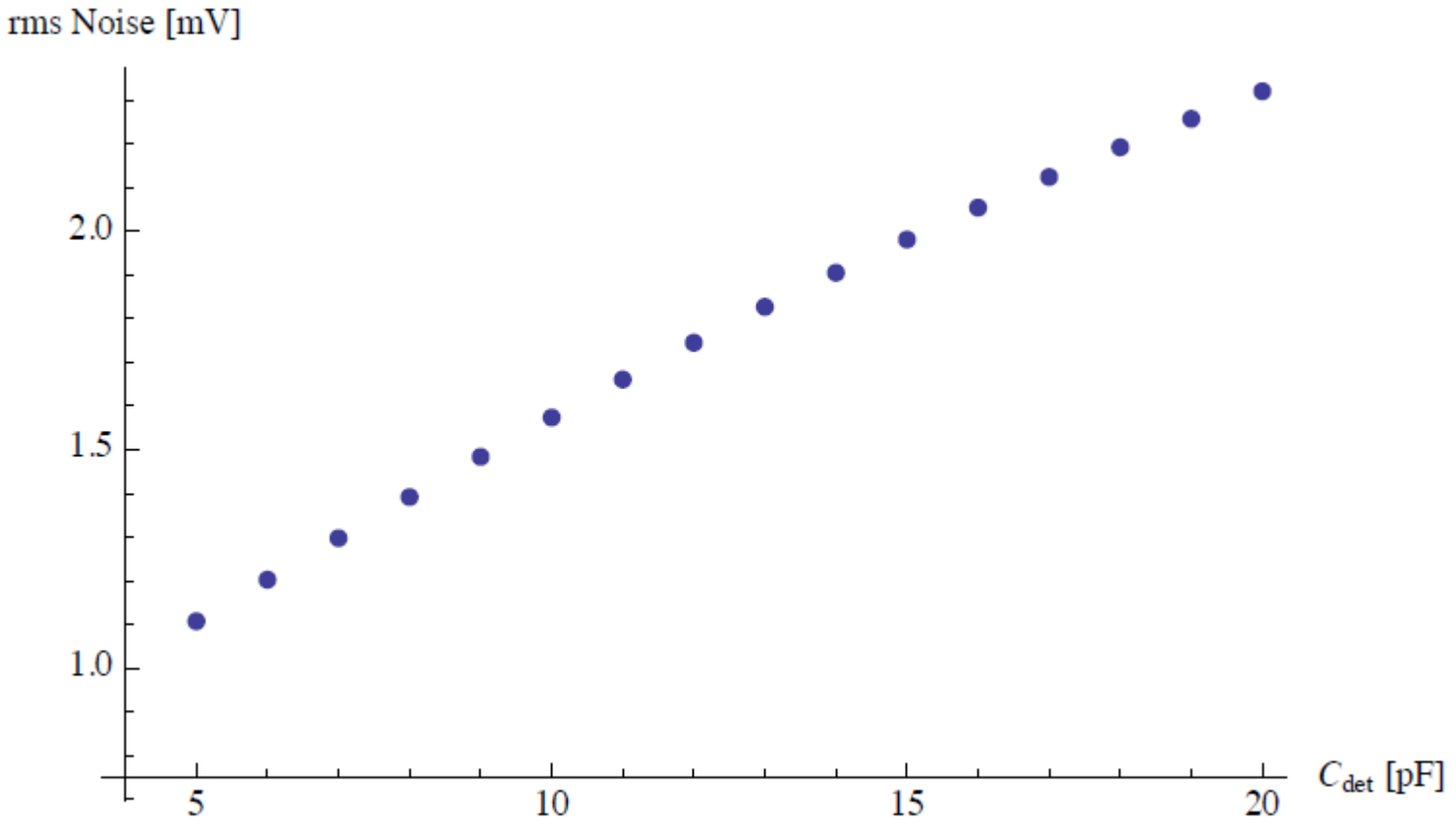
A. Riccardi



Example of output signal

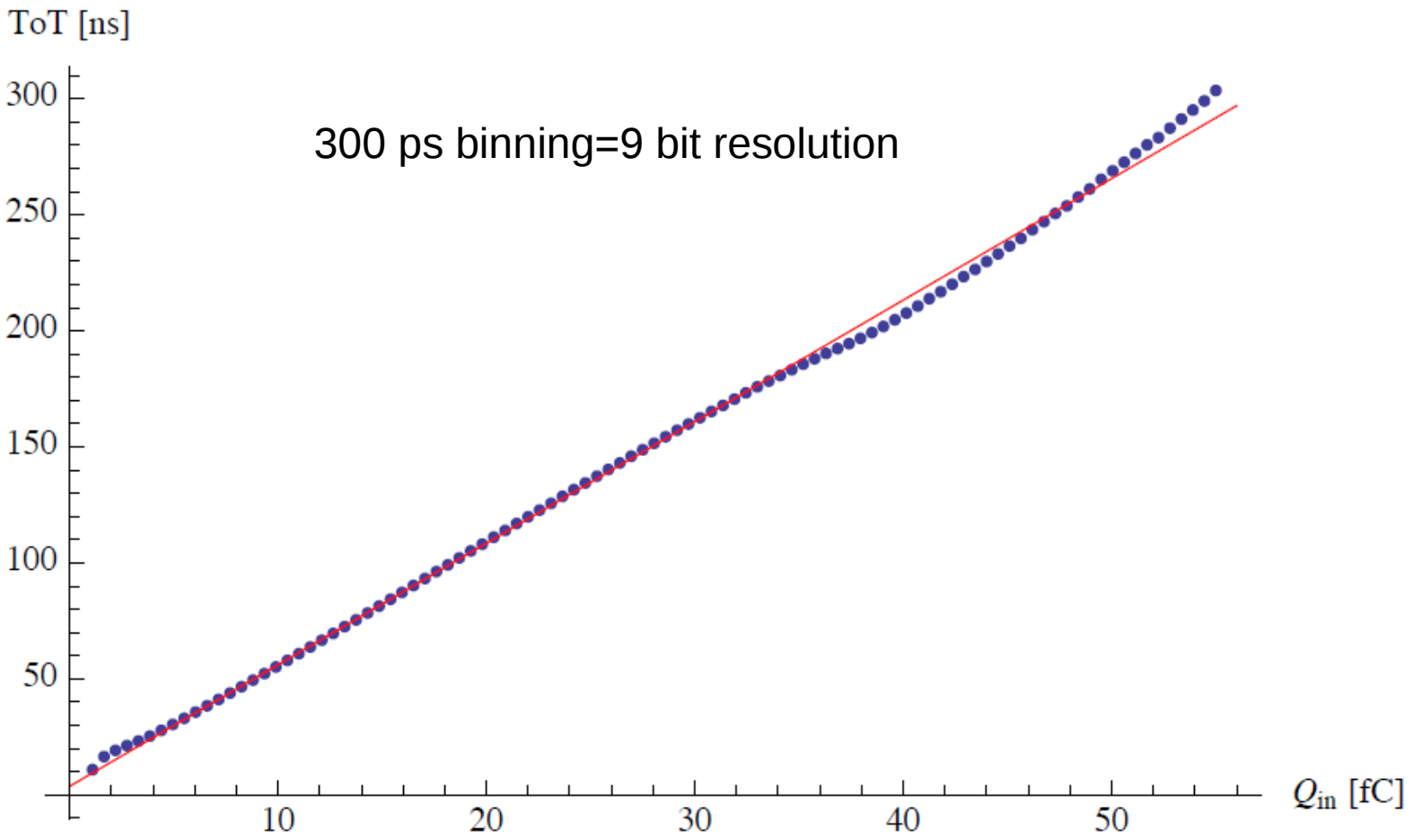


Noise vs capacitance



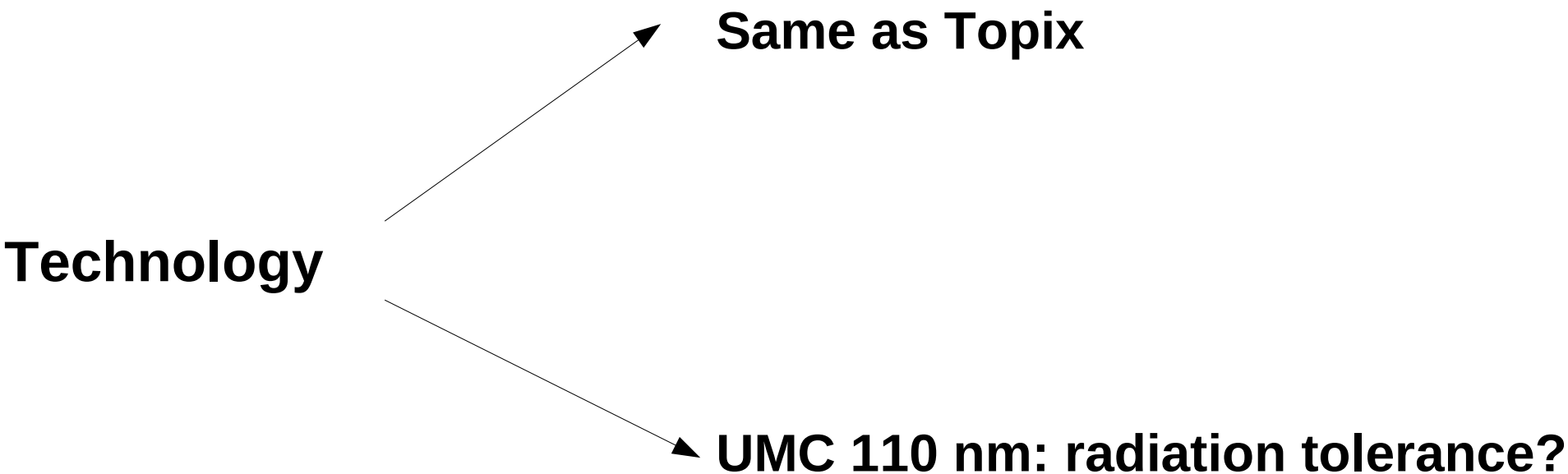
ToT (first trial only---)

Show[exp, th]

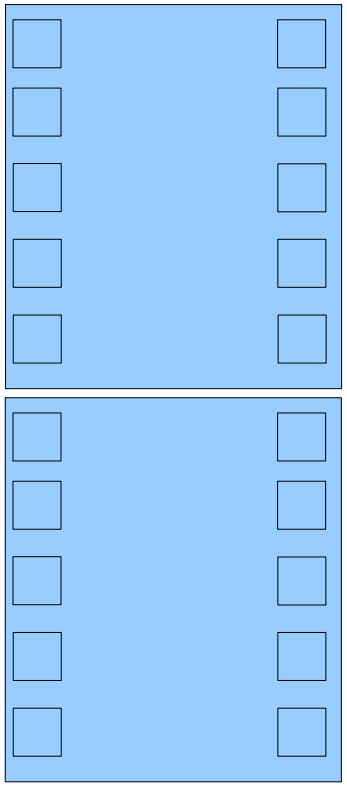


300 ps binning=9 bit resolution

Technology choice



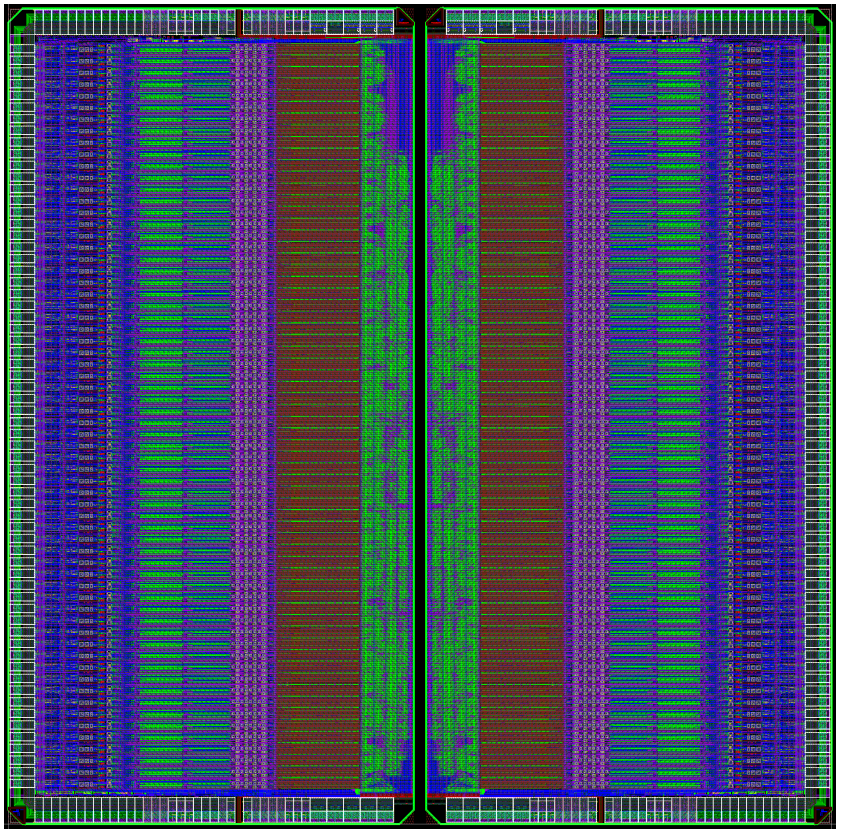
Chip floor plan



Buttable 64 channel modules: could fit in 5 mm x 5 mm

Bonding pads in front and back

128 equivalent module by dicing chips in couple



Outlook

- A time based-readout with a fast front-end followed by a high resolution TDC could be the fastest way to have a chip of reasonable size, due to synergies with other projects within the group in Torino and re-use of existing block.
- Porting between different technologies seems not to difficult.
- Digital logic must be modified for SEE
- First results from a fast front-end not too bad
- We need to understand better:
  - Charge resolution
  - Impact of signal shape variation
  - PSSR and common mode noise resilience/strategy.

- Freeze a decision on the architecture by the next front-end workshop