GateMate™ FPGA Overview

July 23, 2024

Agenda

1. Introduction to GateMate FPGA

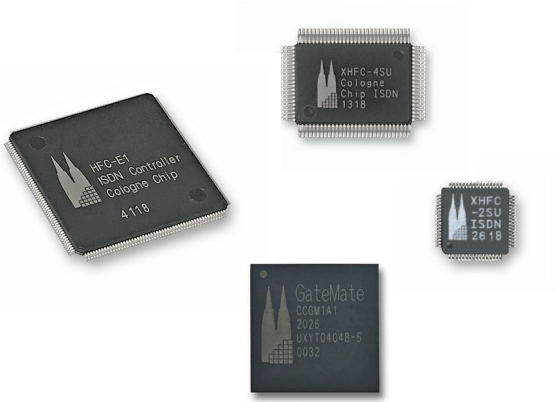
- Architecture Overview
- Features
- Toolchain

2. CPE for Time-to-Digital Converters (TDC)

- CP-lines
- Example

The Company

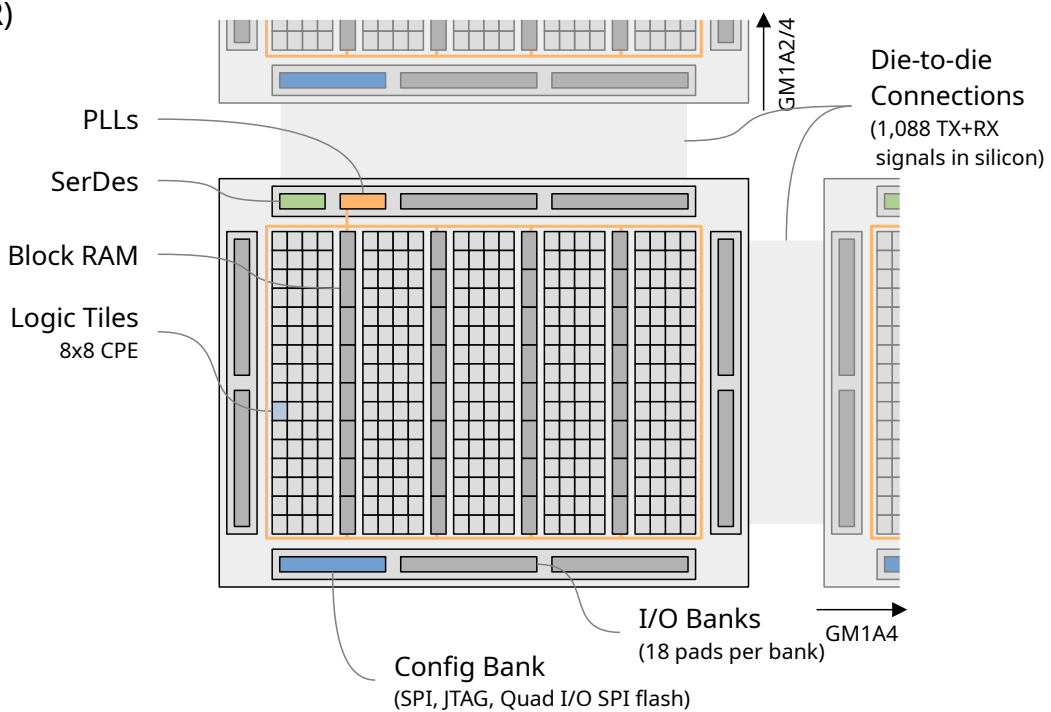
1994	Founding year of **Cologne Chip Designs GmbH**.
1996	Presentation of world's first single-chip-solution for ISDN.
1997 - 2000	Annual growth rate by 100%, introduction of world's first PCI and USB single-chip-solutions for ISDN.
2000	Rebranding to **Cologne Chip AG** and sales in millions of units.
2005	Presentation of first combined S/T and Up transceiver.
2007	Establishment of the latest **XHFC-Series** with open access to drivers and software; part of Linux Kernel since v. 2.6.27.
2020	Introduction of a new product line: **GateMate FPGA**.
2022	GateMate A1 in mass production.



GateMate FPGA

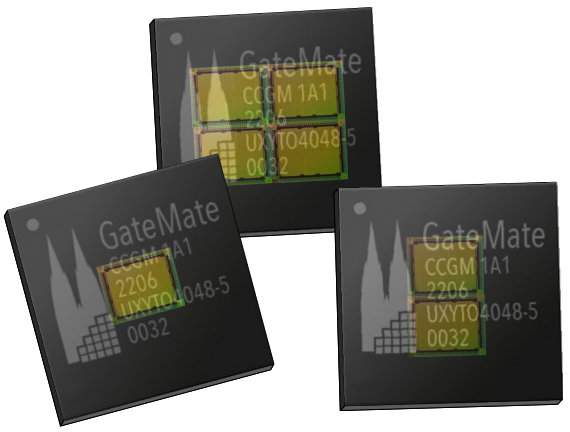
Features at a glance

- Globalfoundries™ 28 nm SLP process (Dresden, GER)
- 20,480 programmable elements (per FPGA-die)
  - 8 inputs or 2x 4 inputs + 2 flip-flops
  - 1- or 2-bit full adder or 2x2-bit multiplier
- All 162 GPIO configurable as single-ended or LVDS differential pairs with DDR support (MIPI D-PHY technically possible)
- 32x 40Kbit dual-port RAM cells (Total 1,280 Kbit)
- 4 Clock Generators (PLLs)
- 5.0 Gbit/s SerDes Controller
- Core voltage from 0.9V to 1.1V
  I/O voltage from 1.2V to 2.5V
- A1, A2, A4: 324-ball FBGA package



GateMate FPGA Series

Feature Summary by Device



Device	CPEs	FFs	Block RAM		PLL	Ser Des	GPIO		Package
			20K	40K			Single-ended	Diff. Pairs (LVDS)	
A1	20,480	40,960	64	32	4	1	162	81	324 FBGA 15x15 mm
A2	40,960	81,920	128	64	8	2	162	81	324 FBGA 15x15 mm
A4	81,920	163,840	256	128	16	4	154	77	324 FBGA 15x15 mm
...									
A25	512,000	1,240,000	1,600	800	100	25	tba	tba	tba

Architecture Features

GateMate FPGA

Central Programming Element

Combinatorical

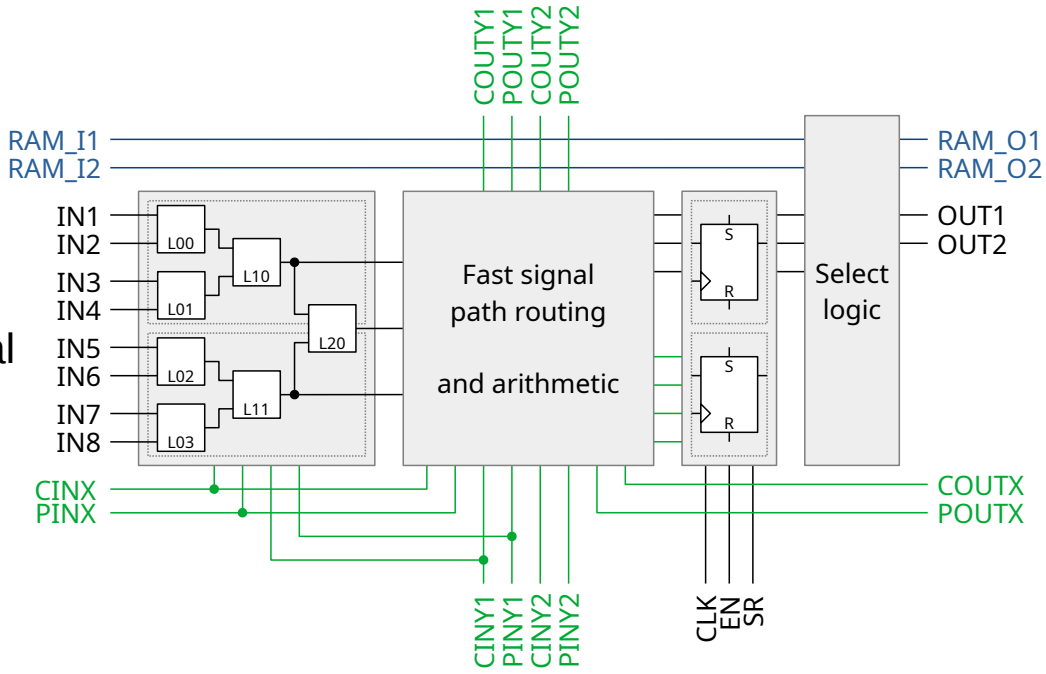
- 8-input function with LUT2-tree
- 2 independent 4-input functions
- 6 inputs for MUX-4 function

Arithmetic

- 1-bit or 2-bit full adder, horizontal or vertical
- 2x2-bit multiplier, expandable to any size

Sequential

- 2 Flip-flops or
- 2 Latches



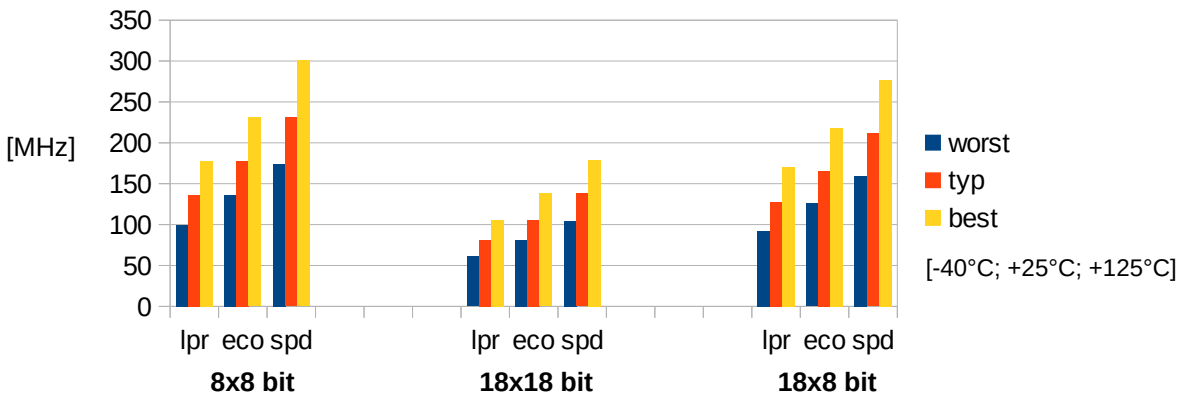
CPE Multipliers

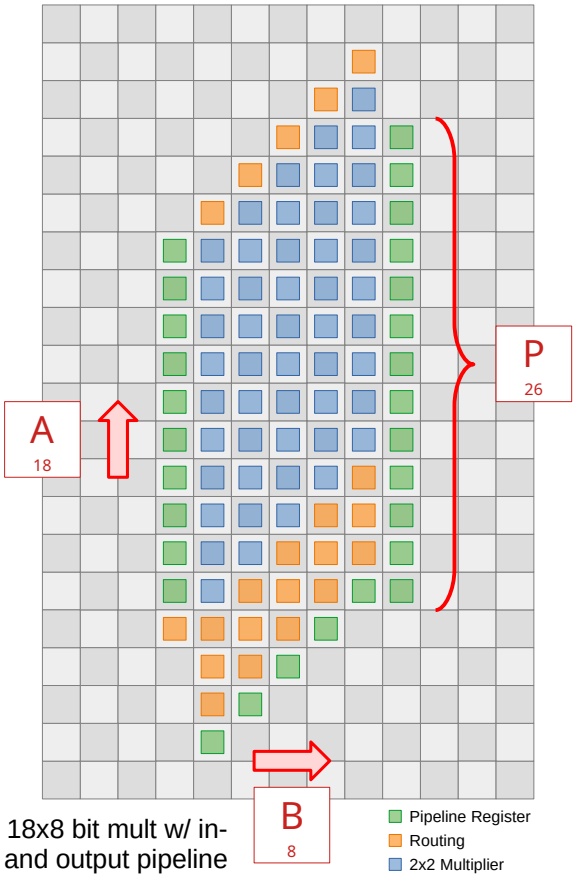
Arbitrarily Scalable Multipliers

- No fixed placement in CPE array
- Optional input and output pipeline stages

Performance

- B(+A)-path is critical





18x8 bit mult w/ in- and output pipeline

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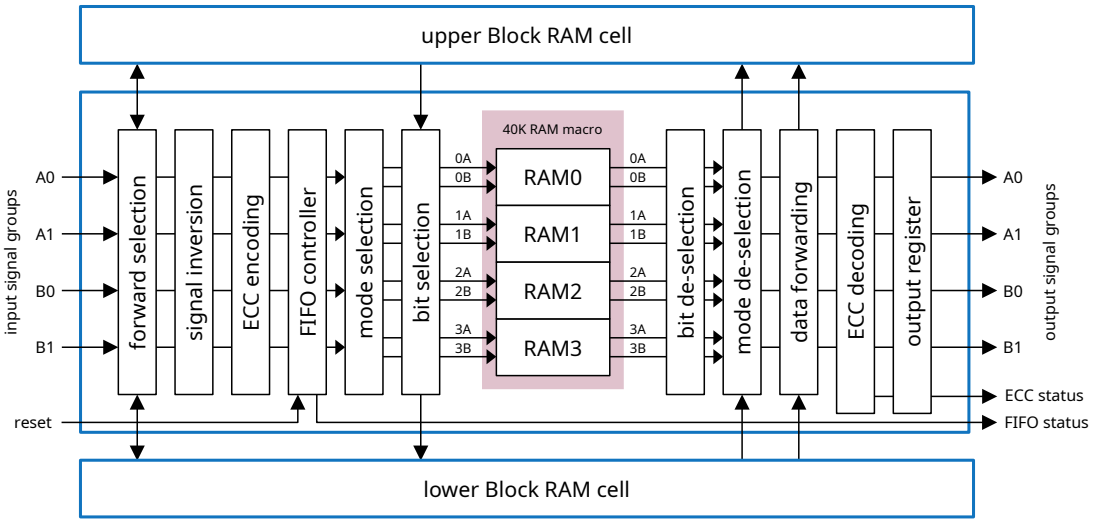
Block RAM

Configurations

- Single 40K cell or
- Two independent 20K cells
- True Dual Port (up to 40 inputs)
- Simple Dual Port (up to 80 inputs)
- FIFO (sync. or async.)
- Error Checking and Correcting



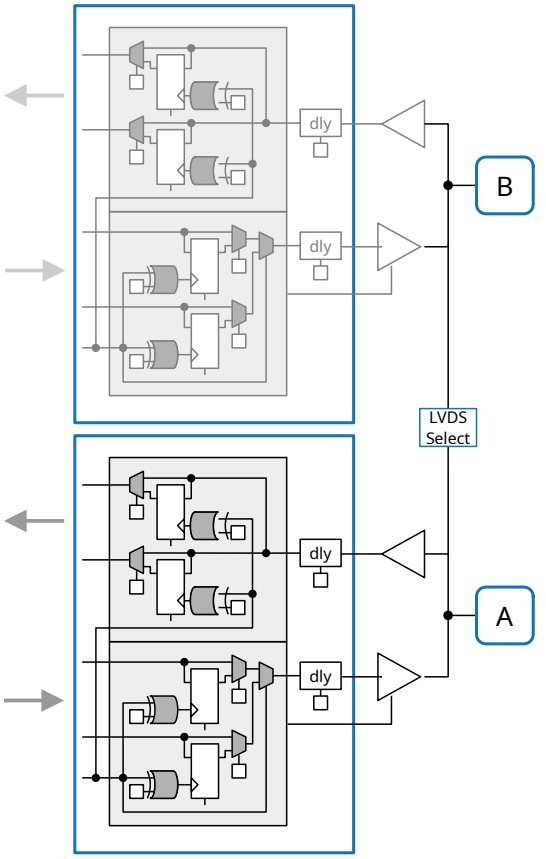
Signal Forwarding

- All cells vertically connected
- Reduces routing overhead

GateMate FPGA

GPIO Cells

- Each bank has 9 GPIO pairs (total: 162 GPIOs)
- All GPIOs configurable as single-ended or LVDS pairs (total: 81)
- Manual instantiation allows parameterization of
  - IO delays
  - Pin placement
  - Drive strengths
  - Slew rate control
  - Pullup/pulldown configuration
  - Mapping of registers into IO cells
- All GPIOs with double data rate (DDR) support



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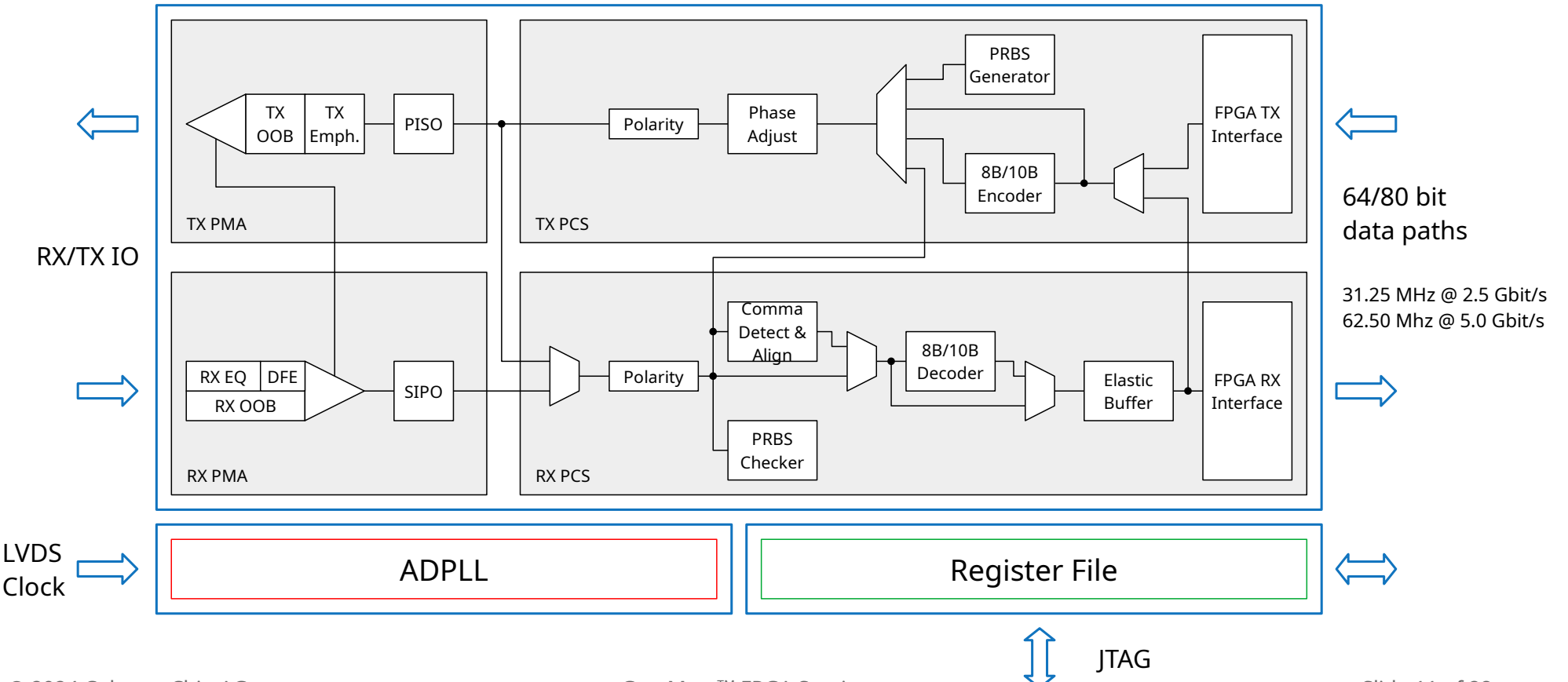
5 Gbit/s Serializer/Deserializer (SerDes)



GateMate FPGA

SerDes Features

Physical Coding Sublayer (PCS)

- Up to 64/80-bit data paths
- 8B/10B encoding and decoding
- Comma detection and byte alignment
- RX clock data recovery (CDR)
- Multiple PRBS generators and checkers
- Phase adjust FIFO for clock correction (elastic buffer)

Physical Medium Attachment (PMA)

- 3-tap decision feedback equalizer (DFE)
- TX pre- and post-emphasis
- Out-of-band (OOB) signaling

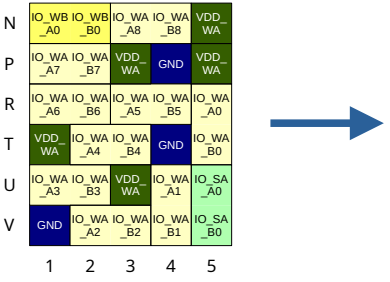
Hardware / Package, Pinout

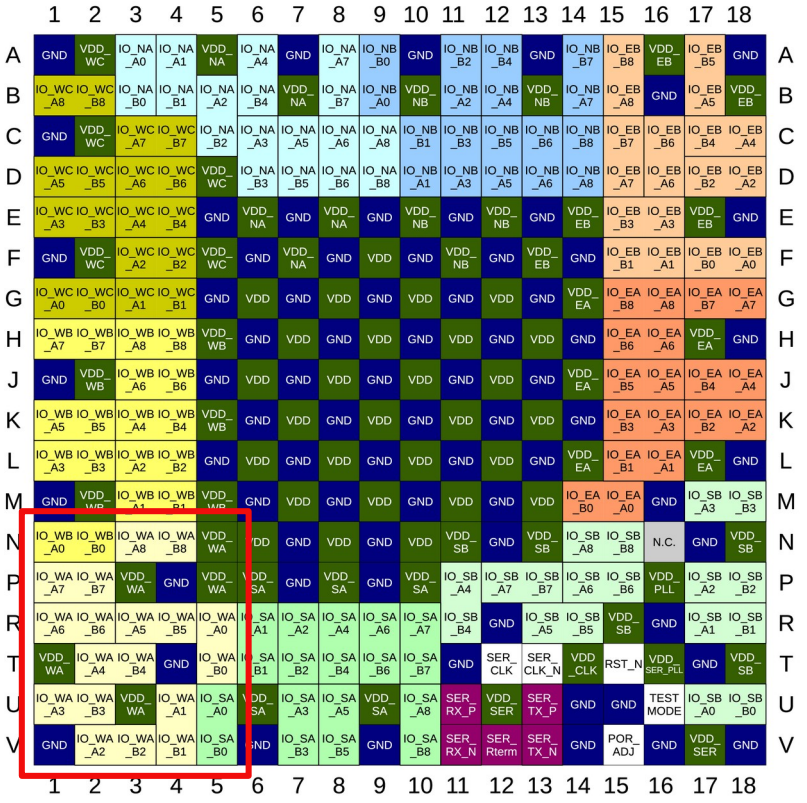
324-FBGA Pinout

CCGM1A1

- 15x15 mm package
- 324 balls, 0.8 mm pitch

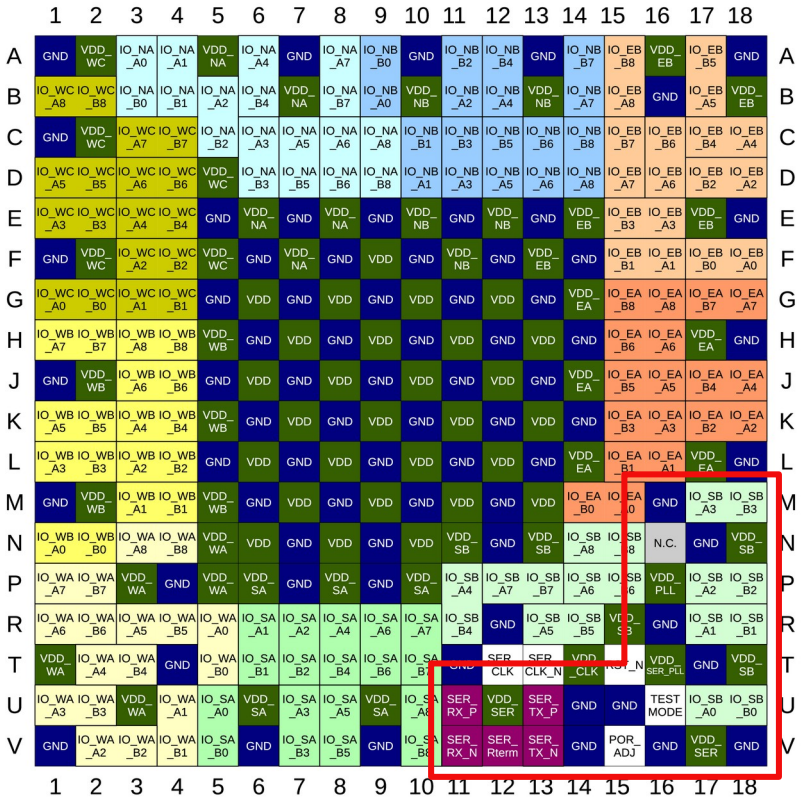
- Only 2 signal layers required
-
- Altium + KiCAD footprints available
- Configuration bank usable as GPIO



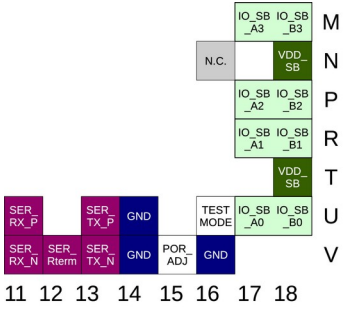


324-FBGA Pinout

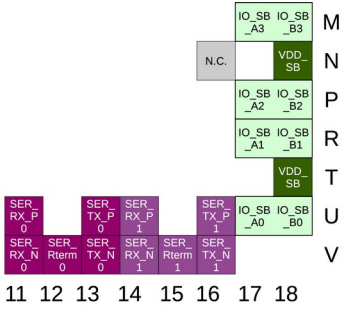
Pin Compatibility



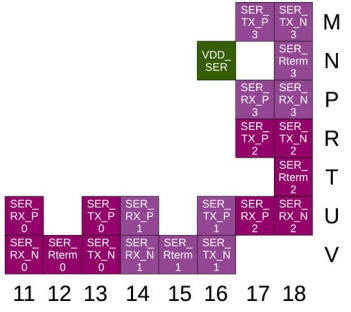
A1



A2



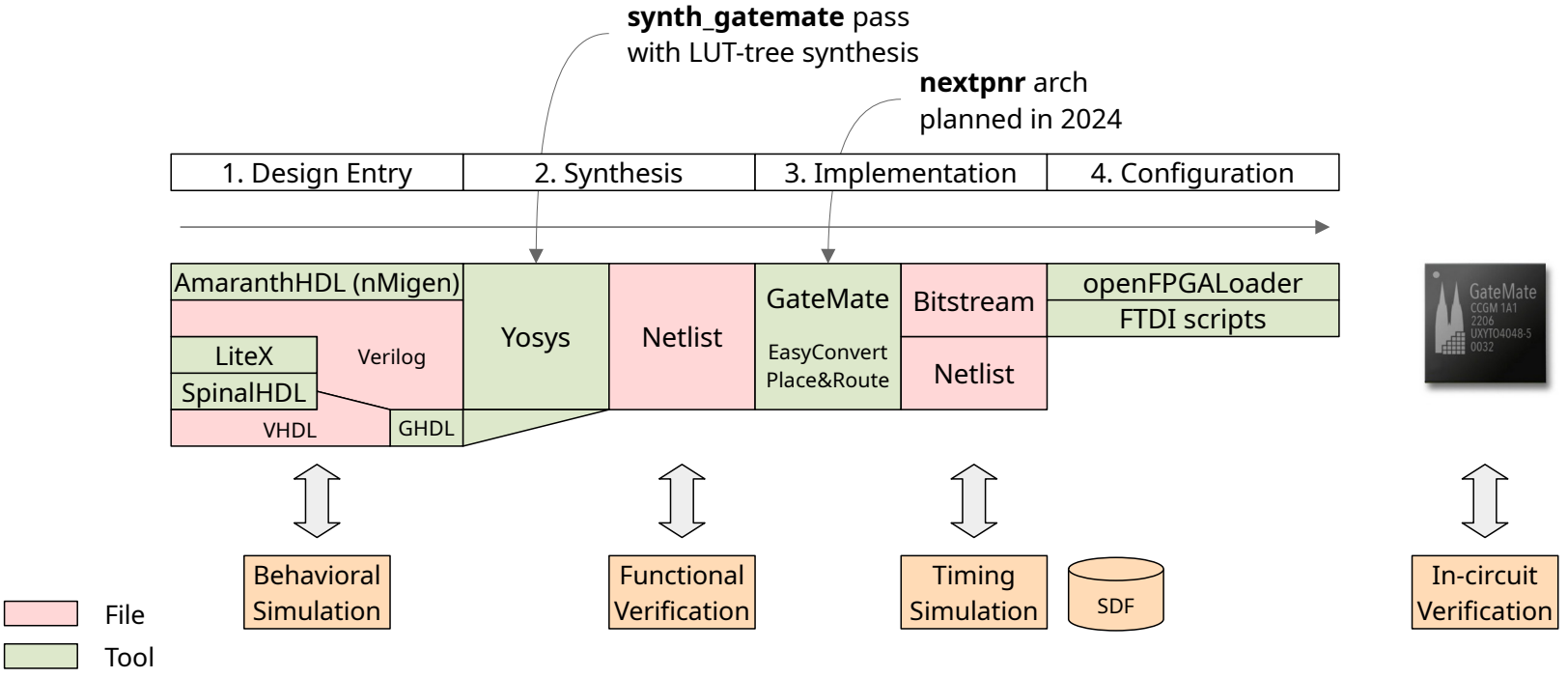
A4



Software / Toolchain

Toolchain

Features at a glance



[1] https://github.com/nmigen/nmigen
[2] https://github.com/enjoy-digital/litex
[3] https://github.com/SpinalHDL/SpinalHDL
[4] https://github.com/YosysHQ/yosys
[5] https://github.com/ghdl/ghdl
[6] https://github.com/trabucayre/openFPGALoader

Toolchain

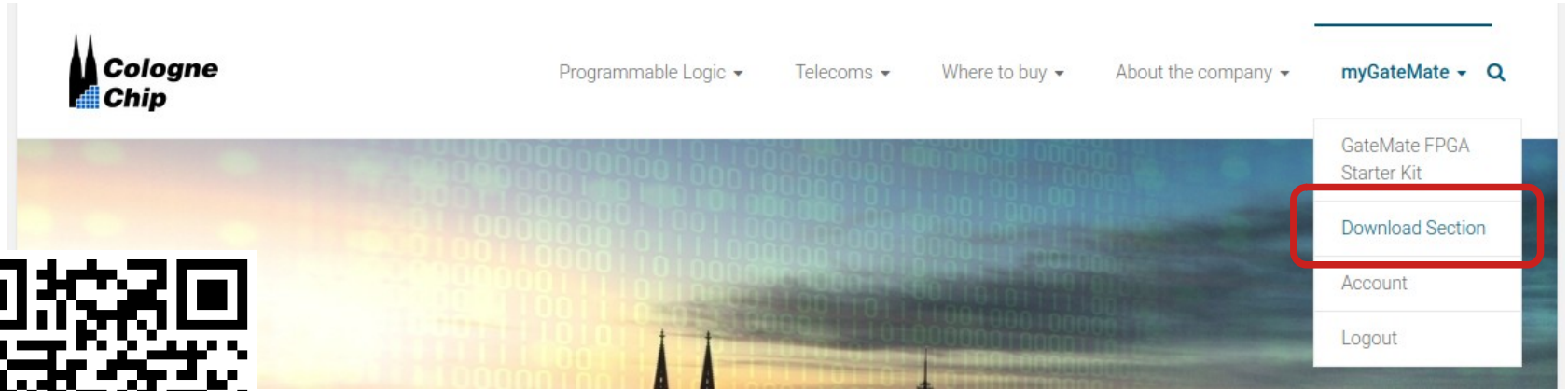
Requirements

- Supported Linux environments
  - Debian-based Linux (Debian, Ubuntu, …) with apt package manage
  - Arch-based Linux (Arch, Manjaro, …) with pacman package manager
  - Red Hat-based Linux (Centos, Fedora, …) with dnf or yum package manager
- Supported Windows environments
  - Windows 7 or later, 64 bit with Zadig USB driver installer (https://zadig.akeo.ie/)
- Third-party simulators
  - Modelsim, Questa Advanced Simulator (https://eda.sw.siemens.com/en-US/ic/modelsim/)
  - Icarus Verilog (http://iverilog.icarus.com/)
  - GHDL, CXXRTL, Verilator, …
- Third-party waveform viewer
  - GTKWave (http://gtkwave.sourceforge.net/)

Toolchain

Easy Way: Download from Website

- Pre-build Software available from Website:

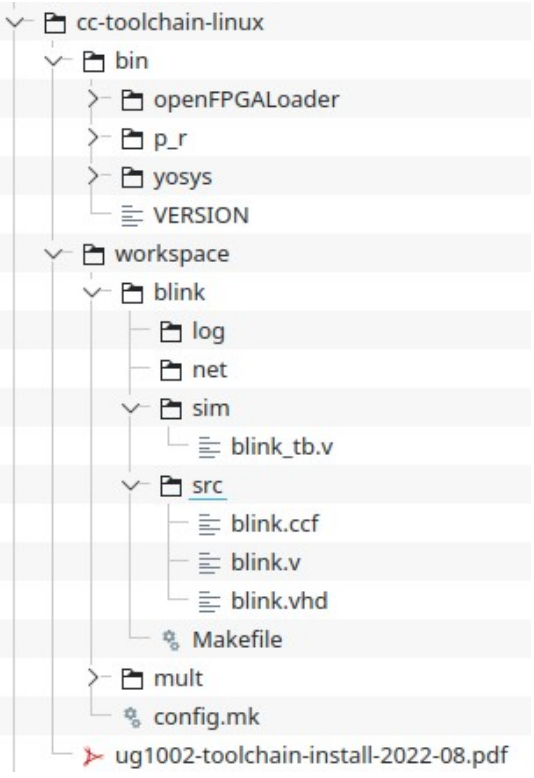


Link to Registration

Toolchain

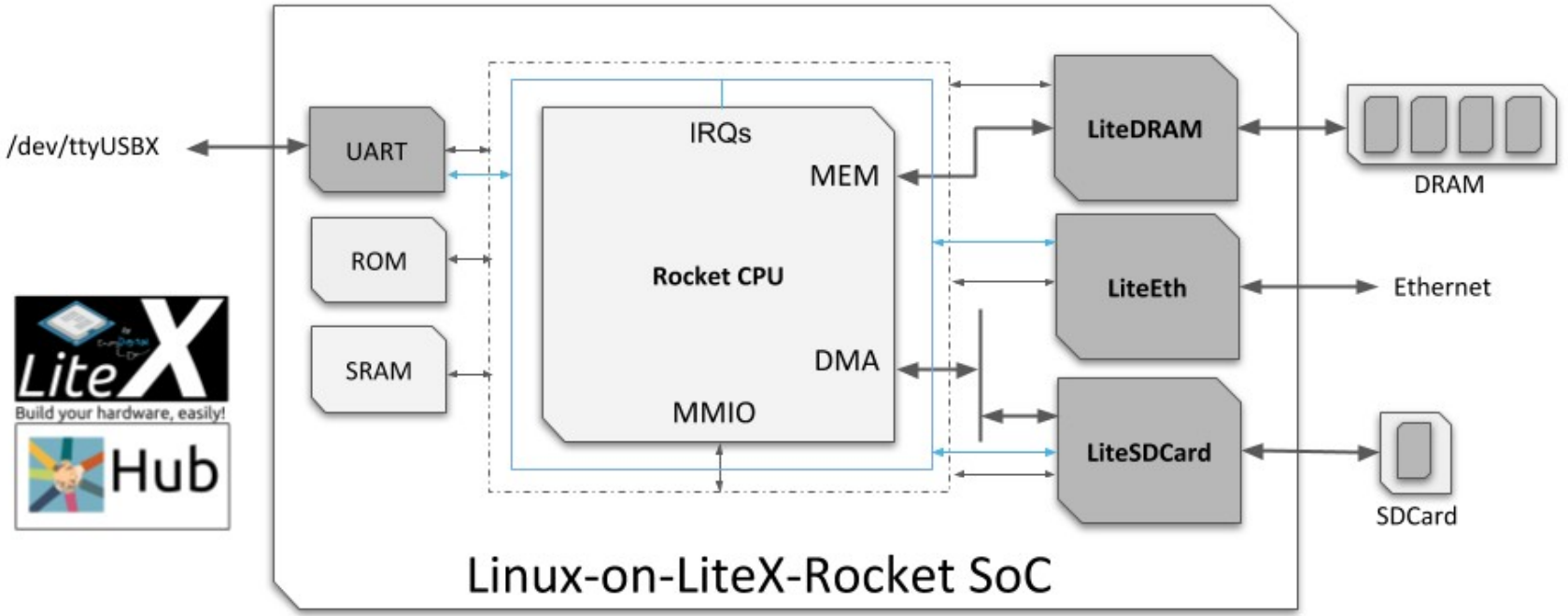
Package Contents

- »bin« directory
  - Executables for Synthesis, Place&Route and Config
- »workspace« directory
  - Example projects (»blink« and »mult«)
  - »sim« simulation testbenches
  - »src« Verilog and VHDL sources
  - »Makefile« script to run toolchain
- Latest Toolchain Installation Guide as PDF



LiteX[1]

Build your hardware, easily!



[1] https://github.com/enjoy-digital/litex

LiteX[1]

Build your hardware, easily!

CPUs

runs Linux

- VexRiscv (-smp)
- PicoRV32
- SERV
- NeoRV32
- ARM Cortex-M
- … (+24 more)

Periphery (via : wishbone, axi, axi-lite)

- S-ATA
- PCIexpress
- DDR2/3/4, HyperRAM
- VGA, DVI, HDMI
- Ethernet
- SD-card, SPI
- JESD204B (ADC, DAC)
- …

VexRiscv with HyperRAM and HDMI

[1] https://github.com/enjoy-digital/litex

GateMate Evaluation Board

Interfaces

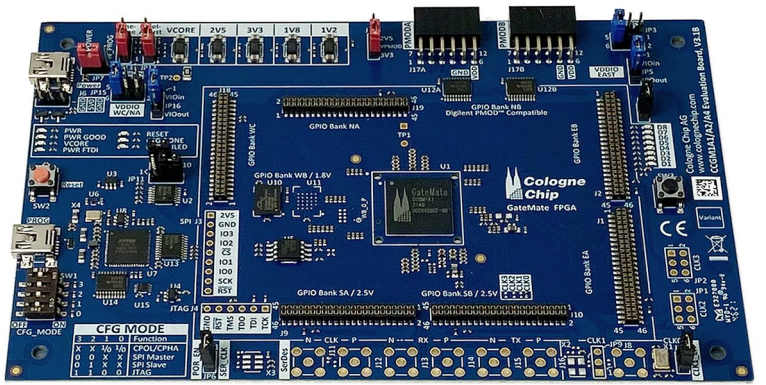
- Six I/O banks + access to SPI/JTAG signals
- Two standard 12-pin Pmod™ compatible connectors
- One high-speed SerDes RX, TX + CLK channel via SMA
- Configuration via flash or on-board USB to SPI/JTAG bridge

Memory

- 64 Mbit Quad-I/O SPI flash
- Up to two HyperBus modules (HyperRAM / HyperFlash)

Power

- User-selectable core and I/O voltages

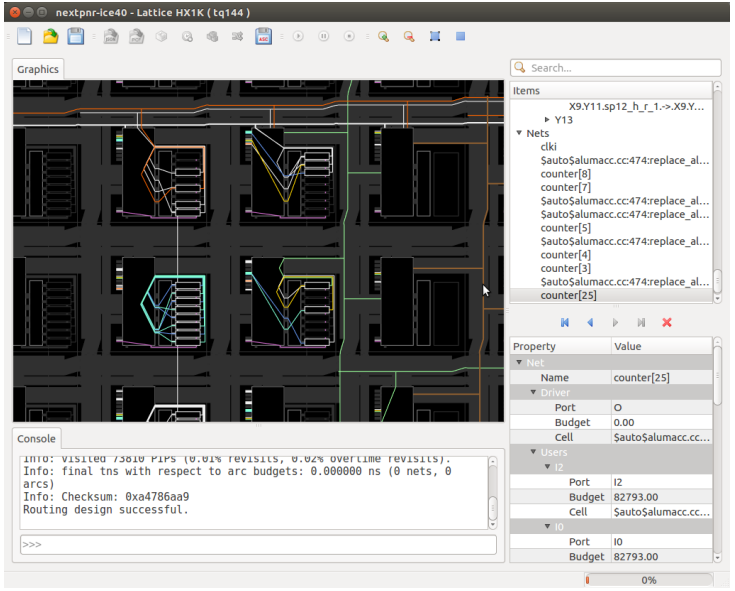


Link to Evaluation Kit

Outlook

2024 Roadmap

- Bitstream Copy Protection IP (EW 2024)
- »nextpnr« support
  - Step 1: Full disclosure of TileGrid and timing data for ChipDB and bitstream generator
  - Step 2: Actual »nexptnr« support
- GateMate A2
  - Engineering Samples available now
- IP Core Support
  - TDC, MIPI, HDMI, Ethernet



High Resolution TDC using GateMate CP-lines

Time-to Digital Converter

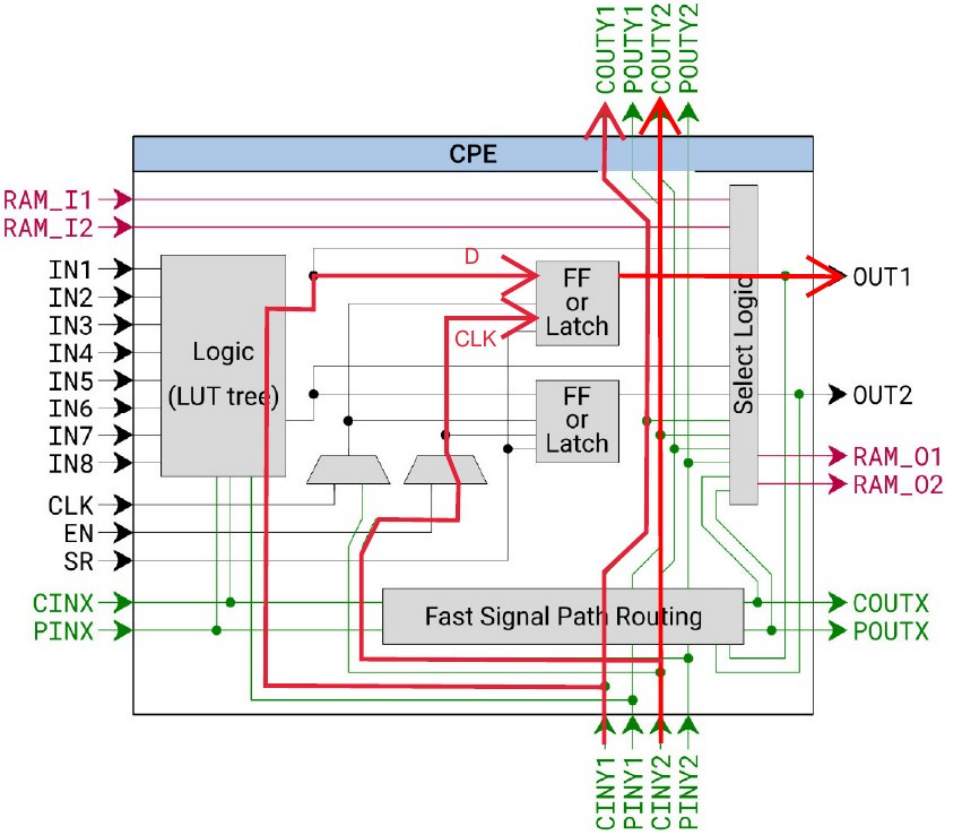
Using CPE CP-lines

Basics

- Measure the time interval between events with high precision
- Widely used in high-energy physics experiments, medical imaging, …

CC-FPGA-TDC

- Asynchronous input signal runs through Carry Chain
- Position of the 0/1 transition is stored in FF at the next event of system clock on Propagation Chain
- 5 ps resolution



CPE Vision

Implementation and Resource Utilization

- Chain length: 128 CPEs
- Max. Rows: 160

- Easy TDC instantiation using primitive:

```
module tdc_top (
    input wire clk, data,
    output wire q127
);
    wire clk_i;
    wire [127:0] q;

    CC_BUFG bufg_inst (
        .I(clk),
        .O(clk_i)
    );

    (* blackbox *) (* keep *)
    CC_GSI_TDC #(
        .COLUMN(4)
    ) tdc_inst0 (
        .CLK(clk_i),
        .DATA(data),
        .Q(q)
    );

    assign q127 = q[127];
endmodule
```

CPE Array 160x128

Contact

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