

GateMate™ FPGA Overview



Agenda



1. Introduction to GateMate FPGA

Architecture Overview

Features

Toolchain

2. CPE for Time-to-Digital Converters (TDC)

CP-lines

Example

The Company



- 1994 Founding year of **Cologne Chip Designs GmbH**.
- 1996 Presentation of world's first single-chip-solution for ISDN.
- 1997 - 2000 Annual growth rate by 100%, introduction of world's first PCI and USB single-chip-solutions for ISDN.
- 2000 Rebranding to **Cologne Chip AG** and sales in millions of units.
- 2005 Presentation of first combined S/T and Up transceiver.
- 2007 Establishment of the latest **XHFC-Series** with open access to drivers and software; part of Linux Kernel since v. 2.6.27.
- 2020 Introduction of a new product line: **GateMate FPGA**.
- 2022 GateMate A1 in mass production.

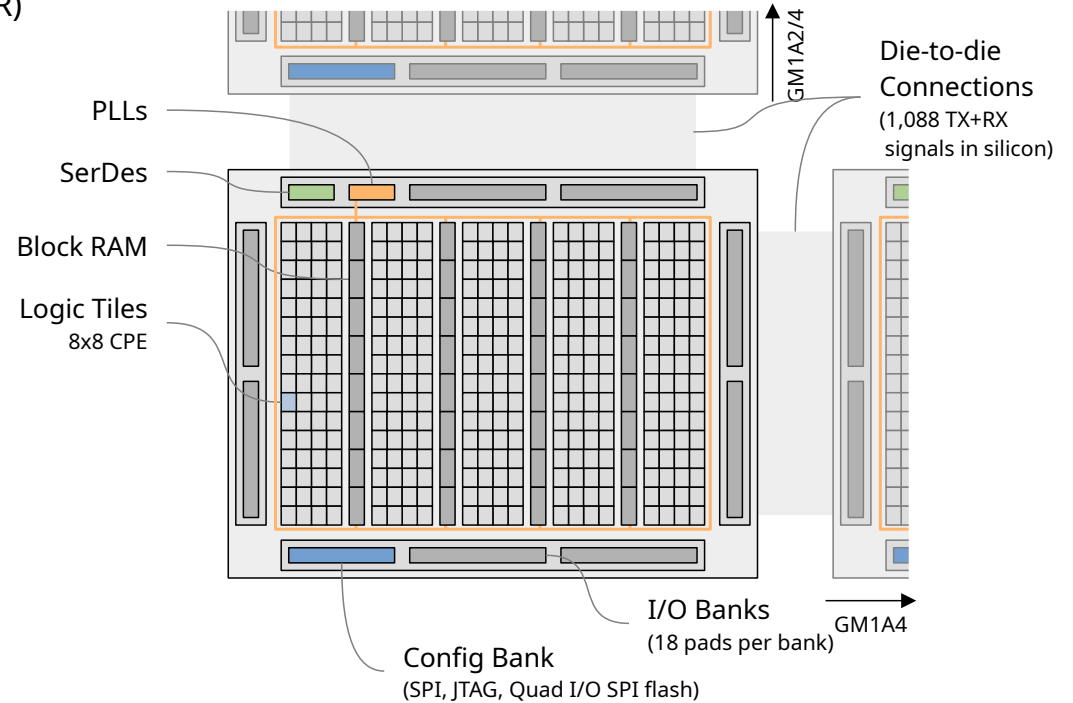


GateMate FPGA

Features at a glance

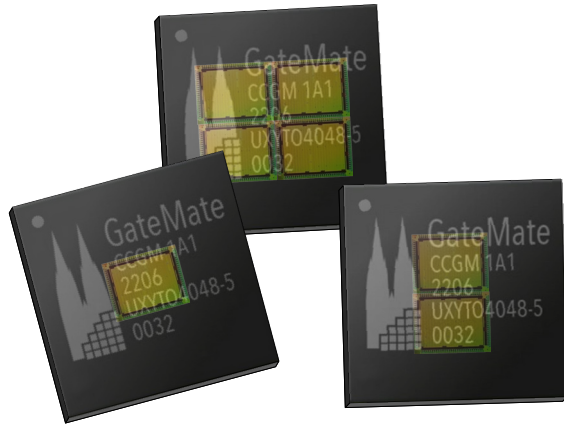


- Globalfoundries™ 28 nm SLP process (Dresden, GER)
- 20,480 programmable elements (per FPGA-die)
 - 8 inputs or 2x 4 inputs + 2 flip-flops
 - 1- or 2-bit full adder or 2x2-bit multiplier
- All 162 GPIO configurable as single-ended or LVDS differential pairs with DDR support (MIPI D-PHY technically possible)
- 32x 40Kbit dual-port RAM cells (Total 1,280 Kbit)
- 4 Clock Generators (PLLs)
- 5.0 Gbit/s SerDes Controller
- Core voltage from 0.9V to 1.1V
I/O voltage from 1.2V to 2.5V
- A1, A2, A4: 324-ball FBGA package



GateMate FPGA Series

Feature Summary by Device



Device	CPEs	FFs	Block RAM		PLL	Ser Des	GPIO		Package
			20K	40K			Single-ended	Diff. Pairs (LVDS)	
A1	20,480	40,960	64	32	4	1	162	81	324 FBGA 15x15 mm
A2	40,960	81,920	128	64	8	2	162	81	324 FBGA 15x15 mm
A4	81,920	163,840	256	128	16	4	154	77	324 FBGA 15x15 mm
...									
A25	512,000	1,240,000	1,600	800	100	25	tba	tba	tba

Architecture Features

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Central Programming Element



Combinatorial

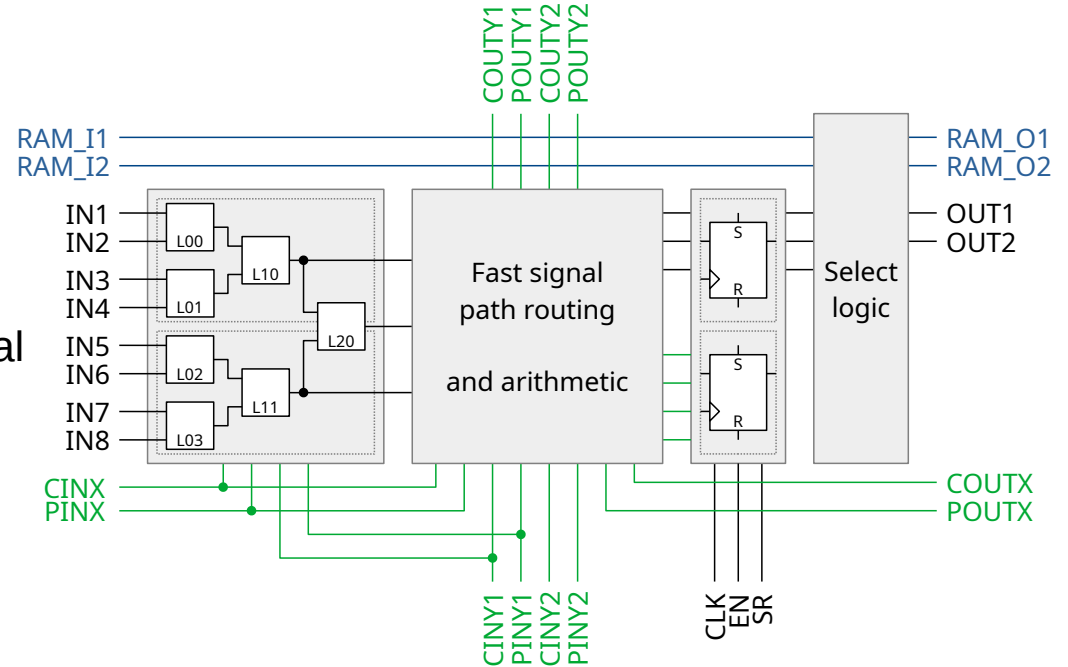
- 8-input function with LUT2-tree
- 2 independent 4-input functions
- 6 inputs for MUX-4 function

Arithmetic

- 1-bit or 2-bit full adder, horizontal or vertical
- 2x2-bit multiplier, expandable to any size

Sequential

- 2 Flip-flops or
- 2 Latches



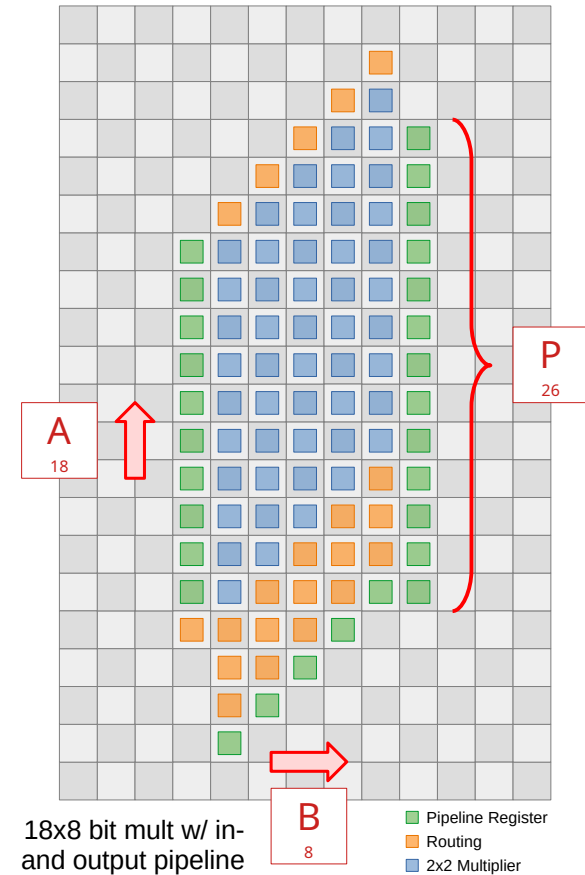
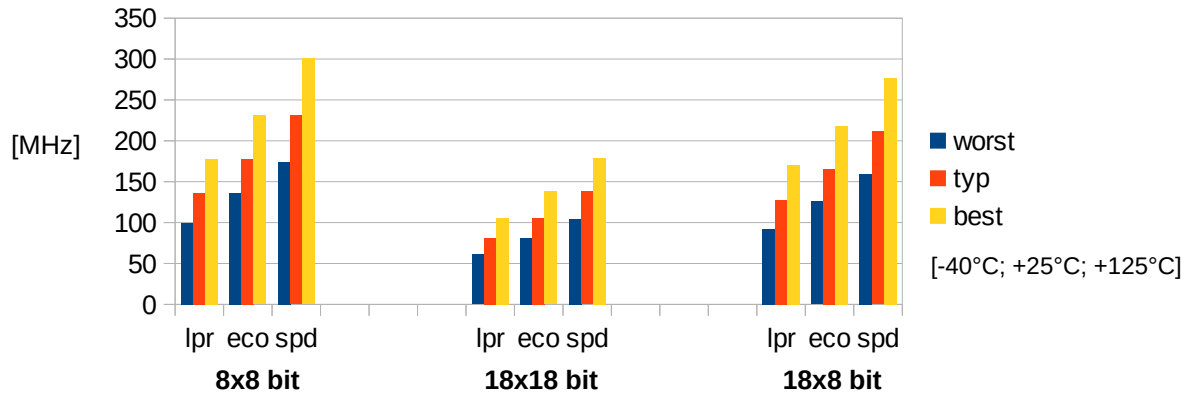
CPE Multipliers

Arbitrarily Scalable Multipliers

- No fixed placement in CPE array
- Optional input and output pipeline stages

Performance

- B(+A)-path is critical



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Block RAM

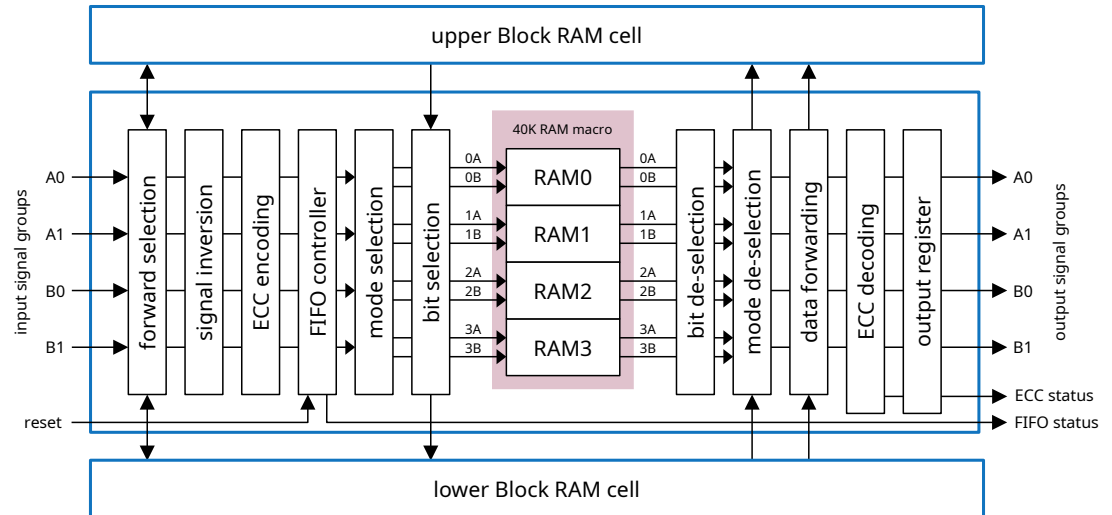


Configurations

- Single 40K cell or
- Two independent 20K cells
- True Dual Port (up to 40 inputs)
- Simple Dual Port (up to 80 inputs)
- FIFO (sync. or async.)
- Error Checking and Correcting

Signal Forwarding

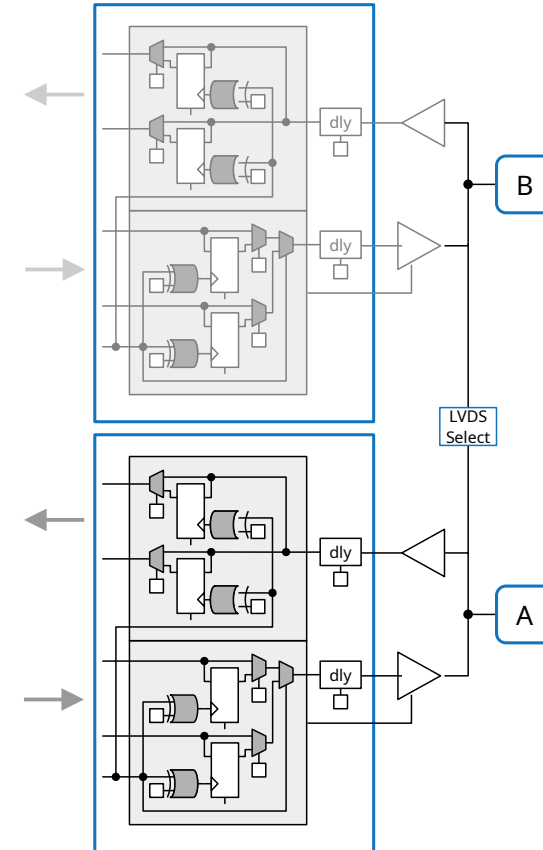
- All cells vertically connected
- Reduces routing overhead



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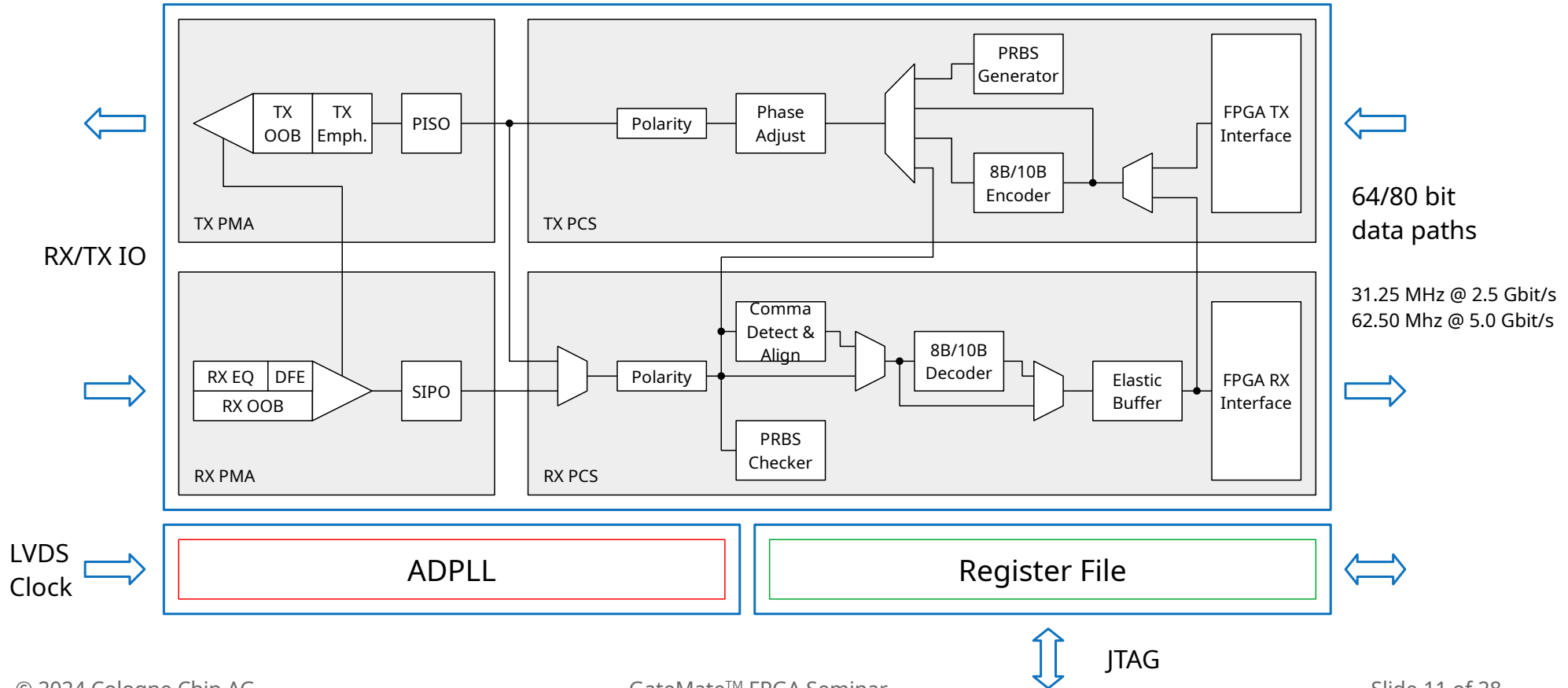
GPIO Cells

- Each bank has 9 GPIO pairs (total: 162 GPIOs)
- All GPIOs configurable as single-ended or LVDS pairs (total: 81)
- Manual instantiation allows parameterization of
 - IO delays
 - Pin placement
 - Drive strengths
 - Slew rate control
 - Pullup/pulldown configuration
 - Mapping of registers into IO cells
- All GPIOs with double data rate (DDR) support



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5 Gbit/s Serializer/Deserializer (SerDes)



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SerDes Features



Physical Coding Sublayer (PCS)

- Up to 64/80-bit data paths
- 8B/10B encoding and decoding
- Comma detection and byte alignment
- RX clock data recovery (CDR)
- Multiple PRBS generators and checkers
- Phase adjust FIFO for clock correction (elastic buffer)

Physical Medium Attachment (PMA)

- 3-tap decision feedback equalizer (DFE)
- TX pre- and post-emphasis
- Out-of-band (OOB) signaling

Hardware / Package, Pinout

324-FBGA Pinout

CCGM1A1



- 15x15 mm package
- 324 balls, 0.8 mm pitch
- Only 2 signal layers required
- Altium + KiCAD footprints available
- Configuration bank usable as GPIO

N	IO_WB_A0	IO_WB_B0	IO_WA_A8	IO_WA_B8	VDD_WA
P	IO_WA_A7	IO_WA_B7	VDD_WA	GND	VDD_WA
R	IO_WA_A6	IO_WA_B6	IO_WA_A5	IO_WA_B5	IO_WA_A0
T	VDD_WA	IO_WA_A4	GND	IO_WA_B0	
U	IO_WA_A3	IO_WA_B3	VDD_WA	IO_WA_A1	IO_SA_A0
V	GND	IO_WA_A2	IO_WA_B2	IO_WA_B1	IO_SA_B0
	1	2	3	4	5



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18		
A	GND	VDD_WC	IO_NA_A0	IO_NA_A1	VDD_NA	IO_NA_A4	GND	IO_NA_A7	IO_NB_B0	GND	IO_NB_B2	IO_NB_B4	GND	IO_NB_B7	IO_NB_B5	VDD_EB	IO_EB_B8	GND	A	
B	IO_WC_A8	IO_WC_B8	IO_NA_B0	IO_NA_B1	IO_NA_A2	IO_NA_B4	VDD_NA	IO_NA_B7	IO_NB_A0	VDD_NB	IO_NB_A2	IO_NB_A4	VDD_NB	IO_NB_A7	IO_EB_A8	GND	IO_EB_A5	VDD_EB	B	
C	GND	VDD_WC	IO_WC_A7	IO_WC_B7	GND	IO_NA_A3	IO_NA_A5	IO_NA_A6	IO_NB_B1	IO_NB_B3	IO_NB_B5	IO_NB_B6	IO_NB_B8	IO_NB_B7	IO_EB_B6	IO_EB_B4	IO_EB_A4		C	
D	IO_WC_A5	IO_WC_B5	IO_WC_A6	IO_WC_B6	VDD_WC	IO_NA_B3	IO_NA_B5	IO_NA_B8	IO_NB_A1	IO_NB_A3	IO_NB_A5	IO_NB_A6	IO_NB_A8	IO_EB_A7	IO_EB_A6	IO_EB_B2	IO_EB_A2		D	
E	IO_WC_A3	IO_WC_B3	IO_WC_A4	IO_WC_B4	GND	VDD_NA	GND	VDD_NA	GND	VDD_NB	GND	VDD_NB	GND	VDD_EB	IO_EB_B3	IO_EB_A3	VDD_EB	GND	E	
F	GND	VDD_WC	IO_WC_A2	IO_WC_B2	VDD_WC	GND	VDD_NA	GND	VDD	GND	VDD_NB	GND	VDD_EB	GND	IO_EB_B1	IO_EB_A1	IO_EB_B0	IO_EB_A0	F	
G	IO_WC_A0	IO_WC_B0	IO_WC_A1	IO_WC_B1	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD_EA	IO_EA_B8	IO_EA_A8	IO_EA_B7	IO_EA_A7	G	
H	IO_WB_A7	IO_WB_B7	IO_WB_A8	IO_WB_B8	VDD_WB	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	IO_EA_B6	IO_EA_A6	VDD_EA	GND	H	
J	GND	VDD_WB	IO_WB_A6	IO_WB_B6	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD_EA	IO_EA_B5	IO_EA_A5	IO_EA_B4	IO_EA_A4	J	
K	IO_WB_A5	IO_WB_B5	IO_WB_A4	IO_WB_B4	VDD_WB	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	IO_EA_B3	IO_EA_A3	IO_EA_B2	IO_EA_A2	K	
L	IO_WB_A3	IO_WB_B3	IO_WB_A2	IO_WB_B2	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD_EA	IO_EA_B1	IO_EA_A1	VDD_EA	GND	L	
M	GND	VDD_WB	IO_WB_A1	IO_WB_B1	VDD_WB	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	IO_EA_B0	IO_EA_A0	GND	IO_SB_A3	IO_SB_B3	M
N	IO_WB_A0	IO_WB_B0	IO_WA_A8	IO_WA_B8	VDD_WA	GND	VDD	GND	VDD	GND	VDD	VDD_SB	GND	VDD_SB	IO_SB_A8	IO_SB_B8	N.C.	GND	VDD_SB	N
P	IO_WA_A7	IO_WA_B7	VDD_WA	GND	VDD_WA	VDD_SA	GND	VDD_SA	GND	VDD_SA	IO_SB_A4	IO_SB_A7	IO_SB_B7	IO_SB_A6	IO_SB_B6	VDD_PLL	IO_SB_A1	IO_SB_B2		P
R	IO_WA_A6	IO_WA_B6	IO_WA_A5	IO_WA_B5	IO_WA_A0	IO_SA_A1	IO_SA_A2	IO_SA_A4	IO_SA_A6	IO_SA_A7	IO_SB_B4	GND	IO_SB_A5	IO_SB_B5	VDD_SB	GND	IO_SB_A1	IO_SB_B1		R
T	VDD_WA	IO_WA_A4	IO_WA_B4	GND	IO_WA_B0	IO_SA_B1	IO_SA_B2	IO_SA_B4	IO_SA_B6	IO_SA_B7	GND	SER_CLK	SER_CLK_N	VDD_CLK	RST_N	VDD_SER_PLL	GND	VDD_SB		T
U	IO_WA_A3	IO_WA_B3	VDD_WA	IO_WA_A1	IO_SA_A0	IO_SA_A3	IO_SA_A5	VDD_SA	IO_SA_A8	SER_RX_P	VDD_SER	SER_TX_P	GND	GND	TEST_MODE	IO_SB_A0	IO_SB_B0			U
V	GND	IO_WA_A2	IO_WA_B2	IO_WA_B1	IO_SA_B0	GND	IO_SA_B3	IO_SA_B5	GND	IO_SA_B8	SER_RX_N	SER_Rterm	SER_TX_N	GND	POR_ADJ	GND	VDD_SER	GND		V
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18		

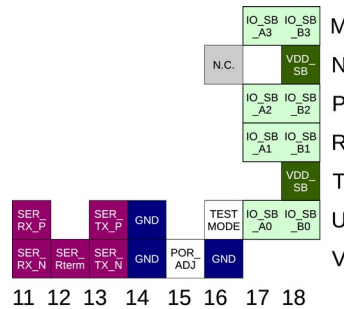
324-FBGA Pinout

Pin Compatibility

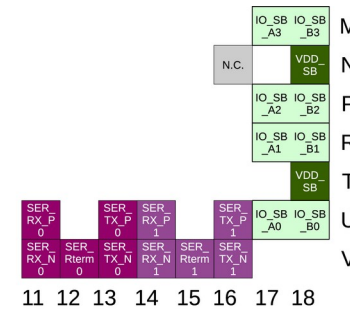


	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A	GND	VDD_WC	IO_NA_A0	IO_NA_A1	VDD_NA	IO_NA_A4	GND	IO_NA_A7	IO_NB_B0	GND	IO_NB_B2	IO_NB_B4	GND	IO_NB_B7	IO_EB_B8	VDD_EB	IO_EB_B5	GND
B	IO_WC_IO_WC_A8_B8	IO_NA_A0	IO_NA_A1	IO_NA_A2	IO_NA_A4	VDD_NA	IO_NA_B7	IO_NB_A0	IO_NB_A2	IO_NB_A4	VDD_NB	IO_NB_A7	IO_EB_A8	GND	IO_EB_A5	VDD_EB	IO_EB_A2	GND
C	GND	VDD_WC	IO_WC_IO_WC_A7_B7	IO_NA_B2	IO_NA_A3	IO_NA_A5	IO_NA_A6	IO_NA_A8	IO_NB_B1	IO_NB_B3	IO_NB_B5	IO_NB_B6	IO_NB_B7	IO_EB_B6	IO_EB_B4	IO_EB_A4	GND	GND
D	IO_WC_IO_WC_A5_B5	IO_WC_IO_WC_A6_B6	VDD_WC	IO_NA_B3	IO_NA_B5	IO_NA_B6	IO_NA_B8	IO_NB_A1	IO_NB_A3	IO_NB_A5	IO_NB_A6	IO_NB_A8	IO_EB_A7	IO_EB_A6	IO_EB_B2	IO_EB_A2	GND	GND
E	IO_WC_IO_WC_A3_B3	IO_WC_IO_WC_A4_B4	GND	VDD_NA	GND	VDD_NA	GND	VDD_NB	GND	VDD_NB	GND	VDD_EB	IO_EB_B3	IO_EB_A3	VDD_EB	GND	GND	GND
F	GND	VDD_WC	IO_WC_IO_WC_A2_B2	VDD_WC	GND	VDD_NA	GND	VDD	GND	VDD_NB	GND	VDD_EB	GND	IO_EB_B1	IO_EB_A1	IO_EB_B0	IO_EB_A0	GND
G	IO_WC_IO_WC_A0_B0	IO_WC_IO_WC_A1_B1	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	IO_EA_B8	IO_EA_A8	IO_EA_B7	IO_EA_A7	GND
H	IO_WB_IO_WB_A7_B7	IO_WB_IO_WB_A8_B8	VDD_WB	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	IO_EA_B6	IO_EA_A6	VDD_EA	GND
J	GND	VDD_WB	IO_WB_IO_WB_A6_B6	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	IO_EA_B5	IO_EA_A5	IO_EA_B4	IO_EA_A4
K	IO_WB_IO_WB_A5_B5	IO_WB_IO_WB_A4_B4	VDD_WB	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	IO_EA_B3	IO_EA_A3	IO_EA_B2	IO_EA_A2
L	IO_WB_IO_WB_A3_B3	IO_WB_IO_WB_A2_B2	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD	IO_EA_B1	IO_EA_A1	VDD_EA	GND
M	GND	VDD_WB	IO_WB_IO_WB_A1_B1	VDD_WB	GND	VDD	GND	VDD	GND	VDD	GND	VDD	IO_EA_B0	IO_EA_A0	GND	IO_SB_A3	IO_SB_B3	GND
N	IO_WB_IO_WB_A0_B0	IO_WA_IO_WA_A8_B8	VDD_WA	VDD	GND	VDD	GND	VDD	VDD_SB	GND	VDD_SB	IO_SB_A8	IO_SB_B8	N.C.	GND	VDD_SB	GND	GND
P	IO_WA_IO_WA_A7_B7	VDD_WA	GND	VDD_WA	VDD_SA	GND	VDD_SA	GND	VDD_SA	IO_SB_A4	IO_SB_A7	IO_SB_B7	IO_SB_A6	IO_SB_B6	VDD_PLL	IO_SB_A2	IO_SB_B2	GND
R	IO_WA_IO_WA_A6_B6	IO_WA_IO_WA_A5_B5	IO_WA_A0	IO_WA_A1	IO_SA_A2	IO_SA_A4	IO_SA_A6	IO_SA_A7	IO_SB_B4	GND	IO_SB_A5	IO_SB_B5	IO_SB_B3	GND	IO_SB_A1	IO_SB_B1	GND	GND
T	VDD_WA	IO_WA_A4	IO_WA_B4	GND	IO_WA_B0	IO_WA_B1	IO_WA_B2	IO_WA_B4	IO_WA_B6	IO_WA_B7	GND	SER_CLK	SER_CLK_N	IO_NLN	VDD_SER_PLL	GND	VDD_SB	GND
U	IO_WA_IO_WA_A3_B3	VDD_WA	IO_WA_A1	IO_SA_A0	VDD_SA	IO_SA_A3	IO_SA_A5	VDD_SA	IO_SA_A6	IO_SA_A7	IO_SA_B7	SER_RX_P0	VDD_SER	SER_TX_P0	GND	TEST_MODE	IO_SB_A0	IO_SB_B0
V	GND	IO_WA_A2	IO_WA_B1	IO_SA_B0	GND	IO_SA_B3	IO_SA_B5	GND	IO_SA_B6	GND	SER_RX_N0	SER_Rterm0	SER_TX_N0	GND	POR_ADJ	GND	VDD_SER	GND

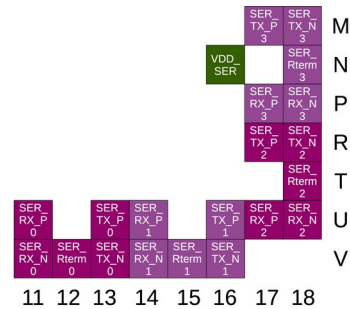
A1



A2



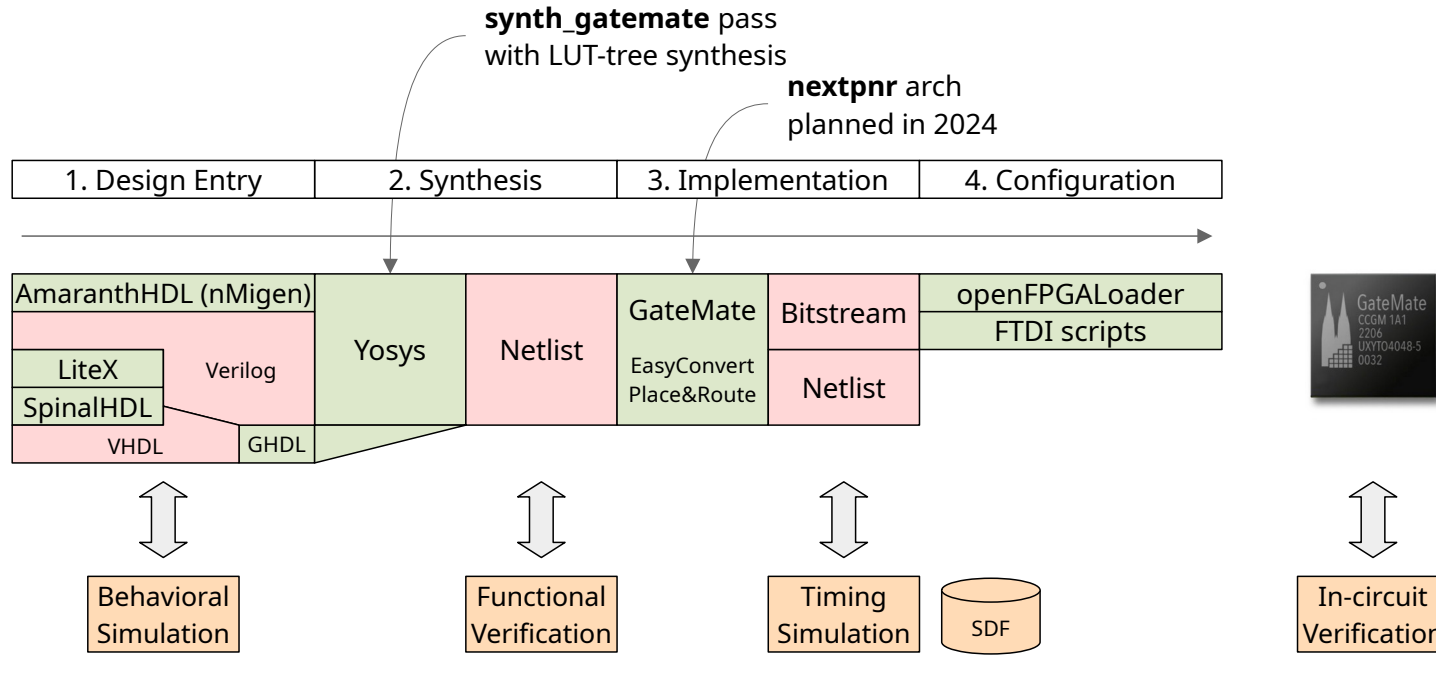
A4



Software / Toolchain

Toolchain

Features at a glance



File
Tool

- [1] <https://github.com/nmigen/nmigen>
- [2] <https://github.com/enjoy-digital/litex>
- [3] <https://github.com/SpinalHDL/SpinalHDL>

- [4] <https://github.com/YosysHQ/yosys>
- [5] <https://github.com/ghdl/ghdl>
- [6] <https://github.com/trabucayre/openFPGALoader>

Toolchain

Requirements




- Supported Linux environments
 - Debian-based Linux (Debian, Ubuntu, ...) with apt package manager
 - Arch-based Linux (Arch, Manjaro, ...) with pacman package manager
 - Red Hat-based Linux (Centos, Fedora, ...) with dnf or yum package manager
- Supported Windows environments
 - Windows 7 or later, 64 bit with Zadig USB driver installer (<https://zadig.akeo.ie/>)
- Third-party simulators
 - Modelsim, Questa Advanced Simulator (<https://eda.sw.siemens.com/en-US/ic/modelsim/>)
 - Icarus Verilog (<http://iverilog.icarus.com/>)
 - GHDL, CXXRTL, Verilator, ...
- Third-party waveform viewer
 - GTKWave (<http://gtkwave.sourceforge.net/>)

Toolchain

Easy Way: Download from Website



- Pre-build Software available from Website:

A screenshot of the Cologne Chip website. The top navigation bar includes the company logo, a search bar labeled "myGateMate", and several menu items: "Programmable Logic", "Telecoms", "Where to buy", and "About the company". A dropdown menu is open under "myGateMate", showing options: "GateMate FPGA Starter Kit", "Download Section" (highlighted with a red rectangle), "Account", and "Logout". The background of the website features a blurred image of a sunset or sunrise over a landscape with spires, overlaid with a grid of binary code (0s and 1s).


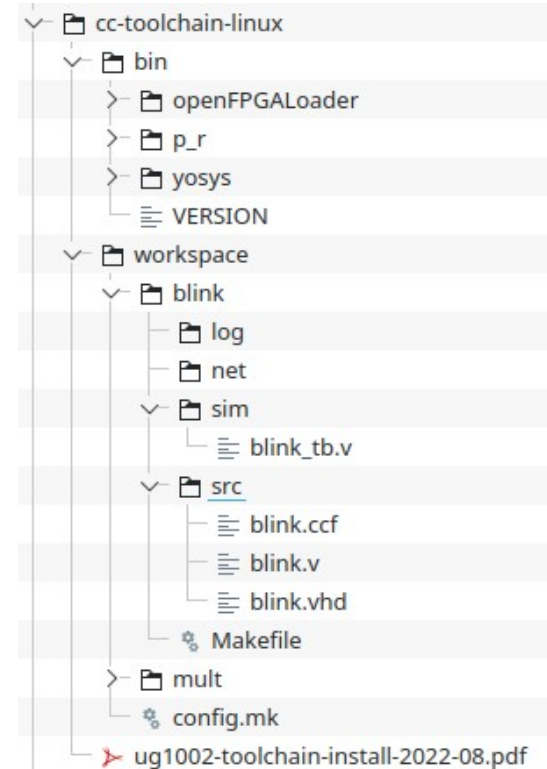
Link to Registration

Toolchain

Package Contents

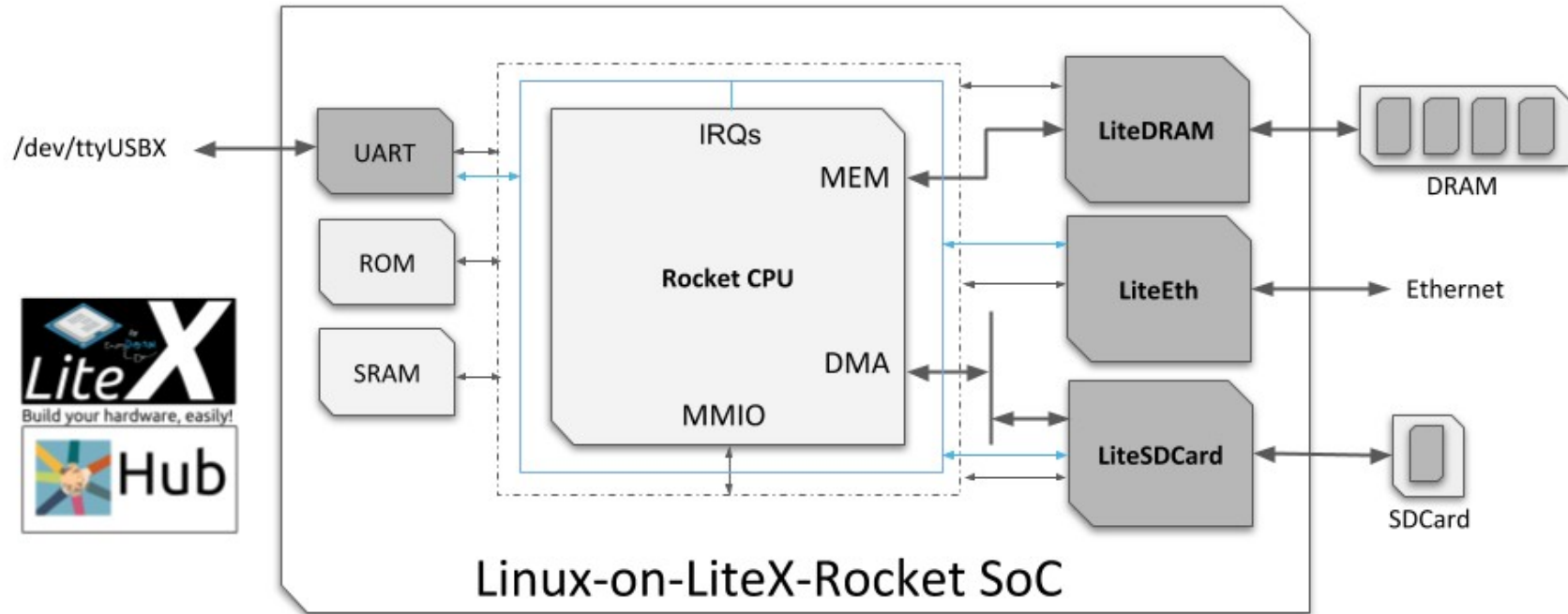


- »bin« directory
 - Executables for Synthesis, Place&Route and Config
- »workspace« directory
 - Example projects (»blink« and »mult«)
 - »sim« simulation testbenches
 - »src« Verilog and VHDL sources
 - »Makefile« script to run toolchain
- Latest Toolchain Installation Guide as PDF



LiteX¹

Build your hardware, easily!



[1] <https://github.com/enjoy-digital/litex>

LiteX¹

Build your hardware, easily!

CPUs

runs Linux

- VexRiscv (-smp)
- PicoRV32
- SERV
- NeoRV32
- ARM Cortex-M
- ... (+24 more)

Periphery (via : wishbone, axi, axi-lite)

- S-ATA
- PCIexpress
- DDR2/3/4, HyperRAM
- VGA, DVI, HDMI
- Ethernet
- SD-card, SPI
- JESD204B (ADC, DAC)
- ...

[1] <https://github.com/enjoy-digital/litex>



VexRiscv with HyperRAM and HDMI

GateMate Evaluation Board

Interfaces

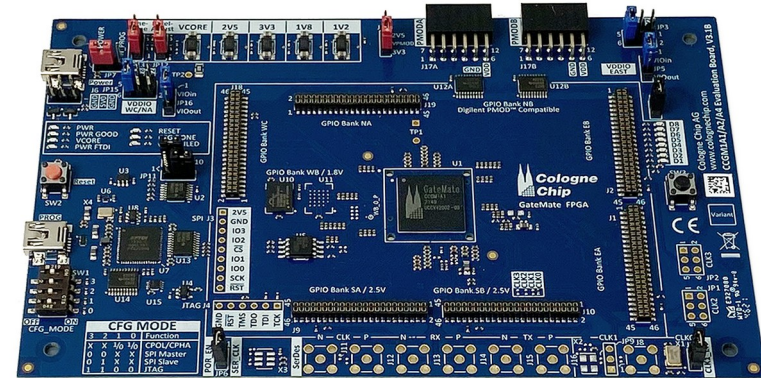
- Six I/O banks + access to SPI/JTAG signals
- Two standard 12-pin Pmod™ compatible connectors
- One high-speed SerDes RX, TX + CLK channel via SMA
- Configuration via flash or on-board USB to SPI/JTAG bridge

Memory

- 64 Mbit Quad-I/O SPI flash
- Up to two HyperBus modules (HyperRAM / HyperFlash)

Power

- User-selectable core and I/O voltages

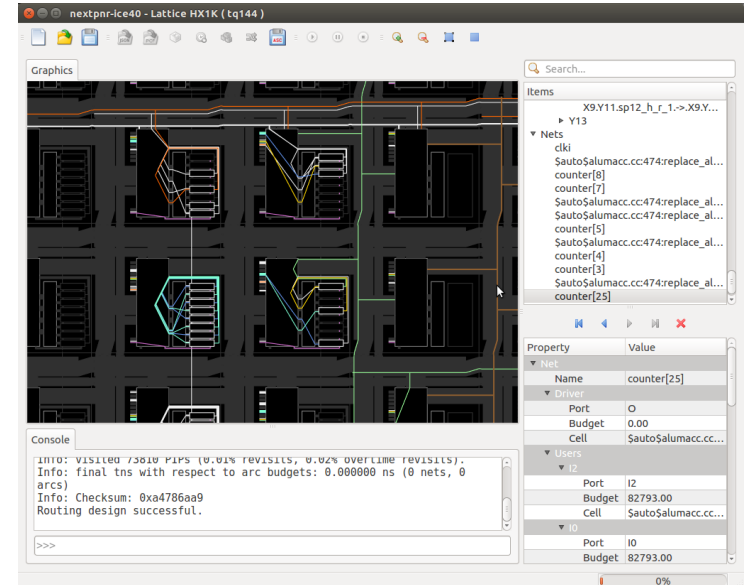


[Link to
Evaluation Kit](#)

Outlook

2024 Roadmap

- Bitstream Copy Protection IP (EW 2024)
- »nextpnr« support
 - Step 1: Full disclosure of TileGrid and timing data for ChipDB and bitstream generator
 - Step 2: Actual »nextpnr« support
- GateMate A2
 - Engineering Samples available now
- IP Core Support
 - [TDC](#), [MIPI](#), [HDMI](#), [Ethernet](#)



High Resolution TDC using GateMate CP-lines

Time-to Digital Converter

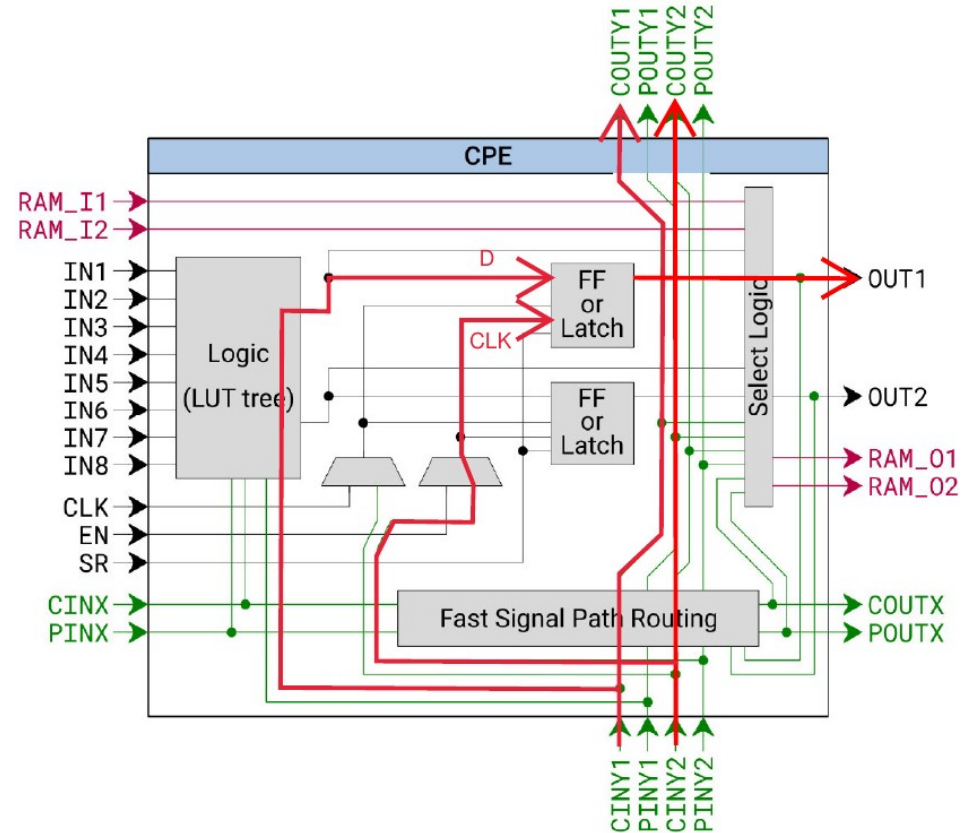
Using CPE CP-lines

Basics

- Measure the time interval between events with high precision
- Widely used in high-energy physics experiments, medical imaging, ...

CC-FPGA-TDC

- Asynchronous input signal runs through Carry Chain
- Position of the 0/1 transition is stored in FF at the next event of system clock on Propagation Chain
- 5 ps resolution



CPE Vision

Implementation and Resource Utilization

- Chain length: 128 CPEs
- Max. Rows: 160
- Easy TDC instantiation using primitive:

```
module tdc_top (  
    input wire clk, data,  
    output wire q127  
);  
    wire clk_i;  
    wire [127:0] q;  
  
    CC_BUFG bufg_inst (  
        .I(clk),  
        .O(clk_i)  
    );  
  
    (* blackbox *) (* keep *)  
    CC_GSI_TDC #(  
        .COLUMN(4)  
    ) tdc_inst0 (  
        .CLK(clk_i),  
        .DATA(data),  
        .Q(q)  
    );  
  
    assign q127 = q[127];  
endmodule
```



CPE Array 160x128

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