PANDA Readout Time Structure

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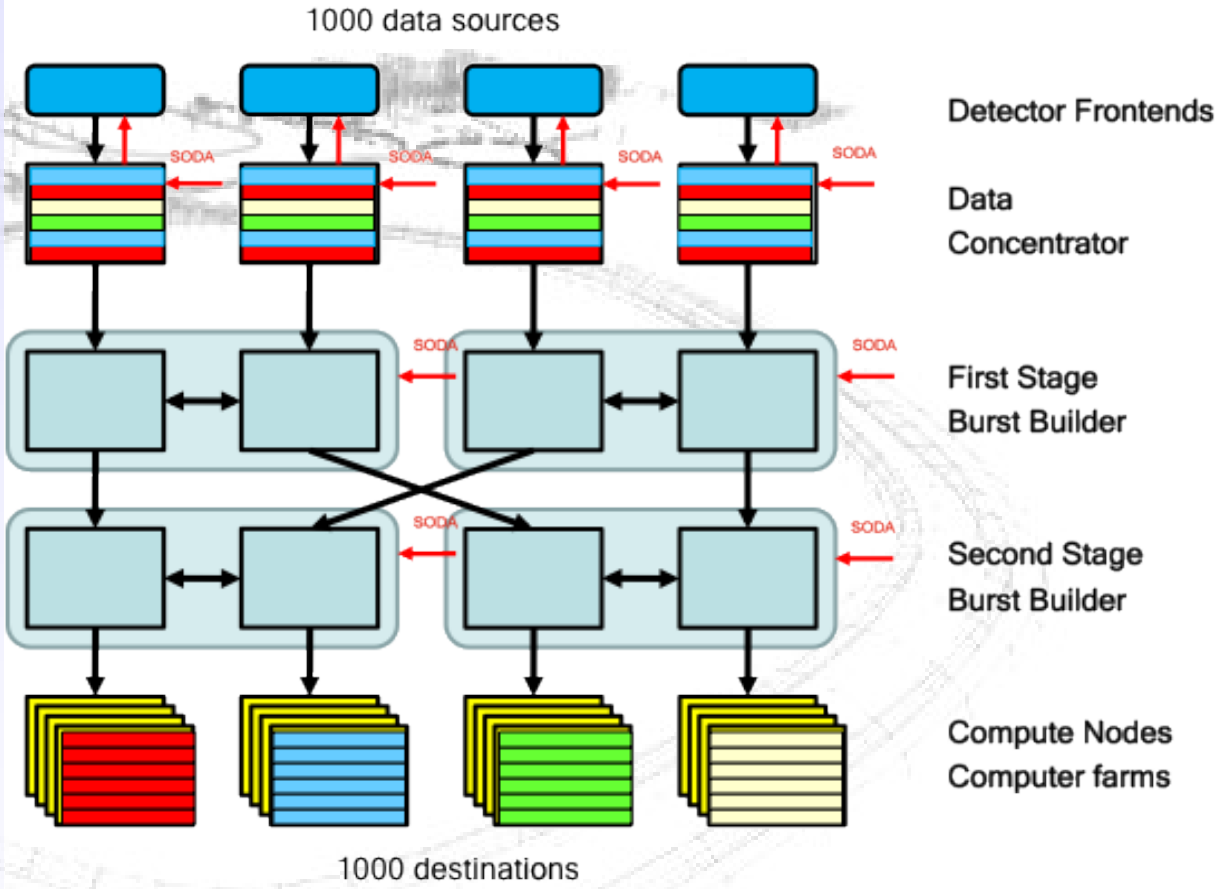
- PANDA DAQ Overview
- Time Structure
- SODA Operation
- Conclusions

PANDA DAQ Overview

Self triggered readout

- Components:
  - Time distribution system
  - Intelligent frontends
  - Powerful compute nodes
  - High speed network
- Data Flow:
  - Data reduction
  - Local feature extraction
  - Data burst building
  - Event selection
  - Data logging after online reconstruction

➔ **Programmable Physics Machine**



Time Structure

- HESR is a storage ring
  - Debunched particle flux
  - No microscopic time structure
- Energy loss in target
  - Cavity for compensation: *barrier bucket*
  - Gap needed to re-accelerate anti-protons
  - Induces time structure
- HESR time structure:
  - Circumference 2 µs
  - Acceleration gap 20%, i.e. 400 ns
  - One HESR cycle is called *burst*
- Grouping 256 bursts into one *super burst*
  - Data of one super burst to arrive at one destination

SODA Operation

- SODA provides:
  - Stable clock for all FEE modules
    - jitter < 20 ps
    - 155.55 MHz
  - Synchronisation of DAQ by regular global resets
  - Structuring readout signals
  - Multiplexing via Concentrators and/or passive splitters
- FEE timestamps
  - Coarse time stamp 6 ns ~ clock
  - TDC measures fine time w.r.t. clock
  - ADC FEE reconstructs fine time w.r.t. clock
- Synchronisation
  - Time bits correlated to frequency of global resets
  - Suitable max. frequency: every burst

SODA Output Signals

Igor Konorov's SODA design

- Clock 155.52 MHz LVDS@2.5V
  - Fulfills jitter requirements
- Signals synchronous to SODA clock, LVTTL@2.5V
  - *Global Reset*
  - *Burst*, '1'- Burst ON
  - *Run Active*, '1' – Run Active
  - *Super Burst*, pulse at start of new SBurst
  - *Destination Enable*, '1' - enable
  - *Trigger*, pulse signal(optional signal)
  - *JTAG* (optional)
  - 6 reserved bits
- Data delivered via high speed serial link, Aurora protocol:
  - Burst Time Tag, 8 bits, time within one burst
  - Burst Number, 8 bits, burst number within super burst
  - Super burst Number, 24(32) bits, super burst number within Run

Conclusions

- Data flow:
  - All pieces of data have a time stamp
  - Buffering to accommodate latencies within the same FE/concentrator
  - No common signal marking individual events
- Key questions to DAQ
  - Full event building before selection?
  - Sub-event building for software trigger?
  - Tracking needed for event building?
- Design questions to SODA
  - Control signals?
  - Return lines?
  - Integration into DAQ fibres?
  - Soft core or mezzanine?
  - Passive or active multiplexing?