VMM3A SOFTWARE AND DAQ INTEGRATION

Leandro Milhomens da Fonseca

SUMMARY

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- 2.1 – Software components
- 2.2 – Plans for future

3 – DAQ
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- 3.2 – New plan

4 – Setup@GSI

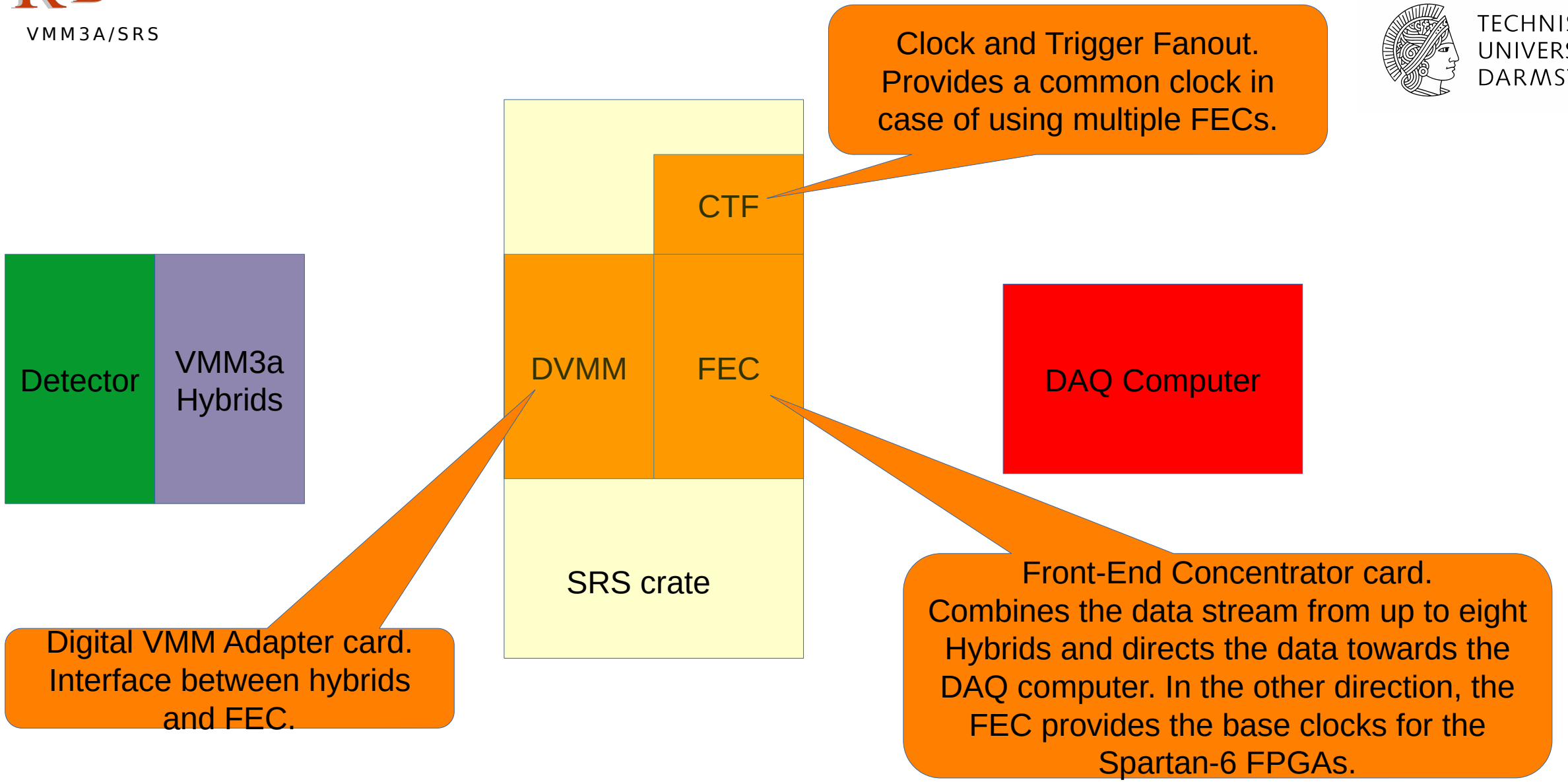
VMM3a – 64-channel front-end ASIC developed at the Brookhaven National Laboratory.

SRS – Scalable Readout System – multi-purpose and highly versatile readout system developed by the RD51 Collaboration.

The goal of the SRS is to provide a common and scalable read-out structure, that can be used independently of the detector type, starting from a few read-out channels and going to several thousand.

Hybrid PCB - Contains 2 VMM3a, the connector to plug it onto the detector and additionally required electronics and a FPGA (Xilinx Spartan 6).

The hybrid was built to integrate the VMM3a chips with the SRS.


Clock and Trigger Fanout. Provides a common clock in case of using multiple FECs.
CTF
Detector
VMM3a Hybrids
DVMM
FEC
DAQ Computer
SRS crate
Digital VMM Adapter card. Interface between hybrids and FEC.
Front-End Concentrator card. Combines the data stream from up to eight Hybrids and directs the data towards the DAQ computer. In the other direction, the FEC provides the base clocks for the Spartan-6 FPGAs.

Software components for VMM3a/SRS

Control software: RD51 VMM slow control software (vmmsc)

Raw data monitor: Wireshark

Data acquisition for offline analysis: tcpdump

Offline reconstruction and online monitoring: vmm-sdat

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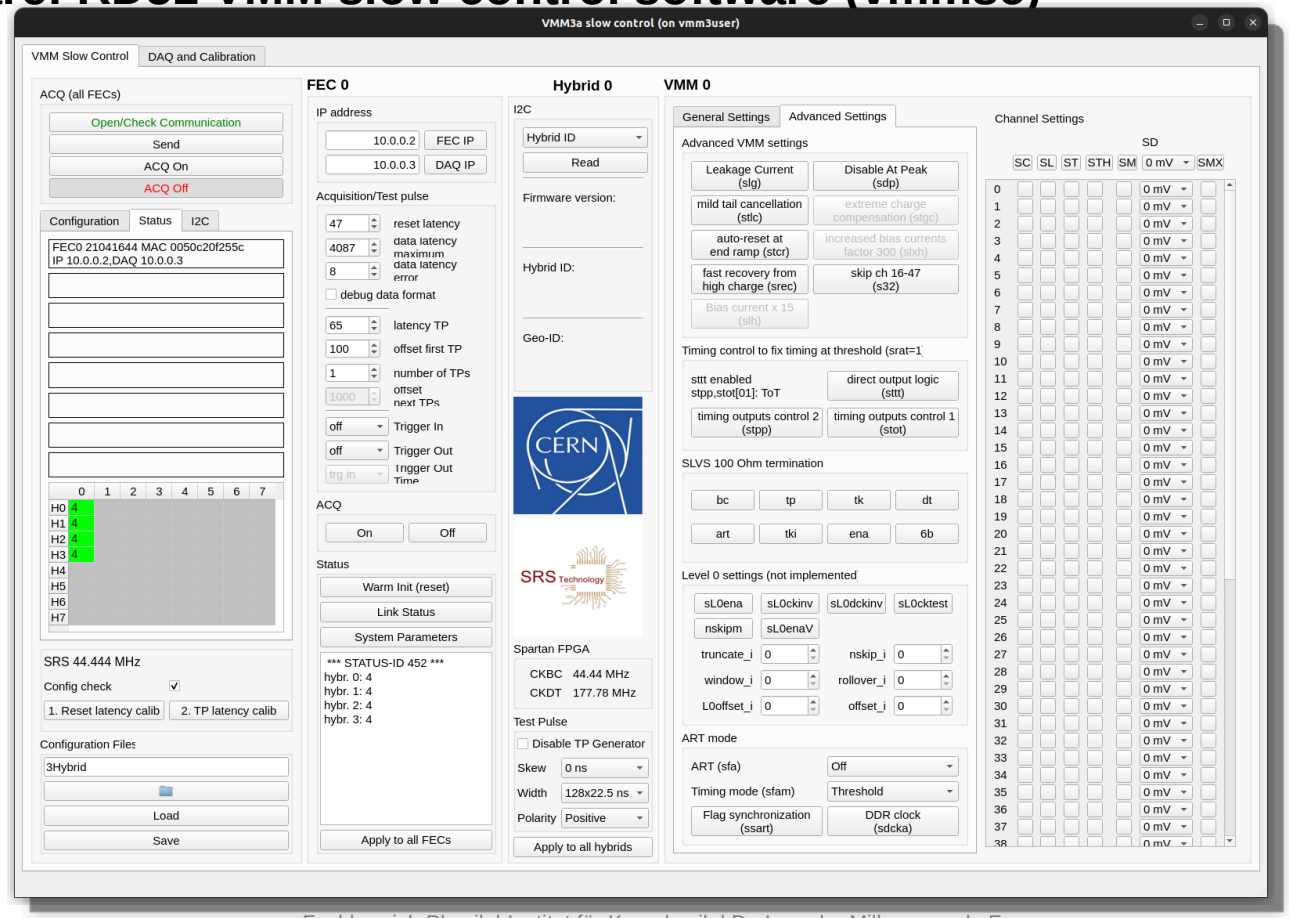

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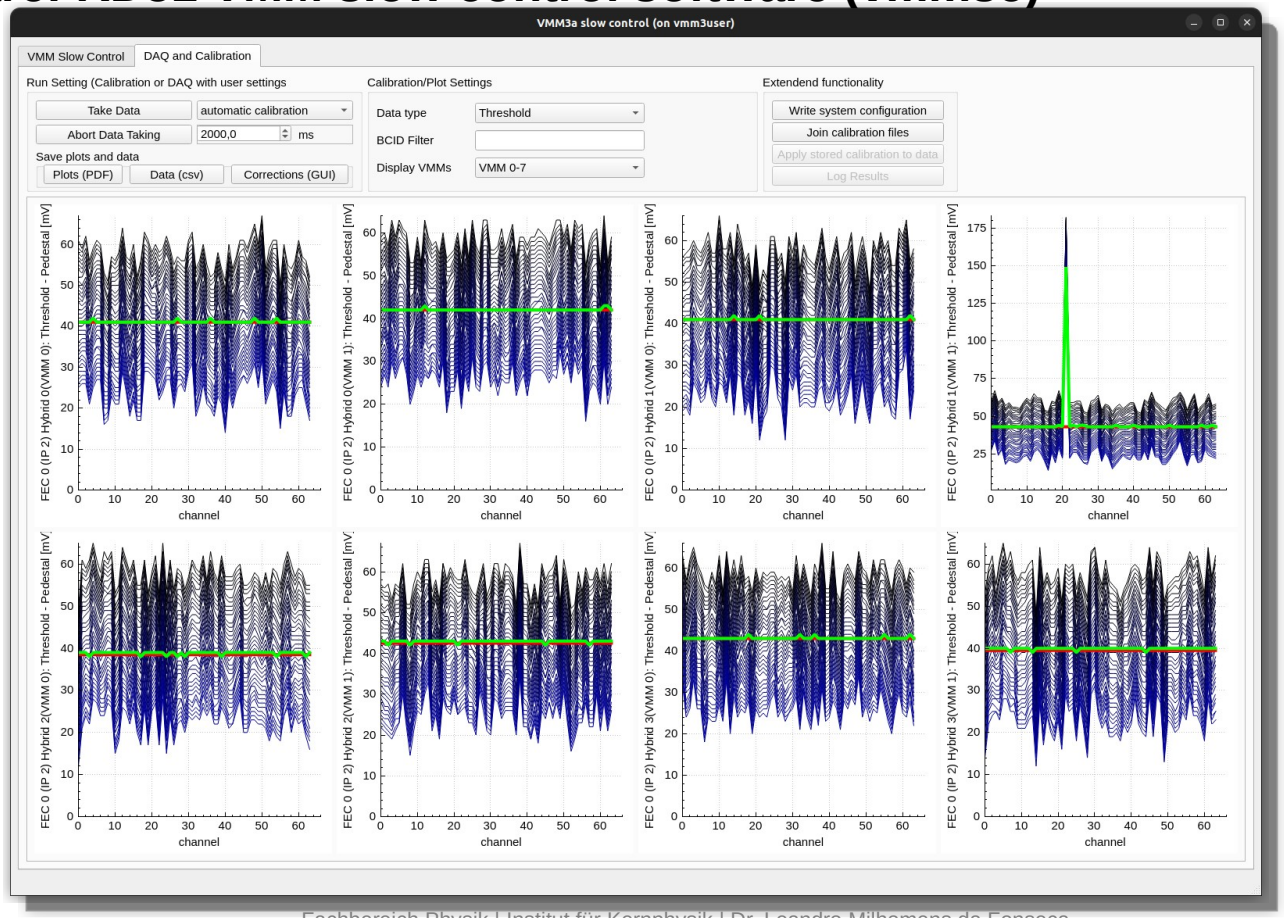

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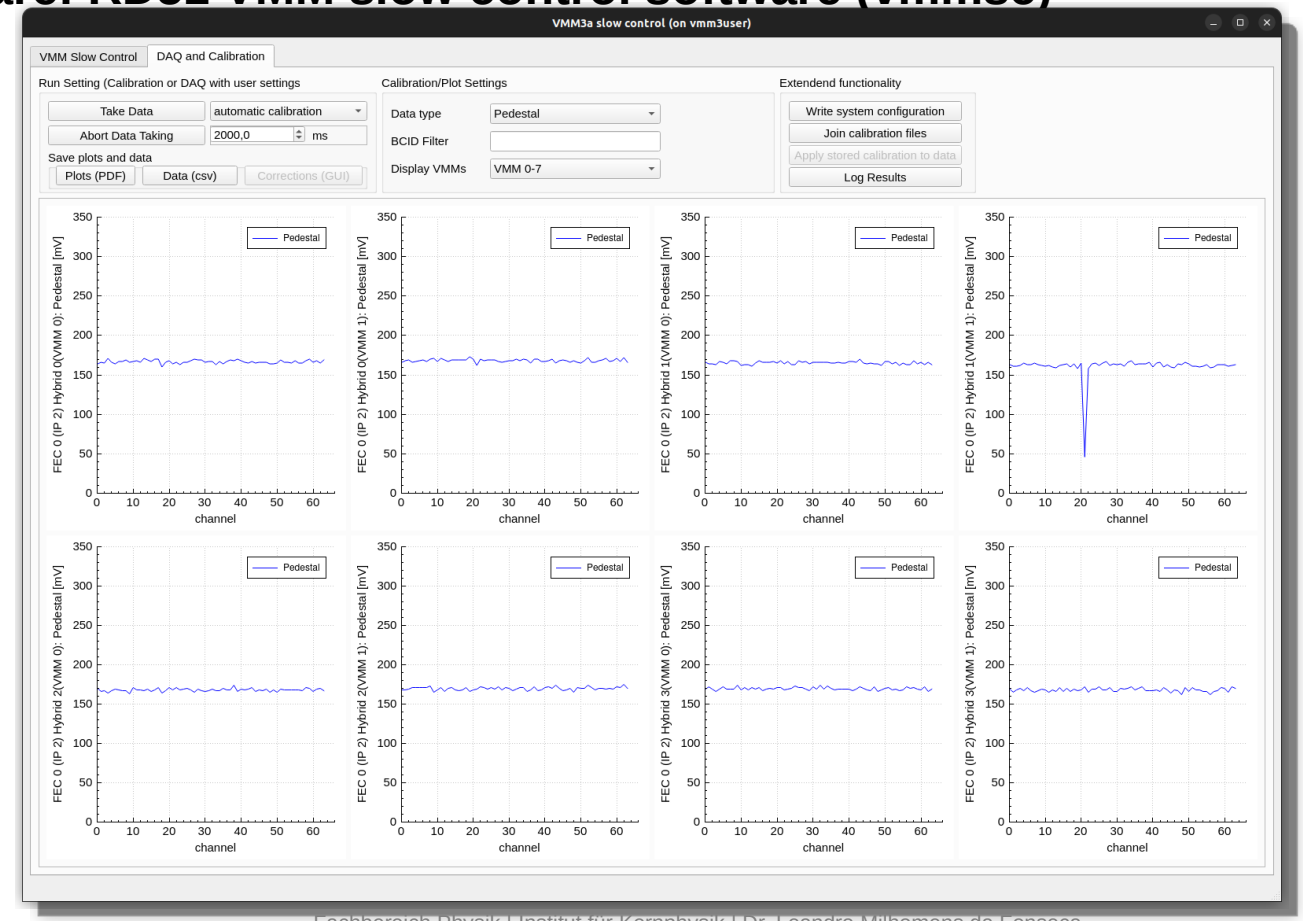

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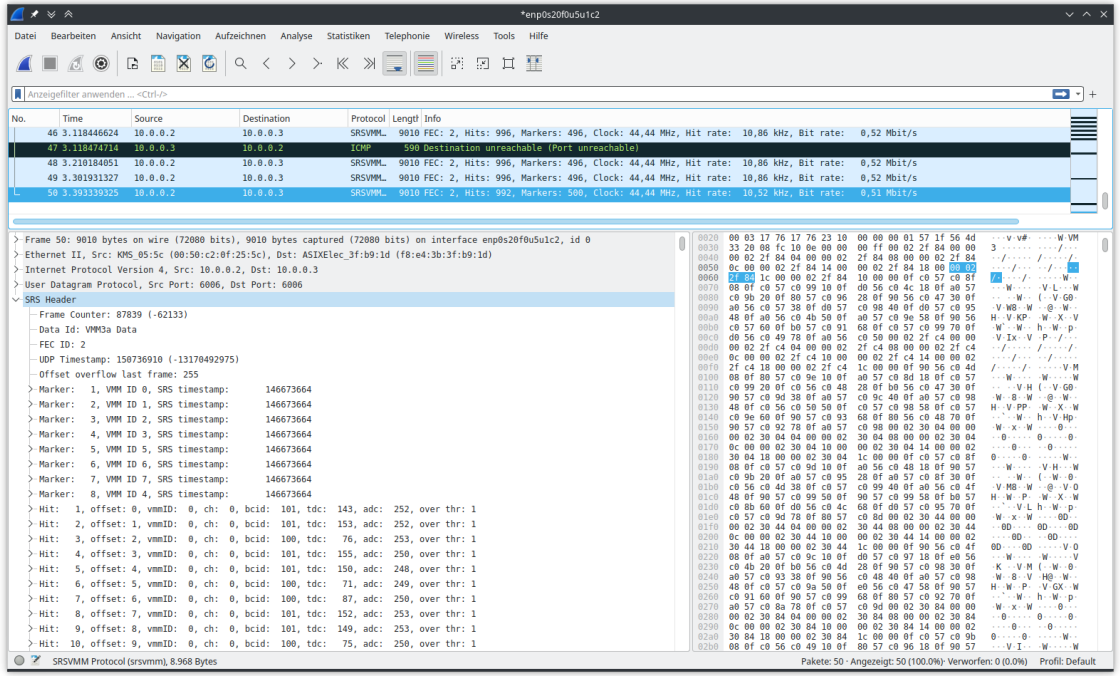
Network protocol analyzer




```
Marker:   8, VMM ID 4, SRS timestamp:       146673664
Hit:   1, offset: 0, vmmID:  0, ch:  0, bcid:  101, tdc:  143, adc:  252, over thr: 1
Hit:   2, offset: 1, vmmID:  0, ch:  0, bcid:  101, tdc:  153, adc:  252, over thr: 1
Hit:   3, offset: 2, vmmID:  0, ch:  0, bcid:  100, tdc:   76, adc:  253, over thr: 1
Hit:   4, offset: 3, vmmID:  0, ch:  0, bcid:  101, tdc:  155, adc:  250, over thr: 1
Hit:   5, offset: 4, vmmID:  0, ch:  0, bcid:  101, tdc:  150, adc:  248, over thr: 1
Hit:   6, offset: 5, vmmID:  0, ch:  0, bcid:  100, tdc:   71, adc:  249, over thr: 1
Hit:   7, offset: 6, vmmID:  0, ch:  0, bcid:  100, tdc:   87, adc:  250, over thr: 1
Hit:   8, offset: 7, vmmID:  0, ch:  0, bcid:  101, tdc:  152, adc:  253, over thr: 1
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Data acquisition for offline analysis: tcpdump

Command-line packet analyzer

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Raw data monitor: Wireshark

Data acquisition for offline analysis: tcpdump

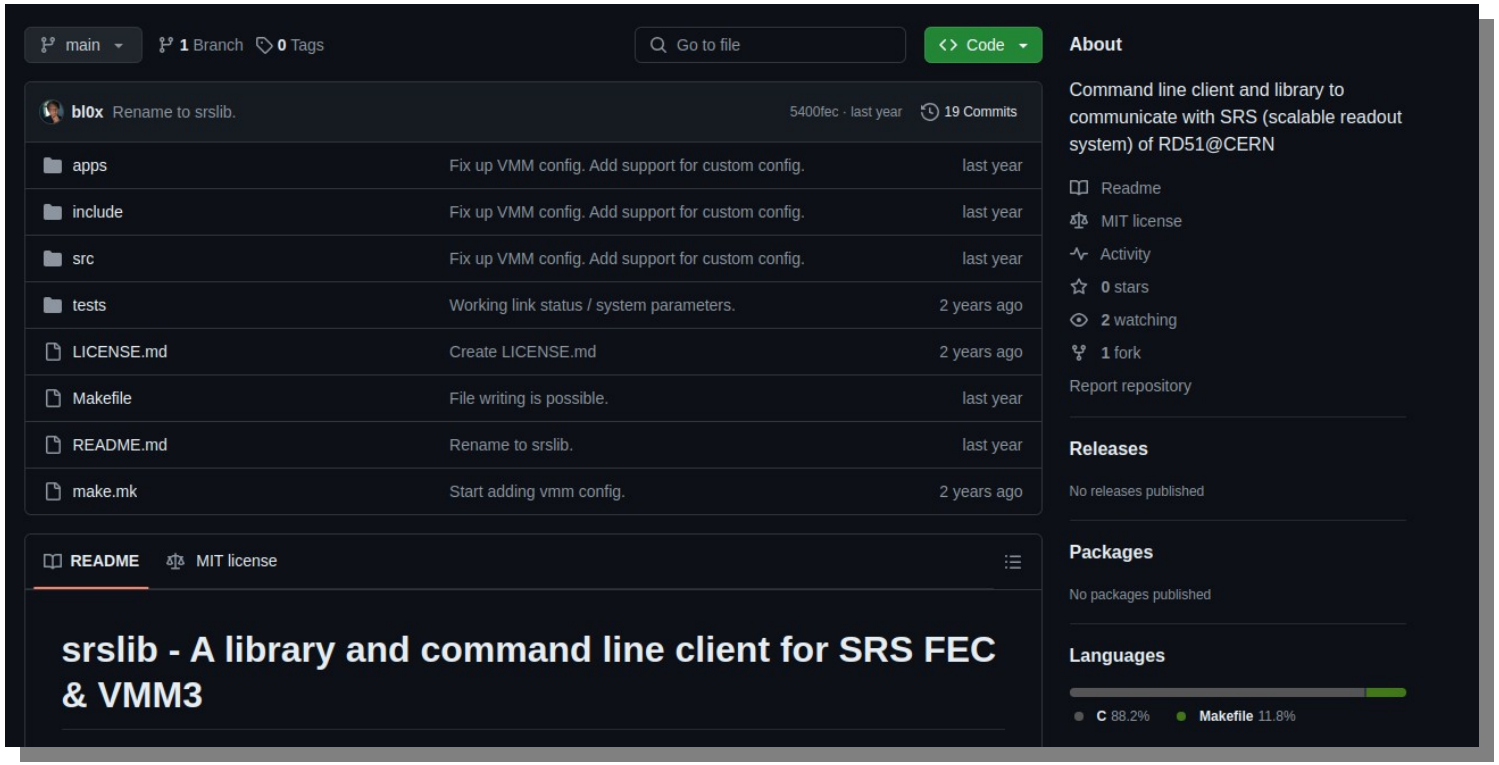
Offline reconstruction and online monitoring: vmm-sdat

VMM3a/SRS Data Analysis Tool: Analysis software for VMM3a data, recorded with the SRS or the ESS readout as PCAPNG file. From the PCAPNG file, a root tree with the hits and clusters is created.

Plans for future

srslib - A library and command line client for SRS FEC & VMM3

Development started by Bastii



R3B SOFTWARE

GSI TECHNISCHE UNIVERSITÄT DARMSTADT

Plans for future

srslib - A library and command line client for SRS FEC & VMM3

Included:

Control/monitoring for SRS FEC & VMM3a hybrids
Readout of data

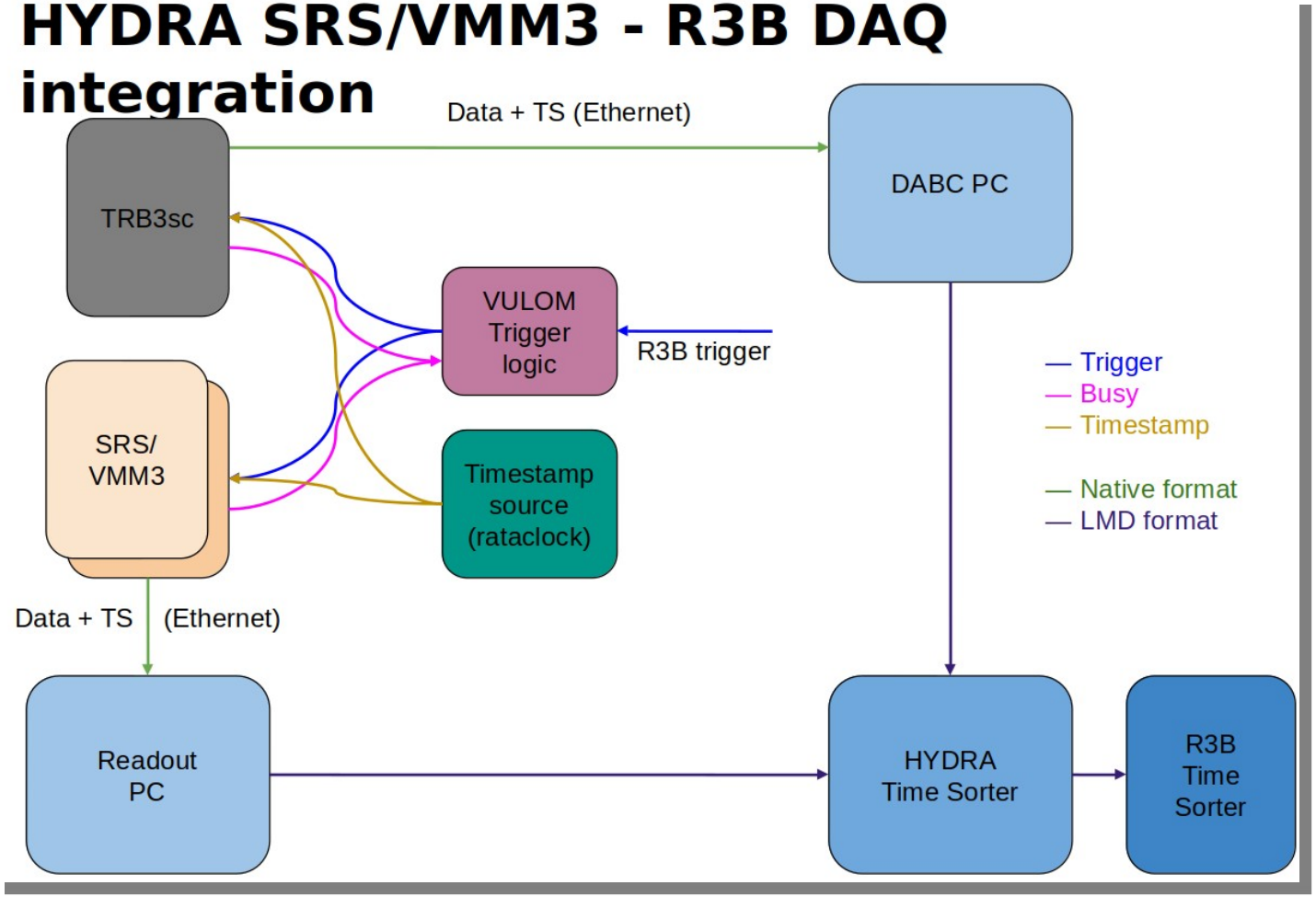
Not (yet) included:

Calibration routines
Graphical user interface
Sophisticated data transport

Work will be done by me in the next months.
Any help is welcome.

Previous plan

Slide from Bastii's presentation from Jan/2023



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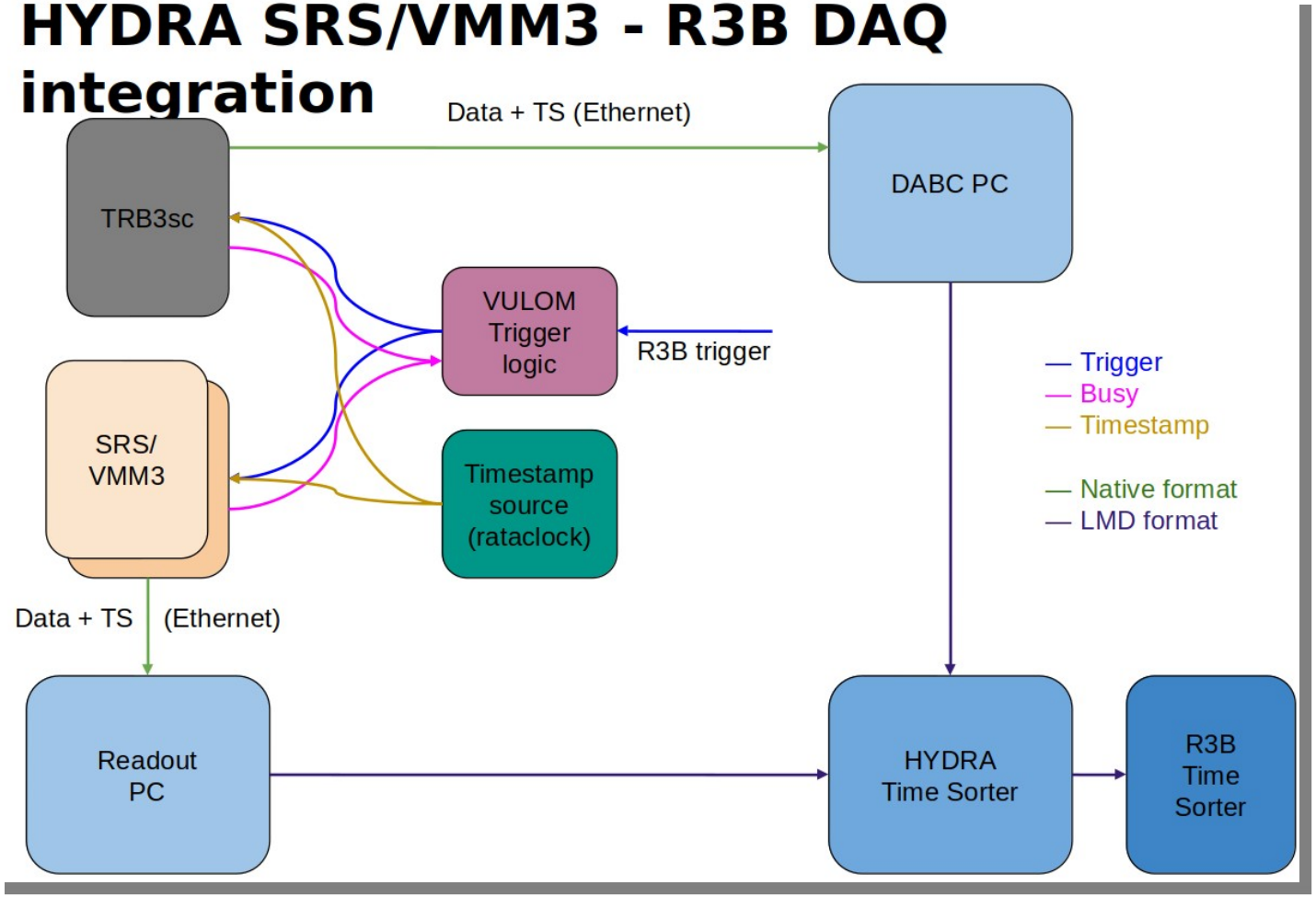

Needs firmware modification

No help from VMM/SRS group for this

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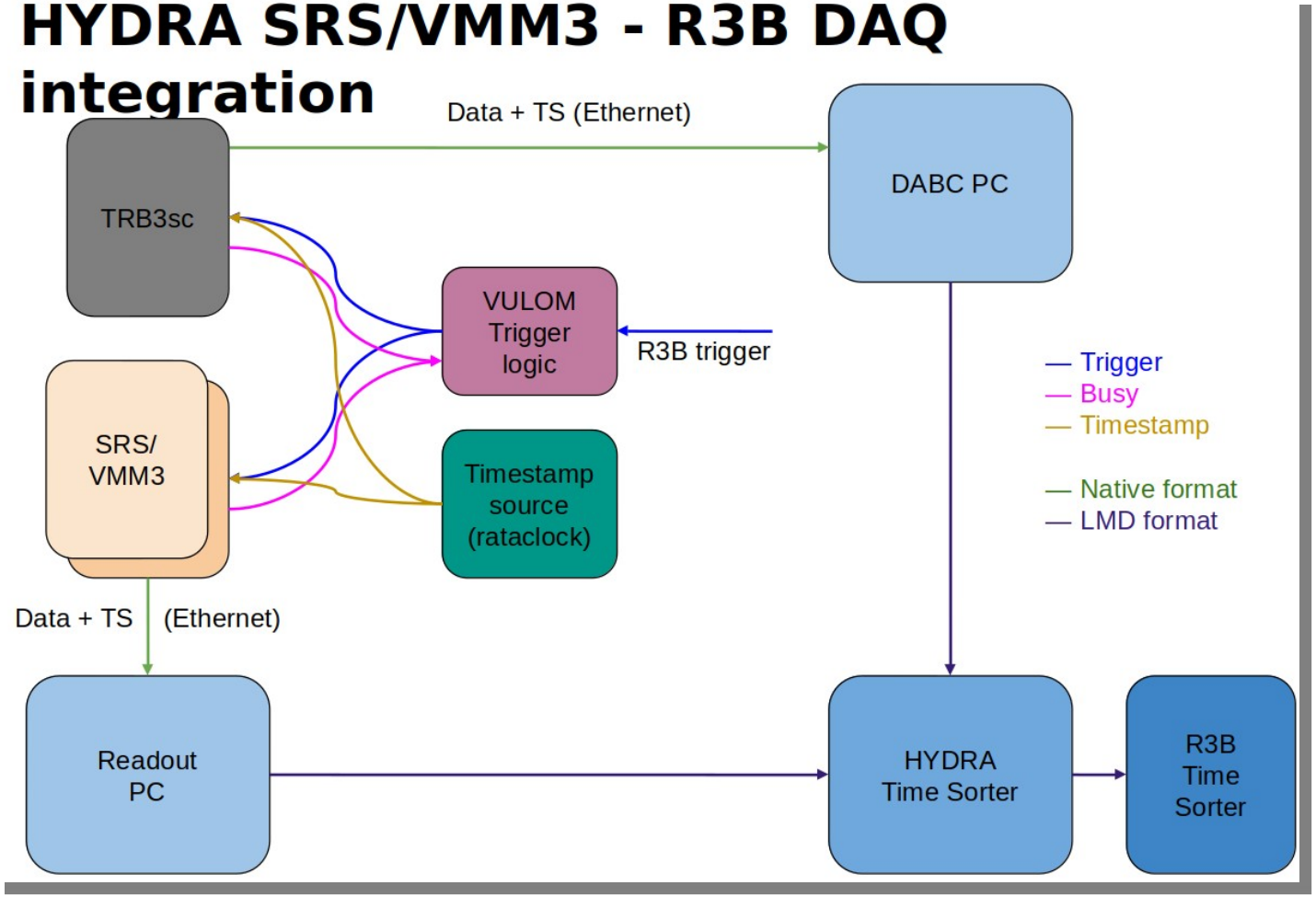

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WE NEED A NEW PLAN

New plan

Bastii suggested using Heimtime, based on his experience with the AMBER collaboration.

"**In order to rather easily share a common time reference with foreign DAQ systems that have no means to use e.g. the serial time protocol, a simple "speaking clock" protocol is implemented.**

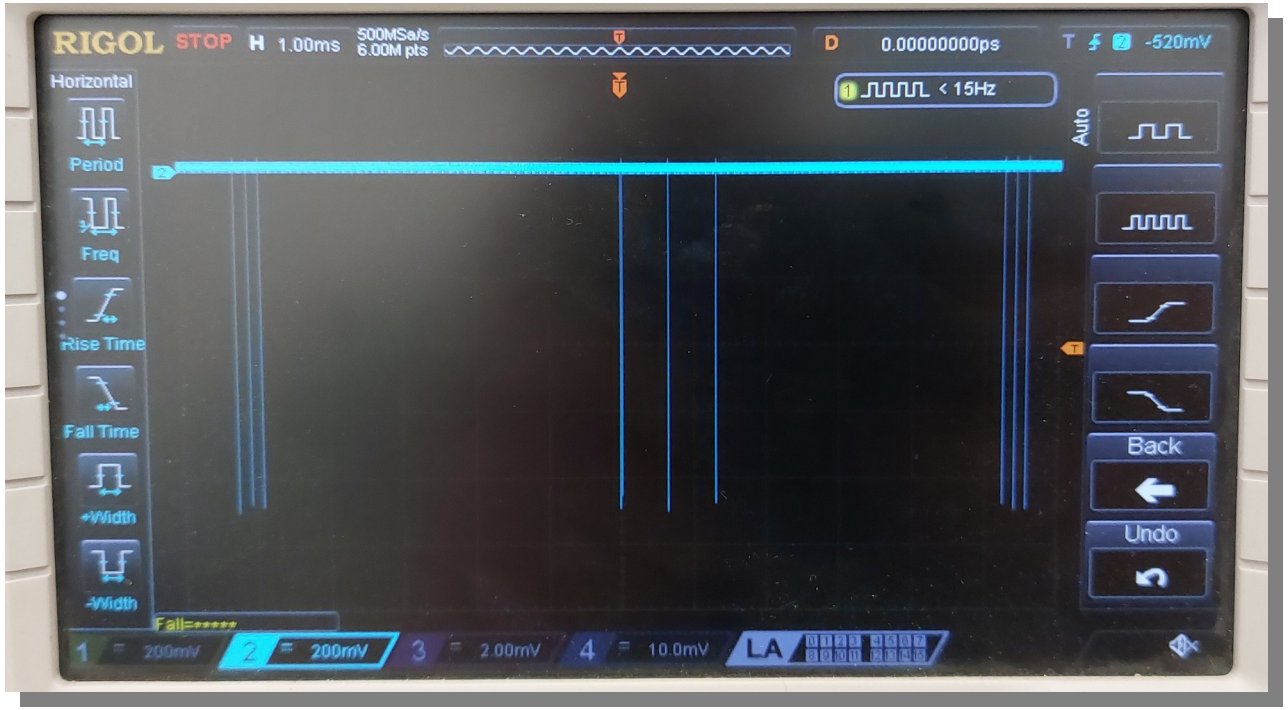
Provided that the foreign DAQ system is able to locally timestamp a received logical signal, it can receive the periodic signals of the heimtime protocol, and **during analysis the common time scale (as provided by the TRLO II) can be recovered**.

The protocol consists of two parts. **Every 2^19 local clock cycles a pulse is generated.** With the local clock of 100 MHz this means every 5.24288 ms (or 190.7 Hz of signals). In order to tell time, for 32 pulses starting every 2^26 ticks (or 128 pulses, or about 0.671 s apart), it delivers two additional pulses. **They either have a separation of 0.16384 or 0.65536 ms. The short separation means 0, and the long separation means 1, in a 32-bit time stamp.** The 32-bit time-stamp starts at local bit 24.

For analysis, reception of one full time message would be enough, as it then can perform dead counting of the pulses. It is naturally recommended to continuously verify that the received timestamps match with the previous ones.

The reason for having both this and the serial timestamp protocol is that the serial protocol lends itself to easy FPGA decoding and precision following, while this Heimtime protocol allows for rather straightforward handling in analysis, without requiring tremendous amounts of data to be recorded by the foreign DAQ system."

Text from the TRLO II documentation (https://fy.chalmers.se/~f96hajo/trloii/vulom4_trlo/)



New plan

HYDRA TPC - VMM3 readout

Hardware	VMM3 front-end + SRS
Particular software / firmware	Software to be decided Standard CERN firmware
Synchronisation	Heimtime
Trigger	System is free running, trigger must happen online in software
Slow control	Electronics: Signal shape, thresholds Gas: — Laser: —
Deadtime	readout rate 3.6 MHz/channel
Stability	Untested

	Red	Orange	Yellow	Green
Timing/sync	To be done, inject Heimtime to the TPC Front-End PCBs			
Data flow	To be done, send hits data to event builder, send to time-order			
Trigger	No external trigger input, but will send Master Start to the TPC Front-End PCBs No internal trigger output.			
Run Ctrl	Requires special startup sequence			
Slow Ctrl	No EPICS interface			
Deadtime	Unknown			
Downtime	Unknown			
Stability	Untested.			
Documentation	New developments undocumented			Original documentation available here

HYDRA TPC is a new detector in R3B. We will try to gather as much as documentation as possible.

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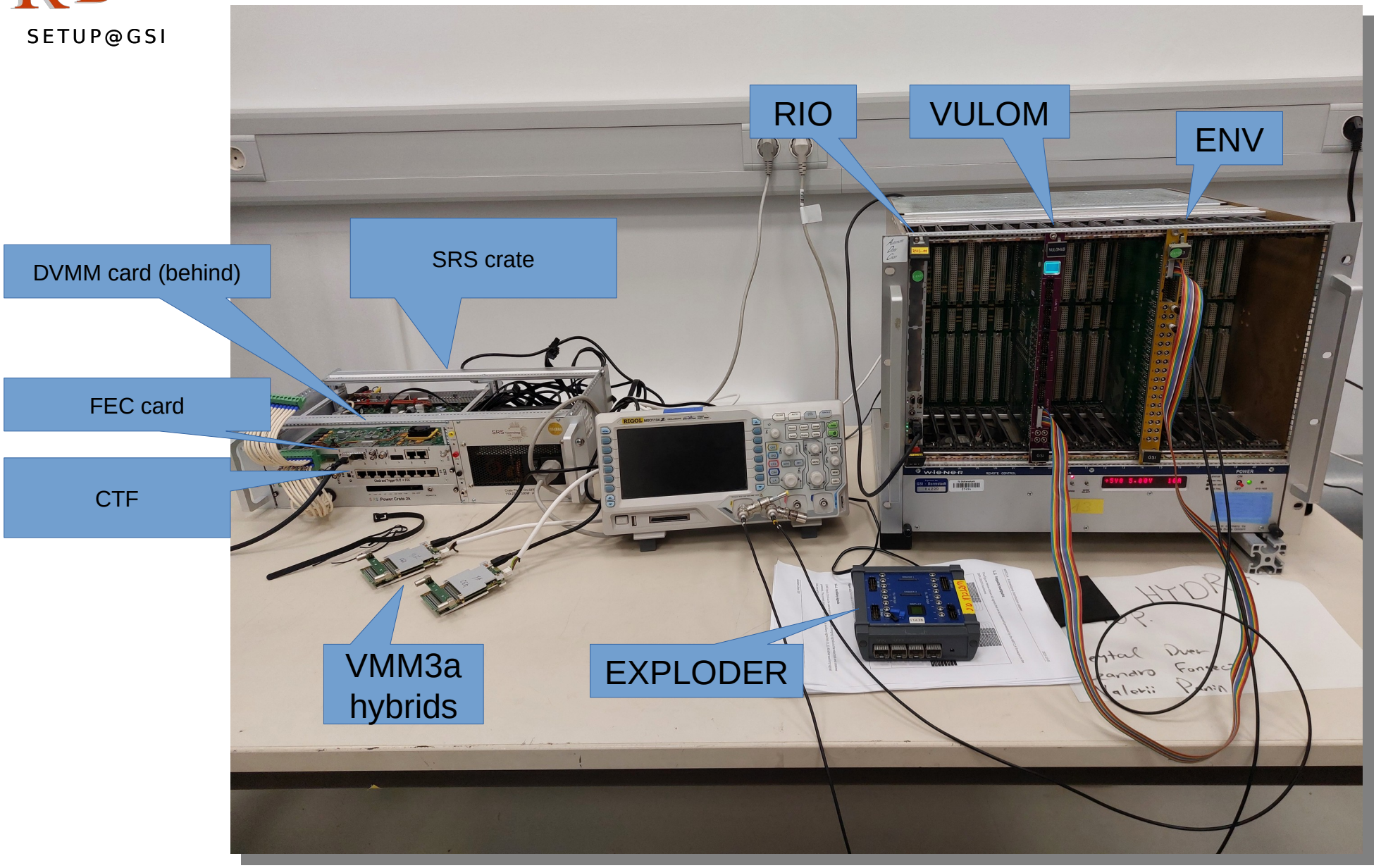
Experts from the RD51 CERN group will be contacted for help and advices.

Hans will support the implementation of the event builder.

Tasks to be finished until the end of the year.

Valerii is involved in this work, helping us.


RIO
VULOM
ENV
SRS crate
DVMM card (behind)
FEC card
CTF
VMM3a hybrids
EXPLODER