

VMM3A SOFTWARE AND DAQ INTEGRATION

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1 – VMM3a/SRS

2 – Software

2.1 – Software components

2.2 – Plans for future

3 – DAQ

3.1 – Previous plan

3.2 – New plan

4 – Setup@GSI

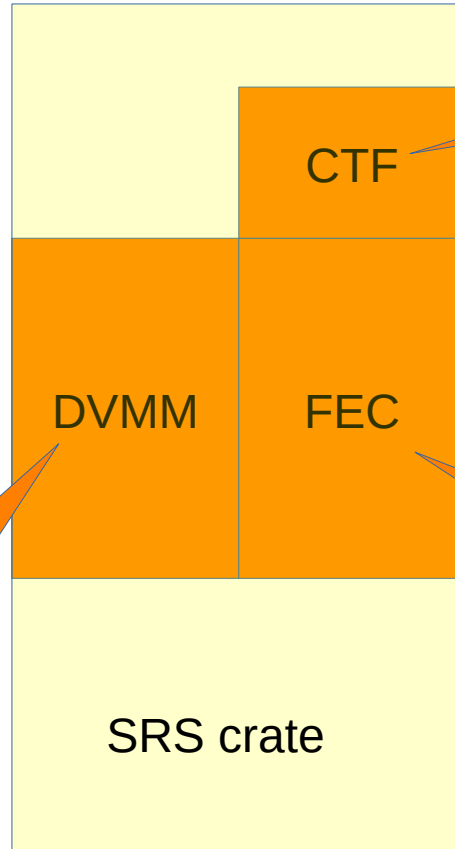
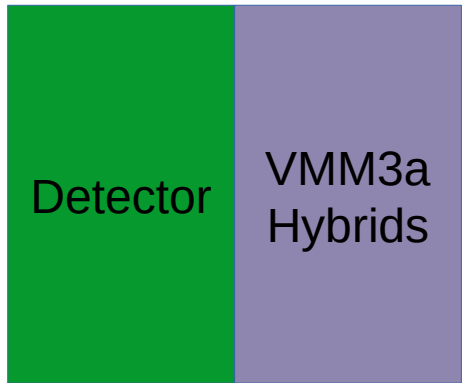
VMM3a – 64-channel front-end ASIC developed at the Brookhaven National Laboratory.

SRS – Scalable Readout System – multi-purpose and highly versatile readout system developed by the RD51 Collaboration.

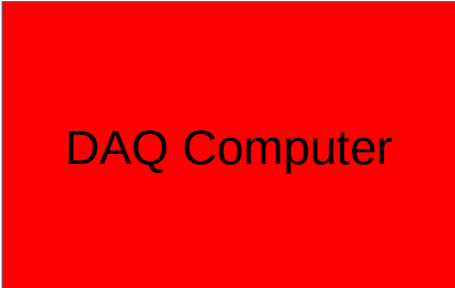
The goal of the SRS is to provide a common and scalable read-out structure, that can be used independently of the detector type, starting from a few read-out channels and going to several thousand.

Hybrid PCB - Contains 2 VMM3a, the connector to plug it onto the detector and additionally required electronics and a FPGA (Xilinx Spartan 6).

The hybrid was built to integrate the VMM3a chips with the SRS.



Clock and Trigger Fanout. Provides a common clock in case of using multiple FECs.



Digital VMM Adapter card. Interface between hybrids and FEC.

Front-End Concentrator card. Combines the data stream from up to eight Hybrids and directs the data towards the DAQ computer. In the other direction, the FEC provides the base clocks for the Spartan-6 FPGAs.

Software components for VMM3a/SRS

Control software: RD51 VMM slow control software (vmmsc)

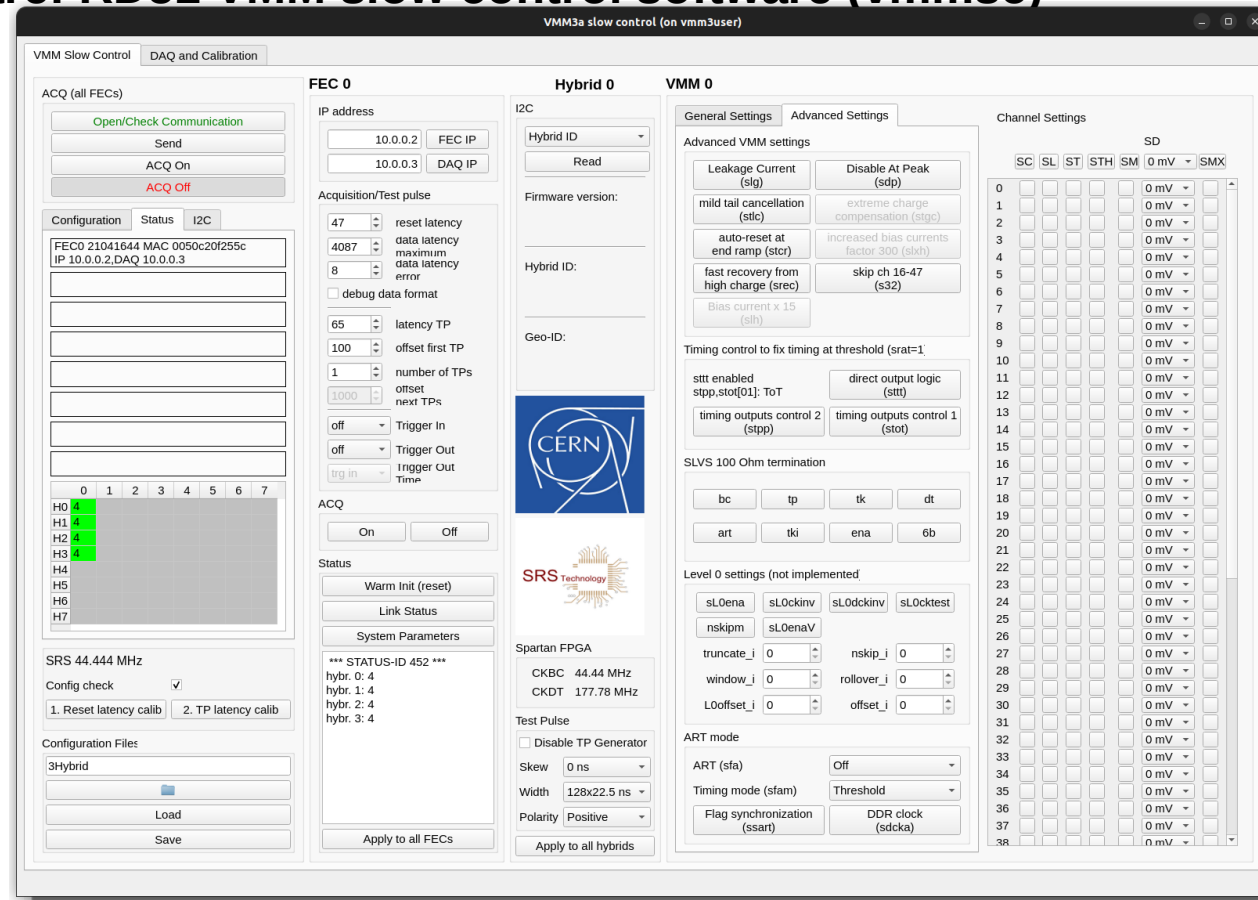
Raw data monitor: Wireshark

Data acquisition for offline analysis: tcpdump

Offline reconstruction and online monitoring: vmm-sdat

Software components for VMM3a/SRS

Control software: RD51 VMM slow control software (vmm3c)

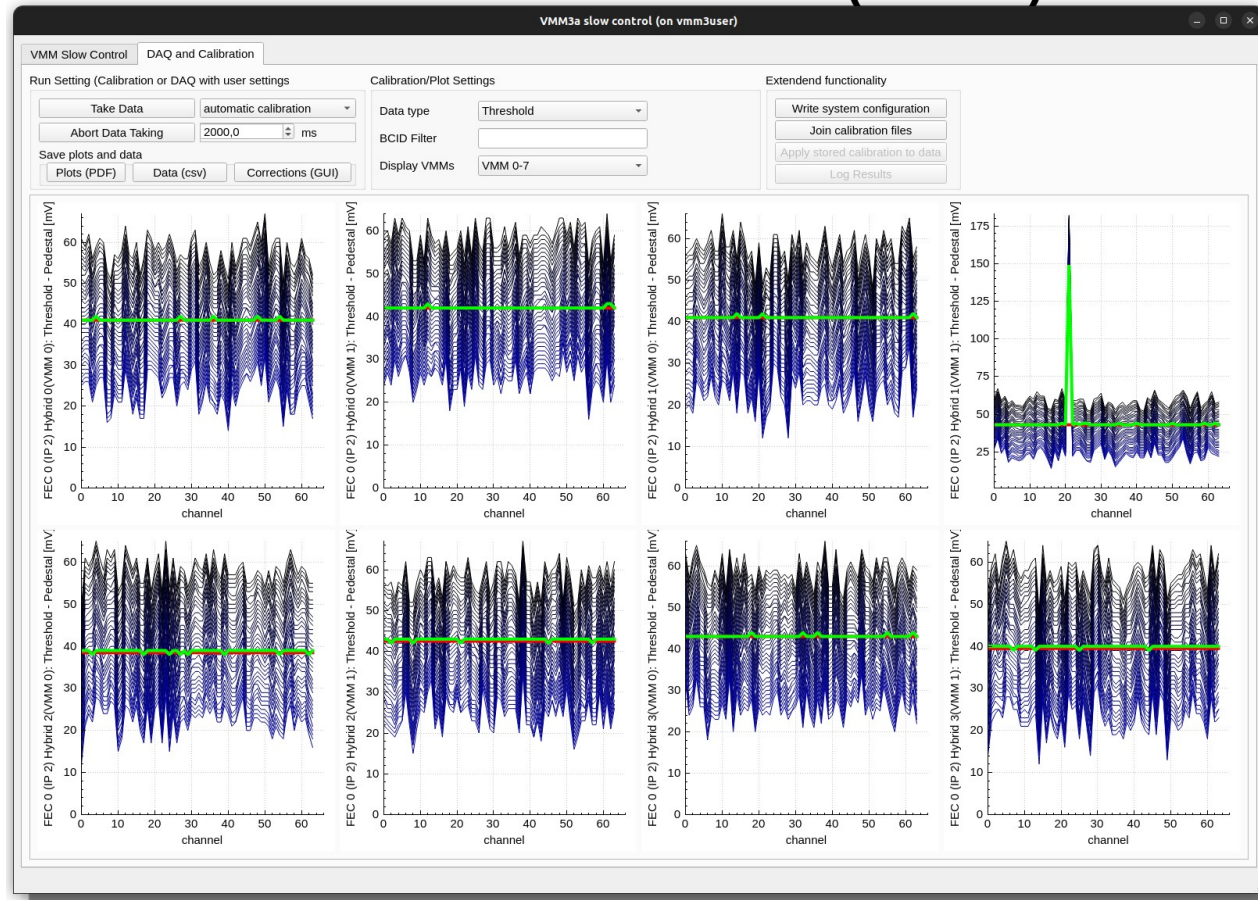


The screenshot displays the 'VMM3a slow control (on vmm3user)' interface, which is divided into several functional areas:

- ACQ (all FECs):** Includes buttons for 'Open/Check Communication', 'Send', 'ACQ On', and 'ACQ Off'. It also features a configuration table with fields for FEC0 (21041644), MAC (0050c20f255c), and IP (10.0.0.2, DAQ 10.0.0.3).
- FEC 0:** Contains IP address settings (10.0.0.2 for FEC IP, 10.0.0.3 for DAQ IP), acquisition/test pulse parameters (e.g., reset latency, data latency, maximum data latency error), and trigger settings (Trigger In, Trigger Out, Trigger Out Time).
- Hybrid 0:** Shows I2C Hybrid ID, Read button, Firmware version, Hybrid ID, and Geo-ID. It also includes logos for CERN and SRS Technology.
- VMM 0:** Divided into 'General Settings' and 'Advanced Settings'. The 'Advanced Settings' section includes parameters for Leakage Current (slg), Disable At Peak (sdp), mild tail cancellation (stc), extreme charge compensation (stgc), auto-reset at end ramp (str), increased bias currents factor 300 (sixh), fast recovery from high charge (srec), skip ch 16-47 (s32), Bias current x 15 (slh), and timing controls (stt, stpp, stot, stot2, stot1).
- Channel Settings:** A table with columns for SC, SL, ST, STH, SM, SD, and SMX, with rows for channels 0 through 38.
- System Parameters:** Displays SRS 44.444 MHz, configuration check status, and system parameters like Warm init (reset), Link Status, and System Parameters.
- Spartan FPGA:** Shows CKBC (44.44 MHz) and CKDT (177.78 MHz) frequencies.
- Test Pulse:** Includes a 'Disable TP Generator' checkbox and skew/width settings.
- ART mode:** Contains settings for ART (sfa), Timing mode (sfam), Flag synchronization (ssart), and DDR clock (sdcka).

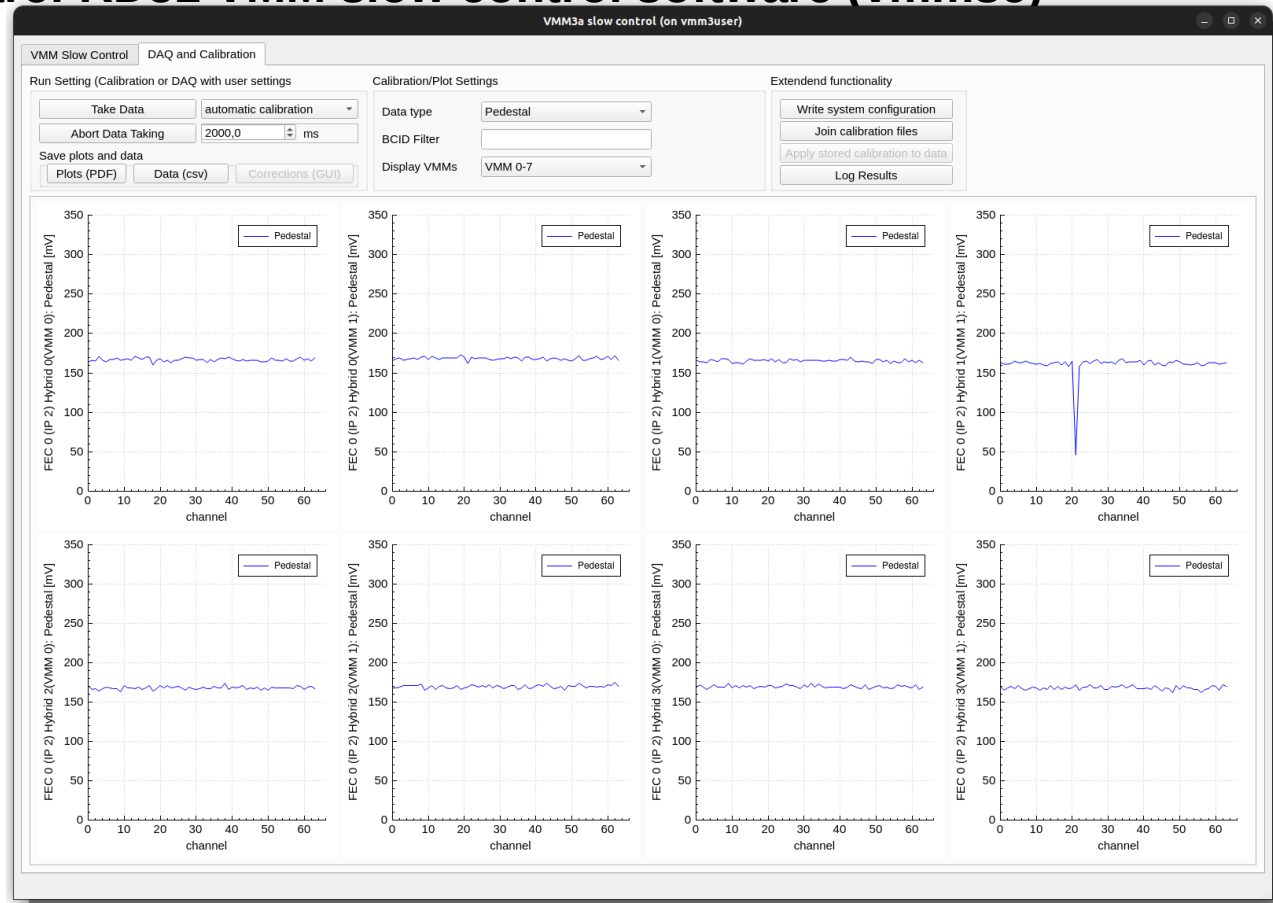
Software components for VMM3a/SRS

Control software: RD51 VMM slow control software (vmmsc)



Software components for VMM3a/SRS

Control software: RD51 VMM slow control software (vmm3sc)

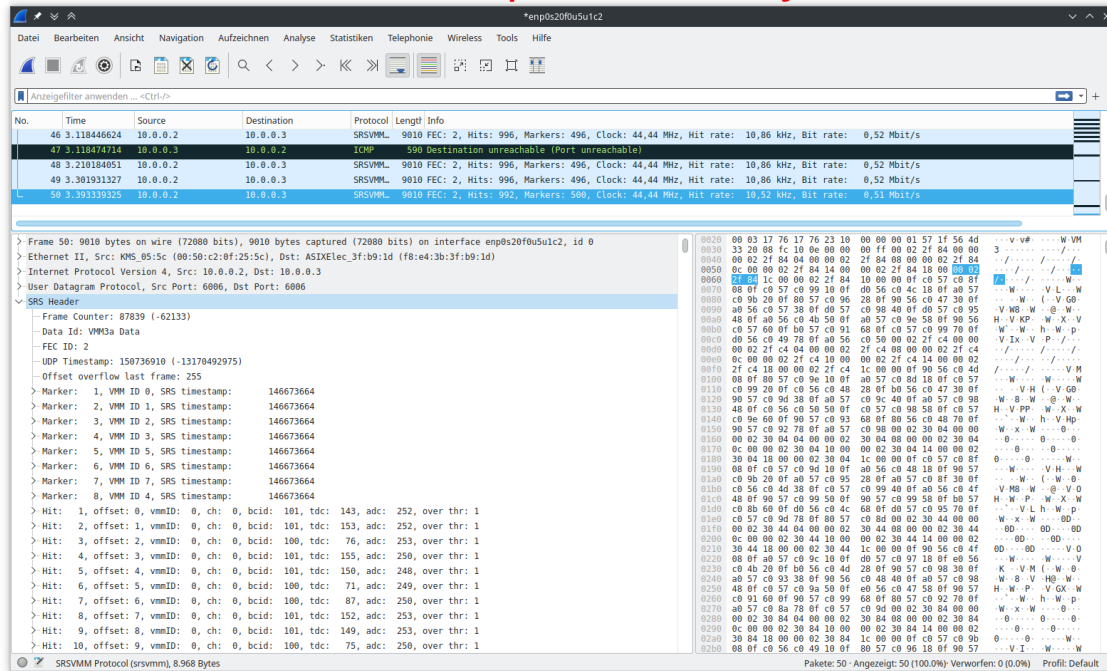


Software components for VMM3a/SRS

Control software: RD51 VMM slow control software (vmm3c)

Raw data monitor: Wireshark

Network protocol analyzer



```

>-Marker:      8, VMM ID 4, SRS timestamp:      146673664
>-Hit:        1, offset: 0, vmmID: 0, ch: 0, bcid: 101, tdc: 143, adc: 252, over thr: 1
>-Hit:        2, offset: 1, vmmID: 0, ch: 0, bcid: 101, tdc: 153, adc: 252, over thr: 1
>-Hit:        3, offset: 2, vmmID: 0, ch: 0, bcid: 100, tdc: 76, adc: 253, over thr: 1
>-Hit:        4, offset: 3, vmmID: 0, ch: 0, bcid: 101, tdc: 155, adc: 250, over thr: 1
>-Hit:        5, offset: 4, vmmID: 0, ch: 0, bcid: 101, tdc: 150, adc: 248, over thr: 1
>-Hit:        6, offset: 5, vmmID: 0, ch: 0, bcid: 100, tdc: 71, adc: 249, over thr: 1
>-Hit:        7, offset: 6, vmmID: 0, ch: 0, bcid: 100, tdc: 87, adc: 250, over thr: 1
>-Hit:        8, offset: 7, vmmID: 0, ch: 0, bcid: 101, tdc: 152, adc: 253, over thr: 1
  
```

Software components for VMM3a/SRS

Control software: RD51 VMM slow control software (vmmsc)

Raw data monitor: Wireshark

Data acquisition for offline analysis: tcpdump

Command-line packet analyzer

Software components for VMM3a/SRS

Control software: RD51 VMM slow control software (vmmsc)

Raw data monitor: Wireshark

Data acquisition for offline analysis: tcpdump

Offline reconstruction and online monitoring: vmm-sdat

VMM3a/SRS Data Analysis Tool: Analysis software for VMM3a data, recorded with the SRS or the ESS readout as PCAPNG file. From the PCAPNG file, a root tree with the hits and clusters is created.

Plans for future

srslib - A library and command line client for SRS FEC & VMM3

Development started by Bastii

The screenshot shows the GitHub repository page for 'srslib'. The repository is owned by 'bi0x' and has 19 commits. The main branch is selected. The repository description is 'Command line client and library to communicate with SRS (scalable readout system) of RD51@CERN'. The repository has 0 stars, 2 watchers, and 1 fork. The repository is licensed under MIT. The repository is currently empty, with no releases or packages published. The repository is written in C (88.2%) and Makefile (11.8%).

File	Description	Last Commit
apps	Fix up VMM config. Add support for custom config.	last year
include	Fix up VMM config. Add support for custom config.	last year
src	Fix up VMM config. Add support for custom config.	last year
tests	Working link status / system parameters.	2 years ago
LICENSE.md	Create LICENSE.md	2 years ago
Makefile	File writing is possible.	last year
README.md	Rename to srslib.	last year
make.mk	Start adding vmm config.	2 years ago

Plans for future

srslib - A library and command line client for SRS FEC & VMM3

Included:

Control/monitoring for SRS FEC & VMM3a hybrids
Readout of data

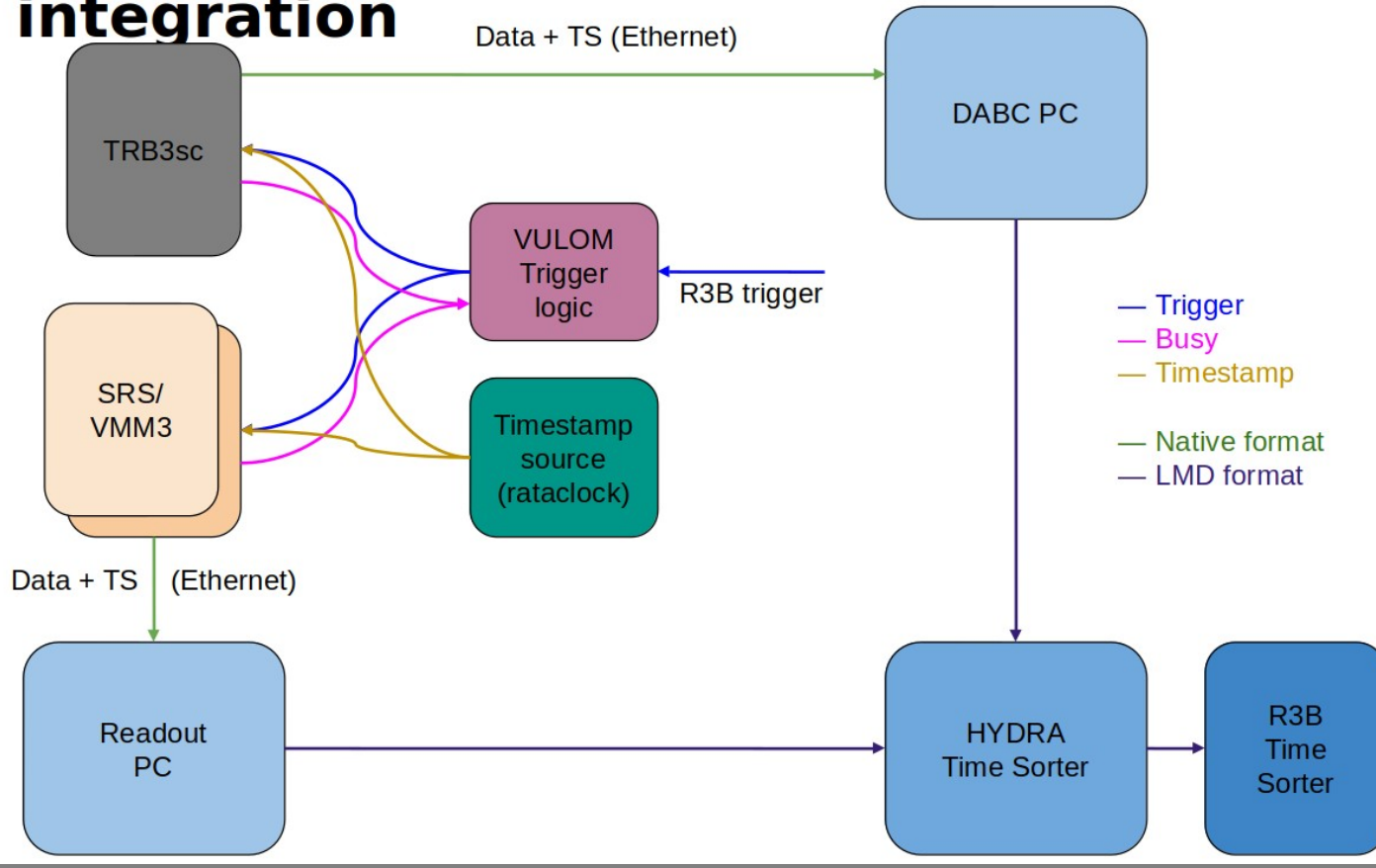
Not (yet) included:

Calibration routines
Graphical user interface
Sophisticated data transport

**Work will be done by me in the
next months.
Any help is welcome.**

Previous plan

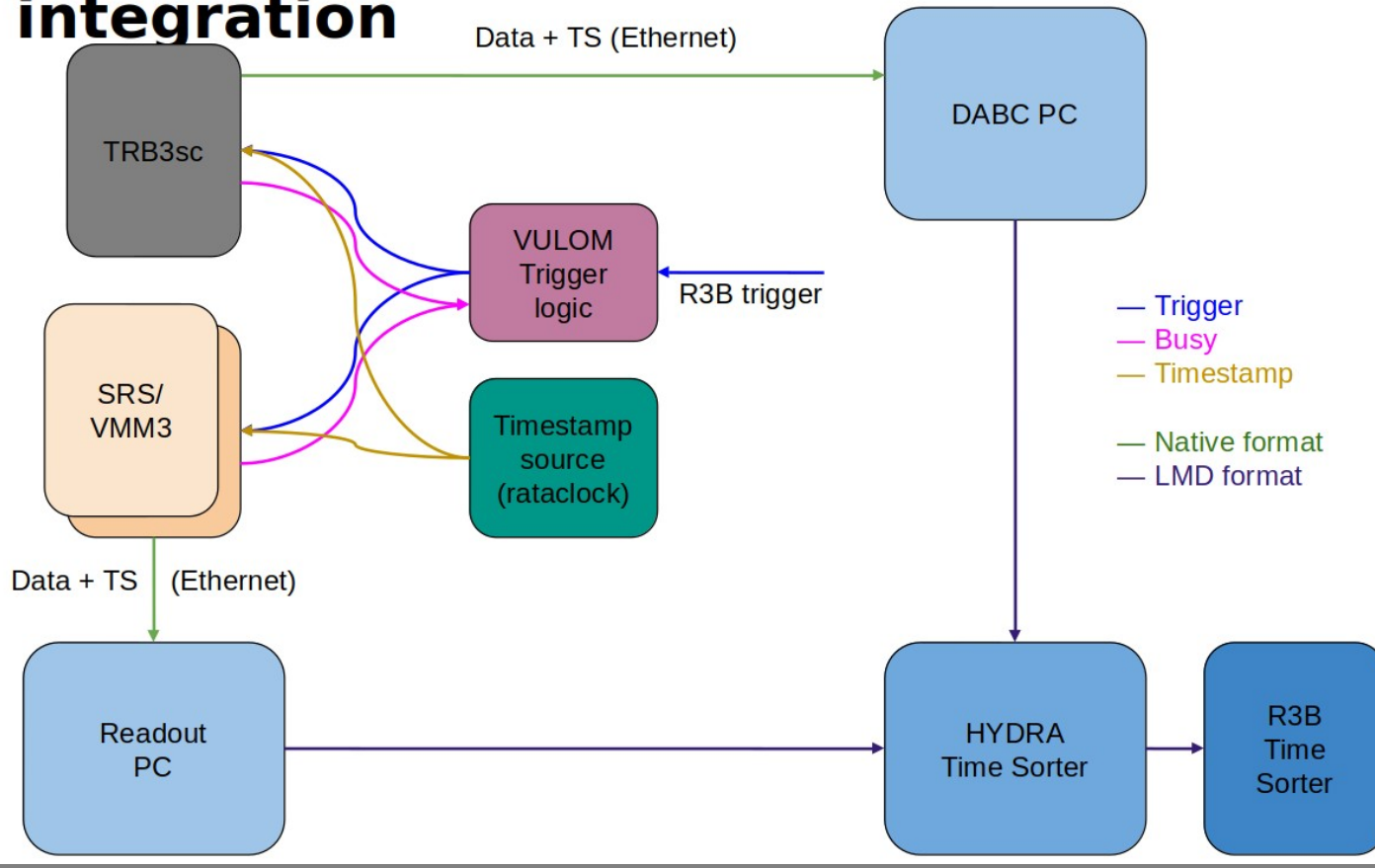
HYDRA SRS/VMM3 - R3B DAQ integration



Slide from Bastii's presentation from Jan/2023

Previous plan

HYDRA SRS/VMM3 - R3B DAQ integration



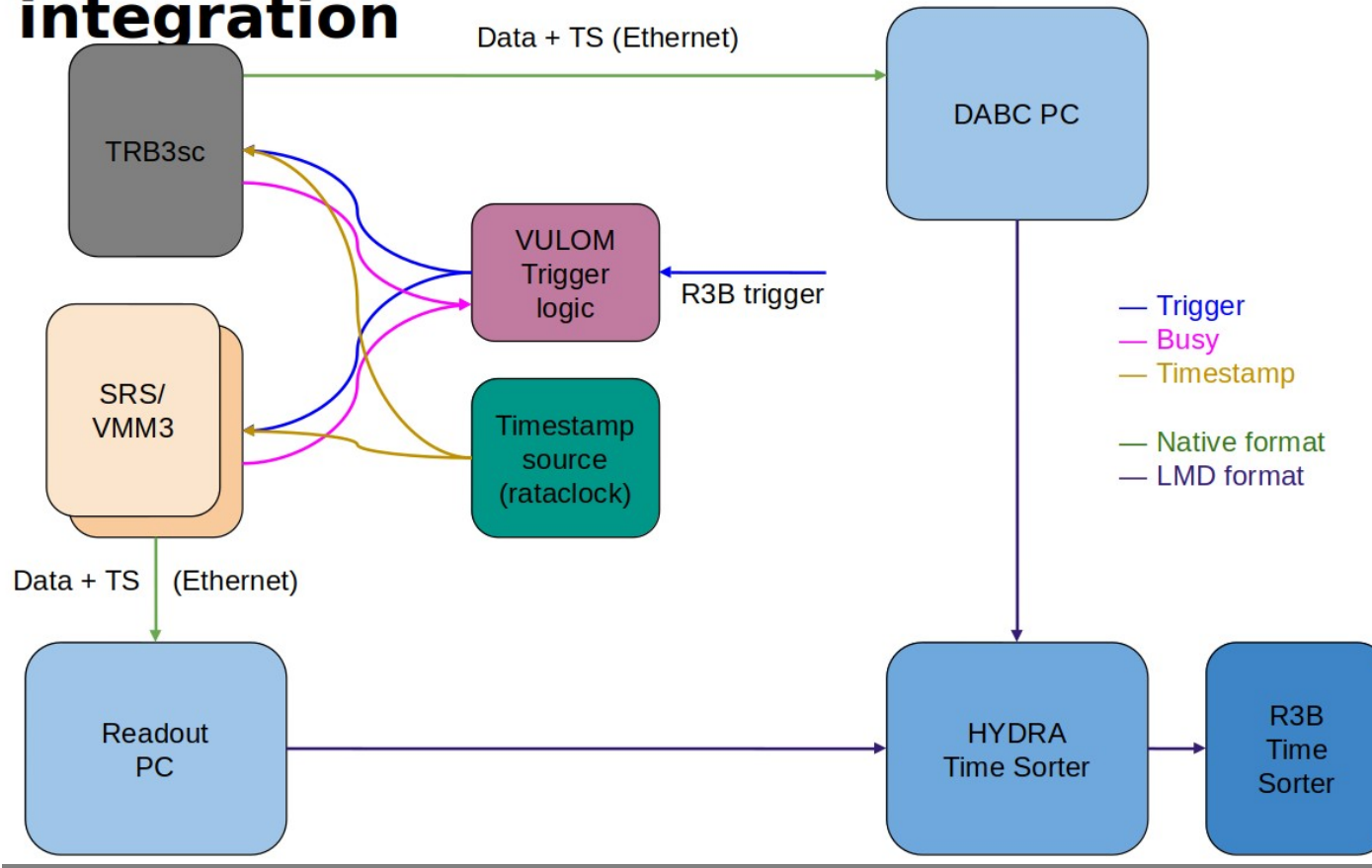
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Needs firmware modification

No help from VMM/SRS group for this

Previous plan

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WE NEED A NEW PLAN

New plan

Bastii suggested using Heimtime, based on his experience with the AMBER collaboration.

"In order to rather easily share a common time reference with foreign DAQ systems that have no means to use e.g. the serial time protocol, a simple "speaking clock" protocol is implemented.

Provided that the foreign DAQ system is able to locally timestamp a received logical signal, it can receive the periodic signals of the heimtime protocol, and **during analysis the common time scale (as provided by the TRLO II) can be recovered.**

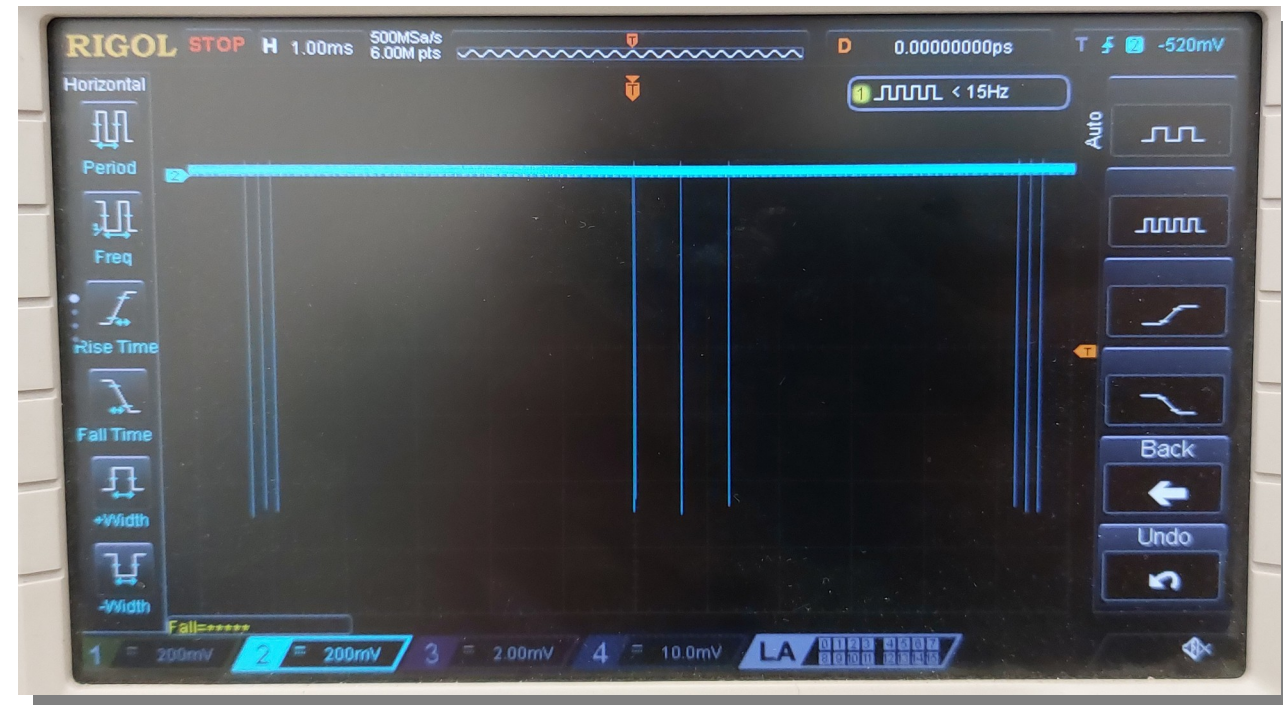
The protocol consists of two parts. **Every 2^{19} local clock cycles a pulse is generated.** With the local clock of 100 MHz this means every 5.24288 ms (or 190.7 Hz of signals). In order to tell time, for 32 pulses starting every 2^{26} ticks (or 128 pulses, or about 0.671 s apart), it delivers two additional pulses. **They either have a separation of 0.16384 or 0.65536 ms. The short separation means 0, and the long separation means 1, in a 32-bit time stamp.** The 32-bit time-stamp starts at local bit 24.

For analysis, reception of one full time message would be enough, as it then can perform dead counting of the pulses. It is naturally recommended to continuously verify that the received timestamps match with the previous ones.

The reason for having both this and the serial timestamp protocol is that the serial protocol lends itself to easy FPGA decoding and precision following, while this Heimtime protocol allows for rather straightforward handling in analysis, without requiring tremendous amounts of data to be recorded by the foreign DAQ system."

Text from the TRLO II documentation

(https://fy.chalmers.se/~f96hajo/trloii/vulom4_trlo/)



New plan

HYDRA TPC - VMM3 readout

Hardware	VMM3 front-end + SRS
Particular software / firmware	Software to be decided Standard CERN firmware
Synchronisation	Heimtime
Trigger	System is free running, trigger must happen online in software
Slow control	Electronics: Signal shape, thresholds Gas: — Laser: —
Deadtime	readout rate 3.6 MHz/channel
Stability	Untested

	Red	Orange	Yellow	Green
Timing/sync	To be done, inject Heimtime to the TPC Front-End PCBs			
Data flow	To be done, send hits data to event builder, send to time-order			
Trigger	No external trigger input, but will send Master Start to the TPC Front-End PCBs No internal trigger output.			
Run Ctrl	Requires special startup sequence			
Slow Ctrl	No EPICS interface			
Deadtime	Unknown			
Downtime	Unknown			
Stability	Untested.			
Documentation	New developments undocumented			Original documentation available here

HYDRA TPC is a new detector in R3B. We will try to gather as much as documentation as possible.

New plan

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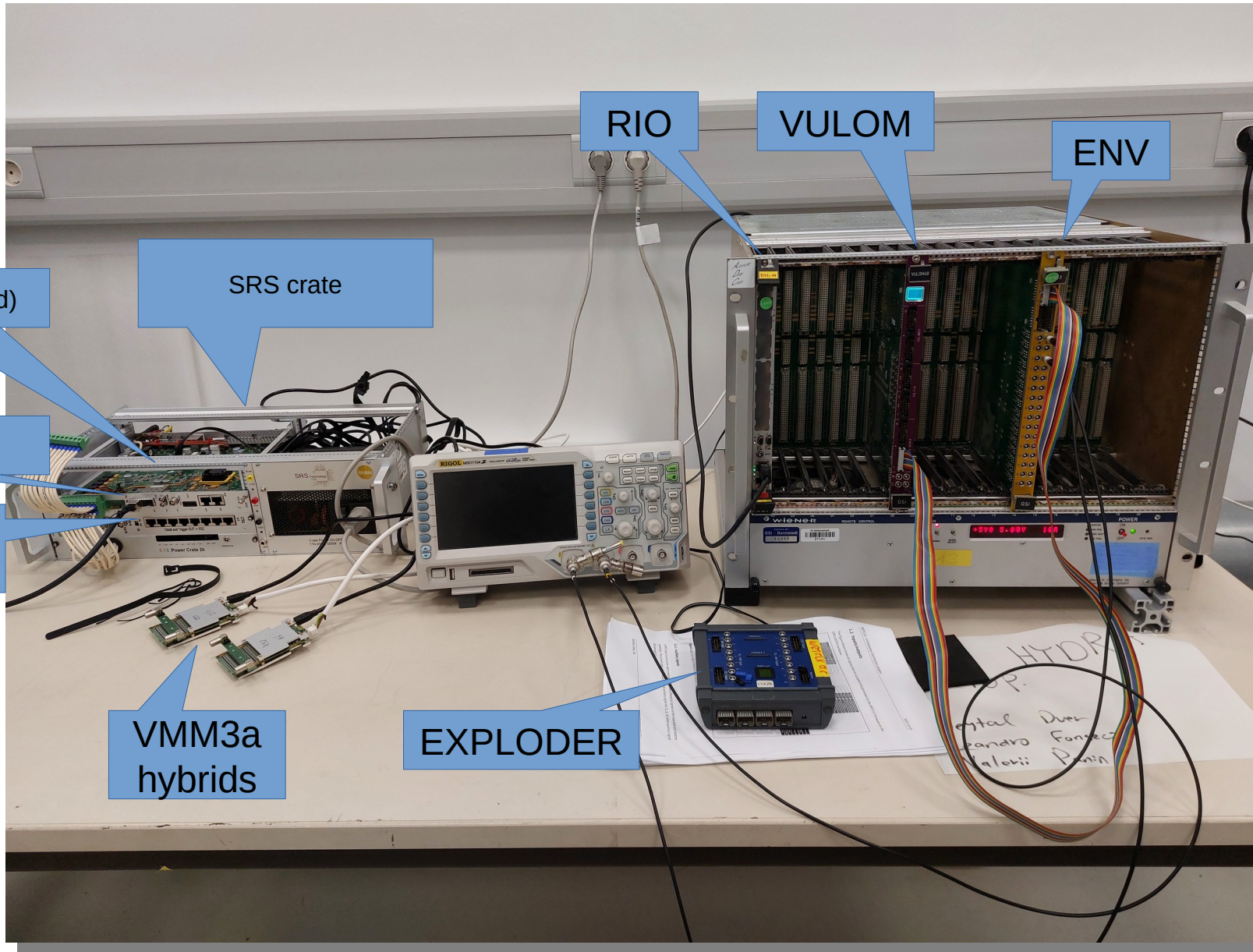
HYDRA TPC is a new detector in R3B. We will try to gather as much as documentation as possible.

Experts from the RD51 CERN group will be contacted for help and advices.

Hans will support the implementation of the event builder.

Tasks to be finished until the end of the year.

Valerii is involved in this work, helping us.



DVMM card (behind)

SRS crate

FEC card

CTF

VMM3a hybrids

EXPLODER

RIO

VULOM

ENV

HYDR
ental Duen
kandro Fonseca
alorio Pavin

