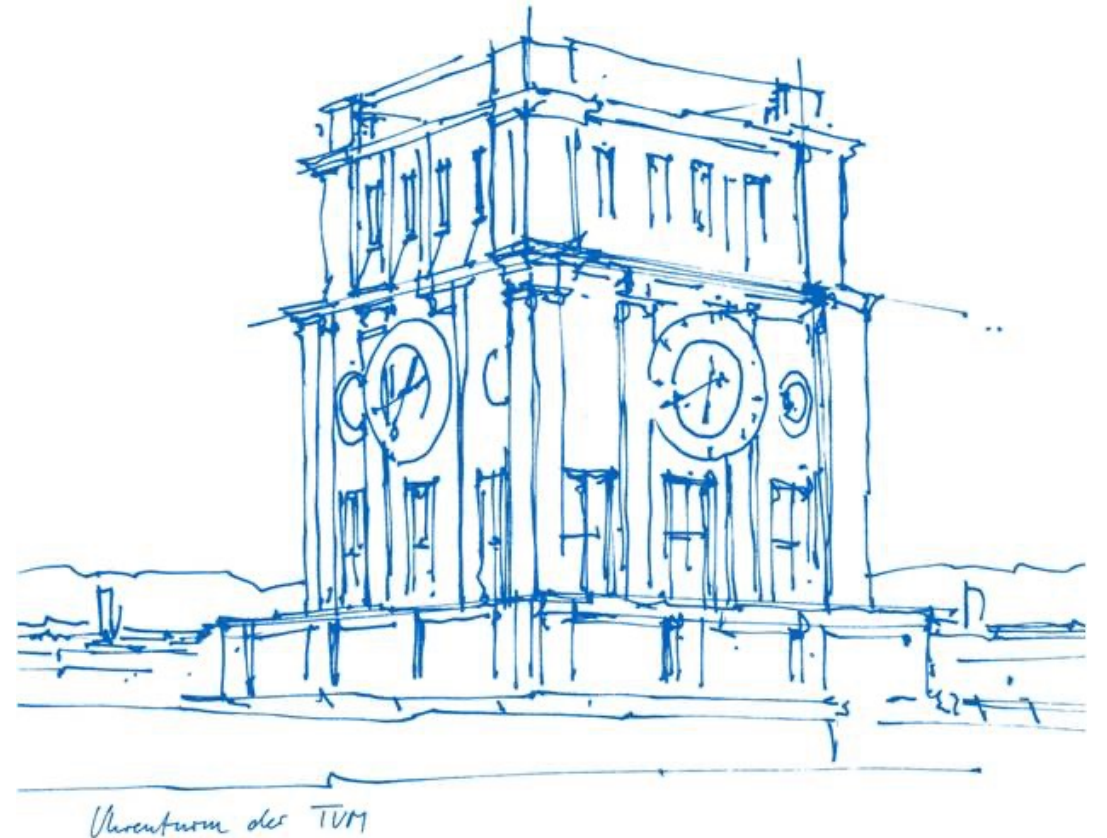


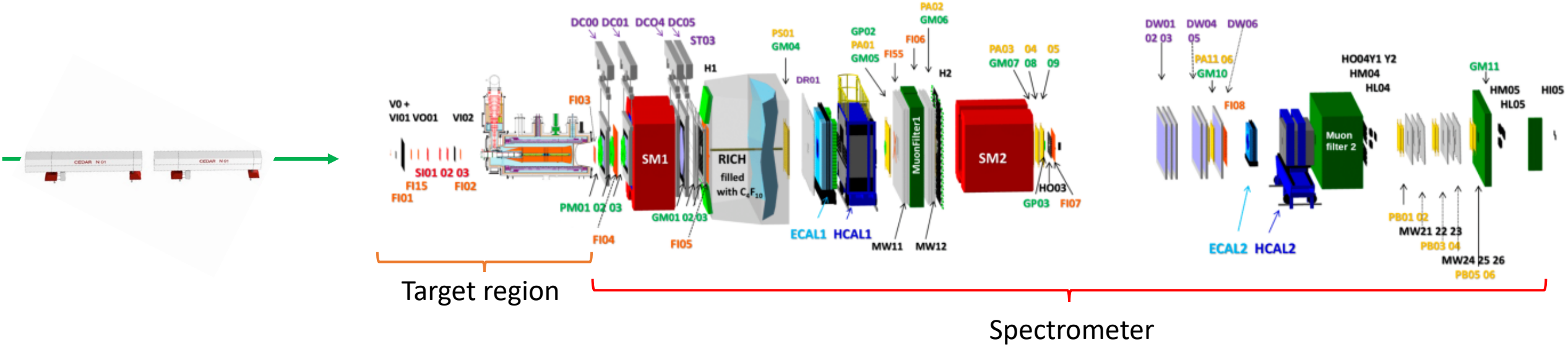
AMBER FriDAQ

Igor Konorov and Martin Zemko
on behalf of DAQ group

PANDA DAQ Workshop
CERN, 26.06.2024



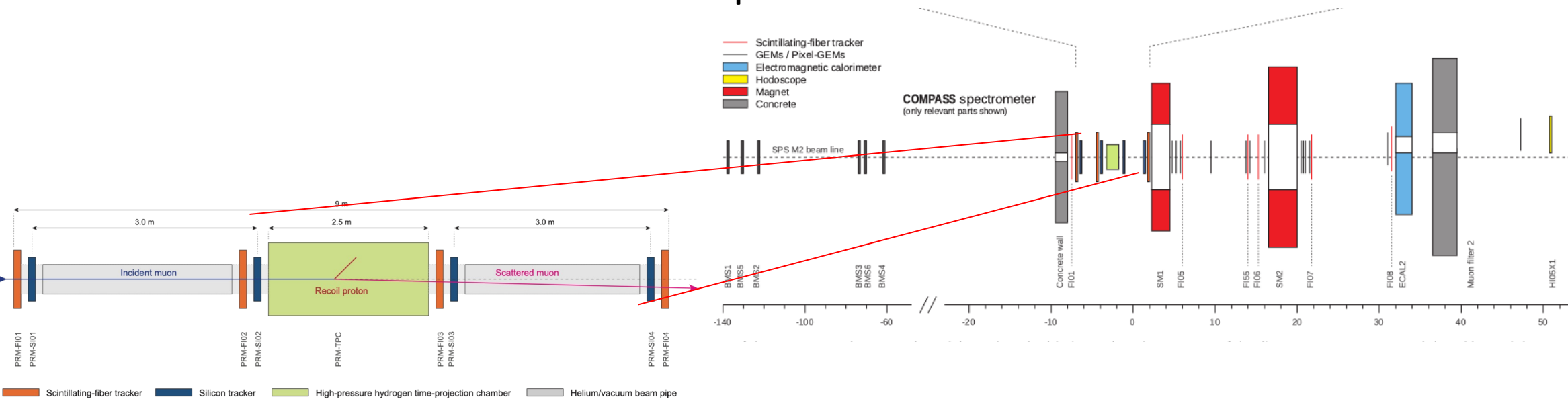
AMBER Experiment



Successor of COMPASS Experiment

- 2023-2024 pbarX : 60 – 250 GeV p LHe, LH2 target Triggered DAQ 20kHz, 300 MB/s

AMBER Experiment



Successor of COMPASS Experiment

- GEM
- MWPC
- ECAL2 Central part

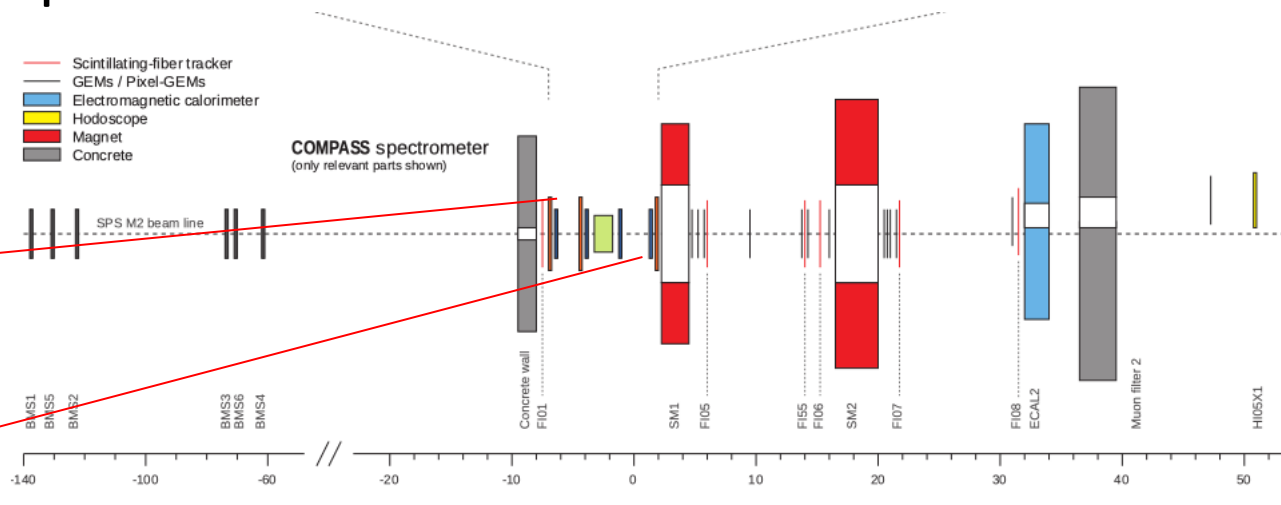
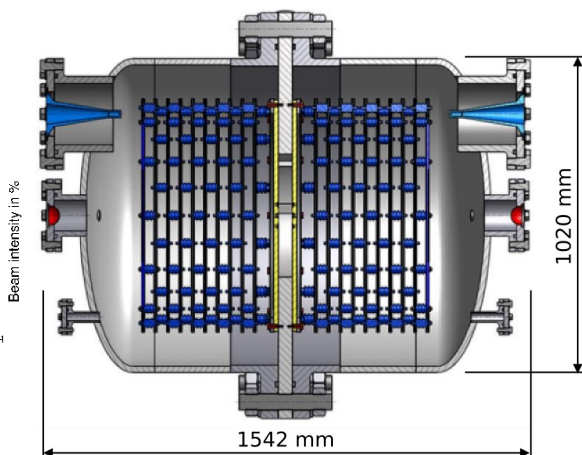
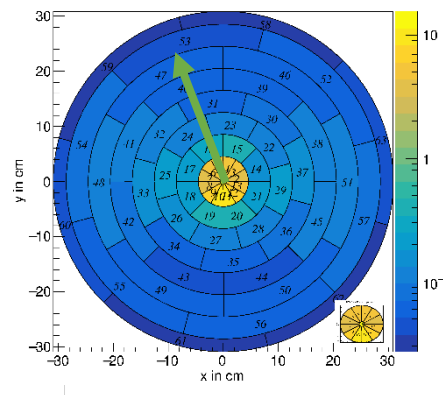
▪ 2023-2024	pbarX	: 60 – 250 GeV p	LHe, LH2 target	Triggered DAQ	20kHz, 300 MB/s
▪ 2025-2026	PRM	: 100 GeV μ^\pm	TPC, small spectrometer	Streaming DAQ	1-2 GB/s

AMBER Experiment

TPC, recoil proton

- < 6% resolution
- 150us drift time
- H2 at 4,20 Bar
- SIS ADC, 120 ch

TPC Event Display (Upstream)



Successor of COMPASS Experiment,

- GEM
- MWPC
- ECAL2 Central part

▪ 2023-2024	pbarX	: 60 – 250 GeV p	LHe, LH2 target	Triggered DAQ	20kHz, 300 MB/s
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AMBER Experiment

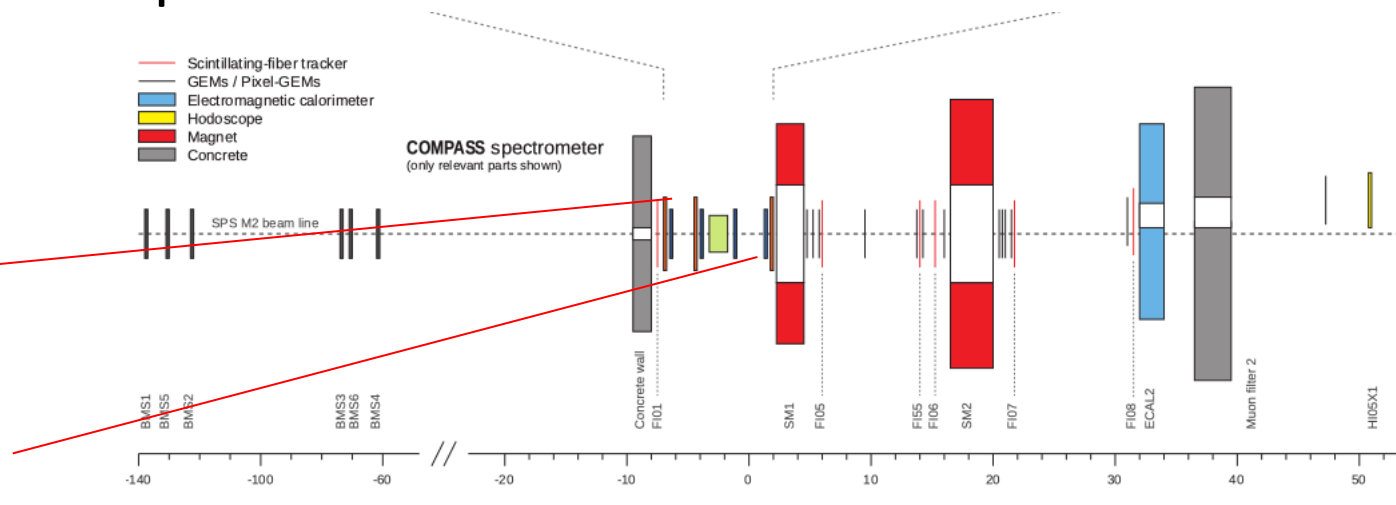
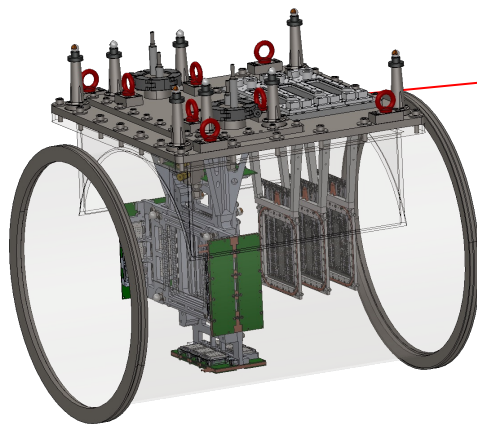
4 stations, 3xPixel planes+4 SciFi planes

Pixel ALPIDE

- 28um x 28um
- 10us gate

SciFi UTS tracking

- 500 um fiber
- < 400 ps resolution

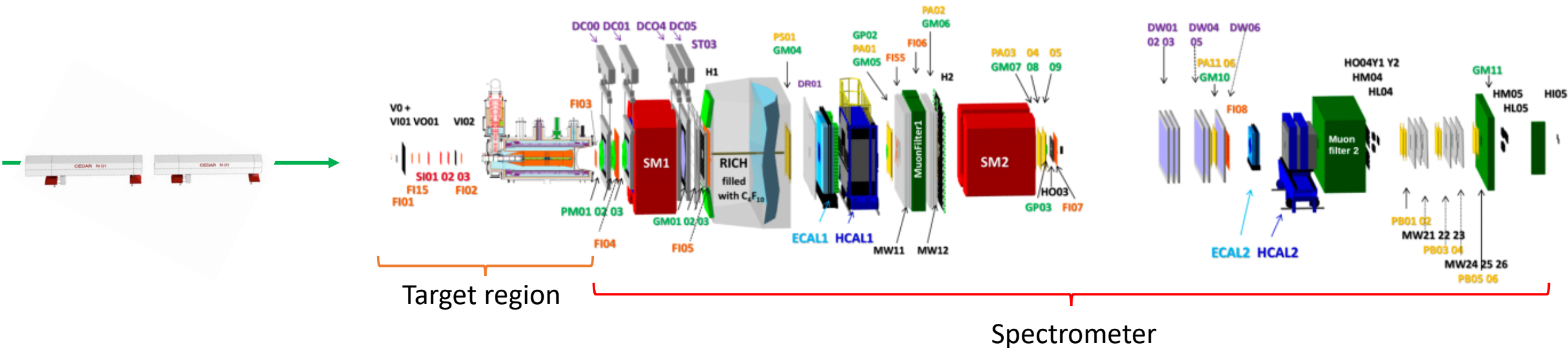


Successor of COMPASS Experiment

- GEM
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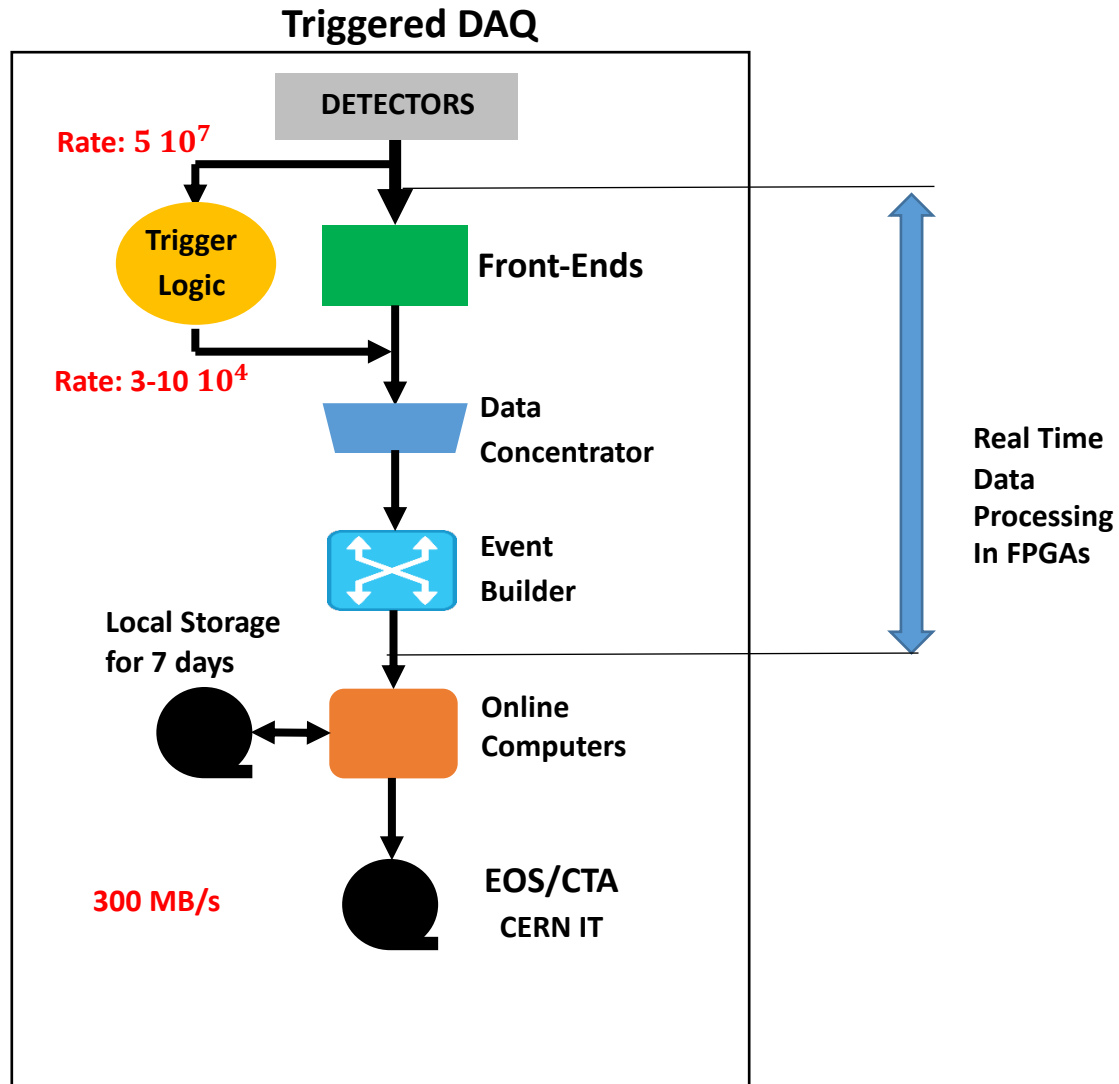
AMBER Experiment



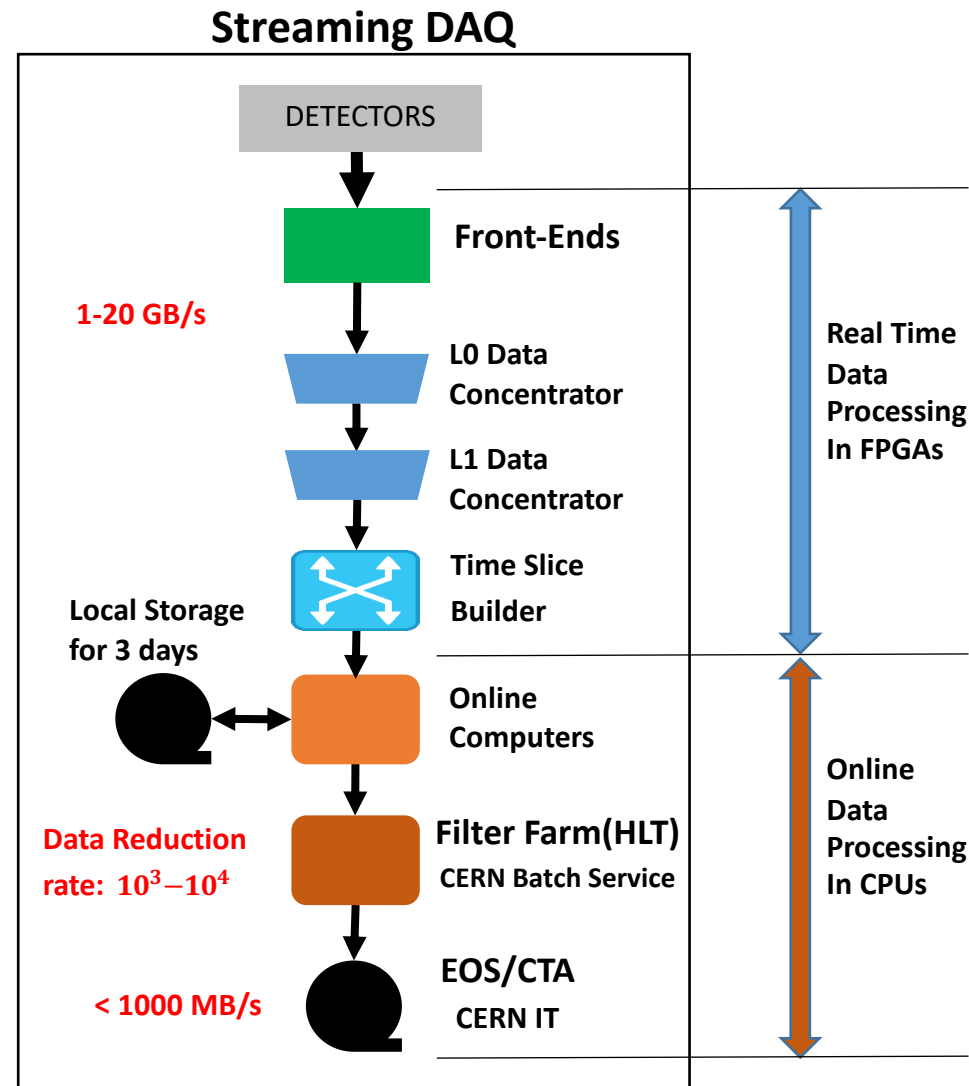
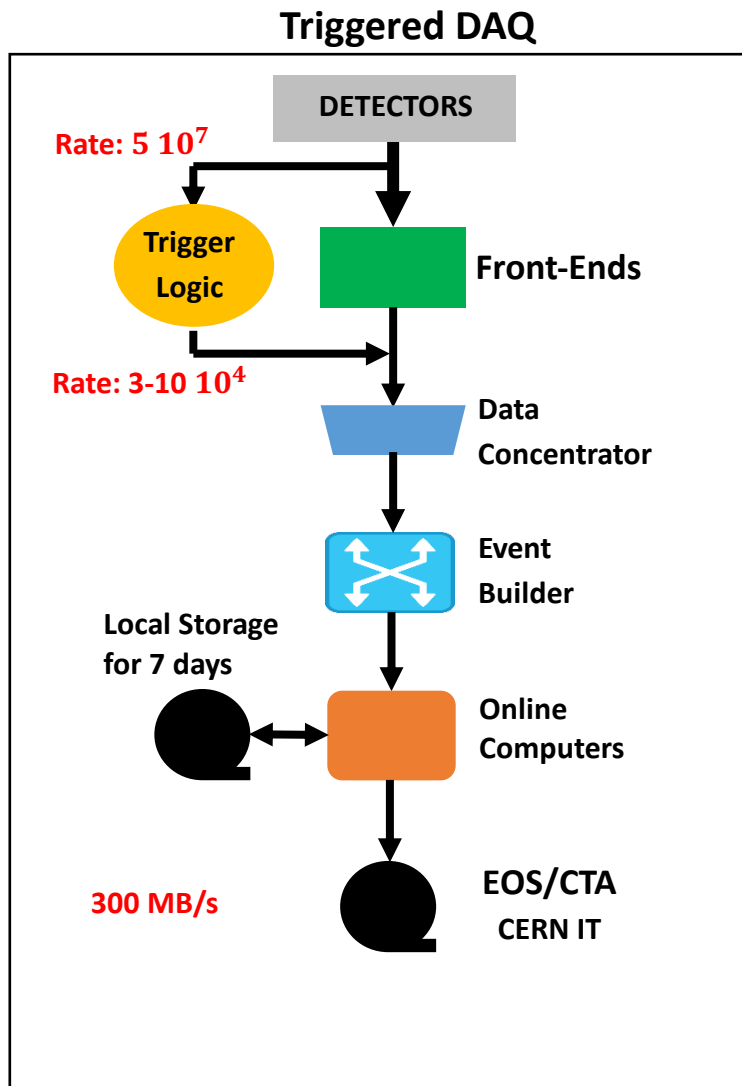
Successor of COMPASS Experiment,

■ 2023-2024	pbarX	: 60 – 250 GeV p	LHe, LH2 target	Triggered DAQ	20kHz, 300 MB/s
■ 2025-2026	PRM	: 100 GeV μ^\pm	TPC, small set of detectors	Streaming DAQ	1-2 GB/s
■ 2028-...	DY	: 190 GeV π^\pm	Full Spectrometer	Streaming DAQ	10 GB/s
■				

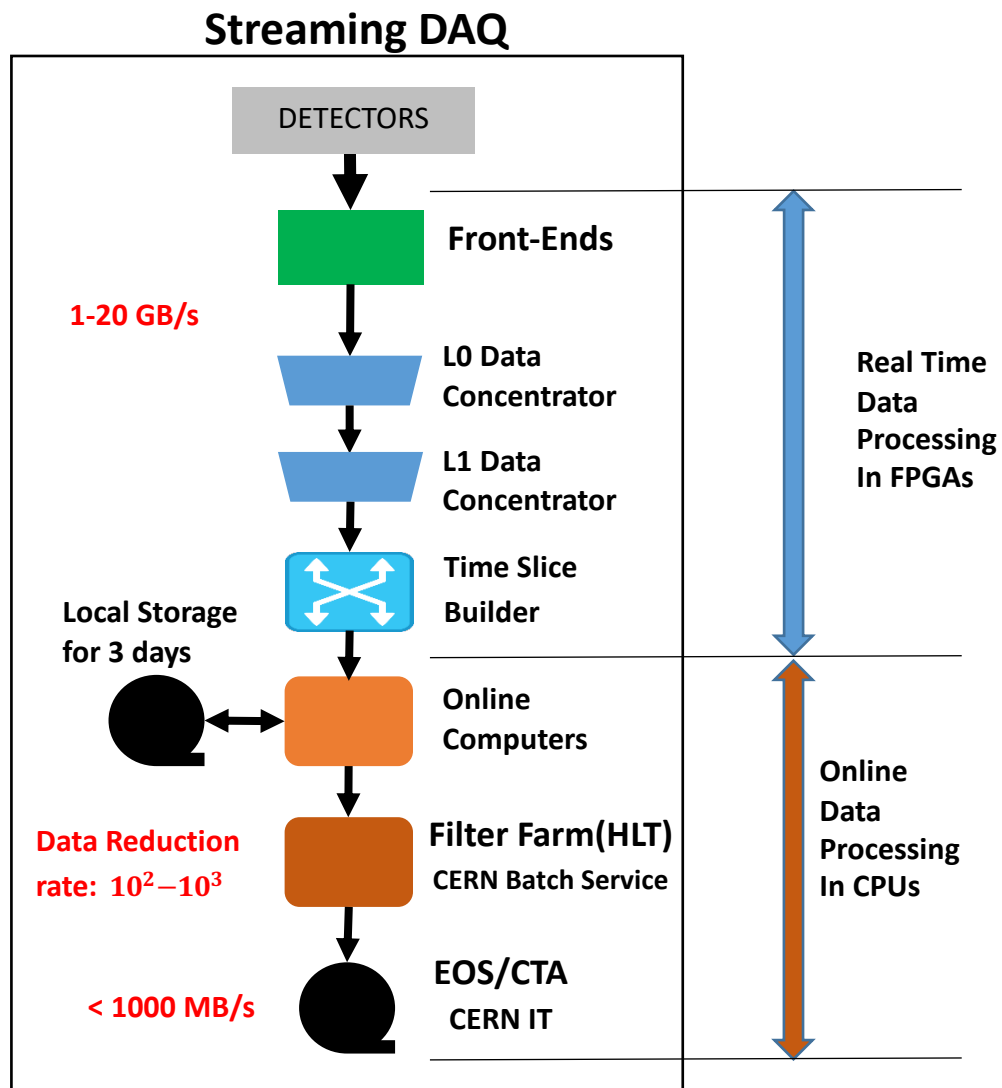
DAQ Architecture Evolution



DAQ Architecture Evolution



DAQ Architecture Evolution



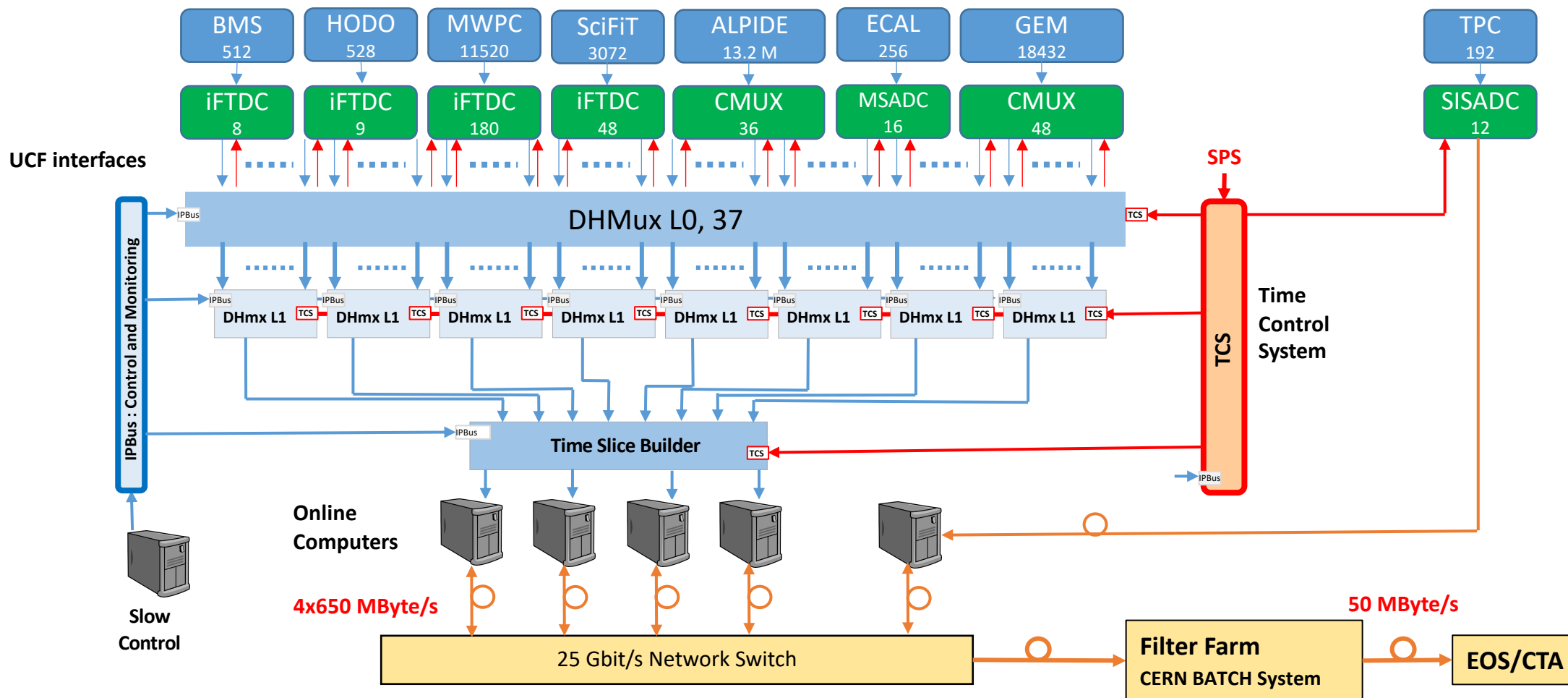
DAQ Framework

- Intelligent data handling, no DAQ crashes
- Congestion free Time Slice Builder in FPGA
- Unified Communication Interfaces (UCF) to FE
- Unified IP Cores

Advantages

- No real time software processes
- Scalability and High performance
- Compactness
- Diagnostics and Reliability
- Low cost
- Data filtering in IT center

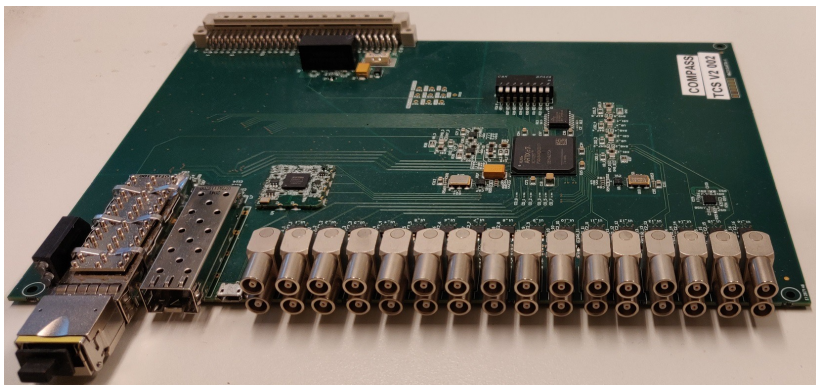
FriDAQ for PRM with TPC



AMBER DAQ Hardware

TCS, Time Synchronization

- Passive optical network
- > 300 destination
- Reset, 38.88 MHz clock
- RUN , SPILL, END
- Time Slice, 1kHz



▪ DHMux, TS Builder

- Virtex6 XC6VLX130T FPGA
- 4 GB DDR3
- 16 High speed links 6.5 gbps
- MUX L0/L1
- TimeSlice Builder

- MUX L0, detector specific, 4GByte
 - 12x3.1Gbps UCF FE links
 - 1x6.25 GbpsAurora
 - Chronological data ordering
 - iFTDC version developed
- MUX L1, generic, 4GByte
 - Multiplexing Time Slices
 - 12:1
 - Being developed
- Buffering data of entire spill



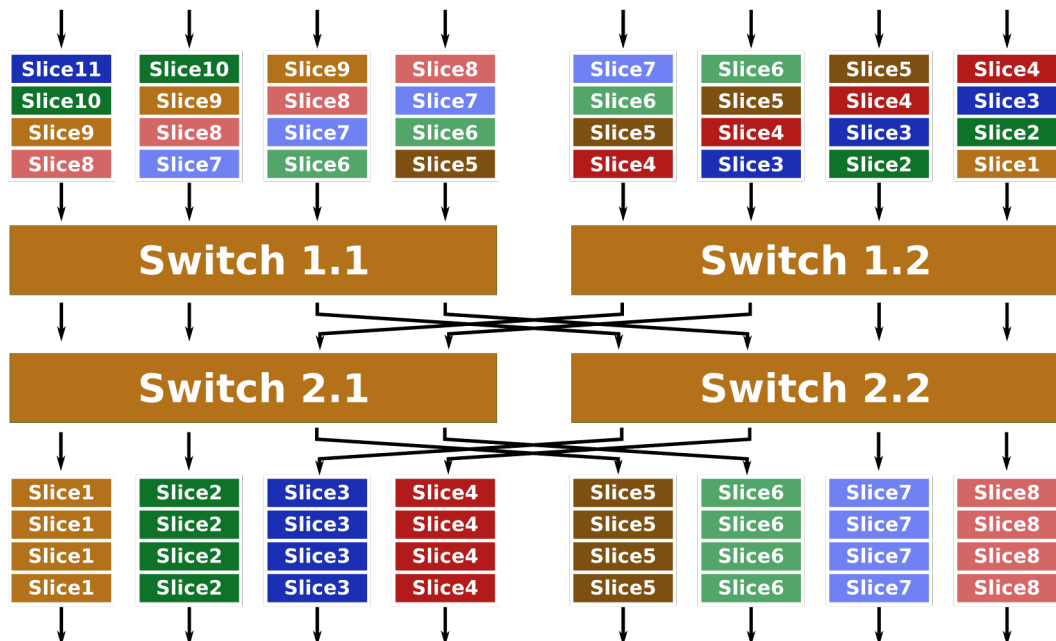
▪ ATCA Integration





Time Slice Builder

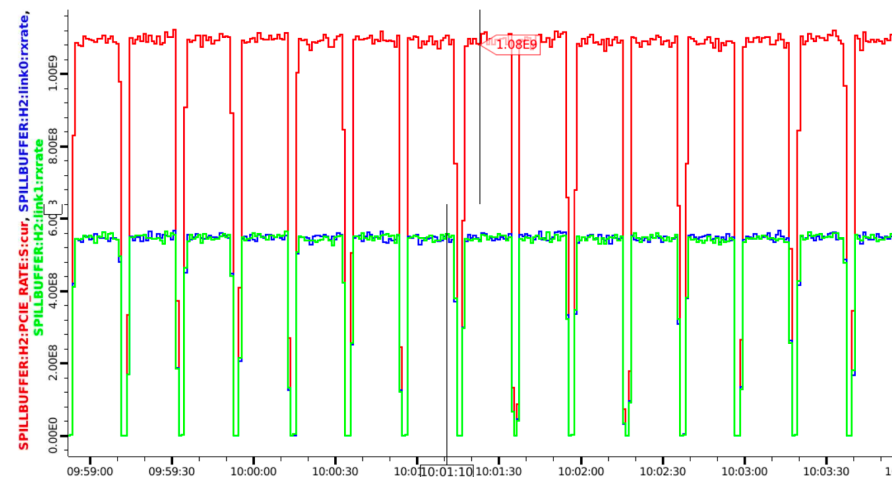
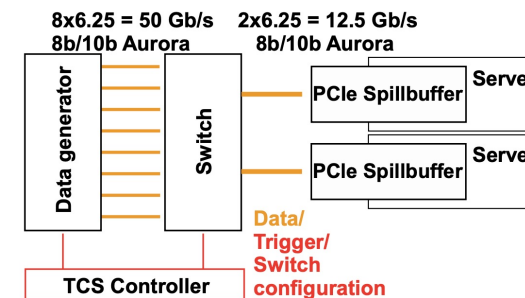
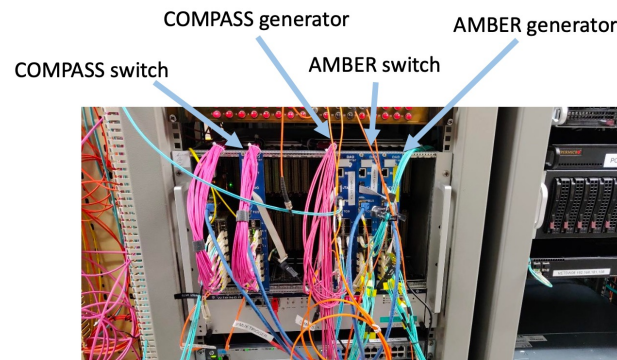
8 x 6.25 Gbps



8 x 6.25 Gbps

Data rate test

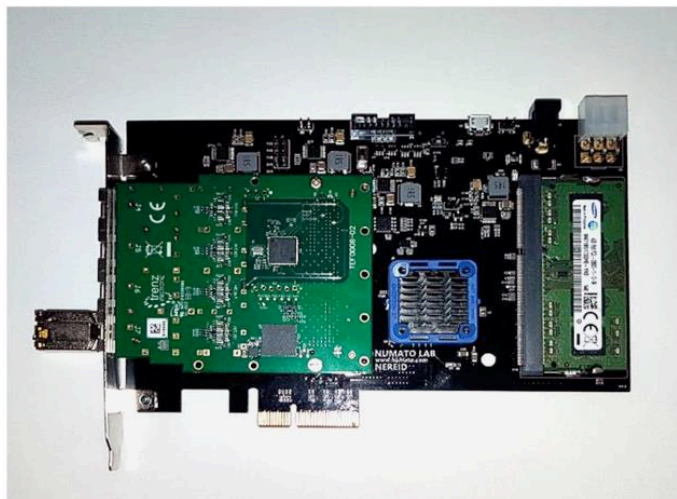
- Random TS size variations
- 580 MB/s => 10 % loss due to data size variation
- 8x 580 MB/s => 4.5 GB/s throughput



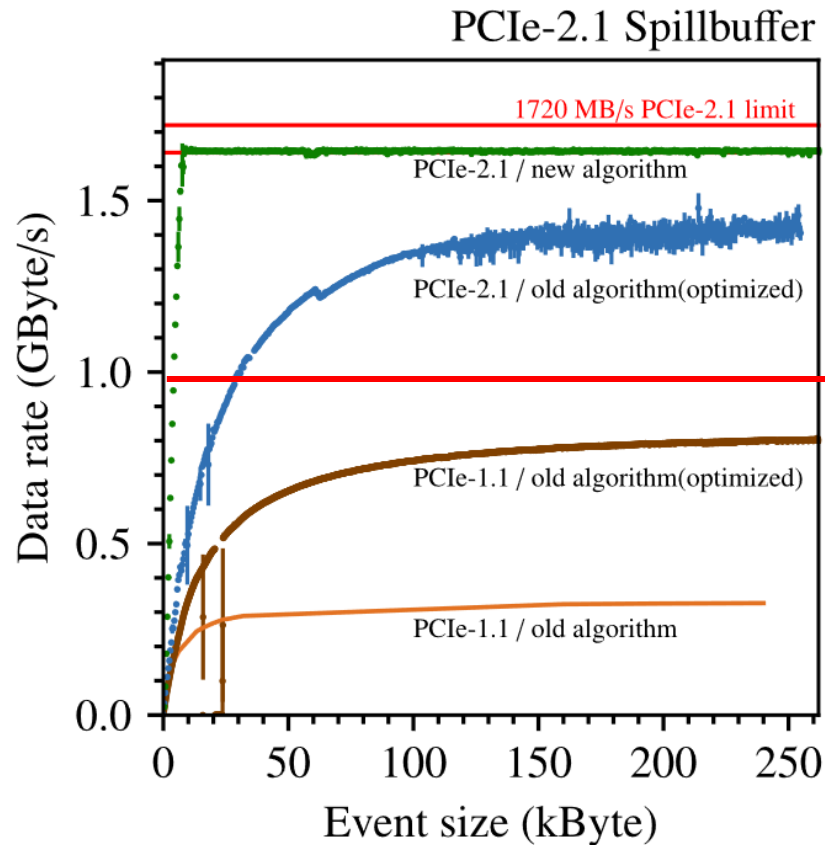
AMBER DAQ Hardware

PCIe card

- Nereid Kintex 7 XC7K160T
- 4 x PCIe-Gen2 interface
- 4 GB DDR3 memory

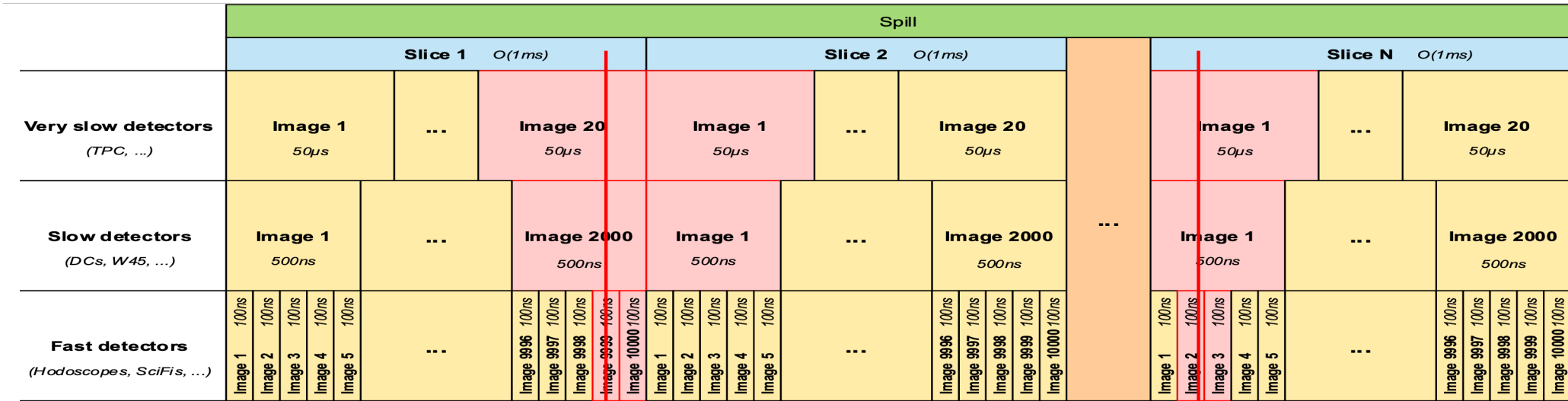
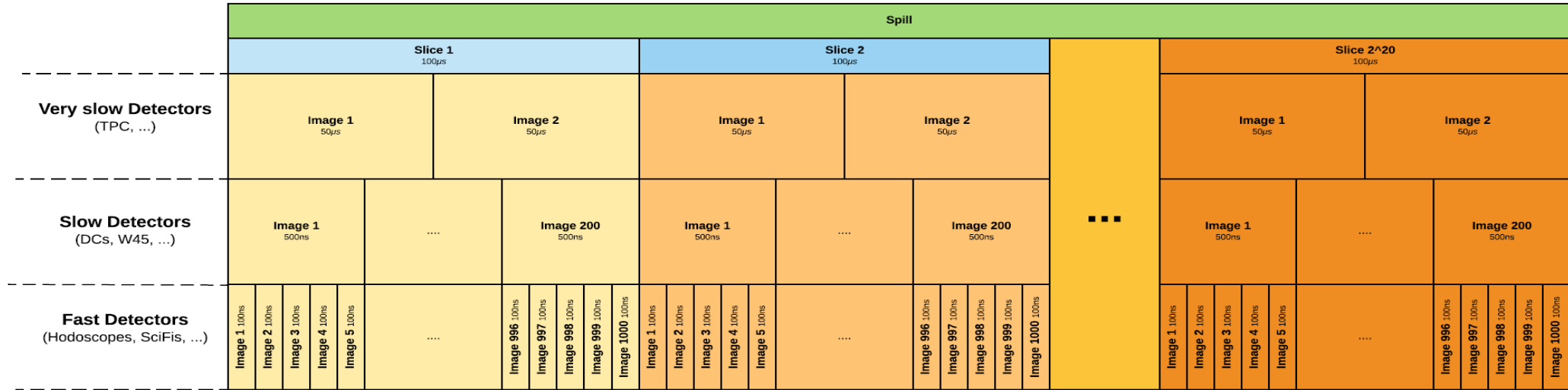


DMA Performance



DAQ Requirements:
> 1 GB/s/Compute Node

Data Structure and Data Reduction

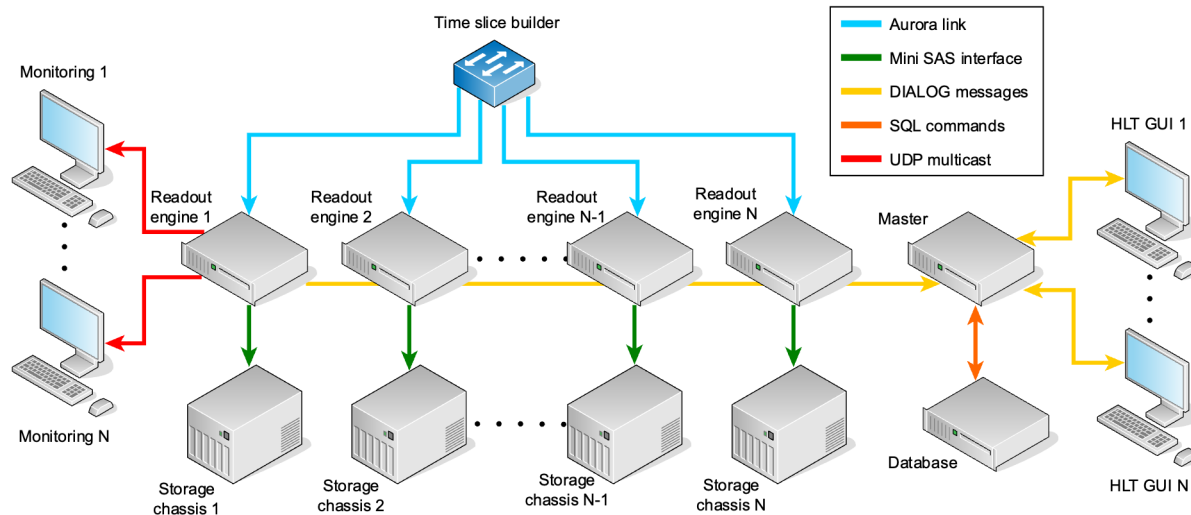


Event candidate 1

Event candidate N

Computing

- 4 readout servers + 4 x 250 TB external chassis connected via Broadcom MegaRAID 9580-8i8e RAID controller
- Storage space split to 3 x RAID 50 volumes and accommodates 3 days of data-taking
- Optimized for maximum sustained throughput of 1 GB/s/server



Databases

- Databases deployed on centralized CERN Database-on-demand service
- Clustered database design with 3 nodes – one primary and two replicas

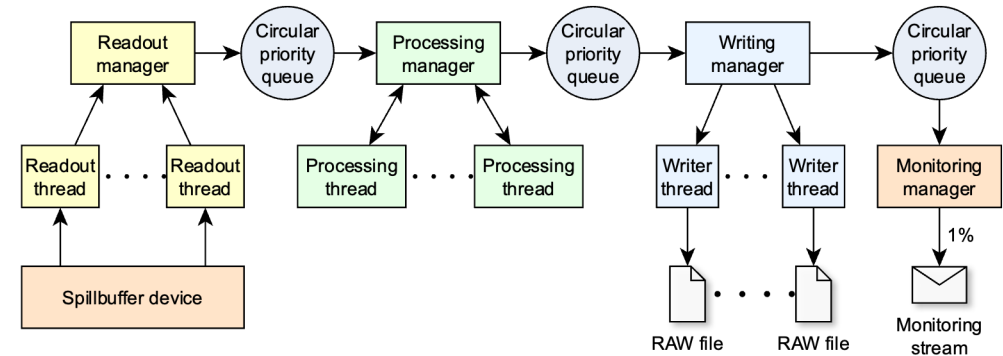
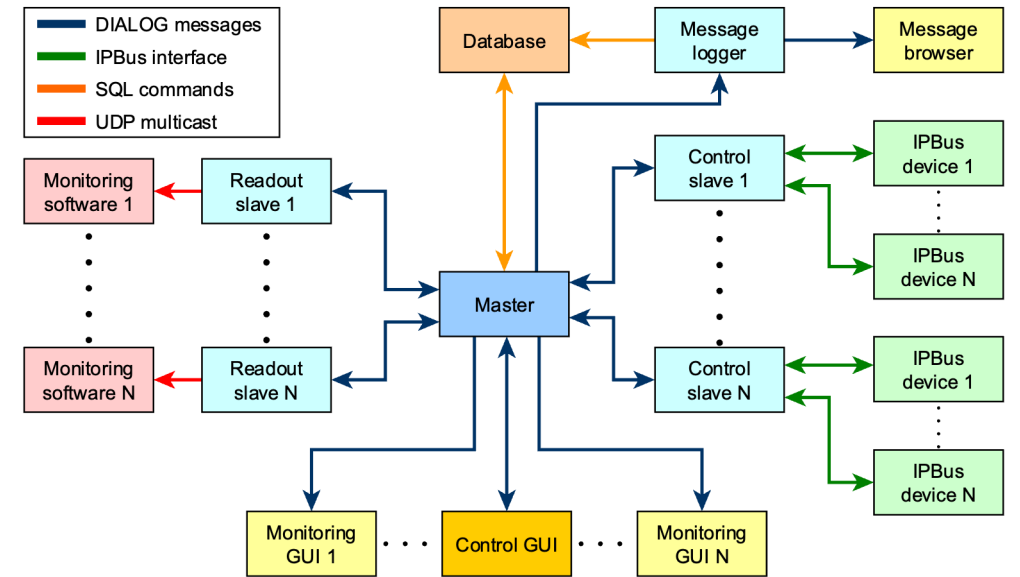
Networking

- Star network topology with a central 100 Gbps switch, custom DHCP and DNS servers
- Second 100 Gbps switch for uplink to data center
- Full data stream is sent to the CERN data center via 2 x 100 Gbps links



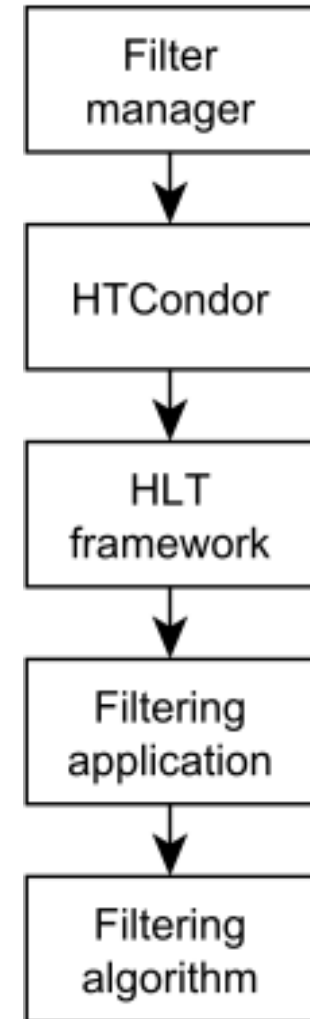
Readout Software

- Master-slave architecture executed on several machines
- Master is central hub and controller
- Two worker processes:
 - **Readout slave** – data extraction from readout cards and processing
 - **Control slave** – monitoring and configuration of IPbus devices
- Custom DIALOG library for message exchange between processes
- Qt graphical user interface for run control and configuration
- Monitoring stream provided by readout servers via UDP multicasting
- All processes contain a global state machine (33 states)
- Centralized log handling



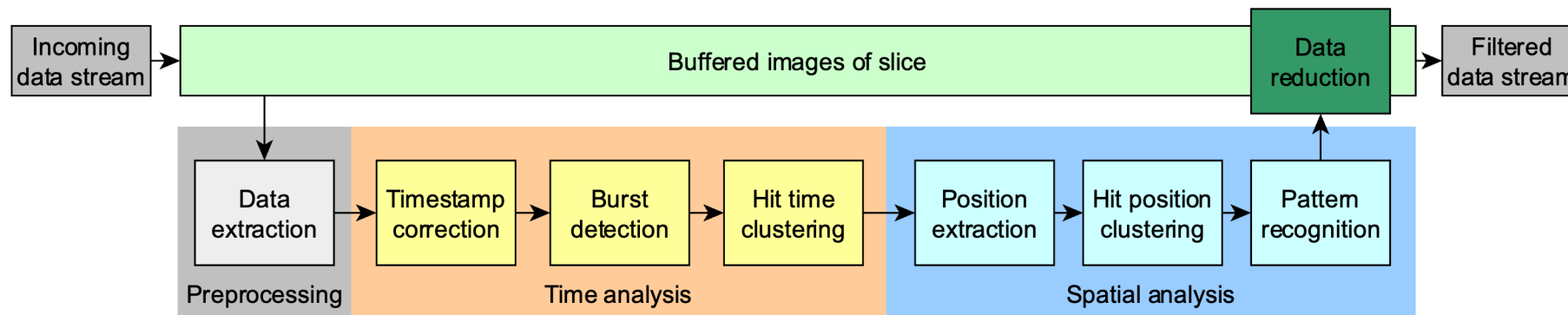
High Level Filter

- High-throughput computational and reconstruction framework written in optimized C++ and Qt
- Runs on the virtualized CERN infrastructure shared with other users → significant cost optimization
- Various algorithms for different physics programmes → modular architecture
- 2 main components:
 - 1. Filtering framework**
 - performs actual data analysis and reduction
 - includes additional tools for data browsing, quality monitoring
 - 2. Filter management system**
 - handles and manages filtering requests



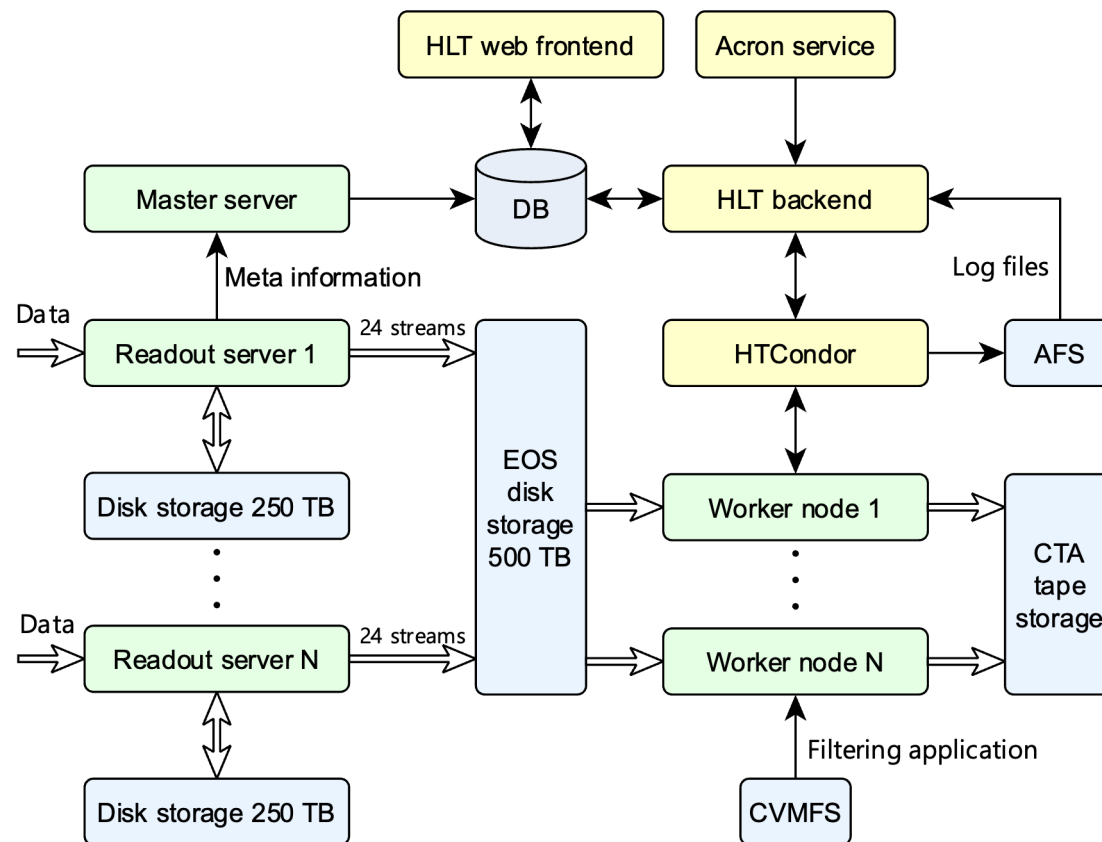
Filtering Pipeline

- Event selection and data reduction based on TPC proton detection and/or partial track reconstruction
- Initially, images are sorted into two exclusive groups:
 - **Primary images** – produced by detectors participating in filter decision
 - **Secondary images** – other images to be filtered
- We analyze primary images to make a decision using two phases:
 - **Time alignment** – processing and calibration of timestamps
 - **Spatial analysis** – analysis of hit positions to determine particle trajectory



Filter Management System

- Automatic handling and monitoring of filtering jobs and tasks
- It consists of two main parts:
 - **Back-end** – based on HTCondor platform for high-performance computing
 - **Front-end** – end user web application, serving as the main user interface
- Runs in the private CERN cloud shared with other experiments (approx. 100k CPU cores)
- Filtered data files are safely written to tapes



Summary

- FriDAQ is successful evolution of FPGA-based triggered DAQ to FPGA-based Streaming DAQ
- FPGA provides real real time solution for Data Handling : error handling, fast recovery
- Readout software decoupled from real time operation by intermediate FPGA buffers and provides average performance of 1GB/s/compute node
- High Level Filtering implemented in CERN virtualized infrastructure replacing triggering system
- The system demonstrated sustained data rate capability of 4 GB/s and fulfils requirements for PRM physics run
 - For DY program two Time-Slice Builders to be employed and number of RE engines increased to 8
 - High Level Filtering is scalable to a higher rates

- Test of FriDAQ with limited number of detectors will be performed in October 2024