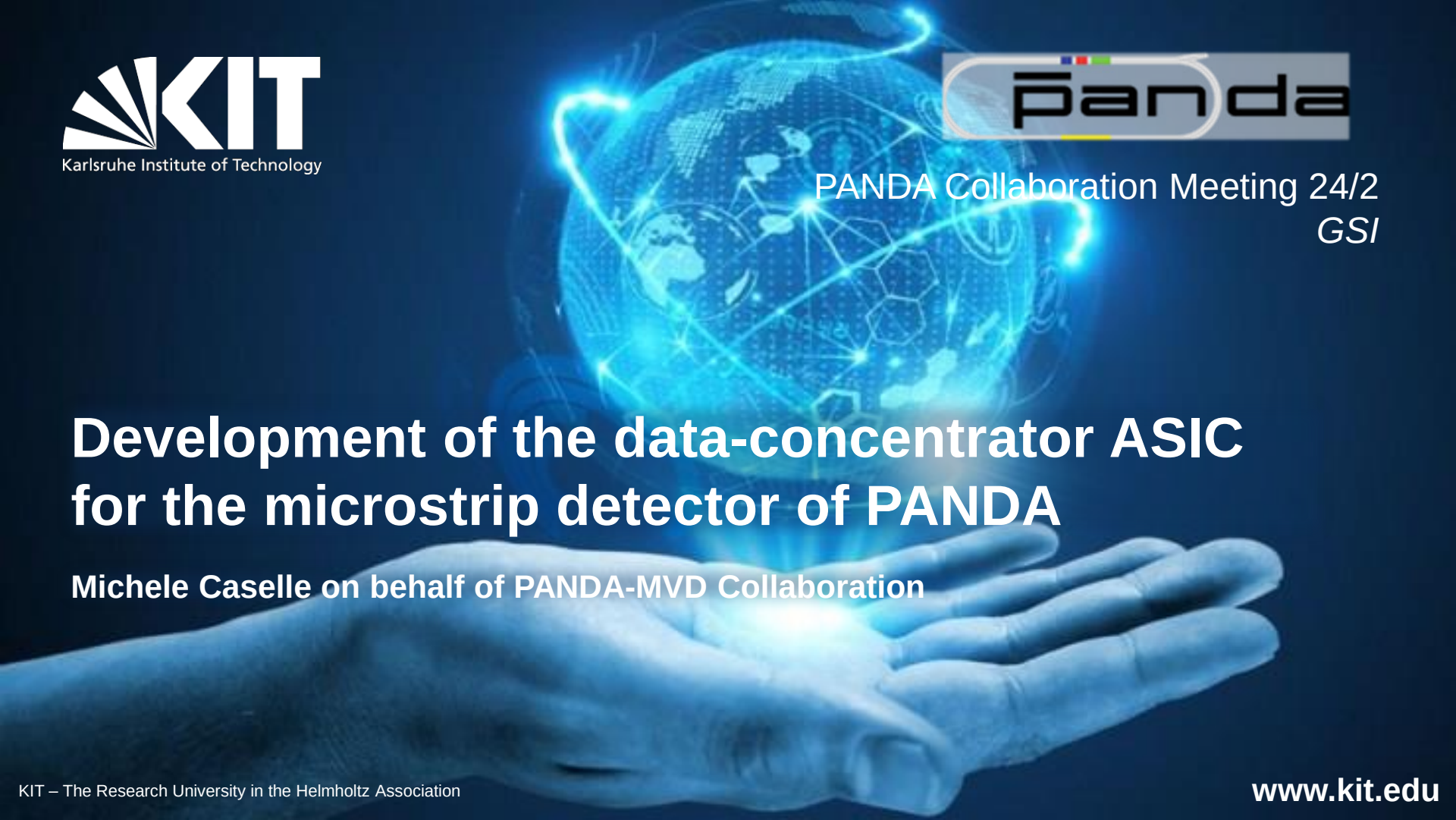


Karlsruhe Institute of Technology

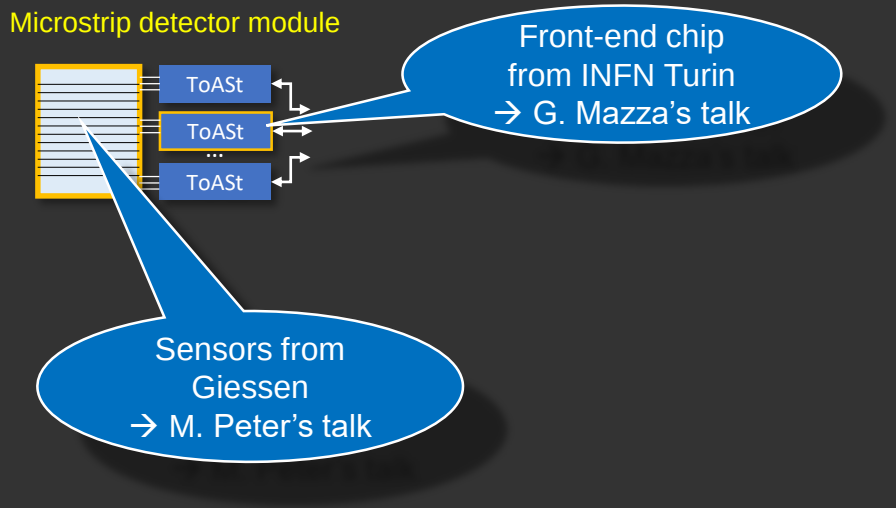
PANDA Collaboration Meeting 24/2
GSI

Development of the data-concentrator ASIC for the microstrip detector of PANDA

Michele Caselle on behalf of PANDA-MVD Collaboration

Towards to detector readout chain

Reduce the number of optical links from/to off-line electronics



Towards to detector readout chain

Reduce the number of optical links from/to off-line electronics

Karlsruhe Institute of Technology

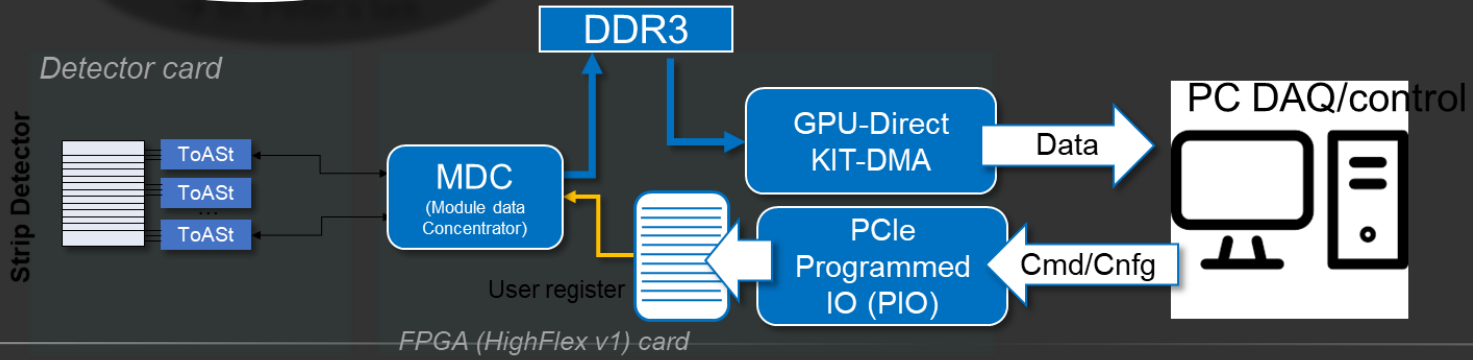
Microstrip detector module

Front-end chip from INFN Turin → G. Mazza's talk

Sensors from Giessen → M. Peter's talk

HighFlex Readut card based on PCIe GPUDirect technology

Configuration / commands / timing



Beam test at COSY and Marburg

Towards to detector readout chain

Reduce the number of optical links from/to off-line electronics

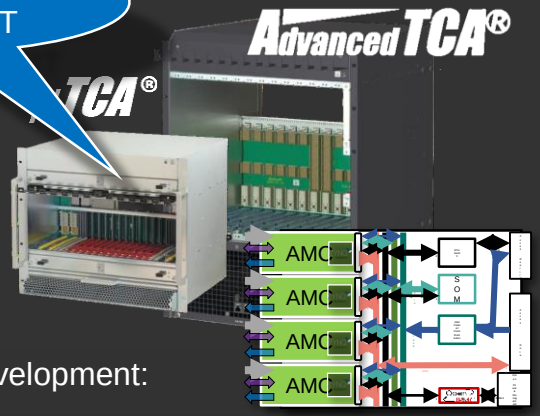
Microstrip detector module

Front-end chip from INFN Turin → G. Mazza's talk

Sensors from Giessen → M. Peter's talk

Off-detector electronics

Off-detector from Uppsala/KIT



Configuration / commands / timing

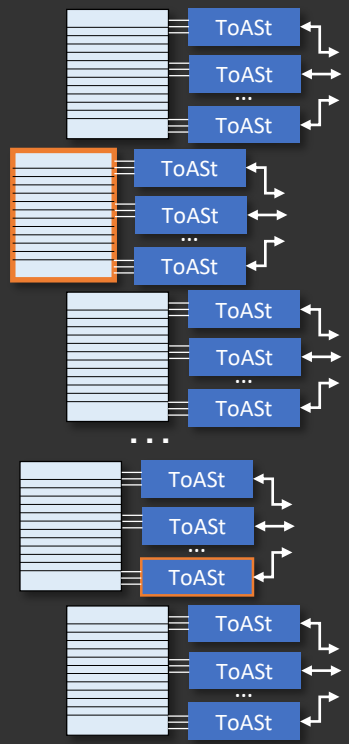
Two AMC cards under development:

- Based on Kintex US+ by Uppsala → P. Marciniewski's Talk
- Based on ZYNQ US+ by KIT → *O. Manzura's talk*
- Common data acquisition fully compliance to µTCA/ATCA and stand-alone readout card for detector test/characterization
- KIT also develop a ATCA carried card to be able to mount up to 4 AMC daughter cards

Towards to detector readout chain

Reduce the number of optical links from/to off-line electronics

Microstrip detector module



Sensors (all shapes): #

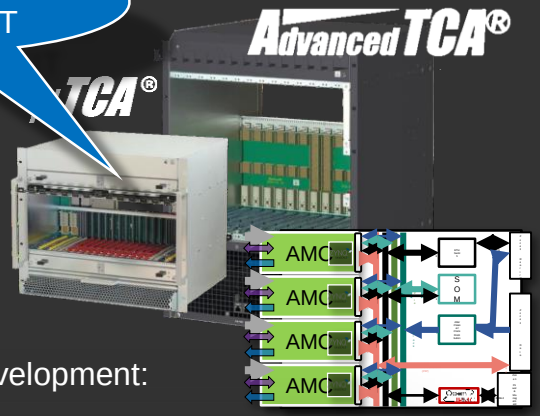
Readout chips (ToASt): # **2788**

Data concentration/formatting and status

Configuration / commands / timing

Off-detector from Uppsala/KIT

Off-detector electronics



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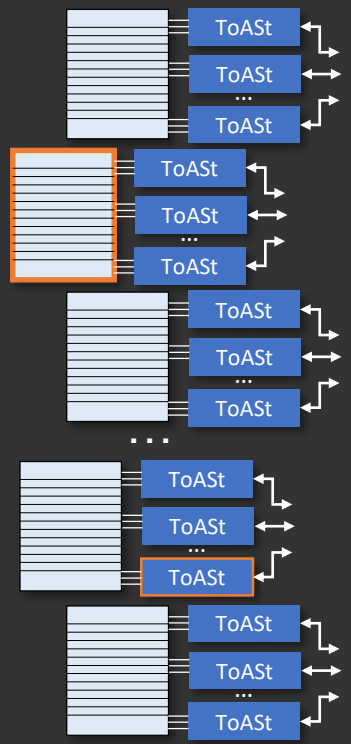
Towards to detector readout chain

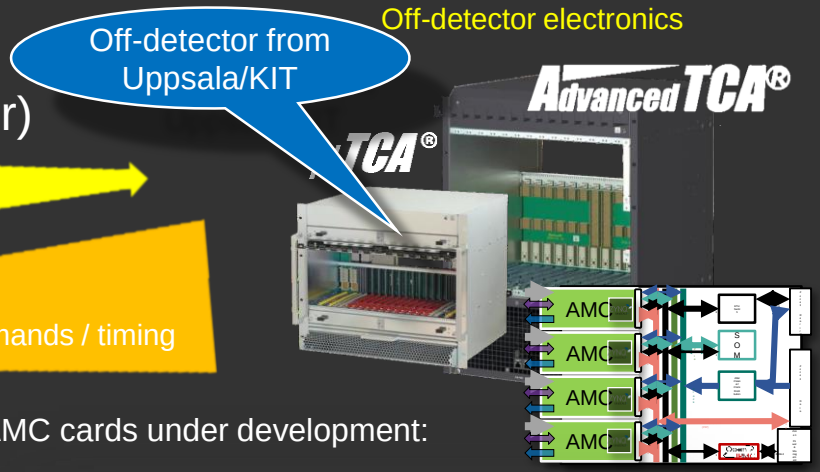
Reduce the number of optical links from/to off-line electronics

Microstrip detector module



MDC (Module data Concentrator)

Off-detector electronics



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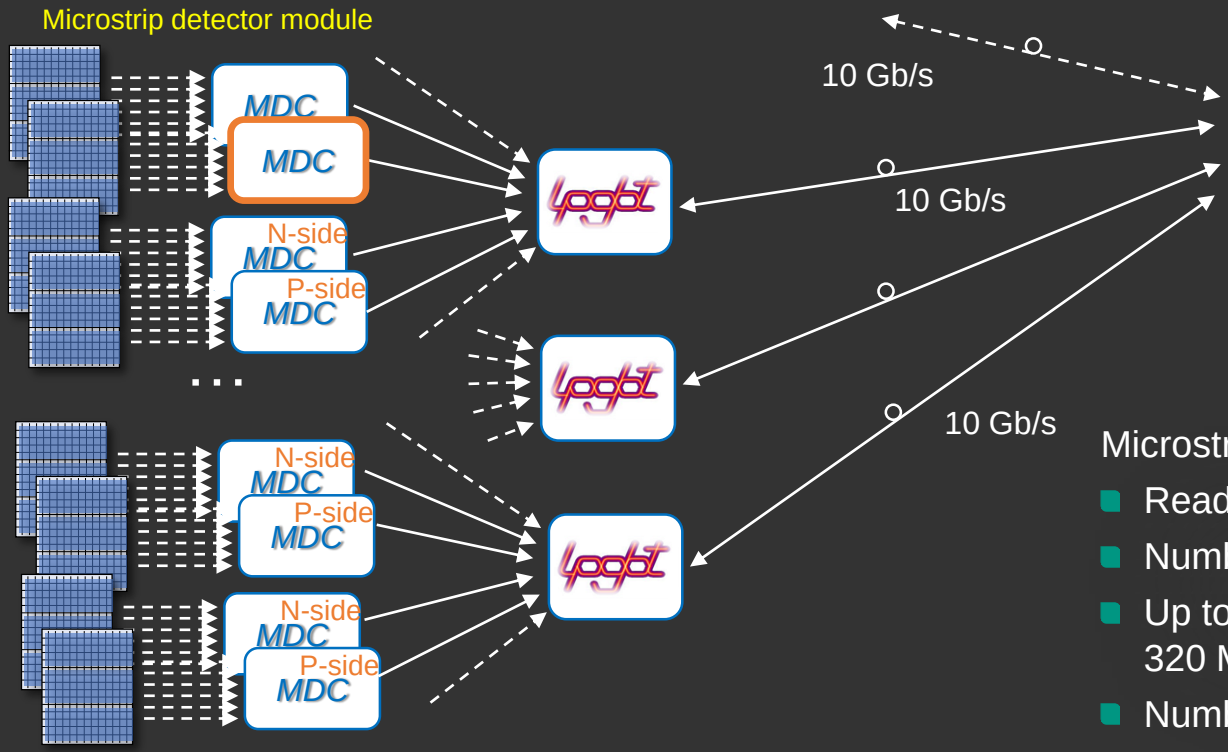
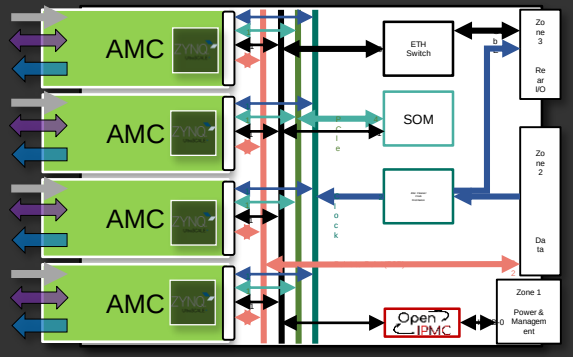
Towards to detector layout simplification

Reduce the number of optical links from/to off-line electronics





Microstrip detector:

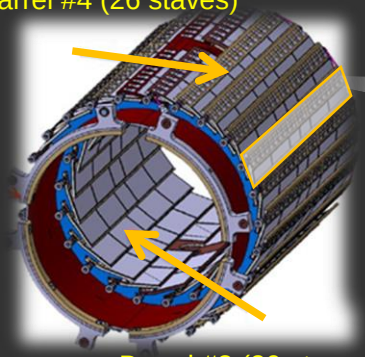
- Readout chips (ToASt): # **2788**
- Number of MDC: **592** @ 320 Mb/s
- Up to 8 detector modules / LpGBT @ 320 Mb/s
- Number of AMC cards: **3**
- Number of ATCA carried card: **1**

Silicon Strip Detector

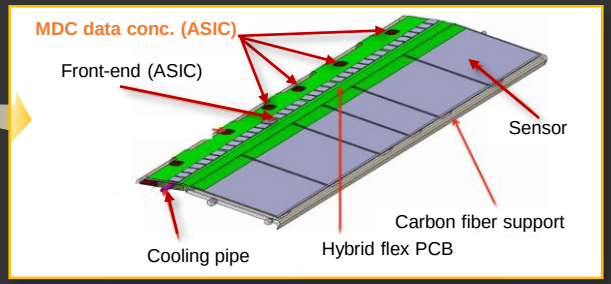
Complex detector modules for both barrel and disk

- **Barrel**
  - # 64 square sensors: 512 x 512 channels
  - # 184 rectangular sensors: 512 x 895 channels

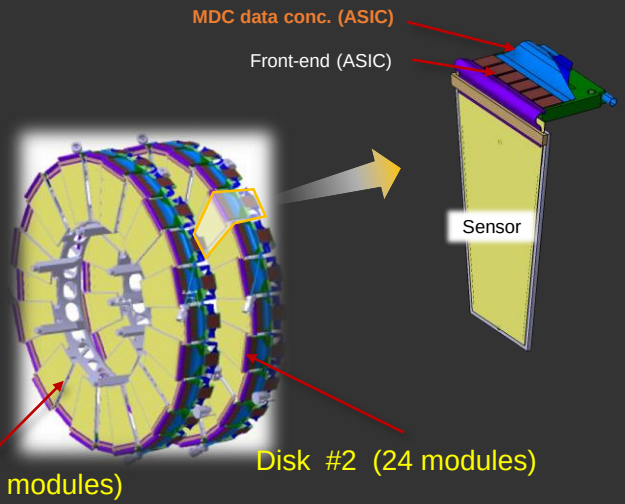
Barrel #4 (26 staves)



Barrel #3 (20 staves)



- **Disk**
  - # 48 trapezoidal sensors: 768 channels per side



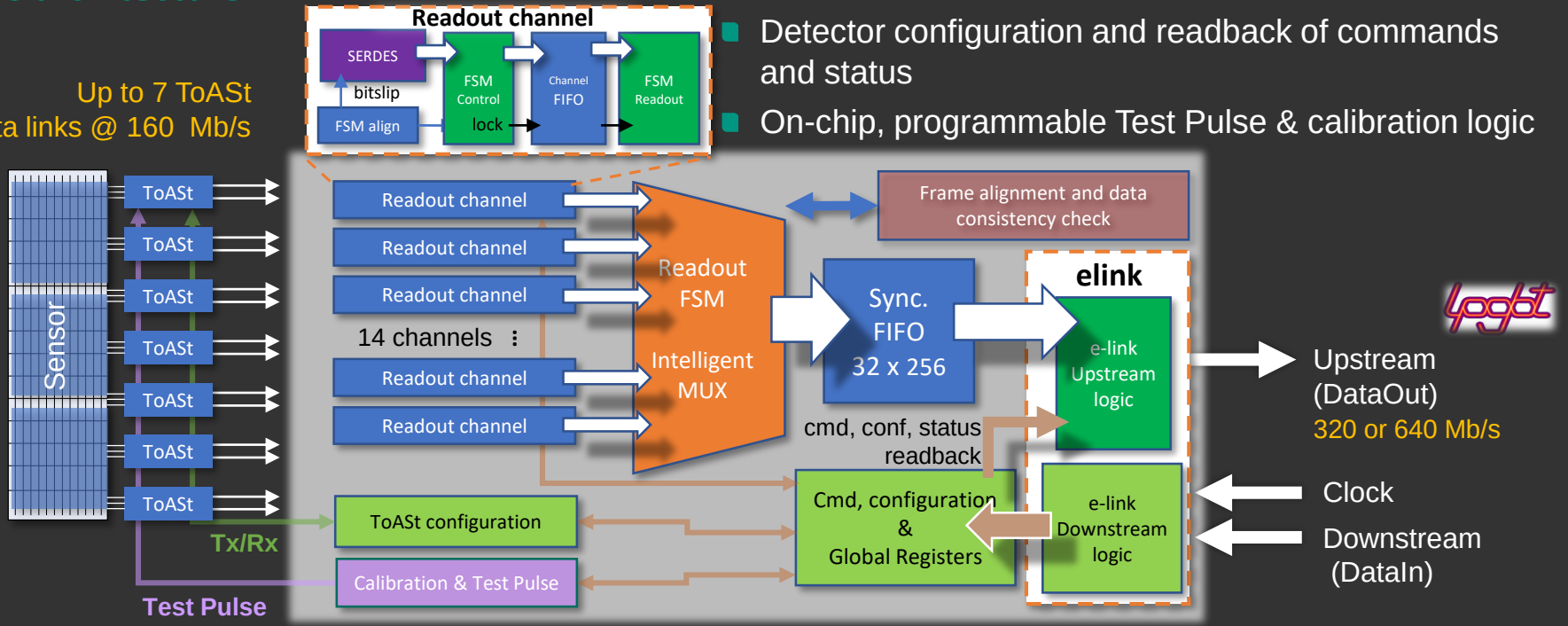
- Number of MDC: #592 ASICs (barrel + Disks) Inside the *active volume*
- Small-area and low-power CMOS technology ASIC
- Rad-tolerant, expected TID: O(10 Mrad/10 years), Single Event protection (SEU), fluence: O(10^{14} n_{eq}/cm^2)

MDC (Module data Concentrator)

ASIC architecture

Up to 7 ToASt
14 data links @ 160 Mb/s

- Detector configuration and readback of commands and status
- On-chip, programmable Test Pulse & calibration logic



Microstrip Detector module

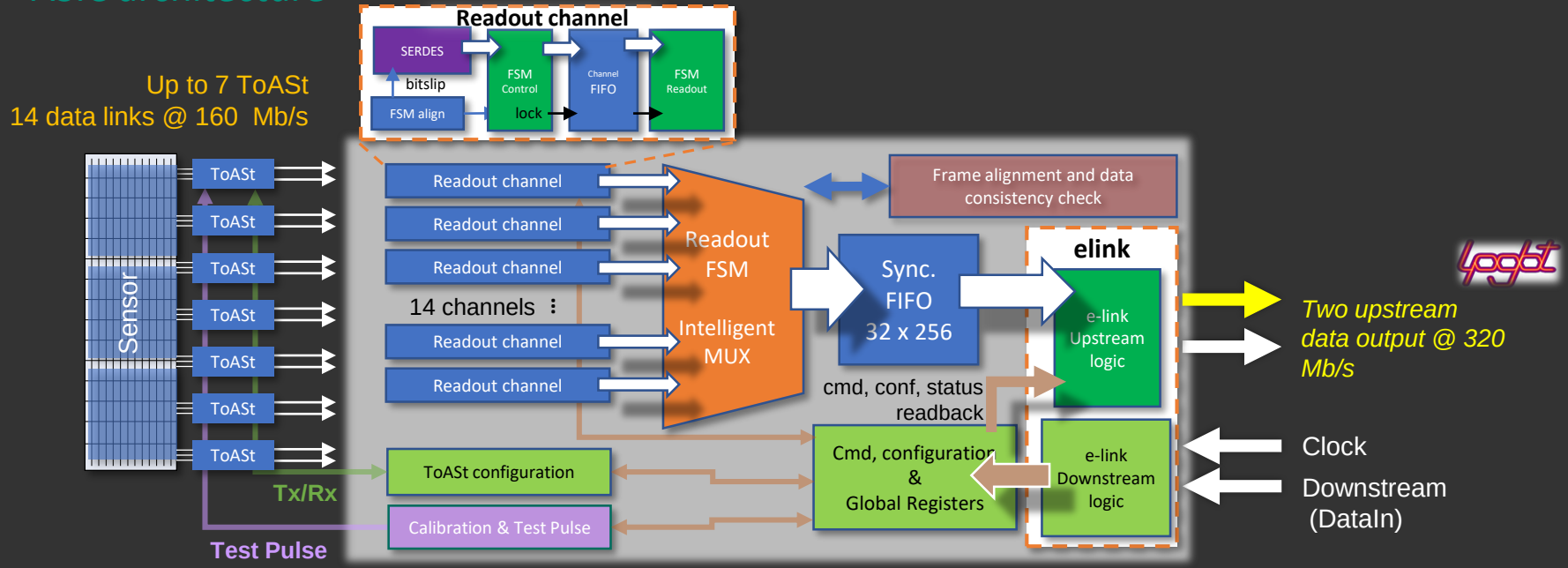
MDC ASIC architecture

LpGBT compatible electrical link

MDC (Module data Concentrator)

News

ASIC architecture



- Two upstream links are implemented to be employed as spare connection and to cope with higher occupancy, more flexibility in the possibility to conceiving new detector module shapes for new application/experiments
- Double Data Rate output driver and logic by Giulio Dellacasa (INFN Turin), operating up to 640 Mb/s *(800 Mb/s 8/10b encoding)*

MDC core

News

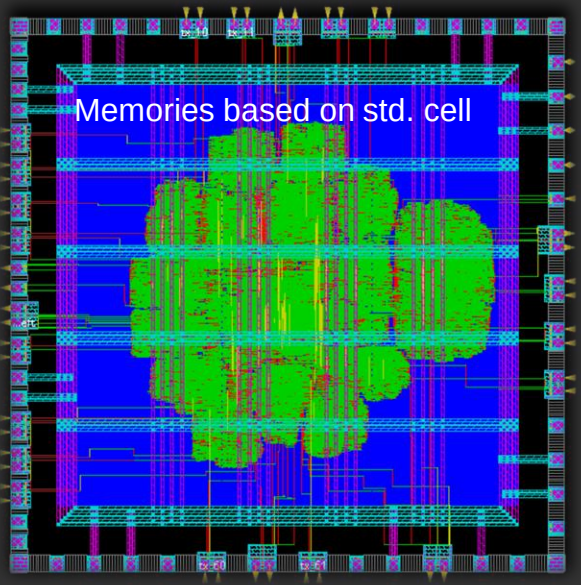
Low-power, small-area, rad-tolerant CMOS ASIC

- All memories / FIFOs replaced by Low Leakage memories logic from Faraday
  - Considerable reduction of the power consumption
  - Layout optimized in area, less occupancy compared to memories implemented by the standard cell
- Detection of anomalies and errors without stopping the data acquisition
  - The readout continues also in presence of critical conditions (i.e. FIFO full or channel not responding)
  - The error flags and status are continuously sent to off-detector electronics
- Programmable test pulse logic for fast execution of S-curver scans
  - Fast calibration of the detector, which is optimized in the time execution
- Programmable polarity of differential clock and input pin (P/N) connections
  - To reduce the routing resources on the detector module

Comparison w/wo faraday memories

Drastic reduction of power consumption and occupancy

PANDA CM 2024_1

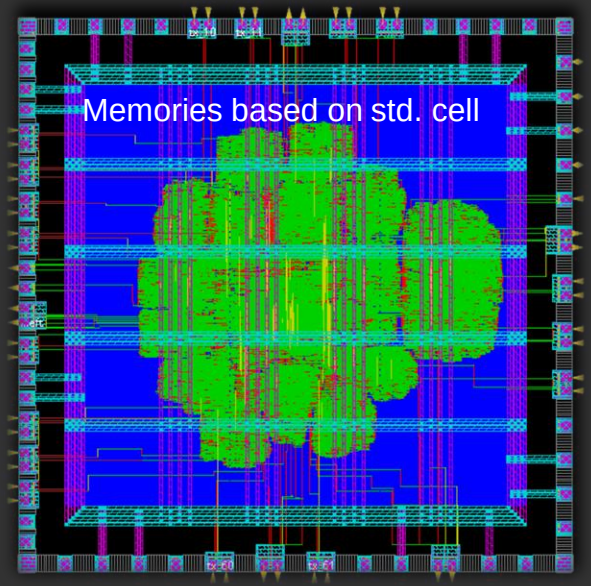


Estimated power consumption: 165 mW @ 1.2V
Density: 40%

Comparison w/wo faraday memories

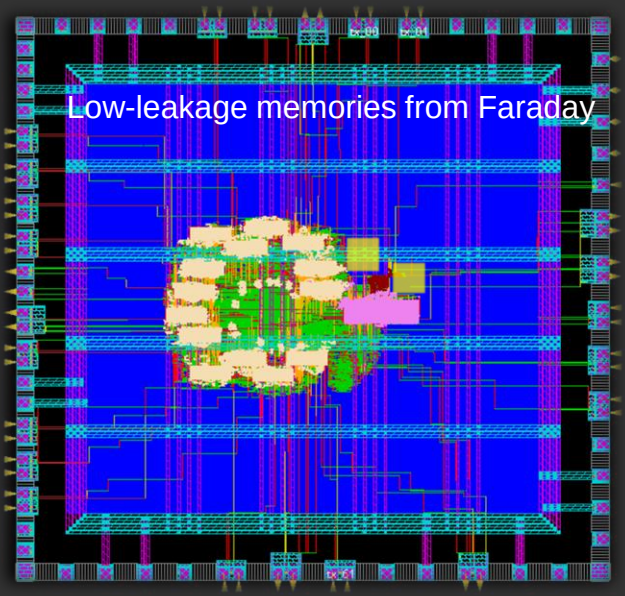
Drastic reduction of power consumption and occupancy

PANDA CM 2024_1



Estimated power consumption: 165 mW @ 1.2V
Density: 40%

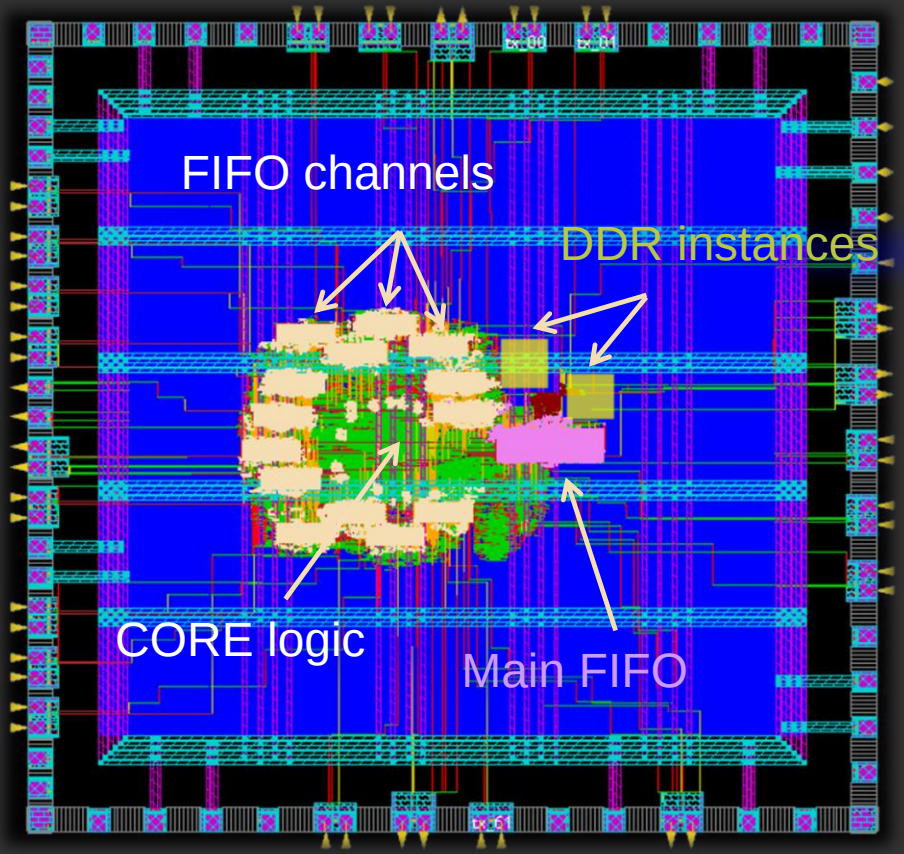
Current version



Estimated power (preliminary): 59.62 mW @ 1.2V
Density: 4.9 %

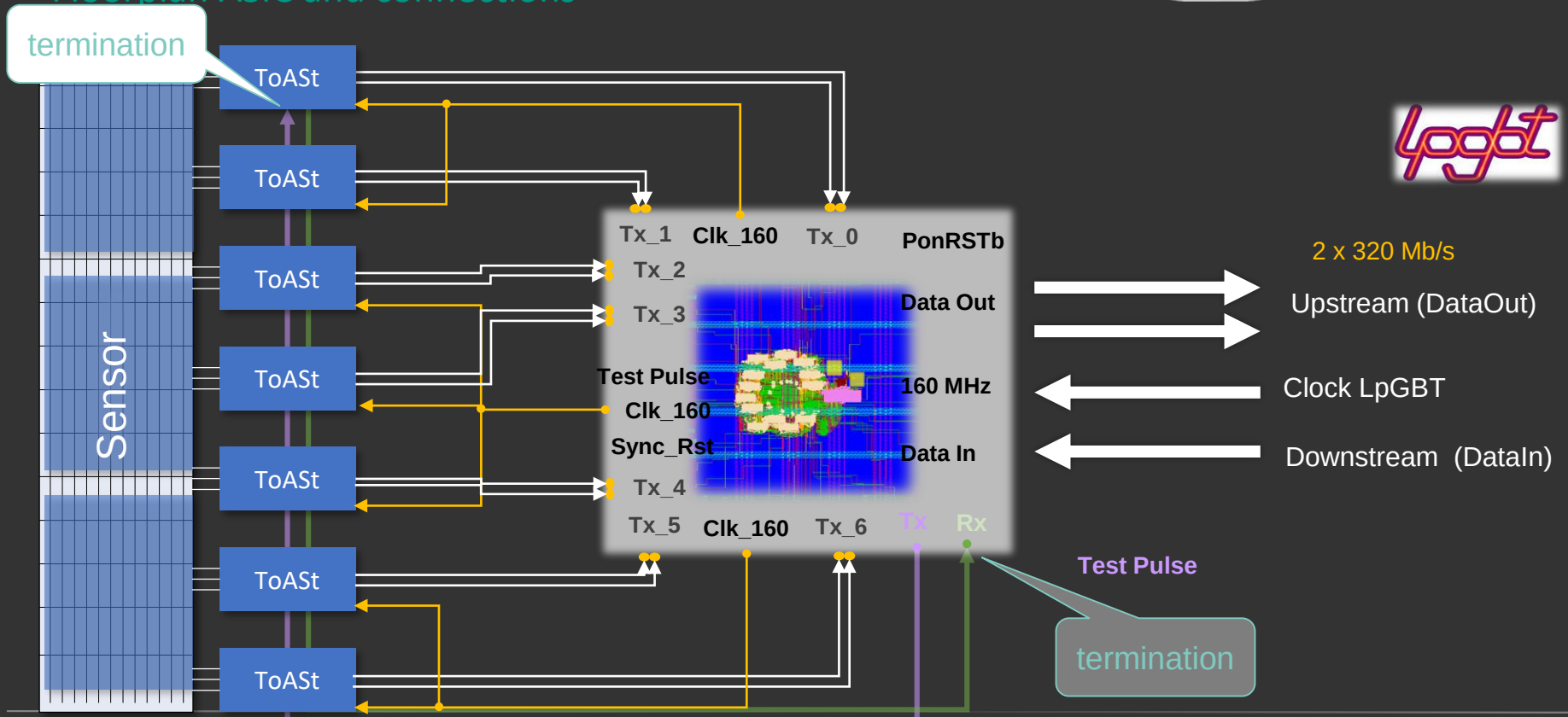
X 2.6

MDC current version



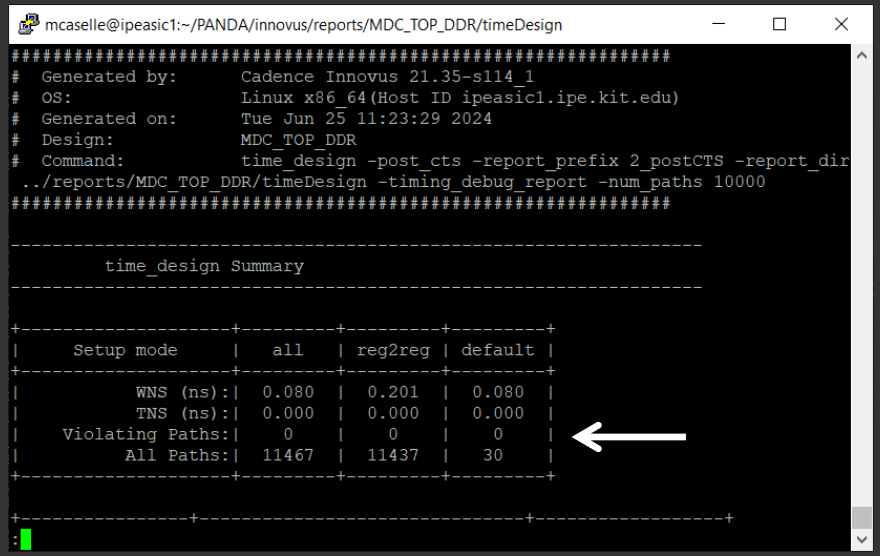
MDC (Module data Concentrator)

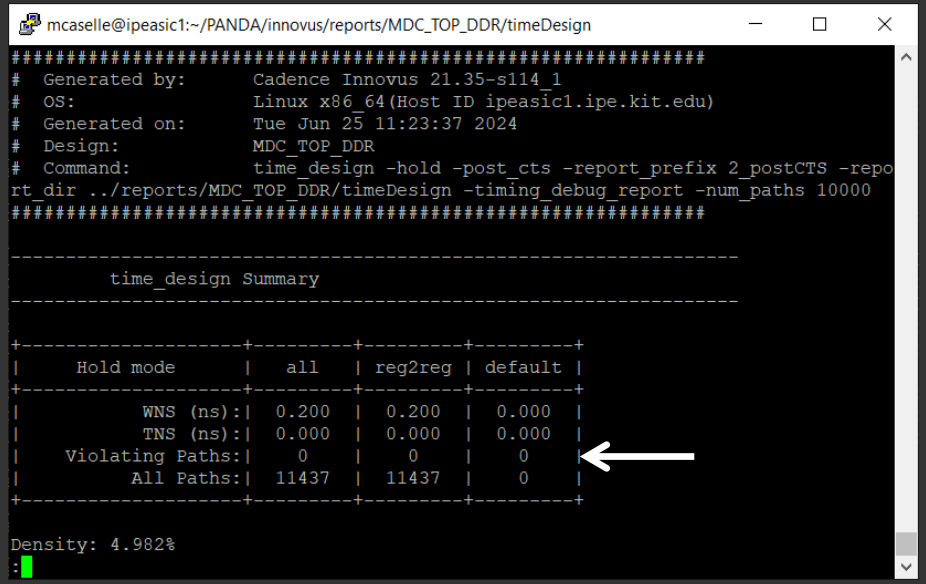
Floorplan ASIC and connections



Timing verification

Preliminary time verification, further improvement are possible

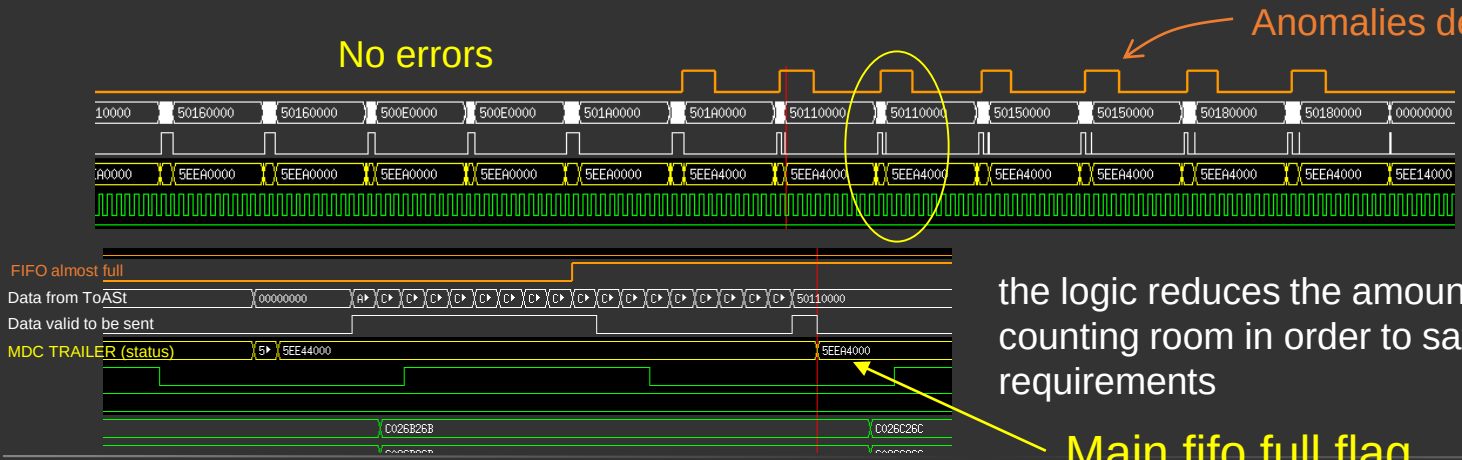




Detection of anomalies and errors

Continuous readout operation also in presence of critical conditions

- Several critical errors could compromise the detector readout, for example, SEU (MDC, ToASt), high occupancy due to a significant number of fake or noisy channels, etc.
- The ***goal*** is to develop a continuous readout mechanism capable of sending information of the anomalies and errors to an off-detector location.
- High-granularity detector recovery mechanism at level of off-detector



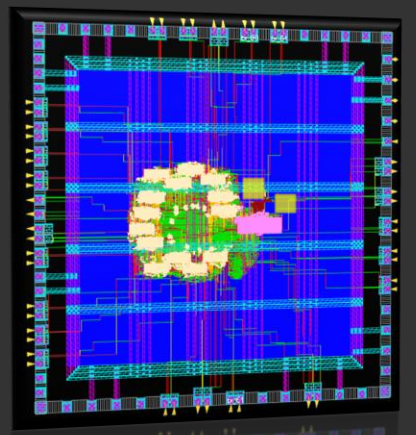
the logic reduces the amount of data it sends to the counting room in order to satisfy the data throughput requirements

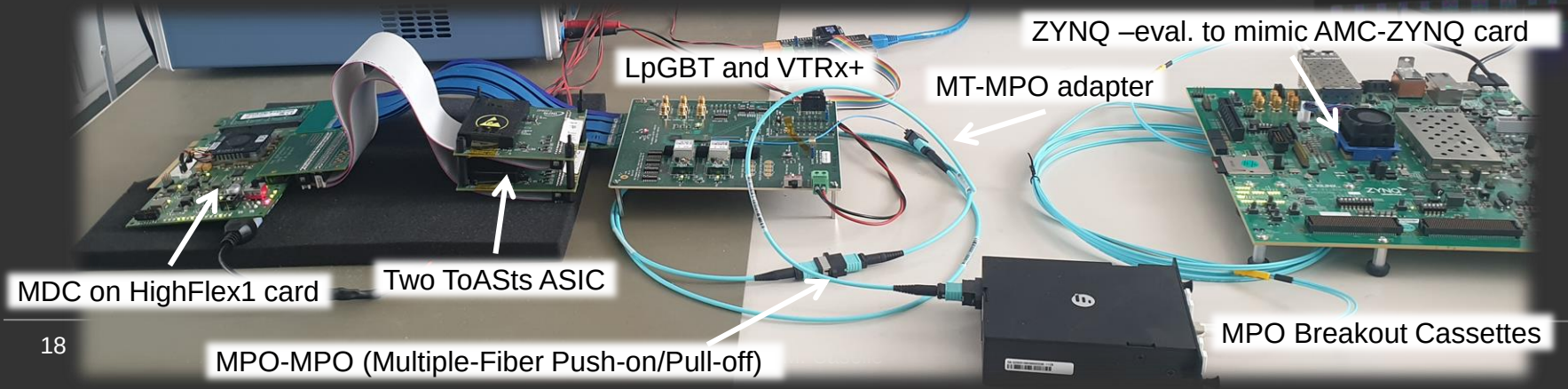
Main fifo full flag

Conclusion & what's next

Fast calibration of the detector

- Final verification of the MDC ASIC is on-going
  - DRC, LVS, timing analysis
- The submission of the ASIC is booked for September, 2nd (2024)
- Established a setup for continuous integration of ToASt, MDC, LpGBT and MMB readout. Test will be continue by using of the MDC-FPGA implementation






Thank you for your attention