



## Overview CB-ELSA DAQ system

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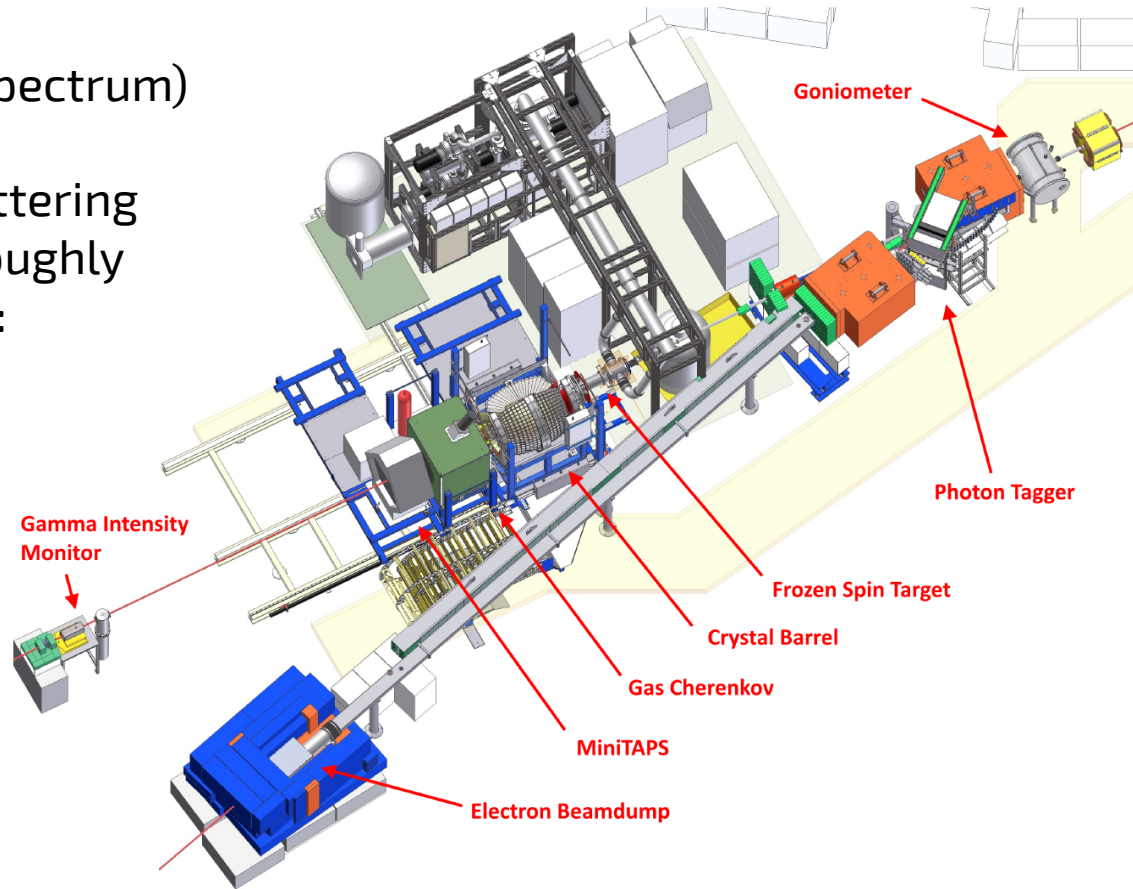
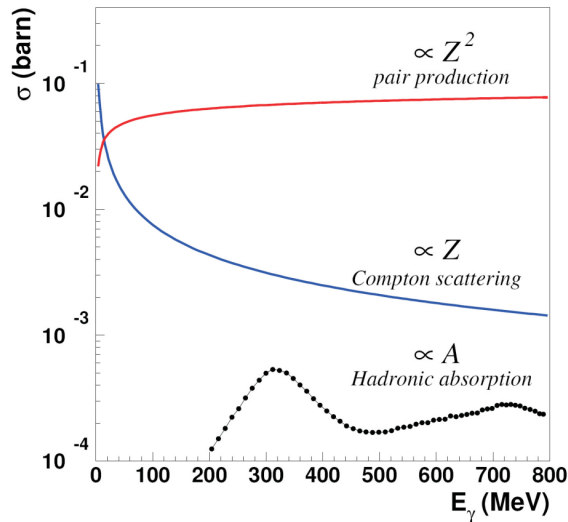
Helmholtz-Instituts für  
Strahlen- und Kernphysik



- CB-ELSA/TAPS experiment
- DAQ-system
- Sync-system
- Ideas for the future

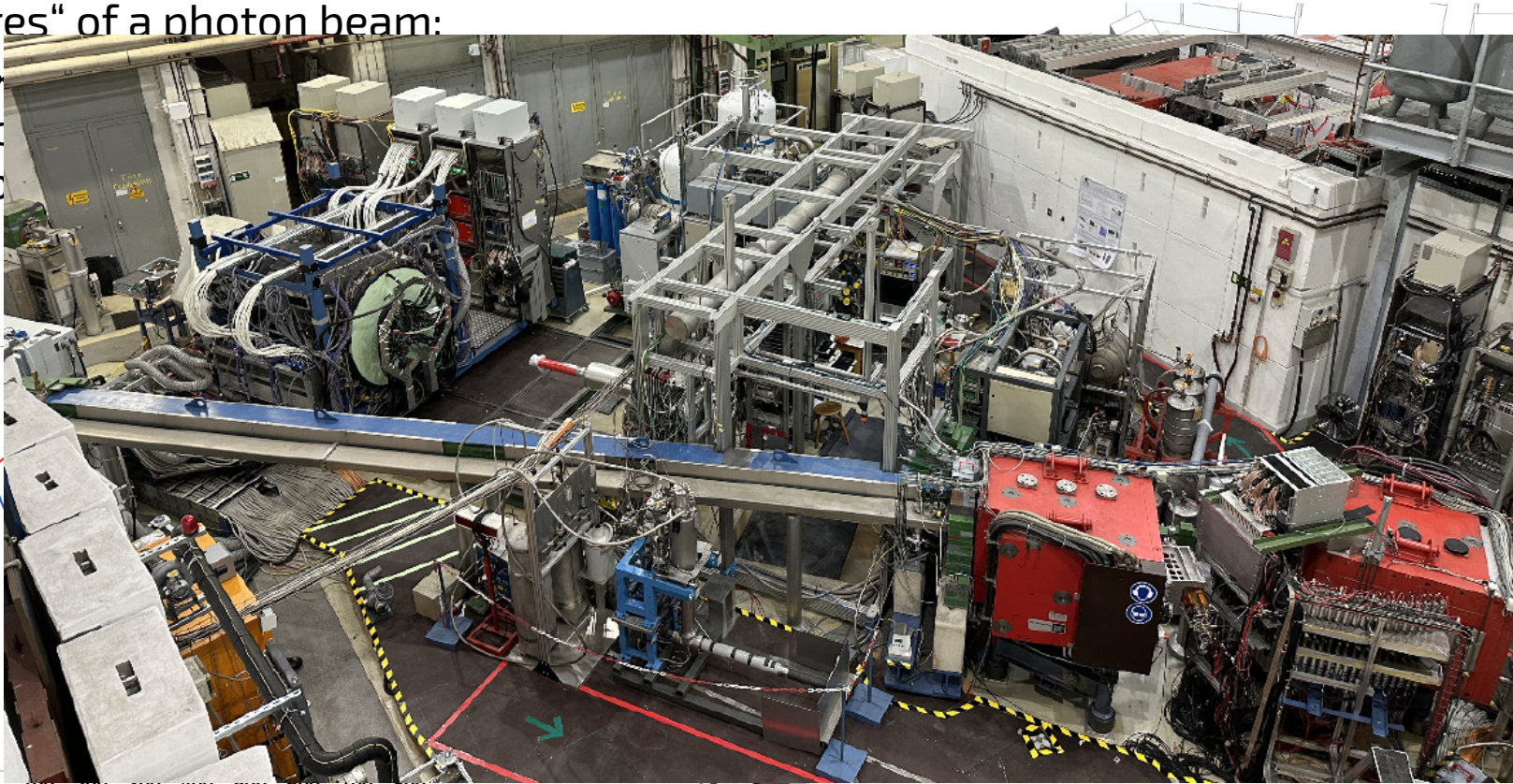
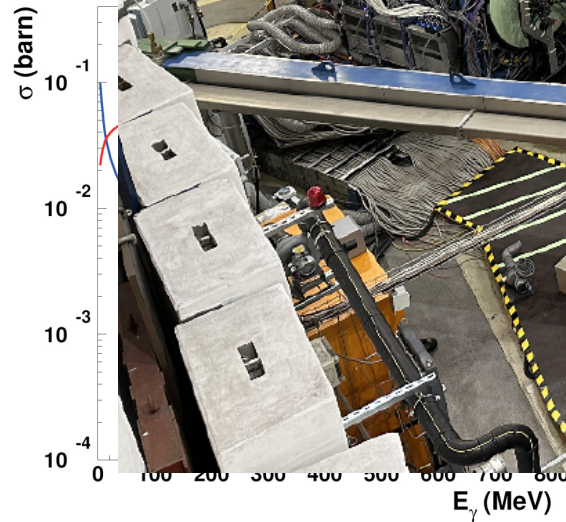
„Features“ of a photon beam:

- No fixed energy (Bremstrahl-spectrum)
- Photon cross section for pair production + compton scattering in a liquid hydrogen target is roughly 1000 times higher than  $\gamma p \rightarrow pX$ :

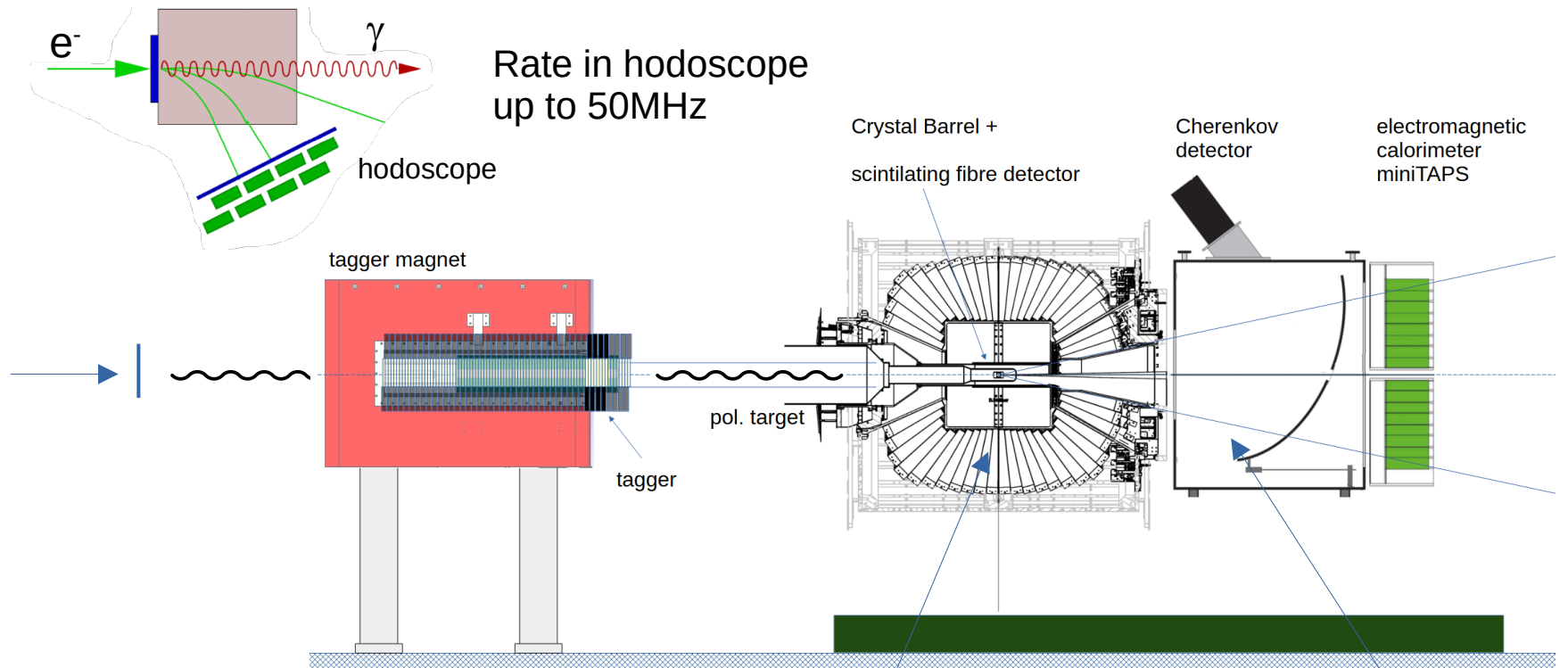


„Features“ of a photon beam:

- No fixed energy
- Photons from pair production in a linac
- 1000 photons per bunch



# Current CB-ELSA/TAPS experiment

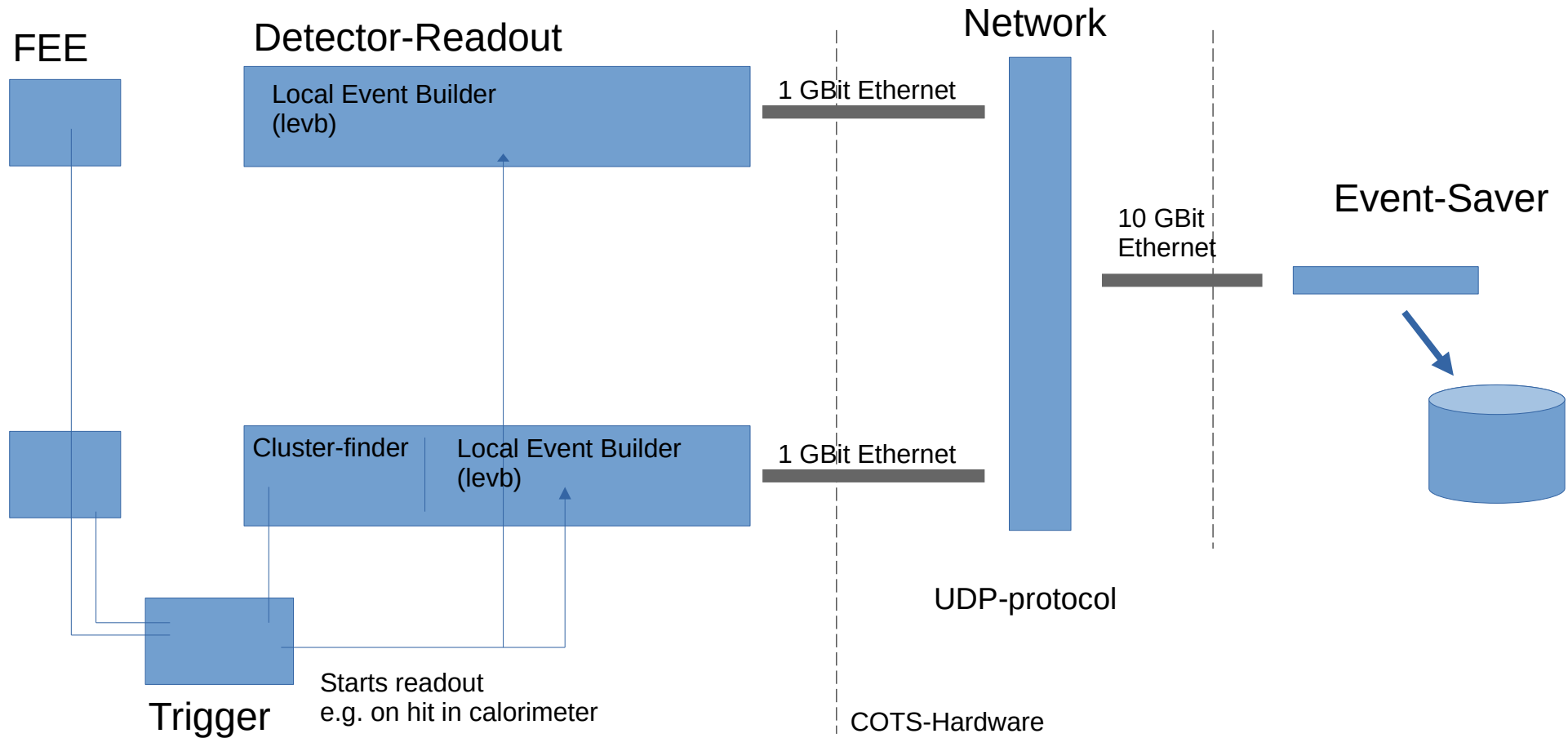


Rate in hodoscope  
up to 50MHz

Trigger is used to reduce data rates  
mainly by looking for hits in the calorimeter

interesting hadronic events  
~10-20kHz

interaction rate  
up to 2MHz

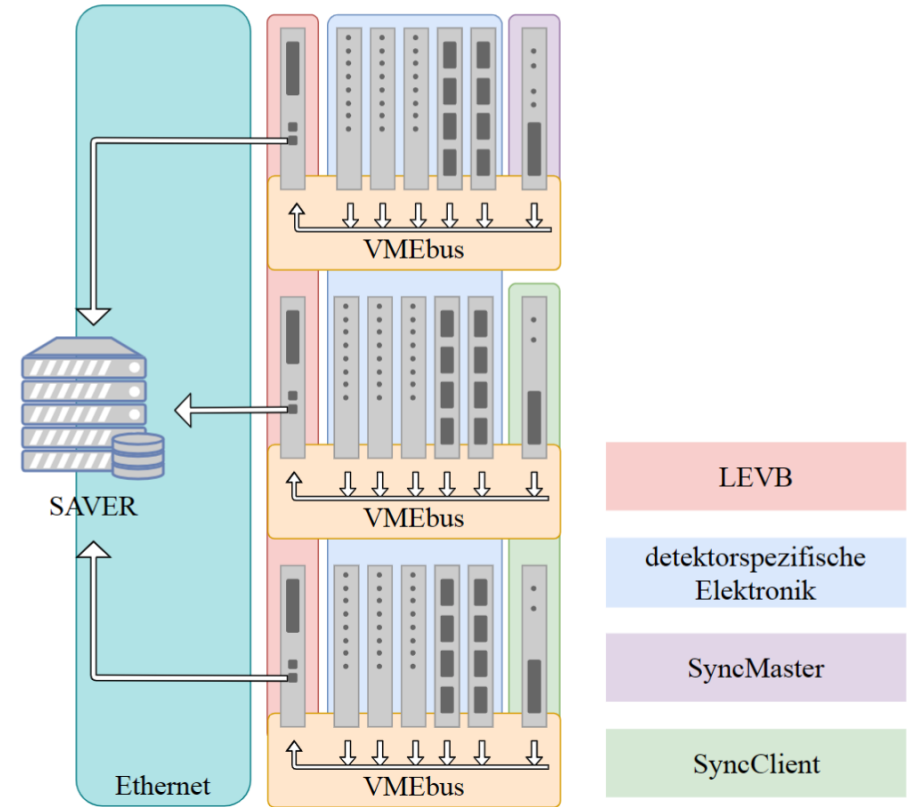




## Hybrid system

- VMEbus based modules
  - CPU  
readout, sync-handling, transport
  - FPGA based  
readout, cluster finding, transport
  - Custom boards (TAPS)
- Crystal Barrel readout
  - based on PANDA FWEC SADC
  - levb on FPGA

Deadtime from readout 50-100 $\mu$ s  
10kHz Trigger rate  $\rightarrow$  50-70% livetime

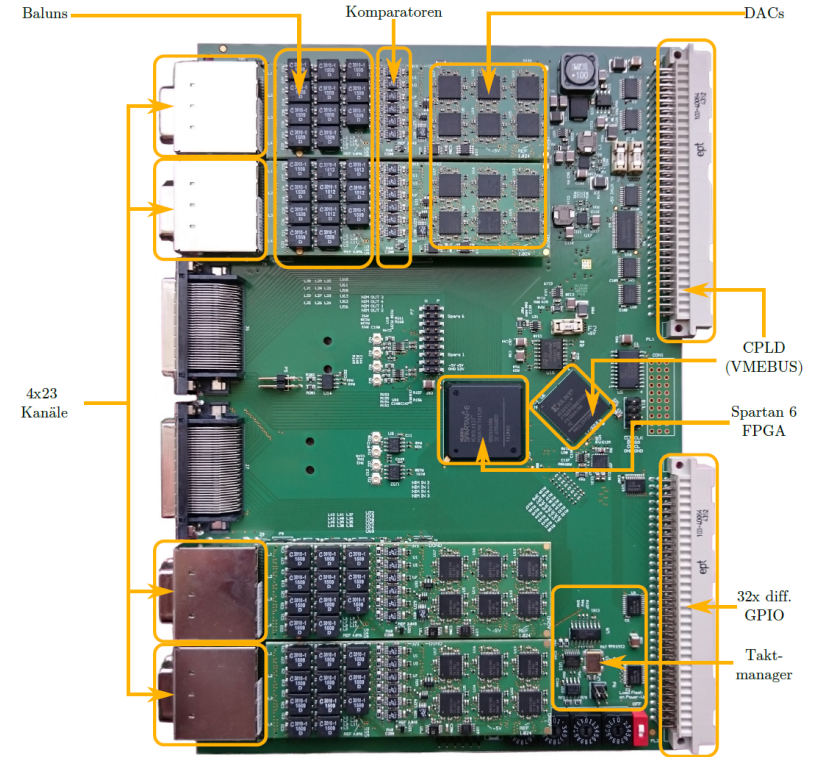


## Cluster finder hardware (trigger / readout)

based on Xilinx Spartan 6 board (ELB)

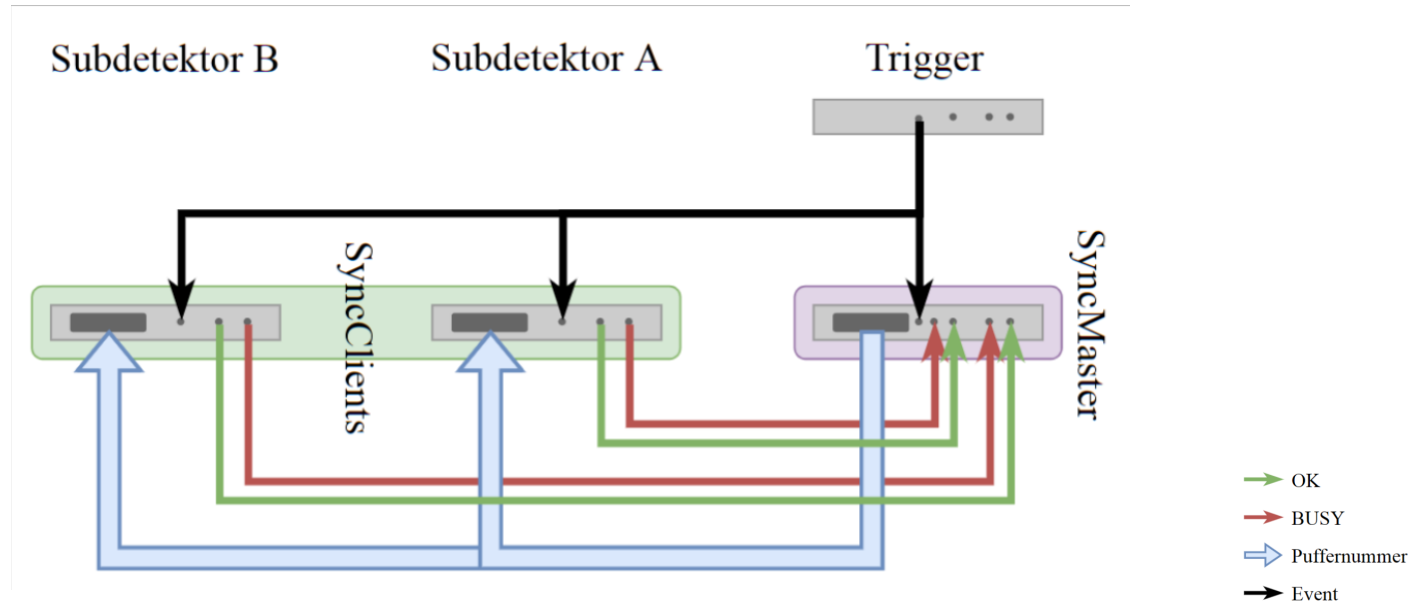
- TDC implementations
  - tapped delay line TDC  
(7bit per 5ns clock cycle  $\rightarrow$   $\sim$ 40ps)
  - sampling TDC based on deserializer  
(2bit per 5ns cycle  $\rightarrow$   $\sim$ 1ns)
- Distributed cluster finding logic  
(special backplane to interconnect boards)
- Discriminators on mezzanine card

replaced VMEbus data transport  
via ext. Gbit card





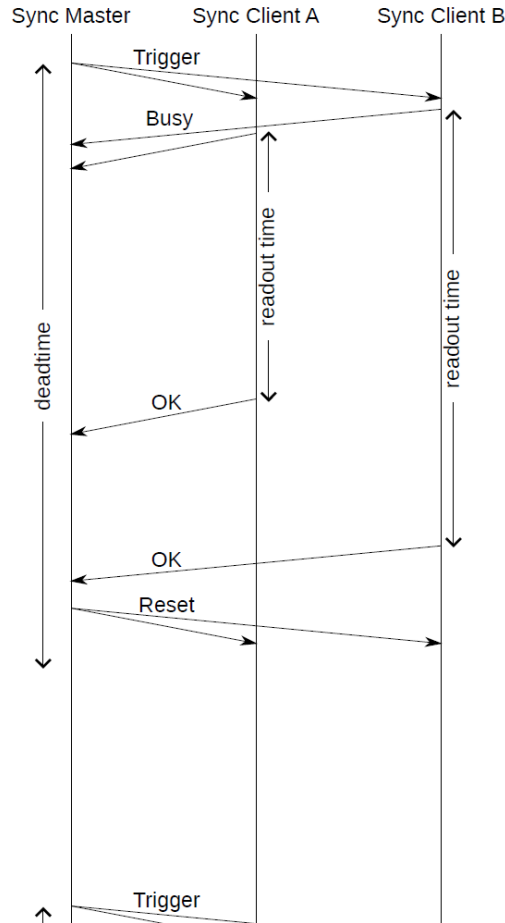
Detectors are read out individually and in parallel. Sync system used to ensure no subdetector misses a trigger.



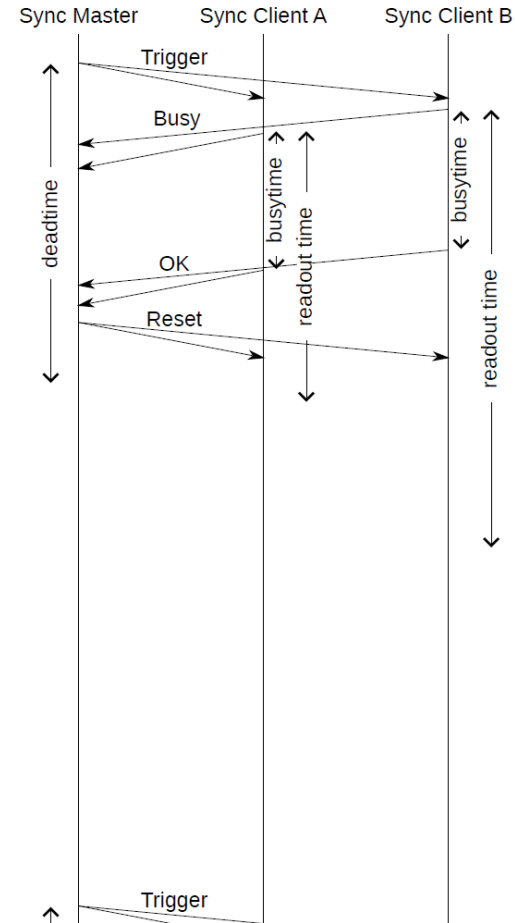
checks for

- successful readout (Busy, OK)
- data integrity (common buffer number)

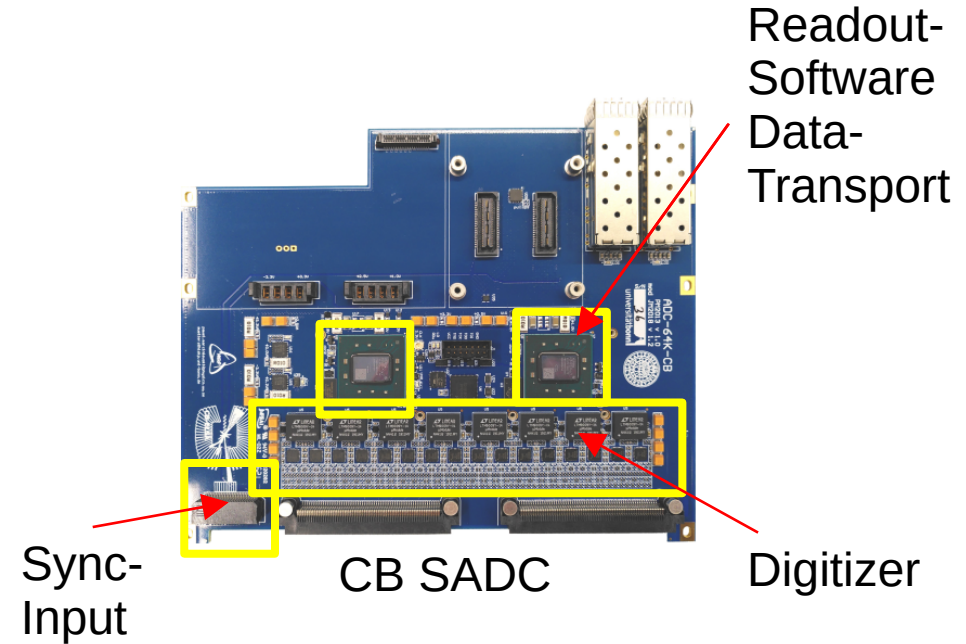
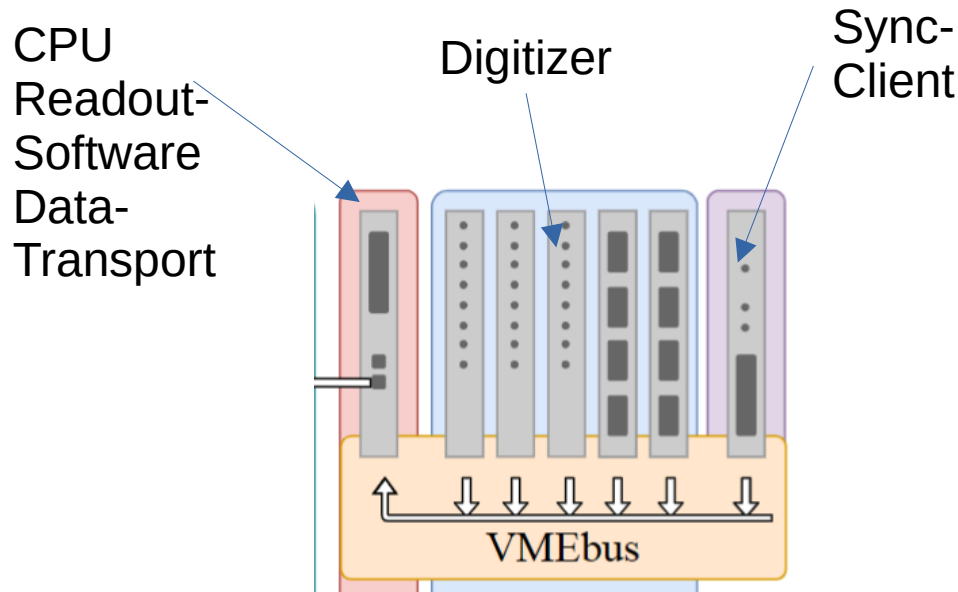
# Sync – system / asynchronous readout



- large buffer available on readout boards
- no need to wait until all data transferred to CPU
- only wait until ready to accept new trigger
- data transfer while waiting for the next trigger
- Not limited to VME readout:  
high-latency transfer (e.g. ethernet) also possible



Concept of LEVB can be integrated on FPGA

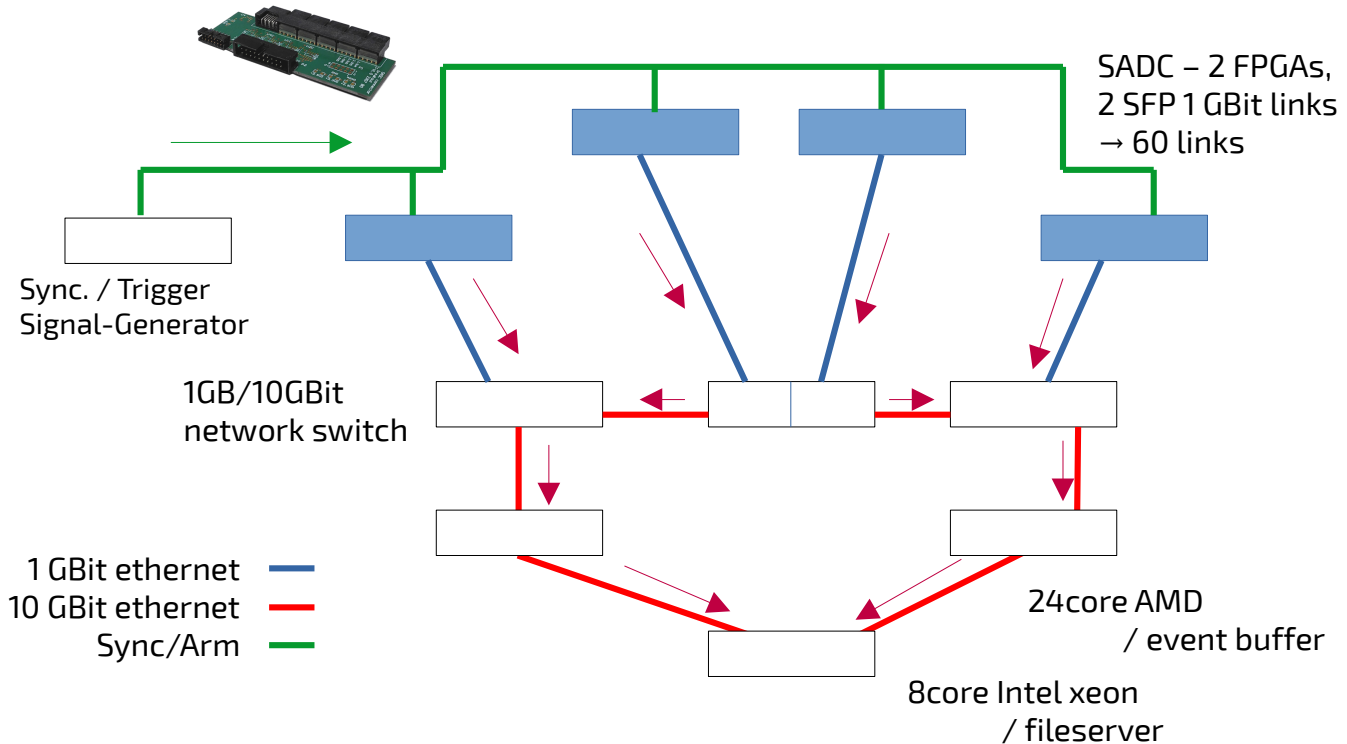


Crystal Barrel SADC readout platform flexibel for triggered or free running readout  
→ Choice by adaption of firmware

CB firmware capable of self triggering, but readout is done over 32chs

No central trigger  
→ self triggered

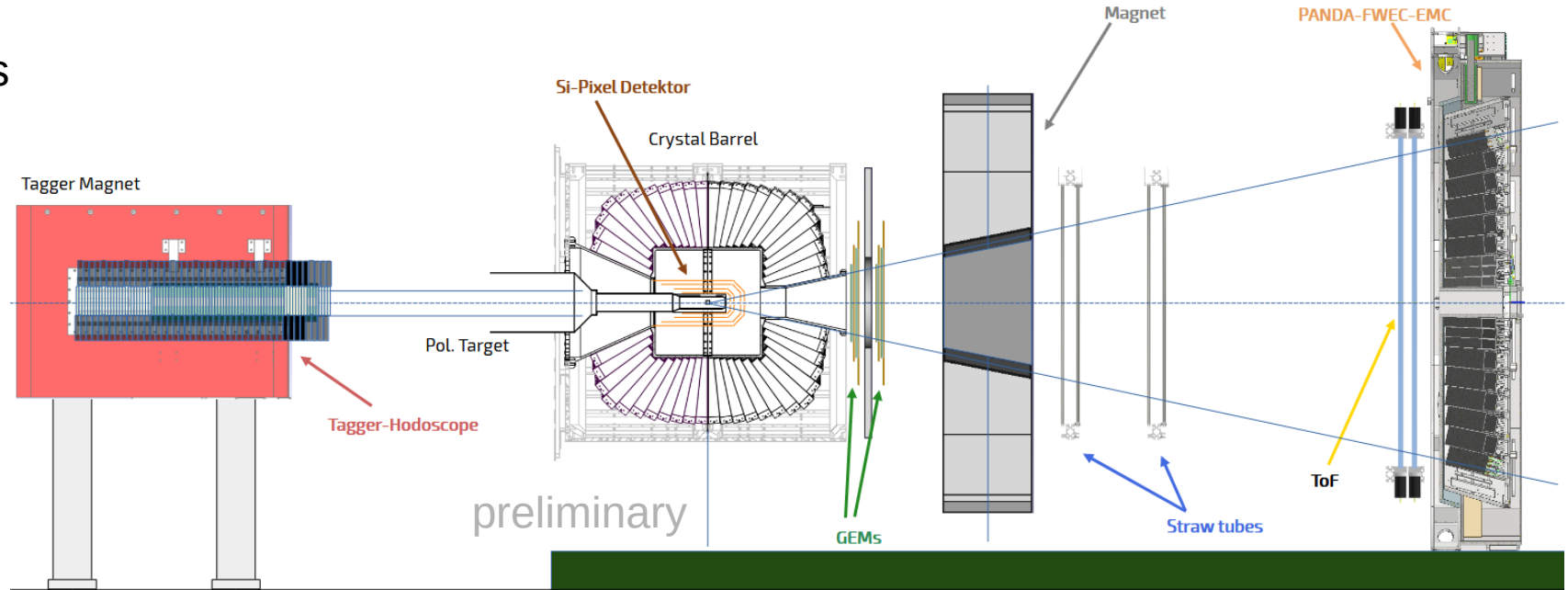
- Readout of 32chs and transport introduces significant deadtime. (waveform transmitted)
- To avoid incomplete events sADCs are blocked (disarmed) for some time



Firmware will be updated to single channel readout.

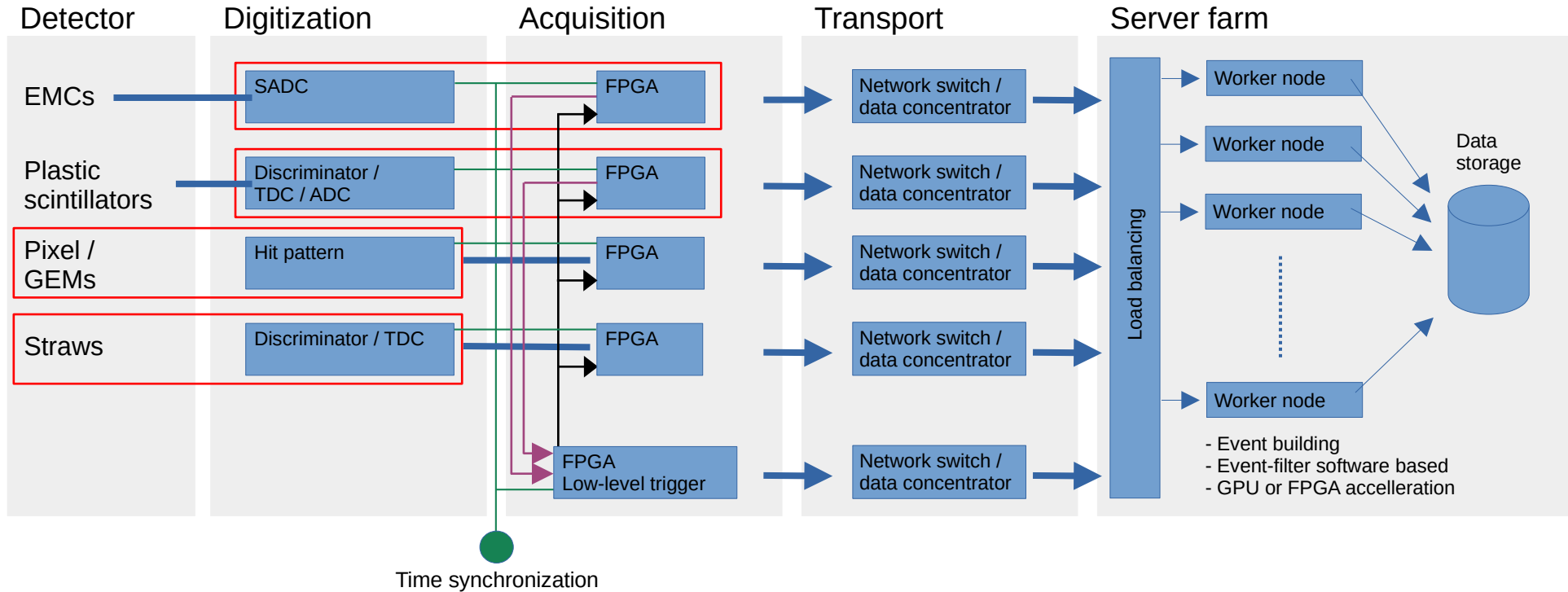
For the upgrade many new detectors will enter

- Pixels
- GEMs
- Straws



New detectors will be FPGA based readout systems

→ CB-ELSA DAQ needs further improvements to integrate new systems





- Current DAQ-system is running fine and is sufficient for current needs

## Future upgrade

- Detailed design/planning:
  - integration of new systems with more free running architecture
  - forward endcap needs some „cluster finder“ for trigger
  - introducing a common time reference for event matching
- Transition from a triggered to a more free running system:
  - new detectors might need it for trigger/filter
  - reuse „hardware trigger“ for a time window to look for wanted events
    - e.g. reduce data rates from tagging system