

PANDA Collaboration Meeting 24/2

PANDA FEE/DAQ Workshop

Nest DAQ

featuring conti. RO w/ FairMQ

and related topics

Content:

NestDAQ Over View

Development status from the test BM

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26.06.2024

Kotaro Shirotori

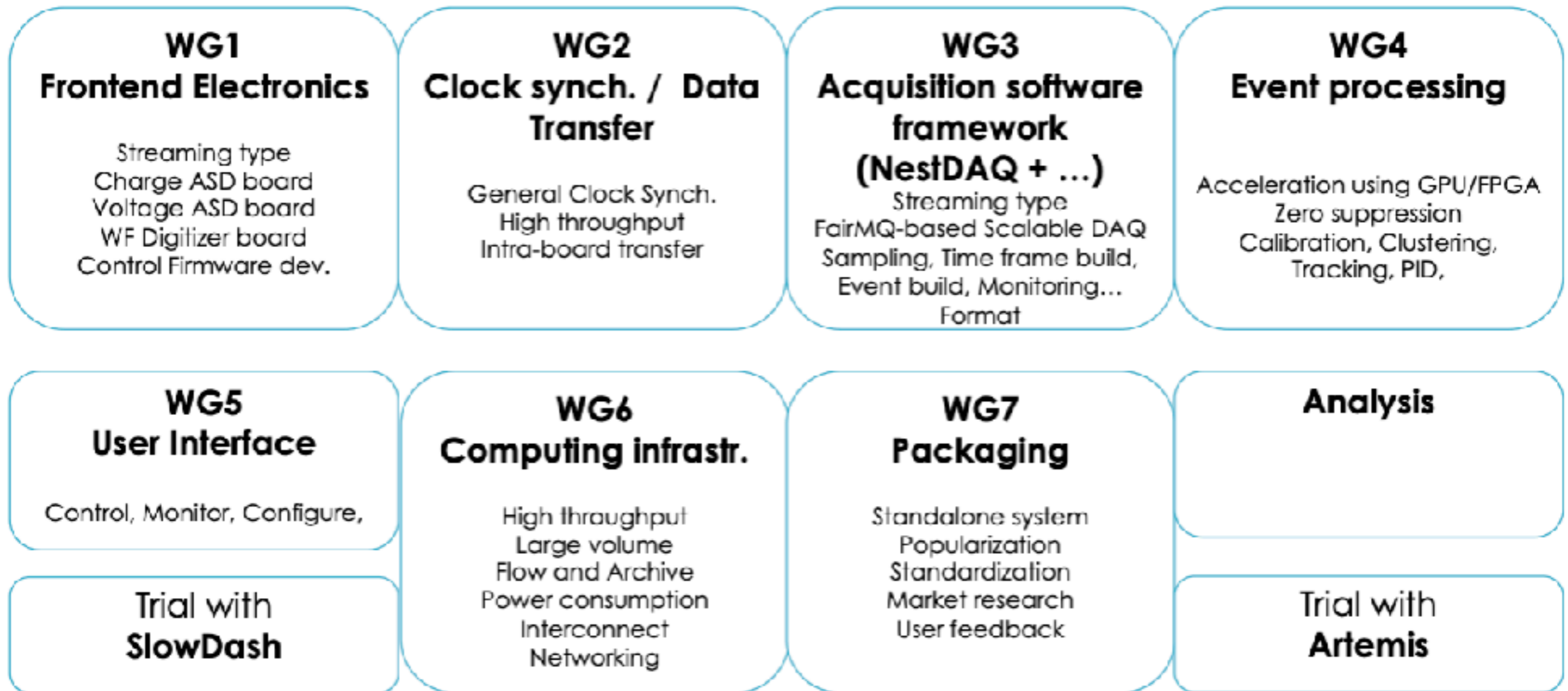
SPADI Alliance

Signal processing and data acquisition infrastructure alliance

- Since ~2022.
- Developing a next generation DAQ/FEE system for nuclear/hadron physics experiments.
- Standardisation, in Japan and beyond.
- Participation from majority of nuclear/hadron physics institutes in Japan.
 - RCNP, KEK
- c.f. Collider Electronics Forum. OpenIT
- very active, relatively a small number of developers
<https://www.rcnp.osaka-u.ac.jp/~spadi/>

SPADI Alliance

Signal processing and data acquisition infrastructure alliance



No ASIC Development (so far)

NestDAQ on GitHub

The screenshot shows the GitHub repository page for `spadi-alliance/nestdaq`. The repository is public and has 4 watches, 5 forks, and 3 stars. The main branch is `main`, with 1 branch and 2 tags. The repository description is "A streaming DAQ implementation for the particle measurements".

The repository structure is as follows:

| File/Folder | Commit Message | Time |
|-----------------------------|--|--------------|
| <code>controller</code> | - add TelemetryPlugin, which outputs log to stdout | 5 months ago |
| <code>examples</code> | - add TelemetryPlugin, which outputs log to stdout | 5 months ago |
| <code>plugins</code> | close #32, fix #33 | 5 months ago |
| <code>scripts</code> | - add TelemetryPlugin, which outputs log to stdout | 5 months ago |
| <code>share</code> | - add checkboxes to wait state transitions (close #26) | 6 months ago |
| <code>.gitignore</code> | import files | 2 years ago |
| <code>CMakeLists.txt</code> | A typo (add_compiler_options --> add_compile_optio... | 5 months ago |
| <code>INSTALL.md</code> | - Changes: WebGui, html | last year |
| <code>LICENSE</code> | Initial commit | 2 years ago |
| <code>README.md</code> | Update README.md | 2 years ago |

The repository also includes a `README` and `MIT license`.

NestDAQ
A streaming DAQ implementation for the particle measurements

Tested system

About
A streaming DAQ implementation for the particle measurements

- Readme
- MIT license
- Activity
- Custom properties
- 3 stars
- 4 watching
- 5 forks

Report repository

Releases 2

- RCNP202307** (Latest)
on Aug 16, 2023
- + 1 release

Packages
No packages published

Contributors 3

- tntakahashi Tomonori Takahashi
- igalashi
- nobukoba

NestDAQ Dependencies

NestDAQ

A streaming DAQ implementation for the particle measurements

Tested system

| System | Version | Compiler | CMake |
|--------|---------|--------------------------|--------------------------------|
| CentOS | 7 | GCC 8.3.1 (devtoolset-8) | 3.14.6 or later (epel: cmake3) |

External packages used with NestDAQ

| Packages | Version | URL |
|------------------|---------|---|
| Redis | 6.0.10 | https://github.com/redis/redis/ |
| Redis TimeSeries | 1.4.18 | https://github.com/RedisTimeSeries/RedisTimeSeries/ |
| Grafana | | |

Dependencies to build NestDAQ

| Packages | Version | URL |
|-----------------|---------------------------|---|
| boost | 1.72.0 or later | |
| FairLogger | 1.9.0 or later | |
| FairMQ | 1.4.26 or later | |
| hiredis | 1.0.0 | https://github.com/redis/hiredis/ |
| redis-plus-plus | 1.2.1 (recipes branch) | https://github.com/sewnew/redis-plus-plus |

Streaming DAQ based on FairMQ

Redis on memory database

NestDAQ Features

- Continuous Readout (based on FairMQ)
- Scalable
- Clock synchronisation (MIKUMARI)
- Data transfer with SiTCP* (TCP implementation on FPGA)
 - 10 Gbps / 1 Gbps
- data stream, divided into a time interval, Heart-Beat-Frame (HBF)
 - 125 MHz, 16bit = 524.288 μ s
- CPU/GPU
- Replayer

*<https://www.sitcp.net/>

DAQ Controller

DAQ controller

RUN number

New value: Auto increment at RUN-Stop
Next : 2048
Latest : 2048
Start :
Stop :

State transition command

Wait Device Ready Wait Ready

Idle > Running

Idle > Device Ready > > Ready > > Running

Idle < Running

Idle < < Device Ready < < Ready < < Running

> Exit

Any state > > Exiting

State Summary

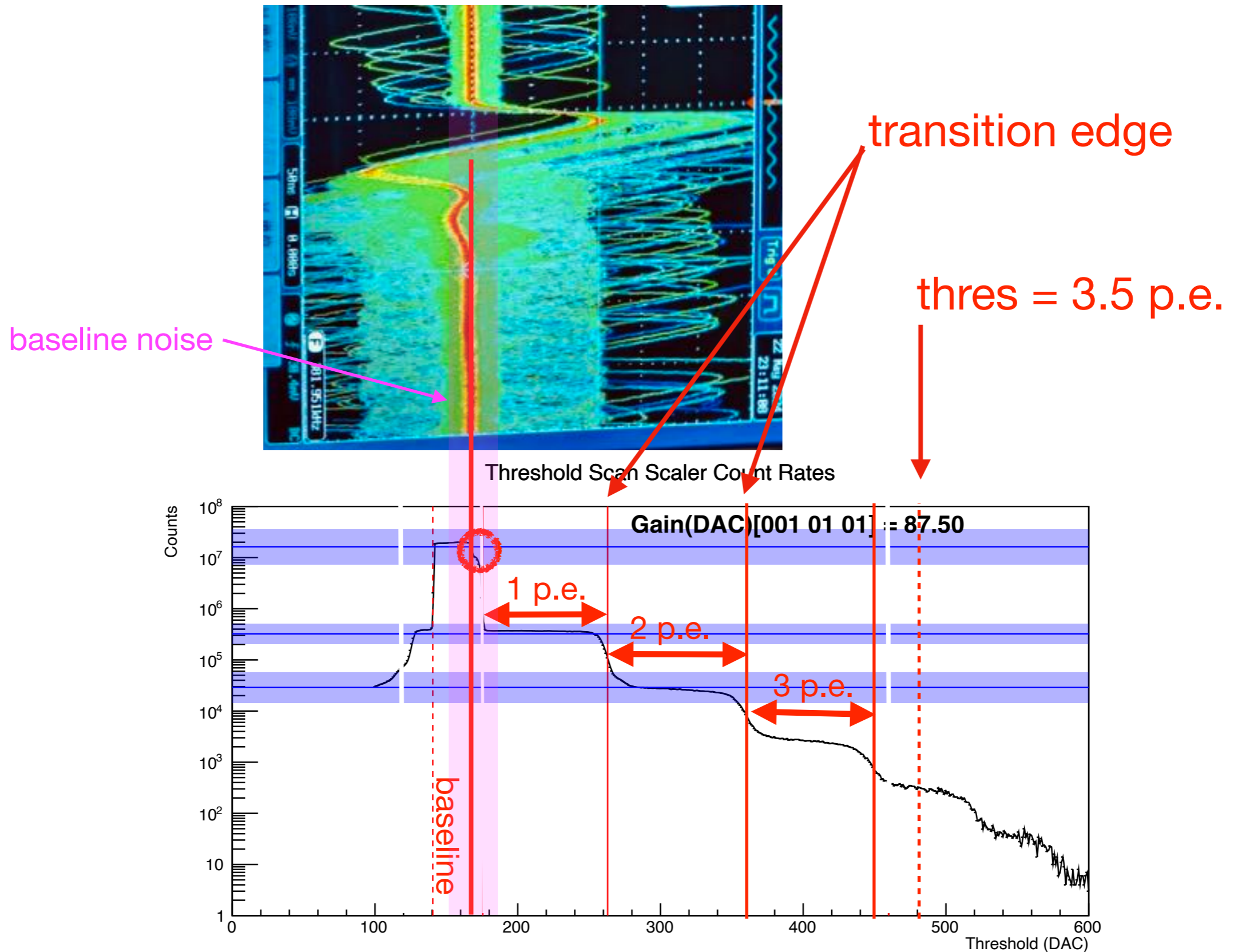
| Service | N | Undef. | Ok | Error | Idle | Init-Device | Init. Bind. | Bound Conn. | Device-Ready | Init-Task Ready | Running | Reset-Task | Reset-Device | Exiting | Last-update |
|---------------------------------|----|--------|----|-------|------|-------------|-------------|-------------|--------------|-----------------|---------|------------|--------------|---------|---------------------|
| AnQSirIdeSampler | 39 | | | | | | | | | | 39 | | | | 2024-06-02T07:45:52 |
| DevSink | 4 | | | | | | | | | | 4 | | | | 2024-06-02T07:45:50 |
| FileSink | 4 | | | | | | | | | | 4 | | | | 2024-06-02T07:45:37 |
| FilterTimeFrameSliceBySomething | 8 | | | | | | | | | | 8 | | | | 2024-06-02T07:45:52 |
| LogicFilter | 4 | | | | | | | | | | 4 | | | | 2024-06-02T07:45:51 |
| SIBuilder | 39 | | | | | | | | | | 39 | | | | 2024-06-02T07:45:52 |
| TimeFrameBuilder | 2 | | | | | | | | | | 2 | | | | 2024-06-02T07:45:51 |
| TimeFrameSlicerByLogicTiming | 8 | | | | | | | | | | 8 | | | | 2024-06-02T07:45:50 |

Slow Dash

- “slow” communication with FEEs using RBCP
 - Remote Bus Control Protocol, a simple memory access protocol for SiTCP
 - Get scaler information implemented on FPGAs, show data rate, hit patterns, time trends, **independently from DAQ**
- DCS



E.g. SiPM Gain Calib.

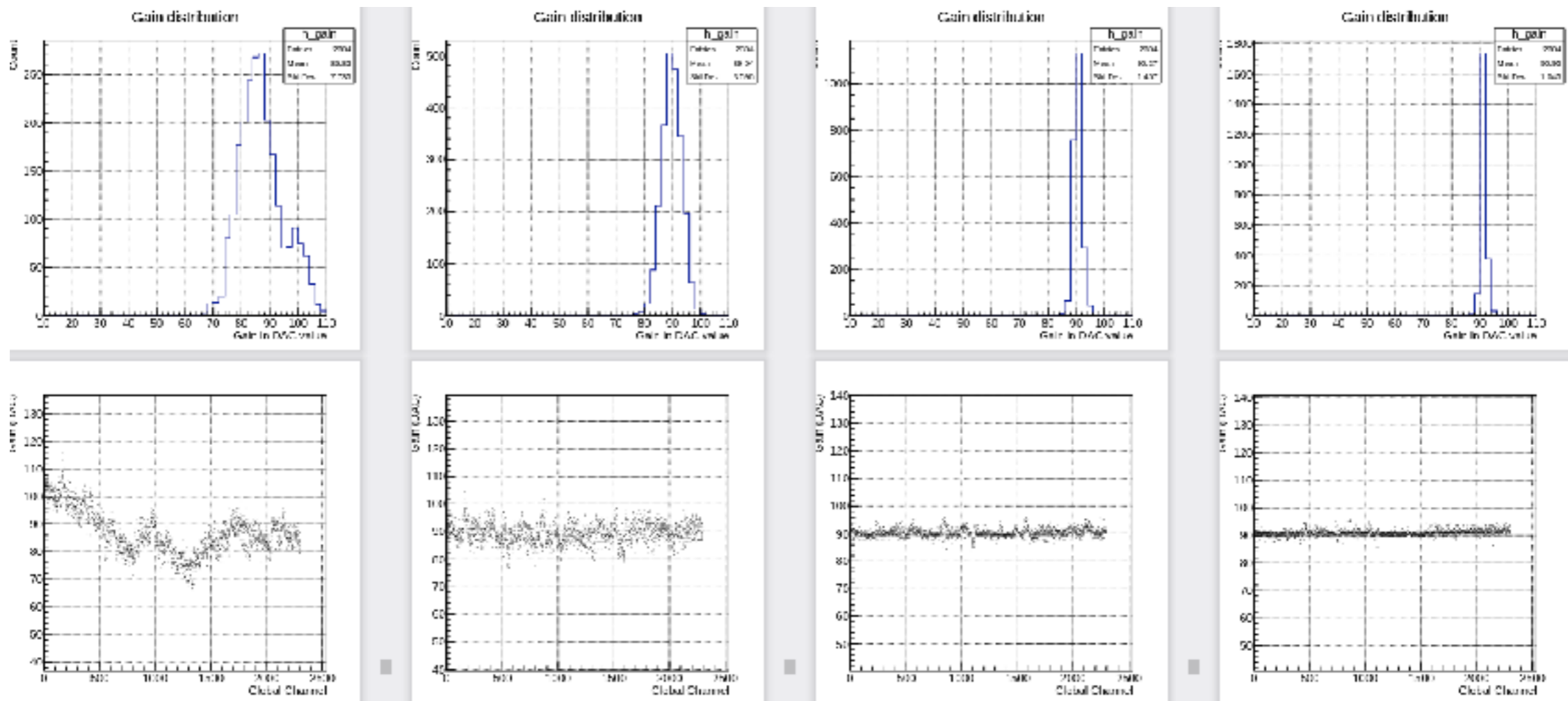


w/o DAQ

E.g. SiPM Gain Calib.

32ch (CITIROC) x 4 (on one FEE card) x 18

2304 ch.



initial status

Course bias adj. per ASIC (32ch)

Fine bias adj. per ch.

Fine bias adj. per ch. 2nd itr.

E.g. temperature monitor

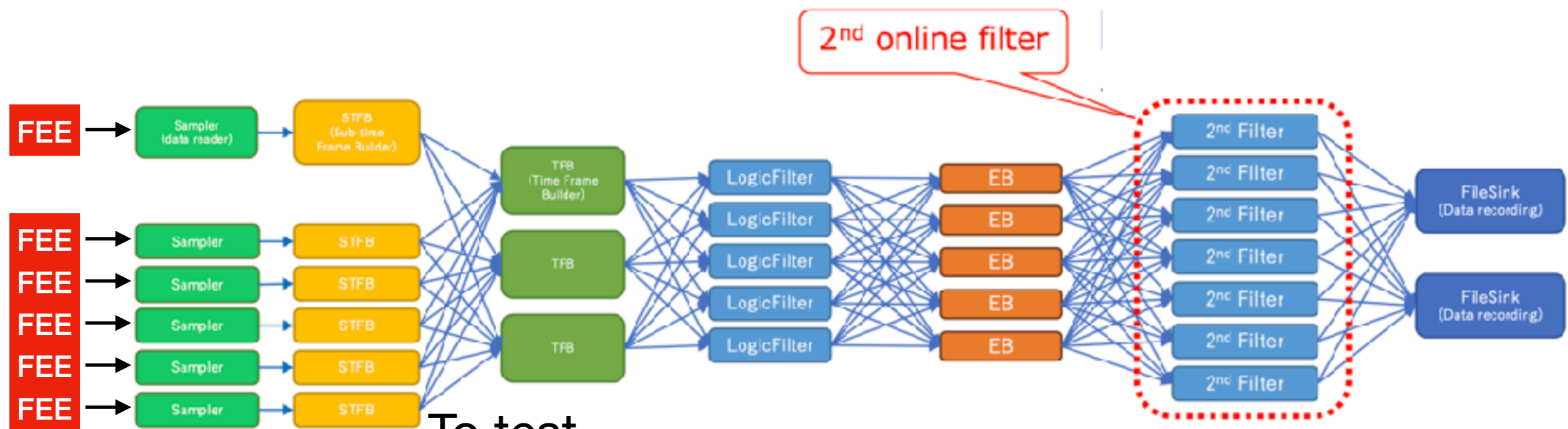


Test with the MARQ Spectrometer@J-PARC

Apr.-May 2024

- Full version @ π 20 beam line
 - 30 MHz 20 GeV/c π^- beam,
 - (7 MHz 6 GeV/c \bar{p} beam)
 - ~25k channel (future)
- Test @K1.8BR beam line
 - K^- beam (<1 MHz)
 - ~5k channel (now)
 - 4.2s spill, 2.0 extraction

Highest requirements among anticipated NestDAQ use cases



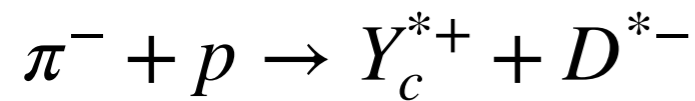
To test

- Improved clock/timing system
- Improved communication format
- higher-level online filtering

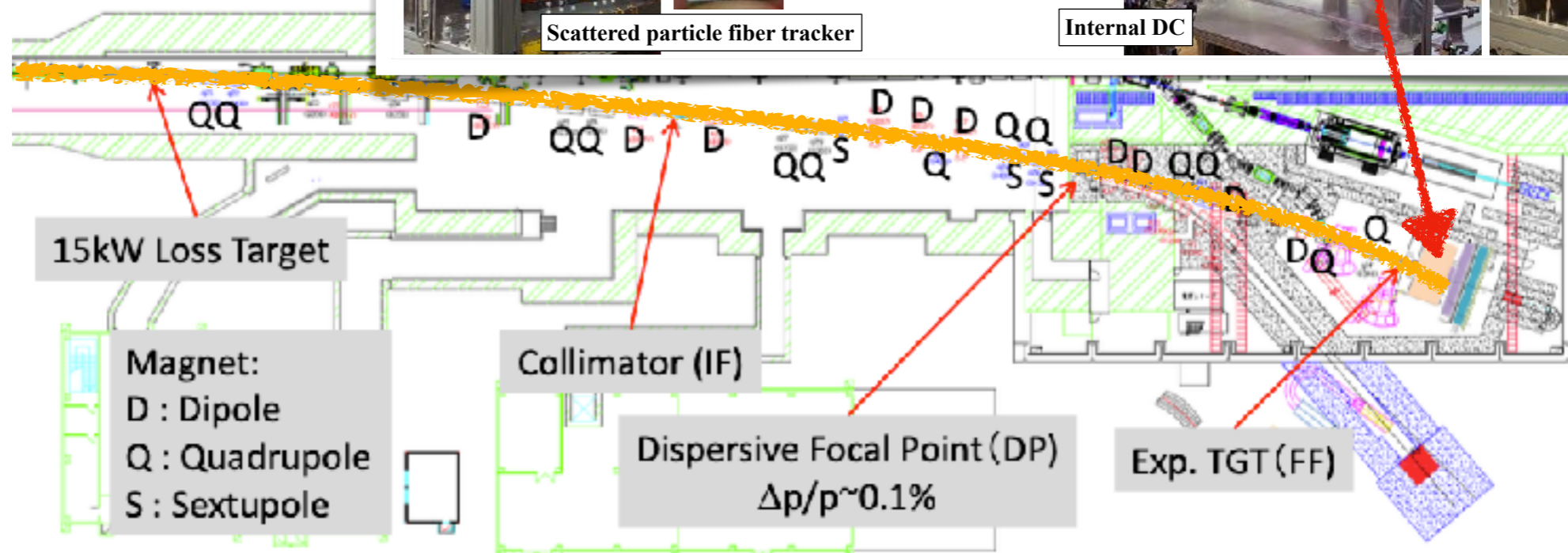
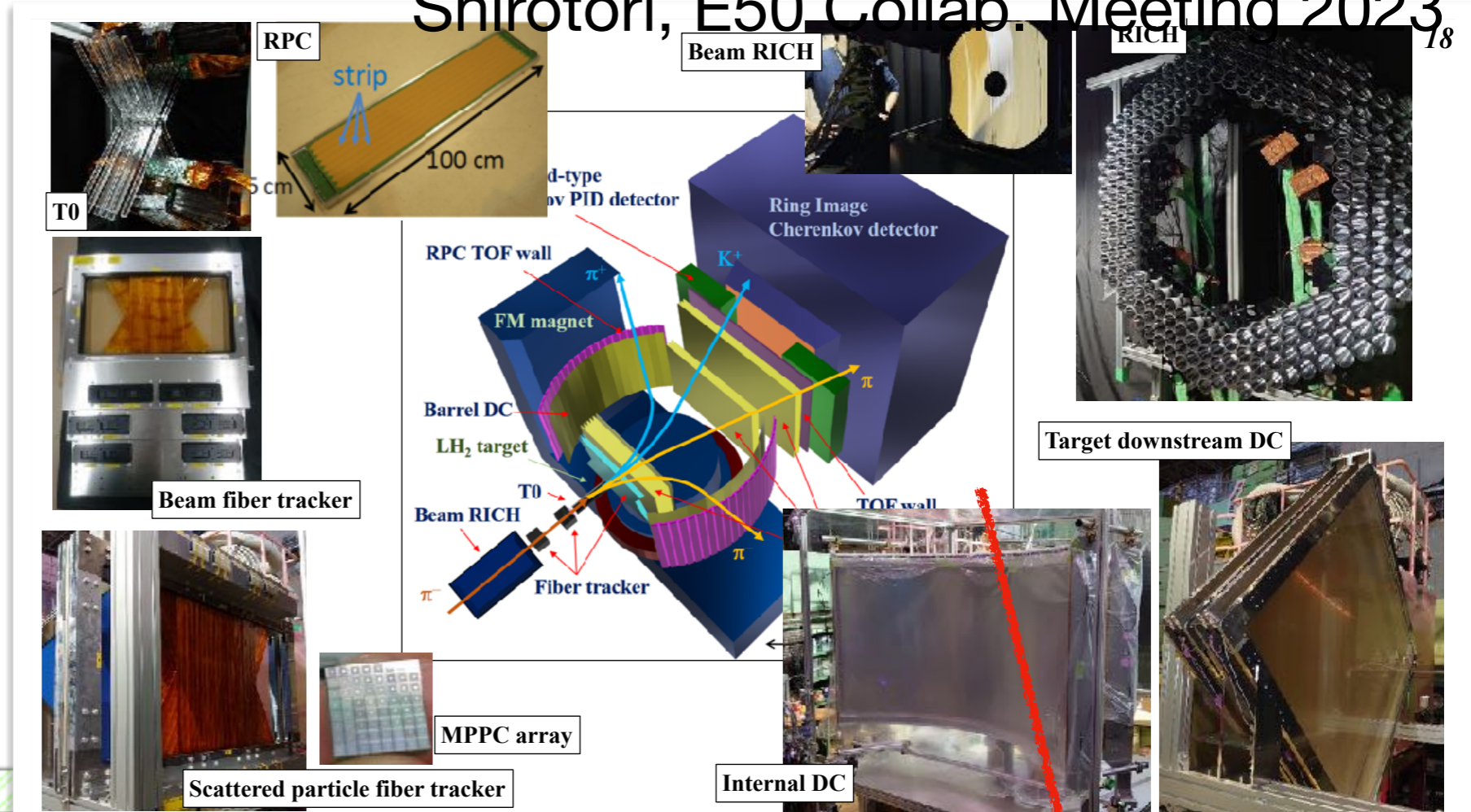
The MARQ Spectrometer in future

Shirotori, E50 Collab. Meeting 2023

MARQ-E50: charmed baryon spectroscopy, internal structure of charmed baryon, diquark correlations

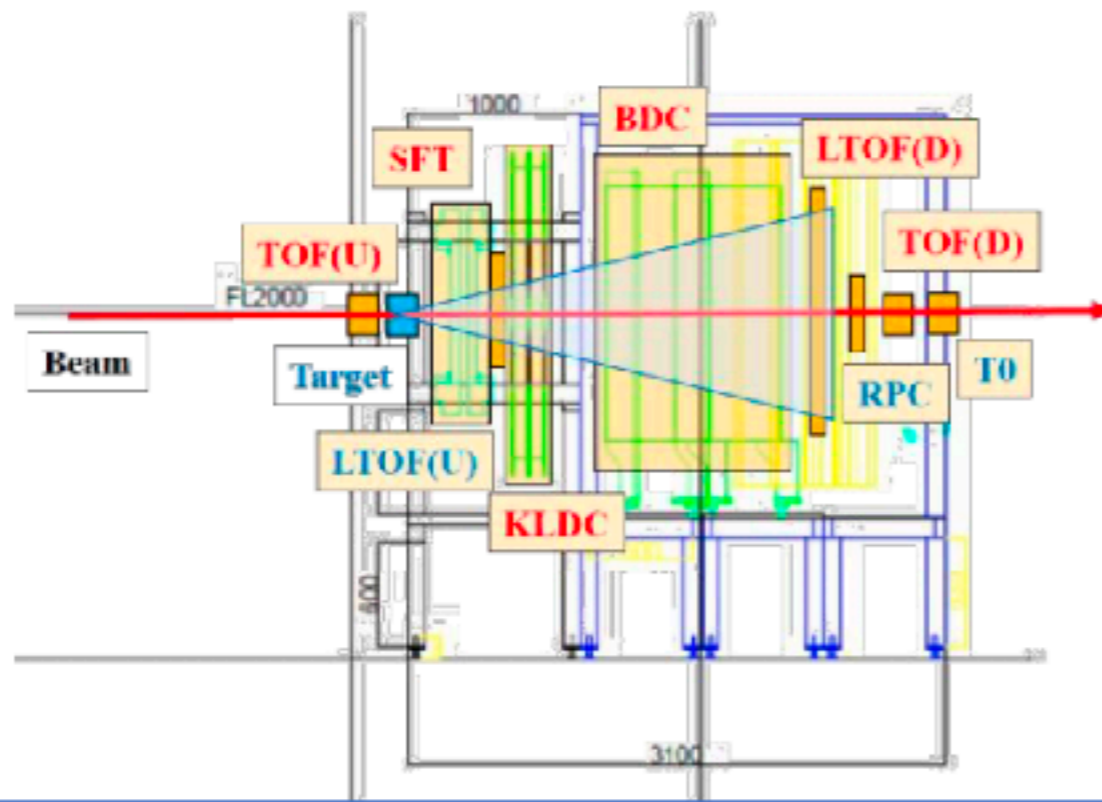


20 GeV/c π^- beam (30 MHz)



High momentum resolution $\Delta p/p \sim 0.1\%$ with dispersion analysis

Test assembly for the 2024Apr BT



| Detector | Front-end electronics | Number of modules | Number of channels |
|---------------|------------------------------|-------------------|--------------------|
| | Clock/time system (MIKUMARI) | 4 | 128 |
| TOF | FPGA HR-TDC (AMANEQ) | 2 | 128 |
| Drift chamber | FPGA TDC (AMANEQ) | 15 | 1920 |
| Fiber tracker | MPPC readout FEE (CIRASAME) | 18 | 2304 |

Key Components

Front-End-Electronics (FEE)

* Total detector channel ~25,000 ch

⇒ **Streaming DAQ: Only timing data (TDC)**

- FEE: 1G/10Gbps network (Optical link)
- Timing synchronization (MIKUMARI)

• MPPC detector: ~20,000 ch

- Scintillating fiber trackers
- RICH, Beam-RICH, Vth AC

⇒ **CIRASAME (ASIC: CITIROC)**

- 128 ch Low-resolution TDC ($\Delta T_{LSB} \sim 1$ ns)

• Timing detector: ~1,000 ch

- T0, RPC, TOF: Amp/PMT + Discriminator

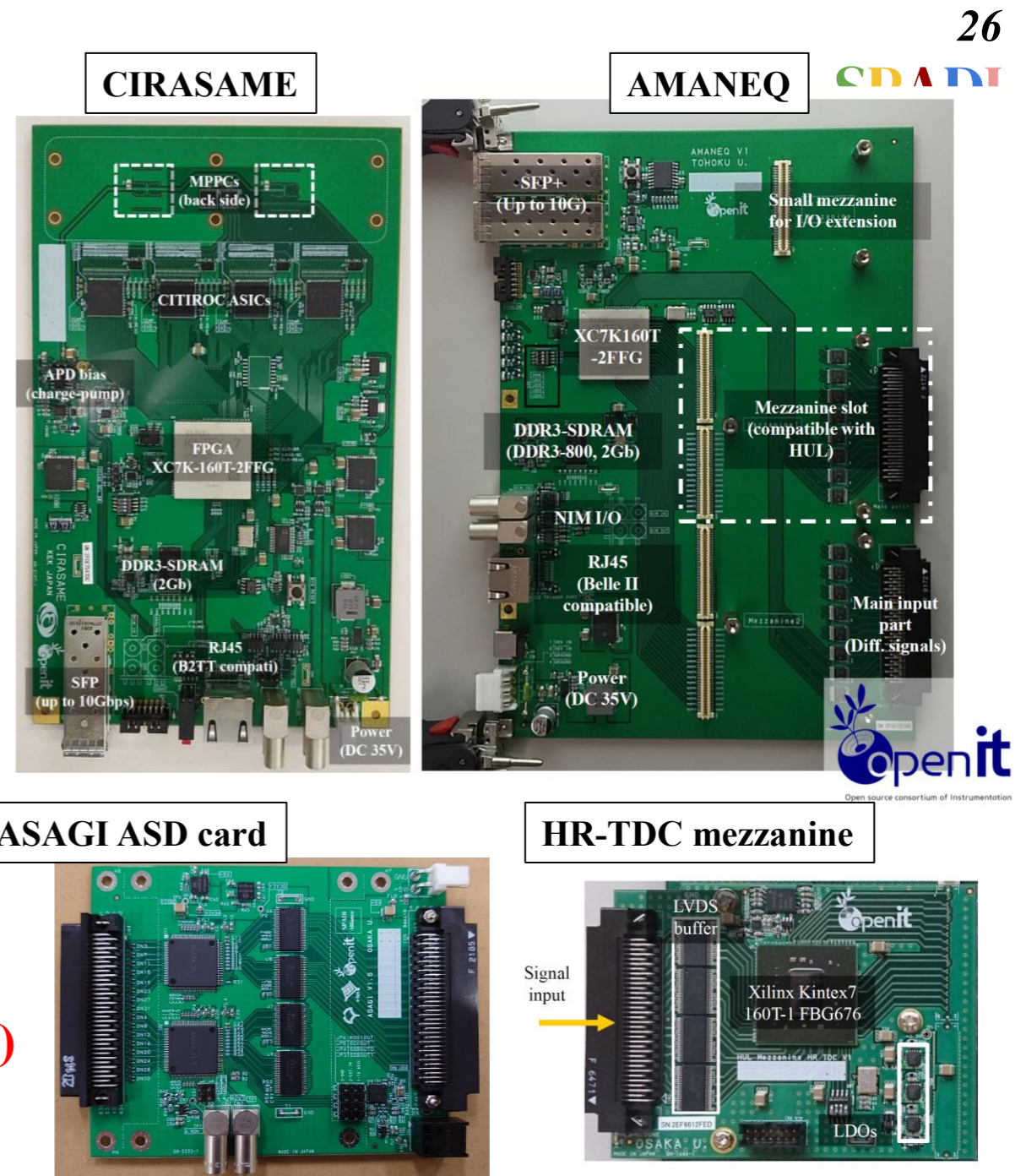
⇒ **AMANEQ (HR-TDC mezzanine)**

- 64 ch High-resolution TDC ($\Delta T_{LSB} \sim 20$ ps)

• Drift chamber: ~4,000 ch

⇒ **ASAGI(ASD) card + AMANEQ (DC mezzanine)**

- ASD card 32 ch → TDC 128 ch
- Low-resolution TDC ($\Delta T_{LSB} \sim 1$ ns)



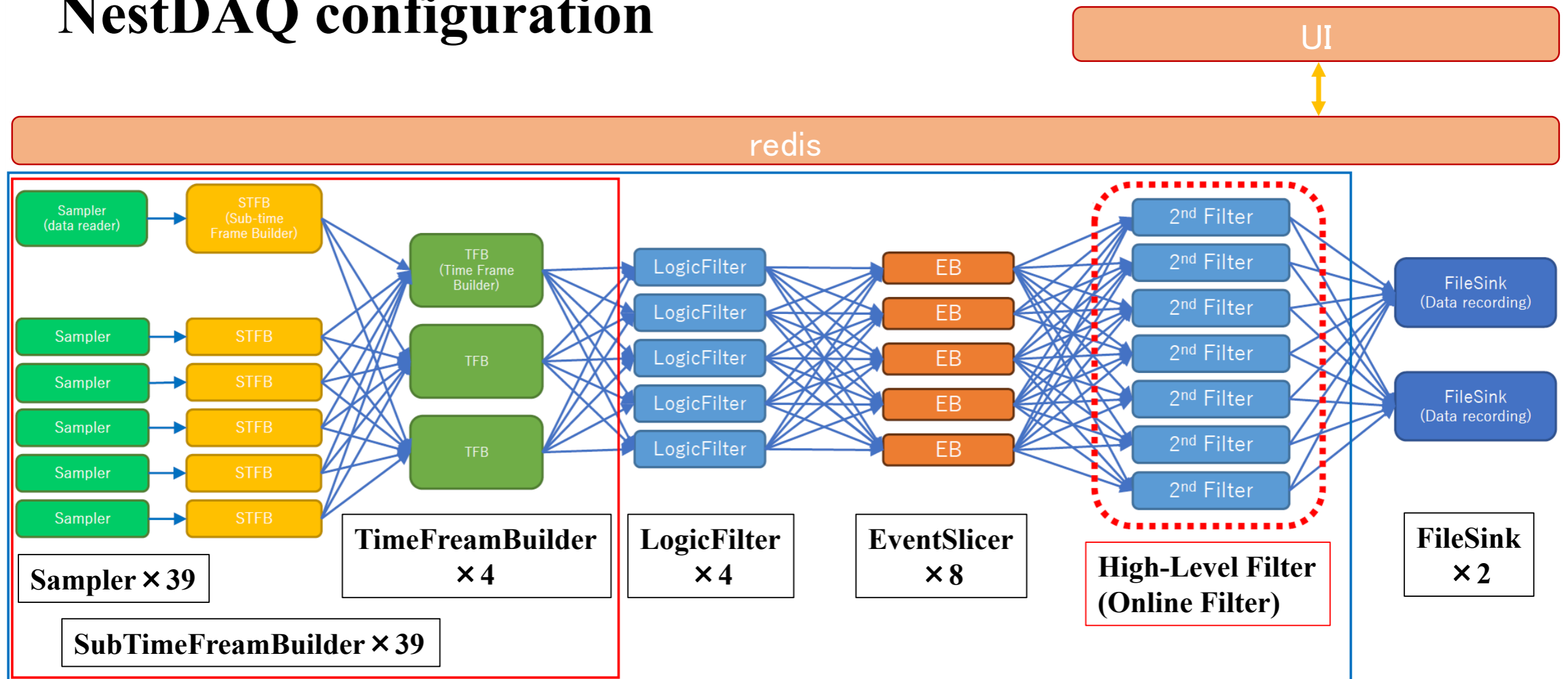
Other key components

- ? RAYRAW
- TPC readout w/ SAMPA chip (SAMIDARE)
- No-delay-cable QDC
 - Slow ADC -> TDC
 - LPF and slow WF digitiser
- WF digitiser

DAQ

NestDAQ configuration

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- **No Filter:** Sampler → STFB → TFB → FileSink
- **Filtered:** TFB → LogicFilter → EventSlicer → High-level Filter → FileSink

Ultimately we want 1/1000 data reduction

General HPC nodes

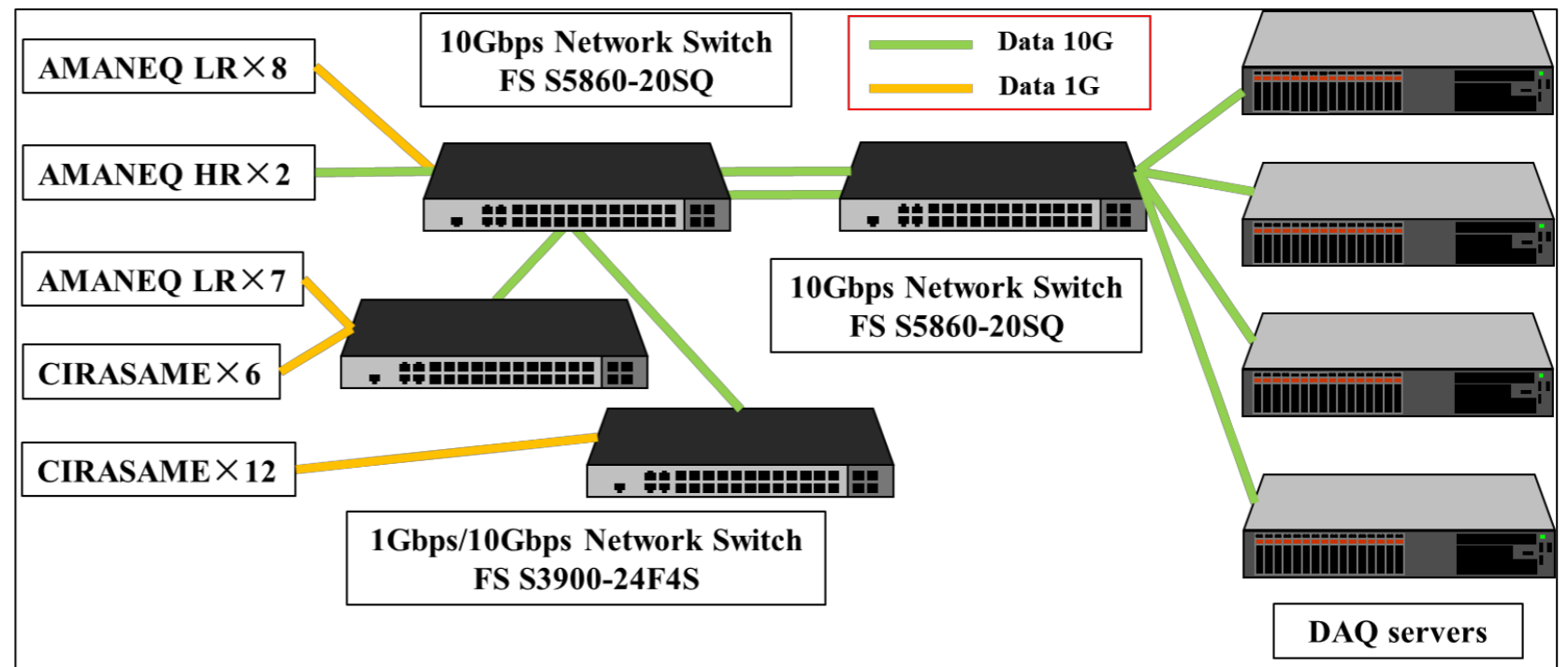
Multiple PC study: DAQ Server performance

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From Y. Igarashi

• DAQ PCs

- 1. e50server03 (192.168.2.51)**
 - AMD EPYC 74F3 24-Core Processor
 - 64 GB Memory
- 2. eyst-daq01 (192.168.2.54)**
 - AMD EPYC 7313P 16-Core Processor
 - 64 GB Memory
 - Intel 82599ES 10-Gigabit SFI/SFP+ Network Connection (rev 01)
- 3. e50server01 (192.168.2.55)**
 - Intel(R) Xeon(R) CPU E5-2630 v4 @ 2.20GHz
 - 20-Core
 - 24 GB Memory
- 4. e50server05 (192.168.2.53)**
 - Intel(R) Xeon(R) CPU E5-2640 v4 @ 2.40GHz
 - 10-Core
 - 32 GB Memory
- 5. nlabdaq5 (192.168.2.20)**
 - AMD Ryzen 9 3900XT 12-Core Processor
 - 16 GB Memory



DAQ Server performance (Passmark bench CPU)

DAQ PCs

- e50server03 (192.168.2.51)
 - AMD EPYC 74F3 24-Core Processor
 - 64 GB Memory
- eyst_daq01 (192.168.2.54)
 - AMD EPYC 7313P 16-Core Processor
 - 64 GB Memory
 - Intel Corporation 82599ES 10-Gigabit SFI/SFP+ Network Connection (rev 01)
- e50server01 (192.168.2.55)
 - Intel(R) Xeon(R) CPU E5-2630 v4 @ 2.20GHz
 - 20-Core
 - 24 GB Memory
- e50server05 (192.168.2.53)
 - Intel(R) Xeon(R) CPU E5-2640 v4 @ 2.40GHz
 - 10-Core
 - 32 GB Memory
- nlabdaq5 (192.168.2.20)
 - AMD Ryzen 9 3900XT 12-Core Processor
 - 16 GB Memory

| | AMD Ryzen 9 3900XT | AMD EPYC 74F3 | AMD EPYC 7313P | Intel Xeon E5-2630 v4 @ 2.20GHz | Intel Xeon E5-2640 v4 @ 2.40GHz |
|---------------------|--------------------------------|---------------------------------|-----------------------------------|--|--|
| Price | \$379 - BUY | \$2585.04 - BUY | \$1204.21 - BUY | \$14.99 - BUY | \$174.9 - BUY |
| Socket Type | AM4 | SP3 | SP3 | FCLGA2011-3 | FCLGA2011-3 |
| CPU Class | Desktop | Server | Server | Server | Server |
| Clockspeed | 3.8 GHz | 3.2 GHz | 3.0 GHz | 2.2 GHz | 2.4 GHz |
| Turbo Speed | Up to 4.7 GHz | Up to 4.0 GHz | Up to 3.7 GHz | Up to 3.1 GHz | Up to 3.4 GHz |
| # of Physical Cores | 12 (Threads: 24) | 24 (Threads: 48) | 16 (Threads: 32) | 10 (Threads: 20) | 10 (Threads: 20) |
| Cache | L1: 768KB, L2: 6.0MB, L3: 64MB | L1: 384KB, L2: 3.0MB, L3: 32MB | L1: 1,024KB, L2: 8.0MB, L3: 128MB | L1: 640KB, L2: 2.5MB, L3: 25MB | L1: 640KB, L2: 2.5MB, L3: 25MB |
| TDP | 105W | 240W | 155W | 85W | 90W |

CPU Mark Rating

As of 1st of June 2024 - Higher results represent better performance

| | | |
|---------------------------------|--|--------|
| AMD Ryzen 9 3900XT | | 32,727 |
| AMD EPYC 74F3 | | 60,666 |
| AMD EPYC 7313P | | 42,032 |
| Intel Xeon E5-2630 v4 @ 2.20GHz | | 11,663 |
| Intel Xeon E5-2640 v4 @ 2.40GHz | | 12,374 |
| PassMark Software © 2008-2024 | | |

CPU Single Thread Rating

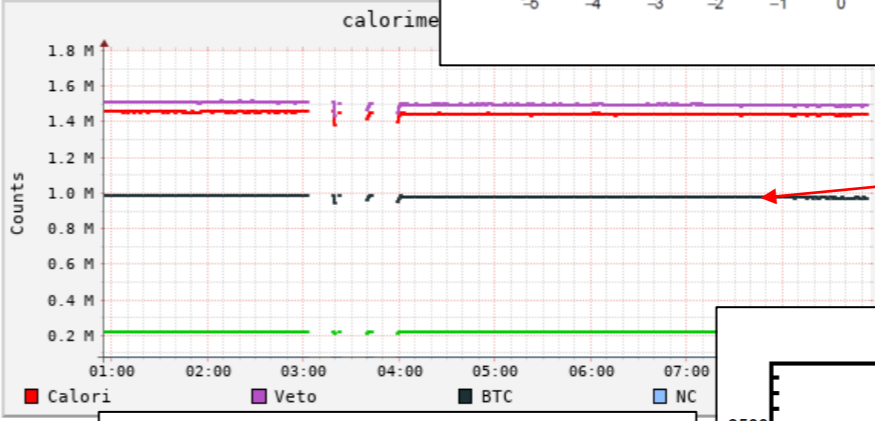
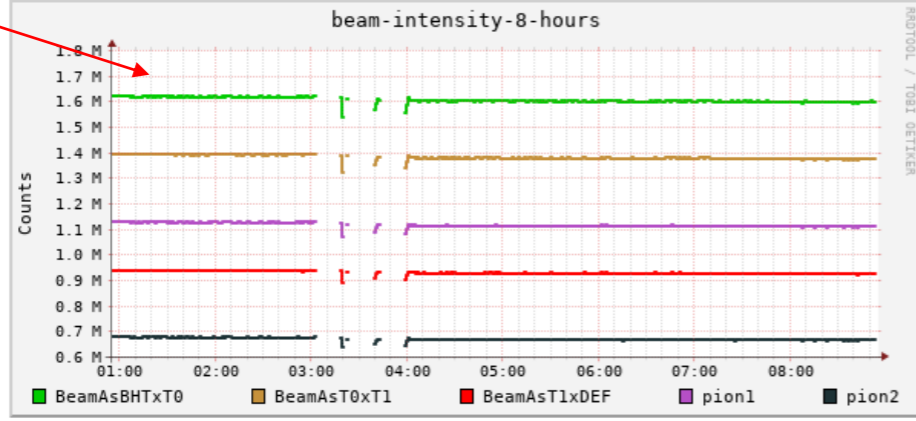
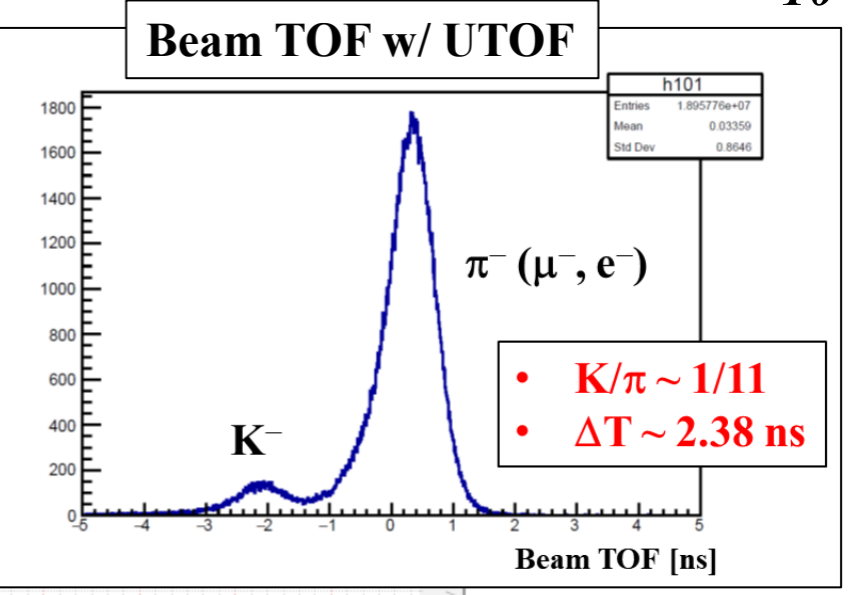
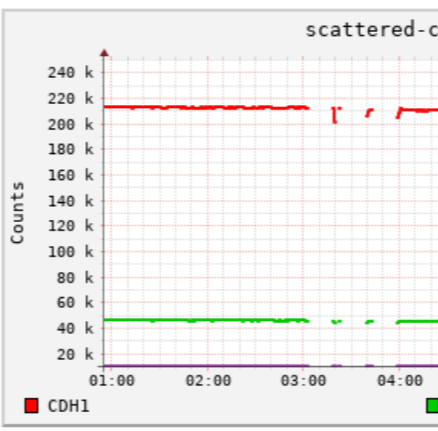
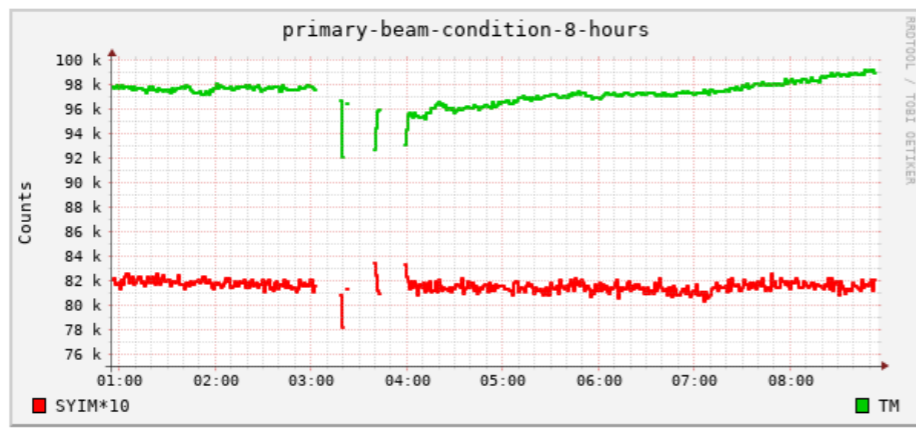
As of 1st of June 2024 - Higher results represent better performance

| | | |
|---------------------------------|--|-------|
| AMD Ryzen 9 3900XT | | 2,749 |
| AMD EPYC 74F3 | | 2,942 |
| AMD EPYC 7313P | | 2,704 |
| Intel Xeon E5-2630 v4 @ 2.20GHz | | 1,744 |
| Intel Xeon E5-2640 v4 @ 2.40GHz | | 1,932 |
| PassMark Software © 2008-2024 | | |

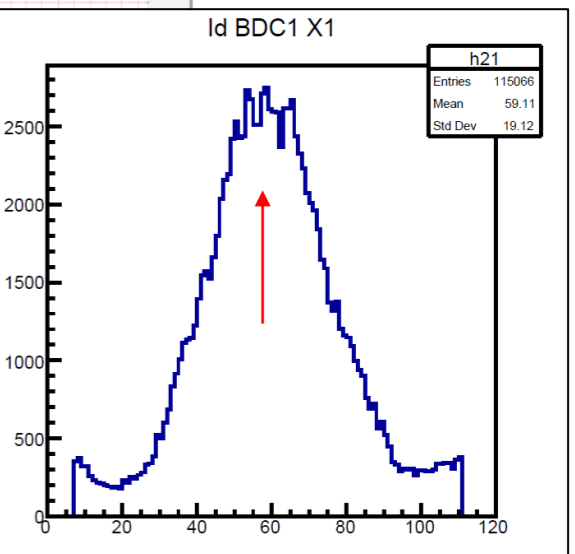
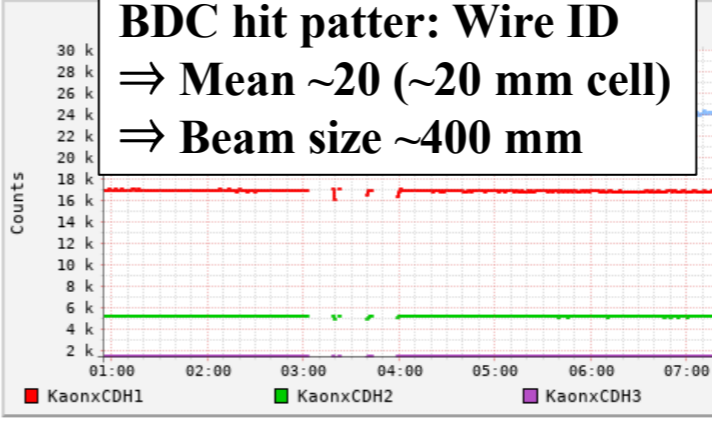
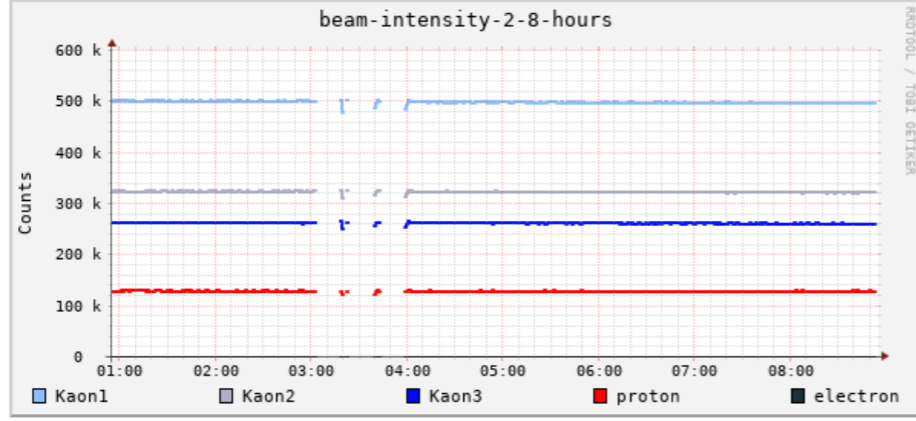
Beam

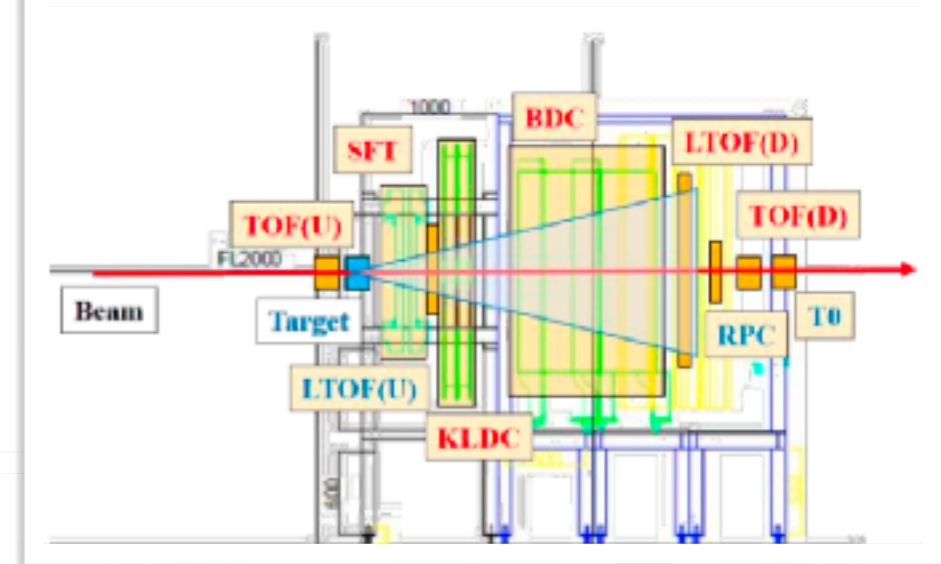
Beam flux: K1.8BR scaler information

All charged
~1.6 M/spill



Counting rate
After calorimeter
~1.0 M/spill





NestDAQ process implementation

- **TFB: Reconstruction of time frame from HBF**
 - Free streaming data (w/o reduction by any selections)
 - All 1-M/spill data can be taken.

⇒ **LogicFilter**: Timing coincidence

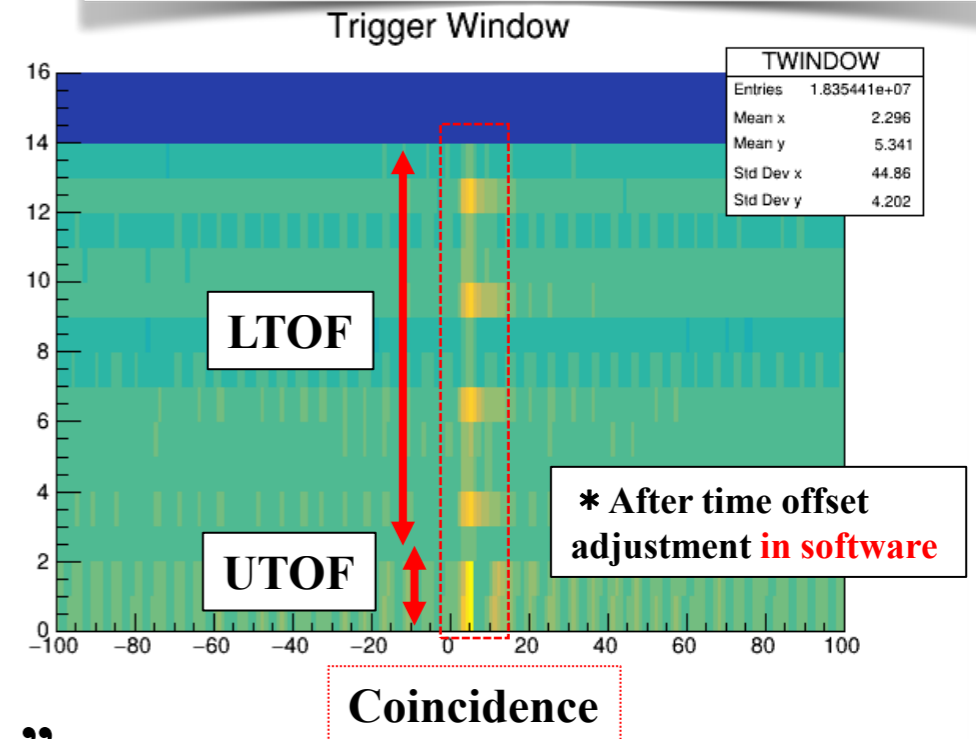
- “Trigger timing” generated w/o reduction
 - UTOF × LTOF timing
 - Coincidence rate: ~200 k/spill (Reduced by detector size)

⇒ **EventSlicer**: Event finding from “Trigger timing”

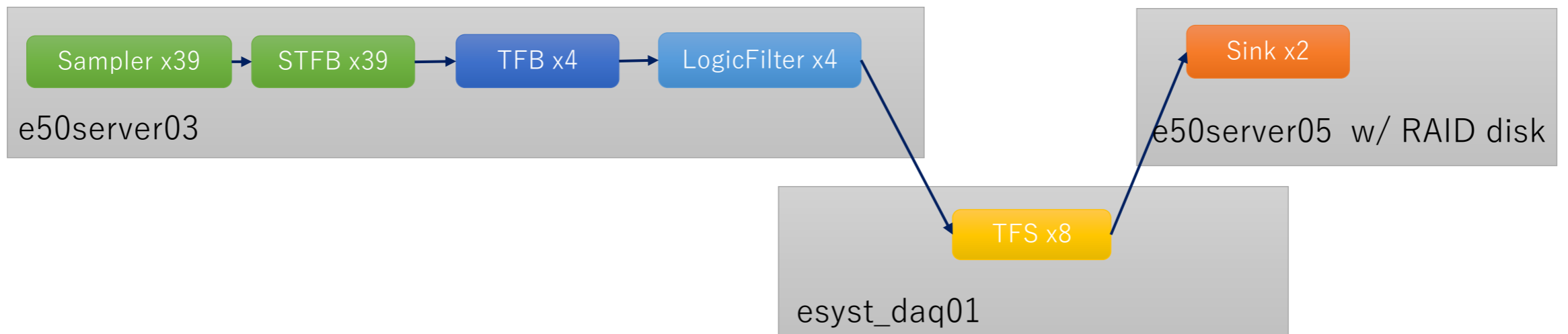
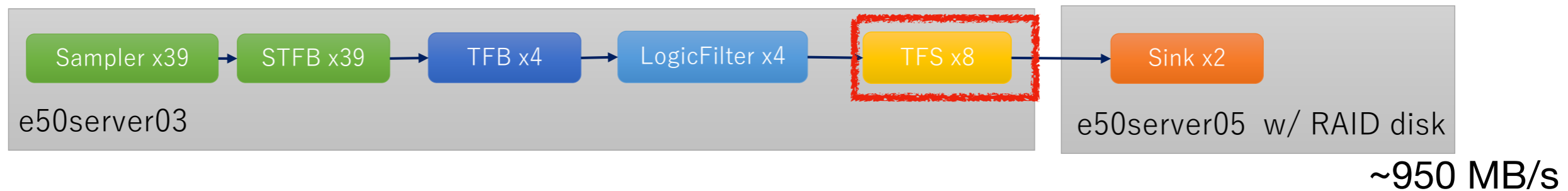
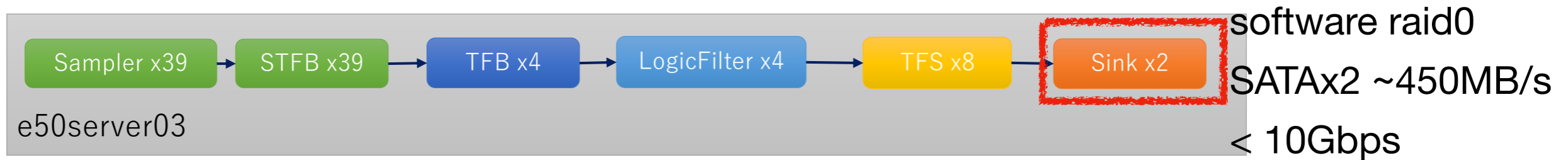
- Slicing window applied according to “Trigger timing”: ± 1000 ns
 - “Trigger timing” is used as reference timing.
- Timing group in Slicing window = “Event” generated w/ reduction

⇒ **High-level Filter**: Event selection using “Event”

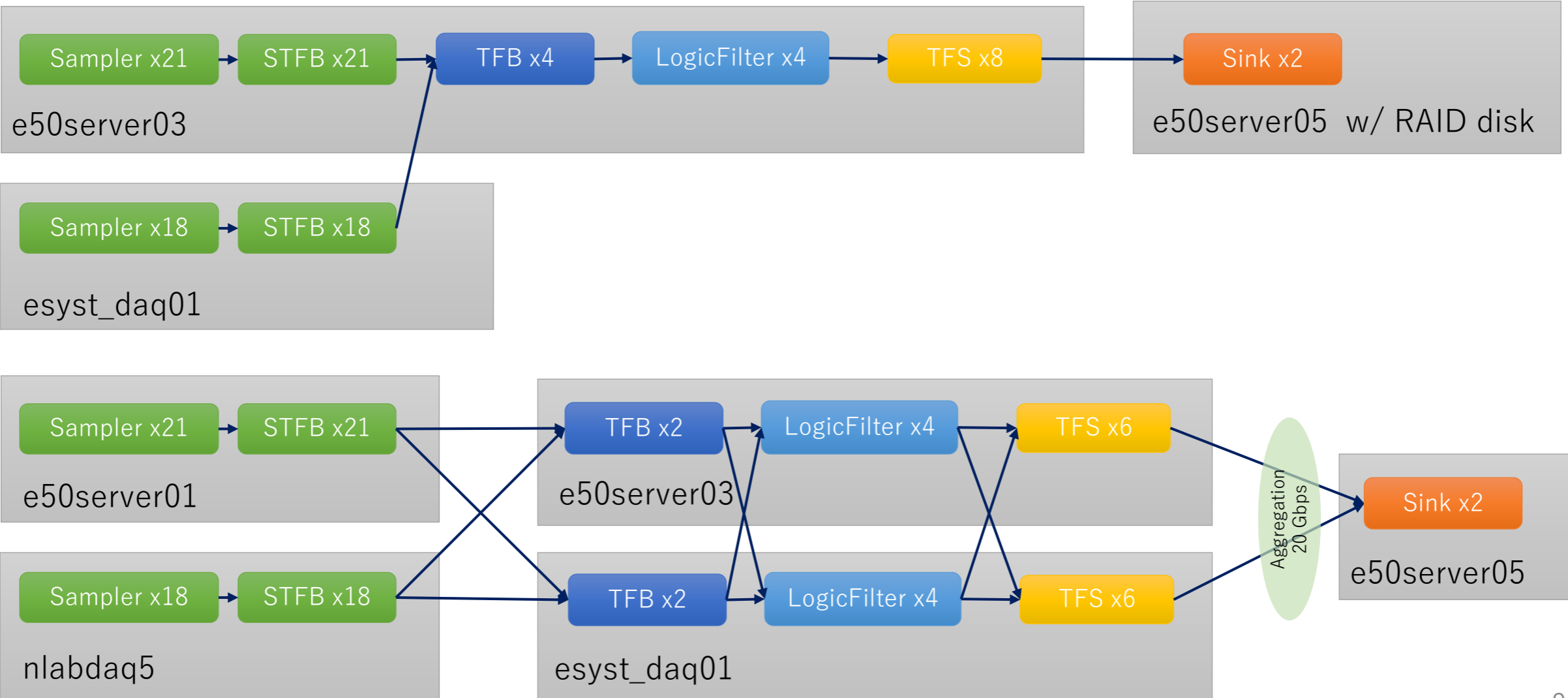
- Event selection like an off-line analysis can be performed.
 - Beam TOF filter: K beam selection using $(T_{T1:MeamTime} - T_{UTOF:MeamTime})$



Data flow with multiple computers



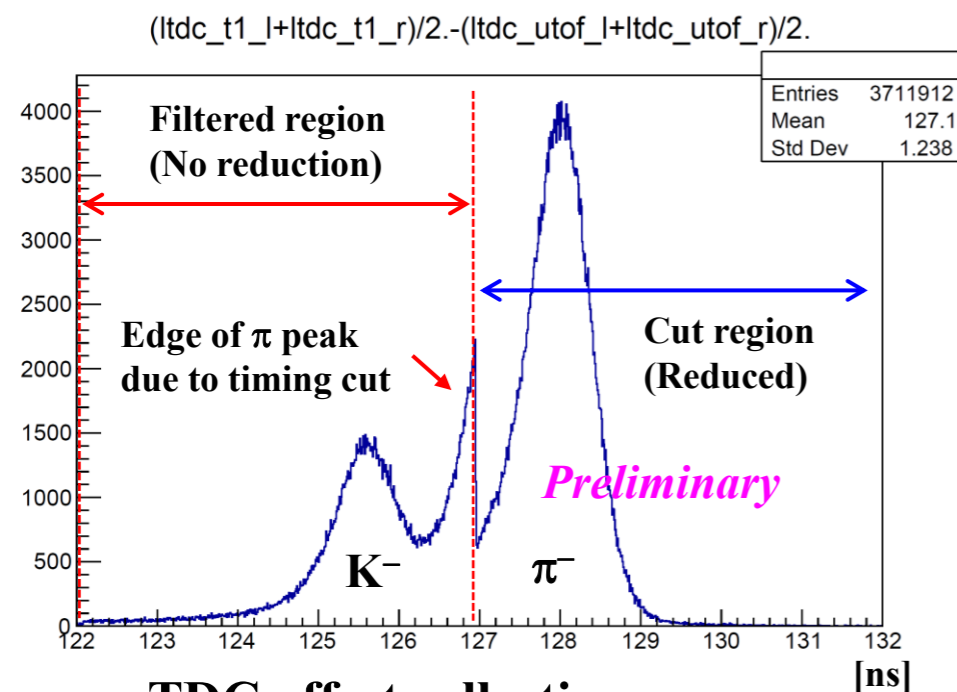
Data flow with multiple computers



High-level Filter status \Rightarrow To be reported by Furukawa-kun

- **Beam TOF filter: K beam selection using $(T_{T1:MeamTime} - T_{UTOF:MeamTime})$**
 - All timing combinations in “Event” (Timing in Slicing window) are used.
- **Correct Beam TOF selection \Rightarrow High-level filter worked well !**

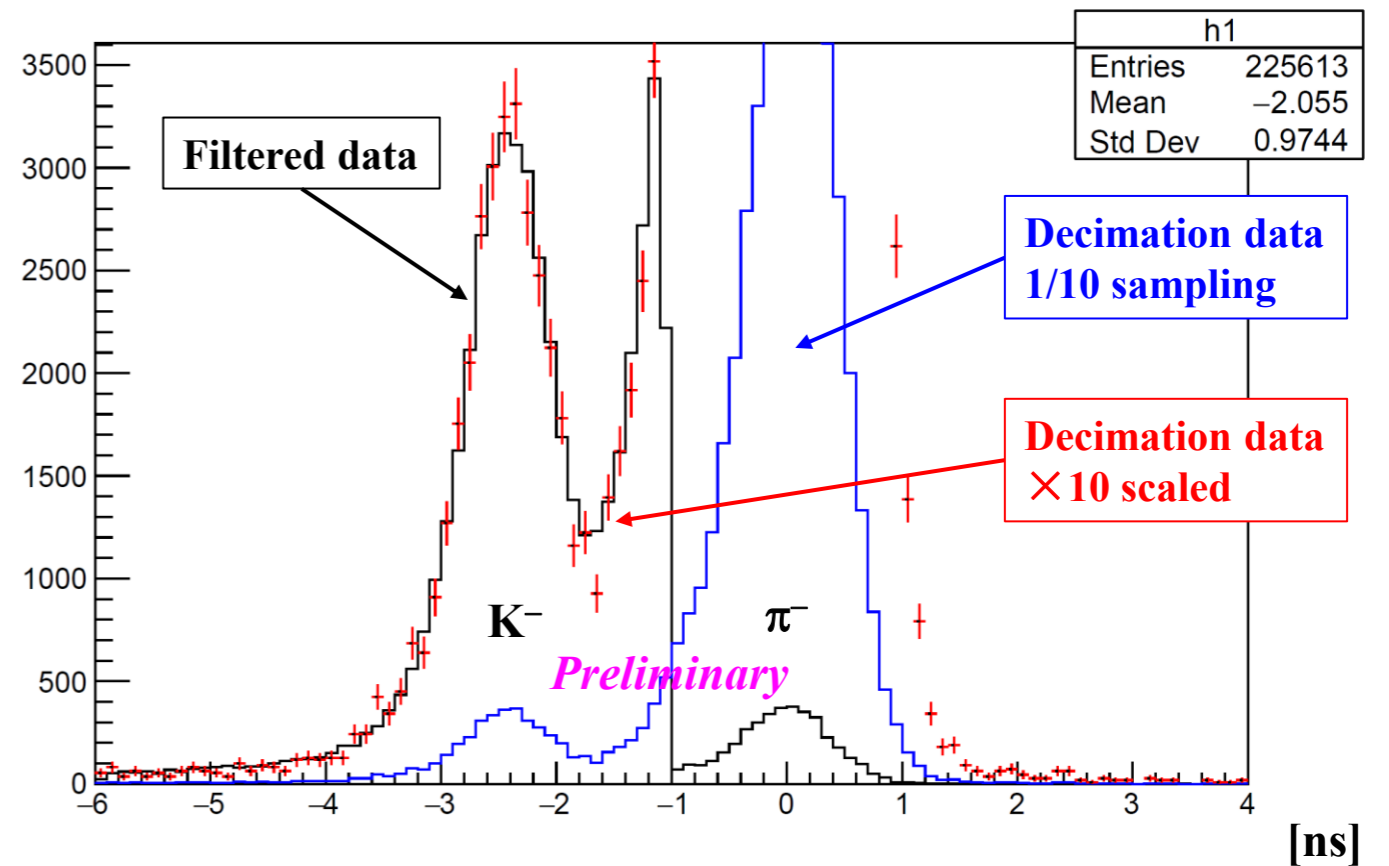
“Raw” data: $T_{T1:MeamTime} - T_{UTOF:MeamTime}$



- TDC offset collection
- TDC timing cut
- 1st hit selection



Beam TOF: $T_{T1:MeamTime} - T_{UTOF:MeamTime}$



Summary

- NestDAQ under active development by the SPADI alliance
- Just had a test BT with MARQ spectrometer (with the highest demands)
 - Gained a lot of experiences to run a continuous readout in practice
 - Flexible and scalable system
 - low/high level online filtering
- Next steps:
 - higher-level filtering, GPU, full system (x5), storage (CephFS/SSD caching)