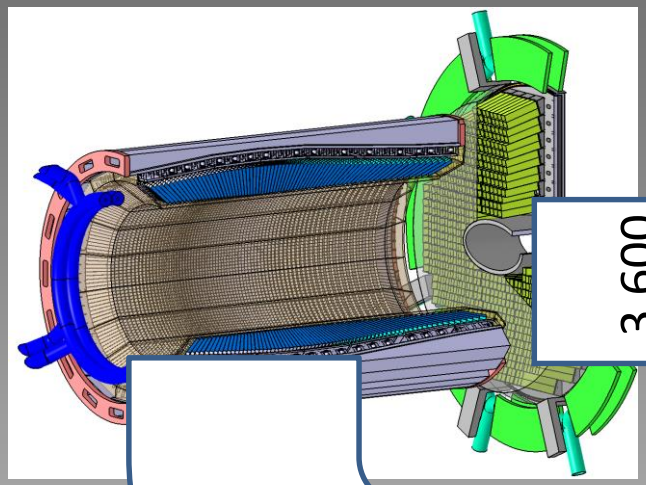
PANDA EMC DAQ modules

PANDA EMC DAQ



3,600

11,952

Photosensor VPTT

Preamplifier Basel

Photosensor APD

Preamplifier APFEL + HDA

14400

???

Uppsala University's commitment

217 ADC 64-ch

??? LVDS_DC

217/(73)

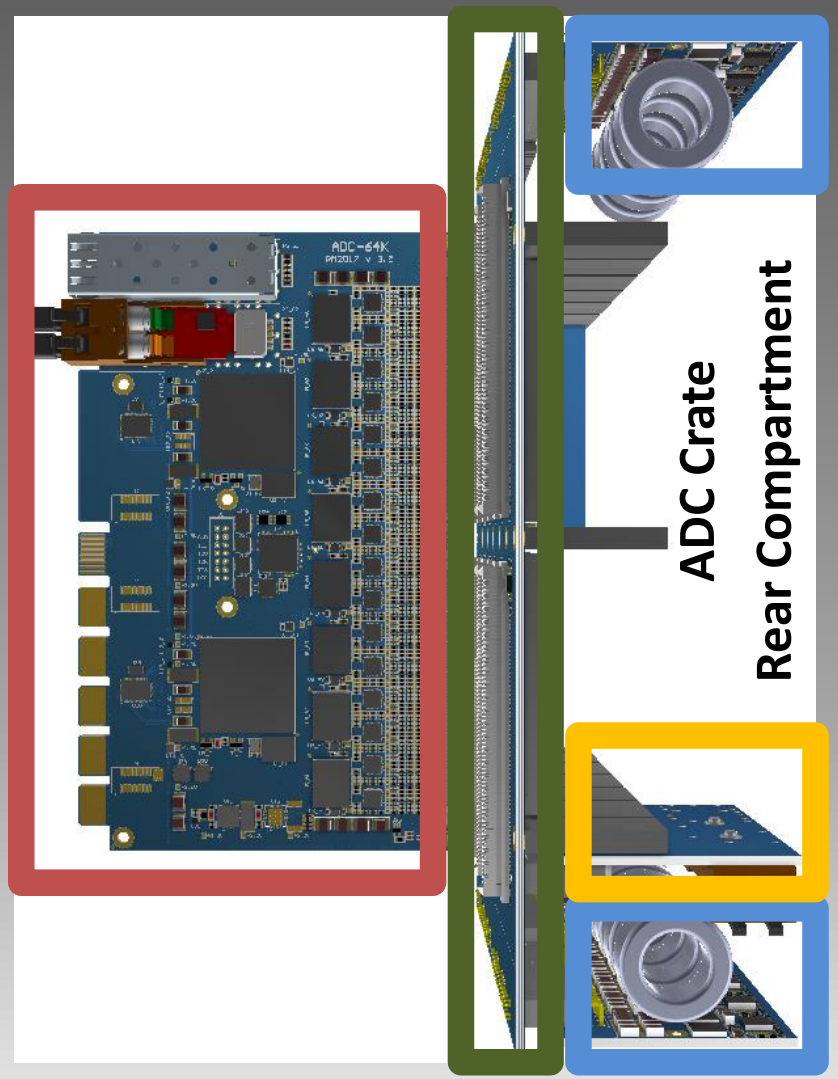
???

4/(2) + ? Data Concentrator, 60-ch

?

Compute Node

ADC system status



- **ADC – 250 + 20**

  > 235 fully working, 15 need attention, 20 not tested

- **Backplanes – 14 x 15-slot**

  12 x 6-slot

  All produced, briefly tested, need thorough test in the system

- **Power supplies 100 x 4-voltages**

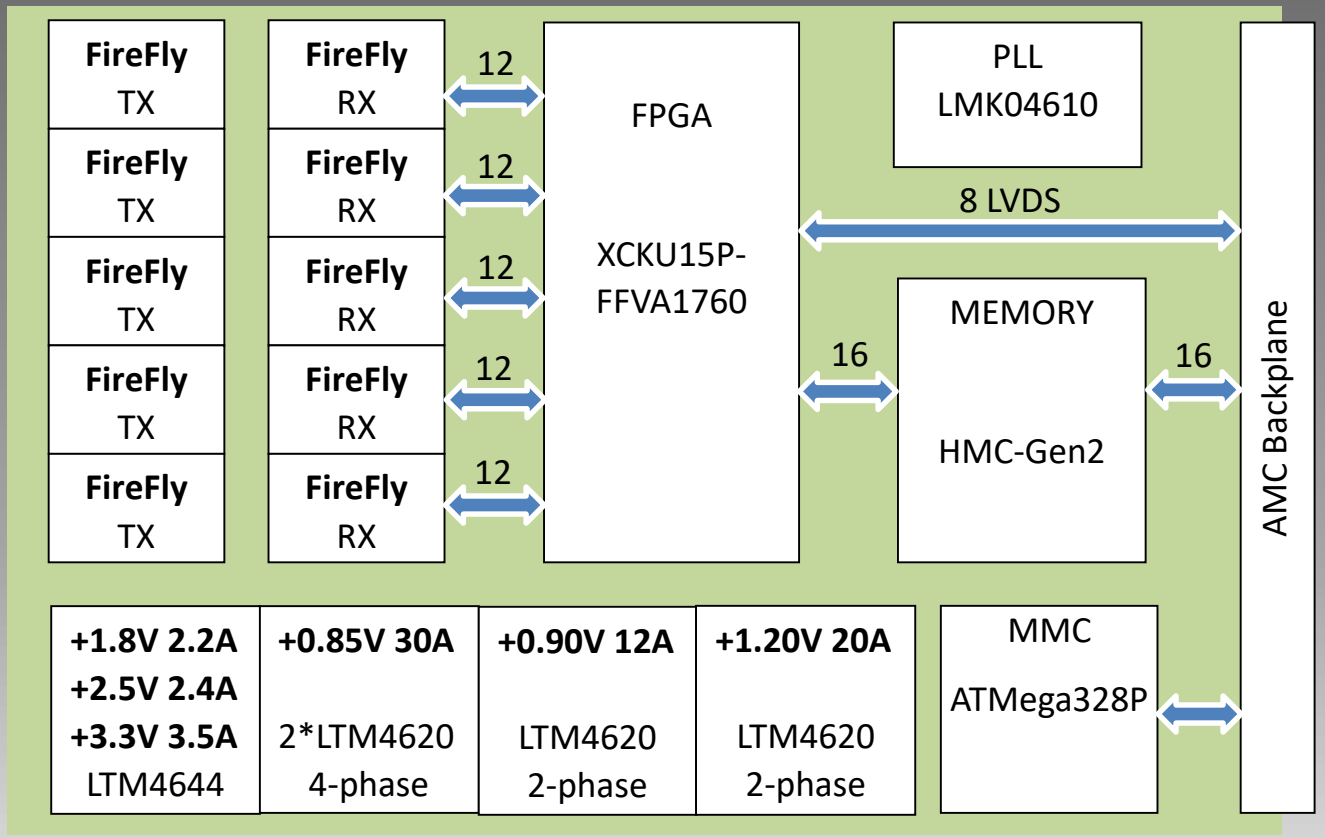
  All PCB produced and assembled, > 60 fully working, the rest needs mechanical assembly and testing

- **Crate contoller**

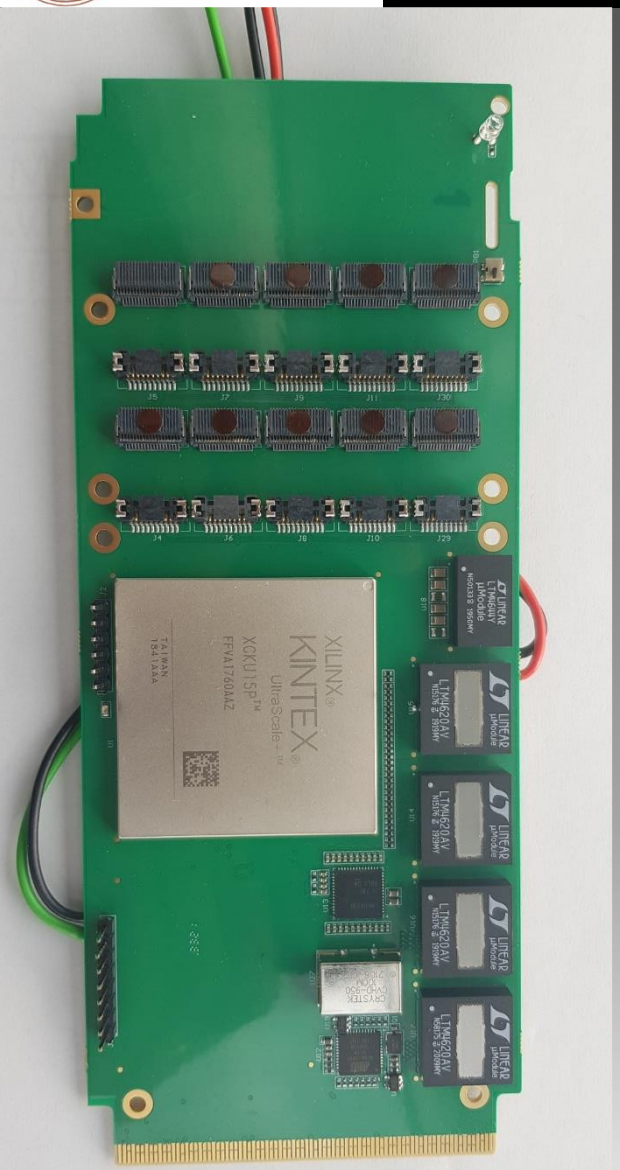
  All components procured, 1 module built, needs tests

PANDA_DC prototyping

PANDA_DC



PANDA_DC prototyping



First two prototypes using **Megtron 6** (undisclosed manufacturer in China)

- Power supply check – one device failed, one OK. The failure attributed to a broken connection on the PCB.

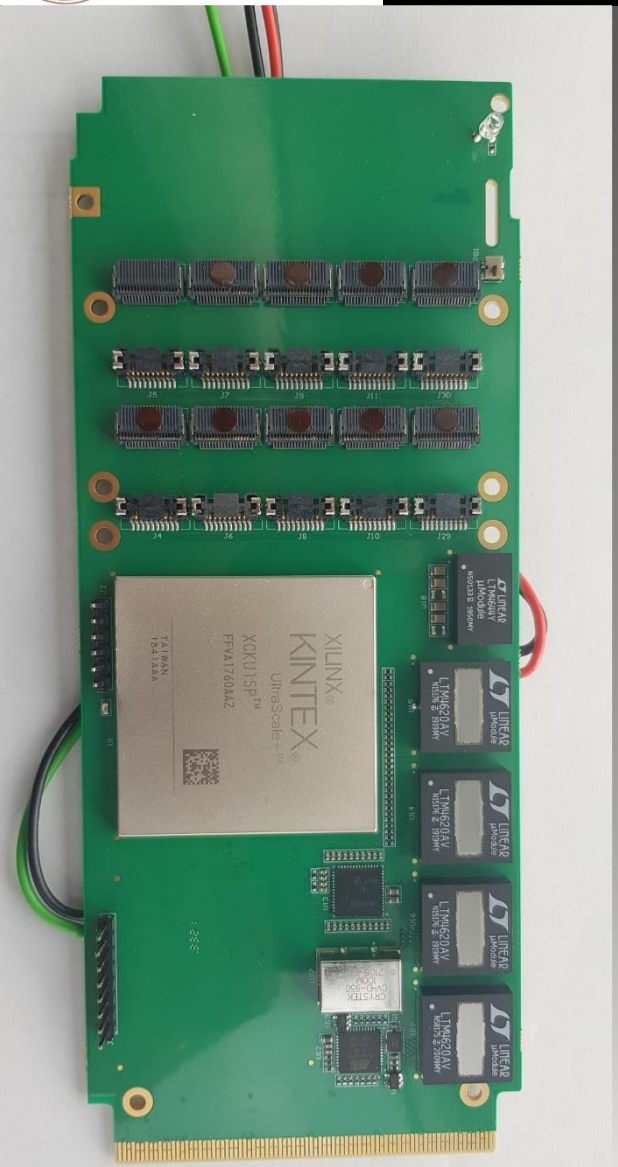
Second two prototypes using **Megtron 7** (undisclosed manufacturer in China)

- One with failing PS, probably for disassembly. The second - some clock inputs were broken (most probably ESD from oscilloscope probe while developping PLL control). This board is **still used** for the DAQ development in Krakow

Third attempt using **Isola** (HLT). 4 PCB out of 10 passed QC

- One board failed in unexplained circumstances. Failure attibuted to ESD or a mechanical stress while handling.
- The second board has no reported failures. **It's used** for firmware evaluation.
- The third board failed when PS didn't start correctly – again a lack of connection either on the PCB or between a pad and a pin

PANDA_DC prototyping

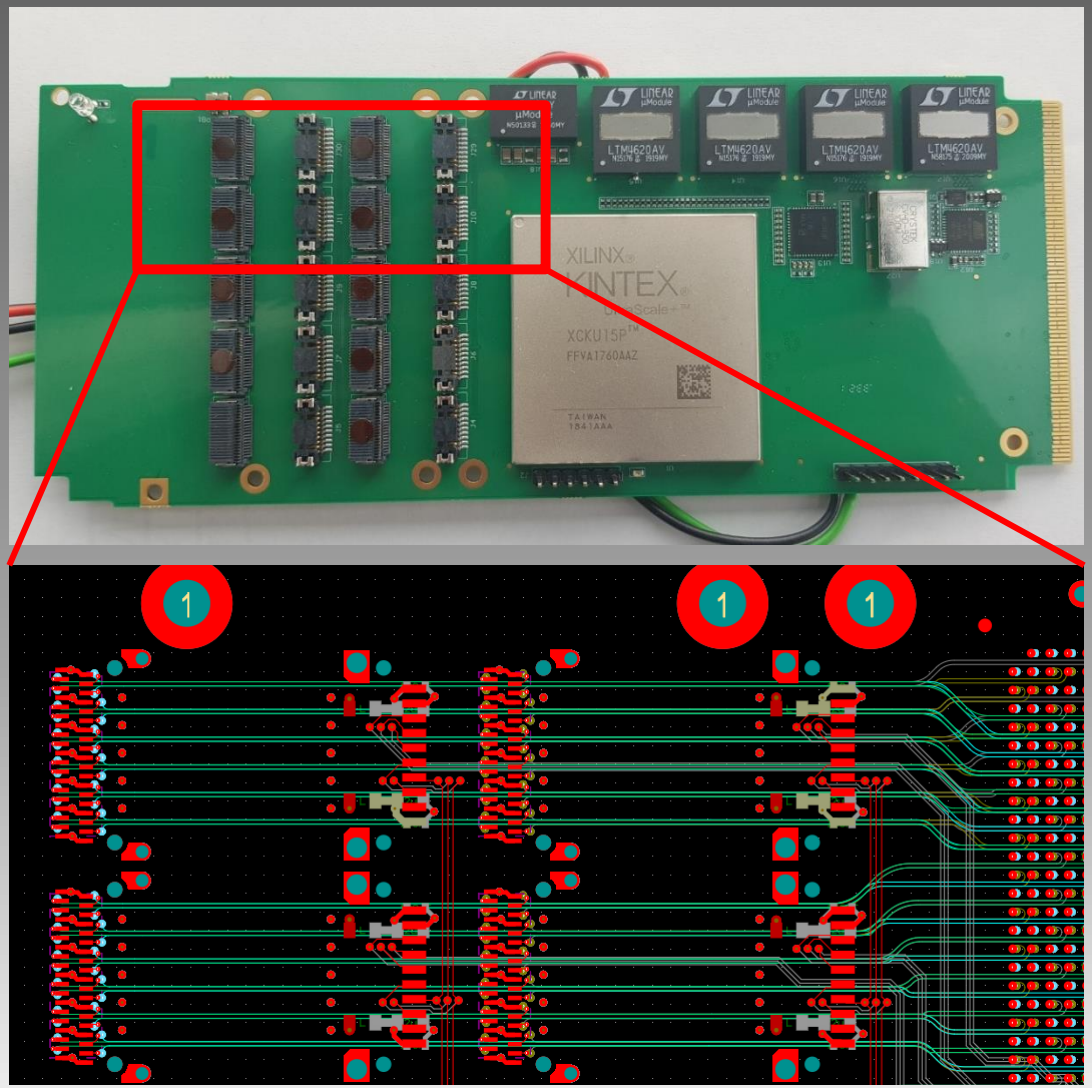


- Manufacturers clearily have problems with this design
- The design was scrutinized and remarks and suggestions from the ICAPE were implemented. This should allow for a more reliable product.
- The focus was made on increasing annular rings for TH vias to 0.5 mm. This resulted in a substantial re-routing of the design.
- Devices extremely sensitive to ESD. Need to be handled with care. Hands grounded + antistatic mate

Fourth attempt using **Isola(?)**, **ICAPE**

The order for 10 pcs was placed, delivery in 8 weeks

What makes the PANDA-DC design so difficult?

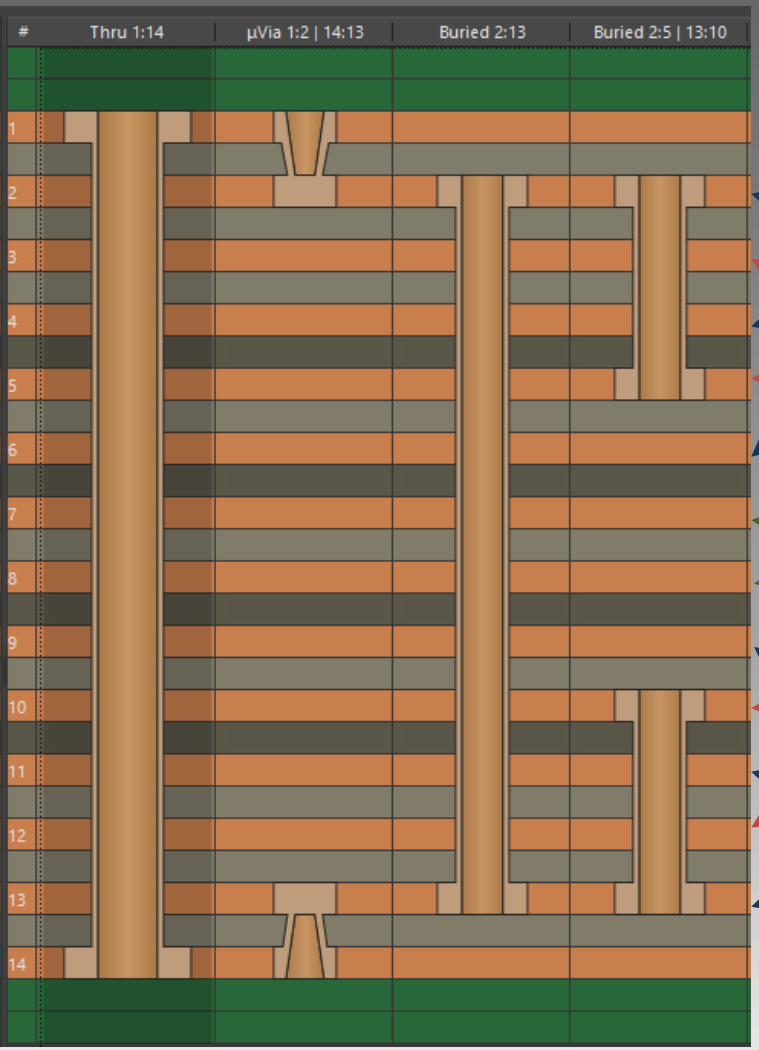


- Five 12-channel differential transmitter/receiver lanes
- 14 Gbit/s per lane
- 24 differentrial lanes per transmitter/receiver pair.
- Lanes must be as short and homogeous as possible
- Routing requires 4 layers for differential lanes

PANDA_DC prototyping

14-layer HDI layout with high-speed substrate

#	Name	Type	Thickness
	Top Overlay	Overlay	
	Top Solder	Solder Mask	0.01mm
1	1_TOP	Signal	0.018mm
	Dielectric 1	Prepreg	0.071mm
2	2_GND	Signal	0.018mm
	Dielectric 2	Prepreg	0.101mm
3	3_DIFF	Signal	0.018mm
	Dielectric 3	Prepreg	0.101mm
4	4_GND	Signal	0.018mm
	Dielectric 4	Core	0.101mm
5	5_DIFF	Signal	0.018mm
	Dielectric 5	Prepreg	0.101mm
6	6_GND	Signal	0.035mm
	Dielectric 6	Core	0.101mm
7	7_PWR	Signal	0.035mm
	Dielectric 7	Prepreg	0.102mm
8	8_PWR	Signal	0.035mm
	Dielectric 8	Core	0.101mm
9	9_GND	Signal	0.035mm
	Dielectric 9	Prepreg	0.101mm
10	10_DIFF	Signal	0.018mm
	Dielectric 10	Core	0.101mm
11	11_GND	Signal	0.018mm
	Dielectric 11	Prepreg	0.101mm
12	12_DIFF	Signal	0.018mm
	Dielectric 12	Prepreg	0.101mm
13	13_GND	Signal	0.018mm
	Dielectric 13	Prepreg	0.071mm
14	14_BOT	Signal	0.018mm
	Bottom Solder	Solder Mask	0.01mm
	Bottom Overlay	Overlay	



GND separation

High-speed differential

Power supply

High-speed differential

GND separation

PANDA_DC power estimation

Settings

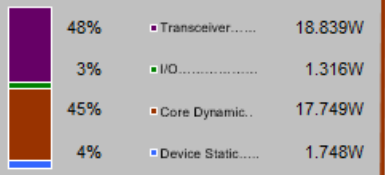
Device	
Family	Kintex UltraScale+
Device	XCKU15P
Package	FFVA1760
Speed Grade	-1
Temp Grade	Extended
Process	Typical
Voltage ID Used	
Characterization	Production (± 15% accuracy)

Environment		
Junction Temperature	☐ User Override	
Ambient Temp		25.0 °C
Effective ΘJA	☐ User Override	
Airflow		500 LFM
Heat Sink		Medium Profile
ΘSA		0.7 °C/W
Board Selection		Medium (10"x10")
# of Board Layers		12 to 15
ΘJB		
Board Temperature		

Implementation	
Optimization	Power Optimization

Summary

Total On-Chip Power	39.7 W	
Junction Temperature	47.4 °C	
Thermal Margin	52.6°C	89.6W
Effective ΘJA		0.6 °C/W



Power supplied to off-chip devices 0.000W

On-Chip Power

Resource	(Jump to sheet)	Power (W)	Power (%)
Core Dynamic	CLOCK	6.626	17
	LOGIC	9.452	24
	BRAM	0.894	2
	DSP	0.772	2
	PLL	0.000	0
	MMCM	0.000	0
	Other	0.005	0
	Hard IP	0.000	0
	URAM	0.000	0
I/O	IO	1.316	3
Transceiver	GTH	10.660	27
	GTY	8.179	21
Device Static		1.748	4

Power Supply

Source	Voltage	Total (A)
V_{CCINT}	0.850	23.644
V_{CCINT_IO}	0.850	0.135
V_{CCBRAM}	0.850	0.070
V_{CCAUX}	1.800	0.324
V_{CCAUX_IO}	1.800	0.196
V_{CCO} 3.3V	3.300	
V_{CCO} 2.5V	2.500	
V_{CCO} 1.8V	1.800	0.596
V_{CCO} 1.5V	1.500	
V_{CCO} 1.35V	1.350	
V_{CCO} 1.2V	1.200	
Vcco 1.0V	1.000	
$MGTV_{CCAUX}$	1.800	0.538
$MGTAV_{CC}$	0.900	2.188
$MGTAV_{TT}$	1.200	5.668
$MGTYV_{CCAUX}$	1.800	0.192
$MGTYAV_{CC}$	0.900	1.414
$MGTYAV_{TT}$	1.200	5.001
-		
V_{CCADC}	1.800	0.008
-		

Messages

P_{TOT} = 39.7W

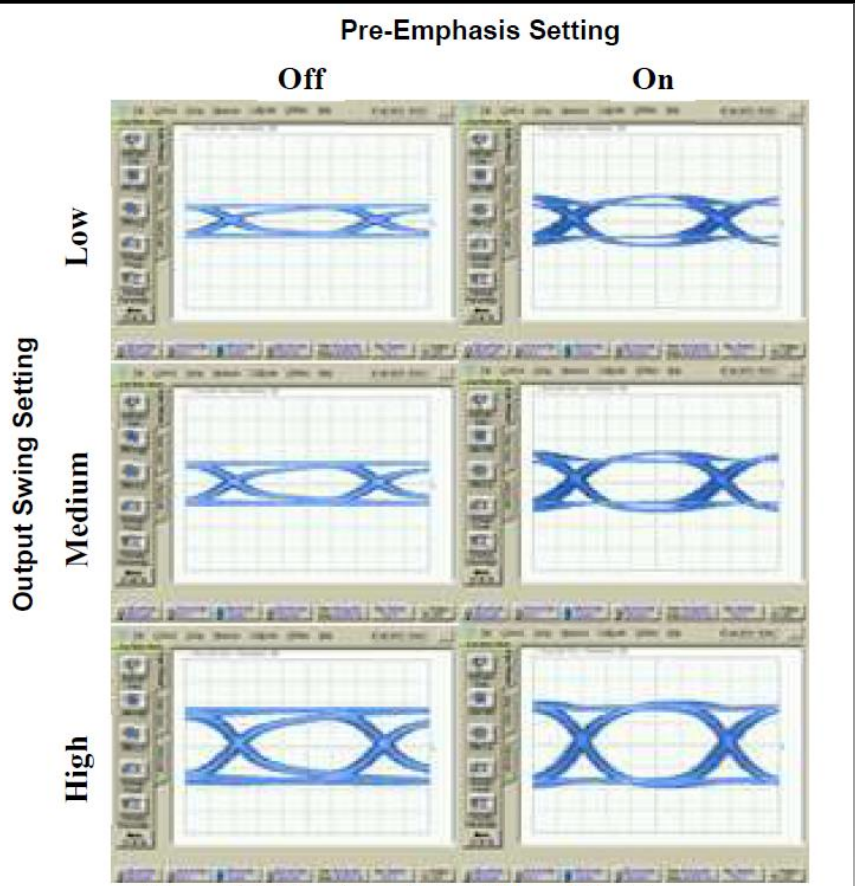
PANDA_DC power estimation

samtec

FireFly™ Optical

14G x12 Data Sheet

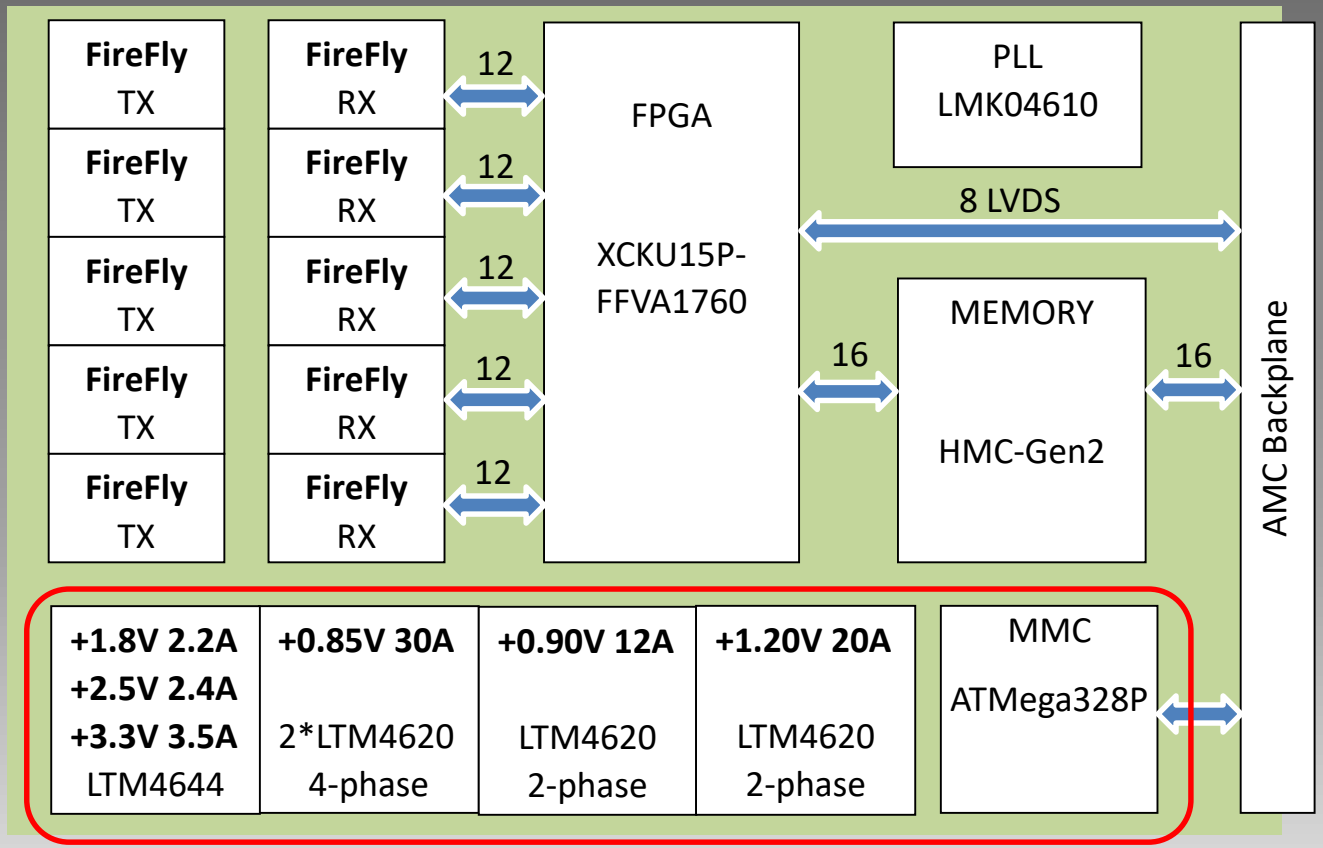
P_{TOT} = 13.4W



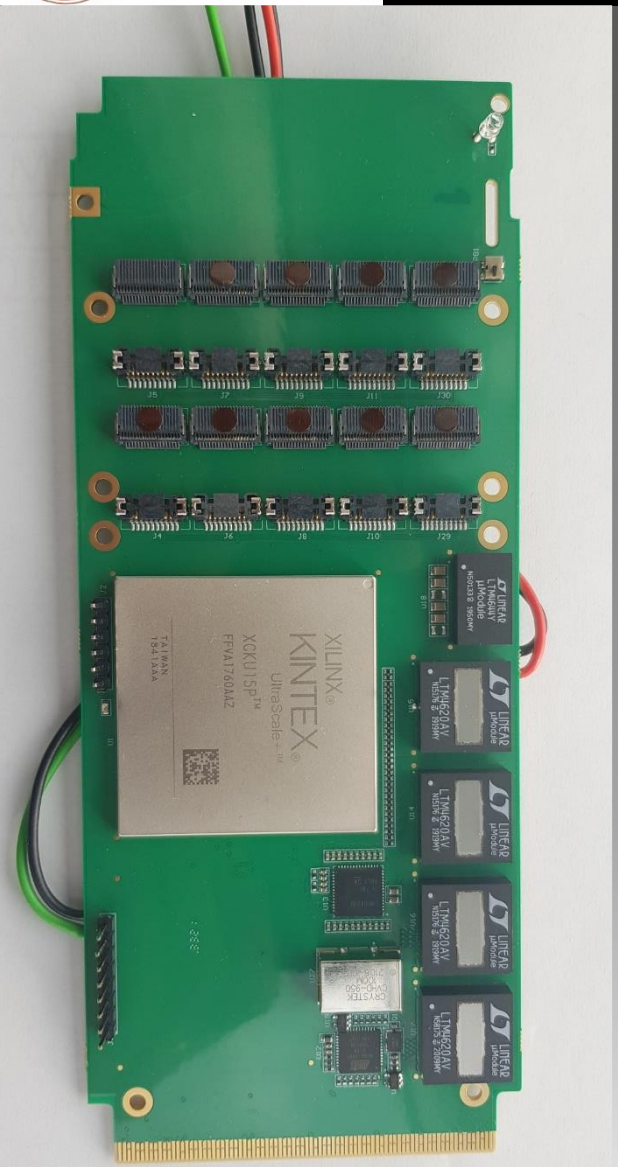
Output Voltage	De-Emphasis	Power Dissipation	
		Typical [mW]	Worst Case [mW]
Low	Off	820	1240
	On	1250	1792
Medium	Off	900	1390
	On	1340	1902
High	Off	1160	1640
	On	1600	2152

PANDA_DC power estimation

Module Power (50W)



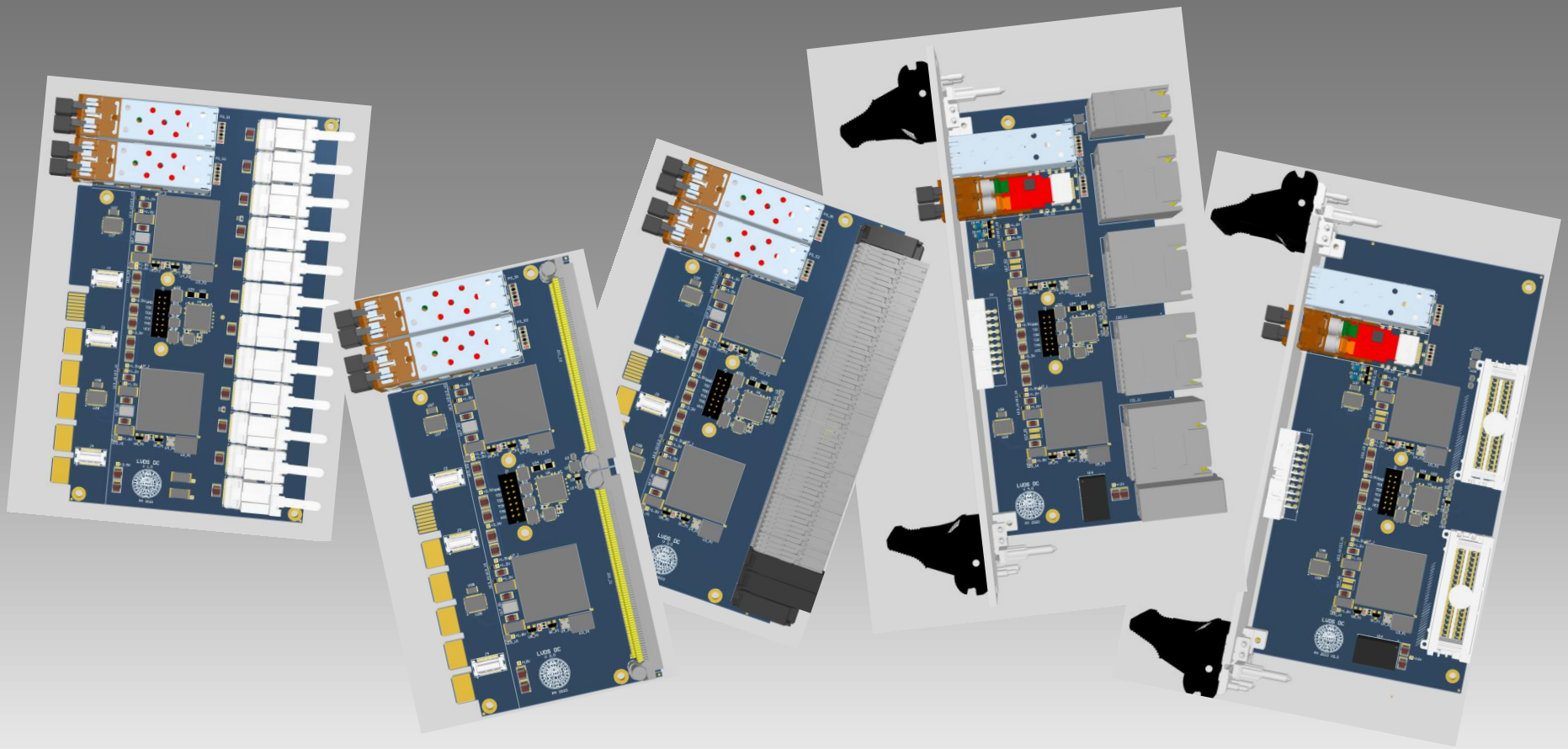
PANDA_DC Status



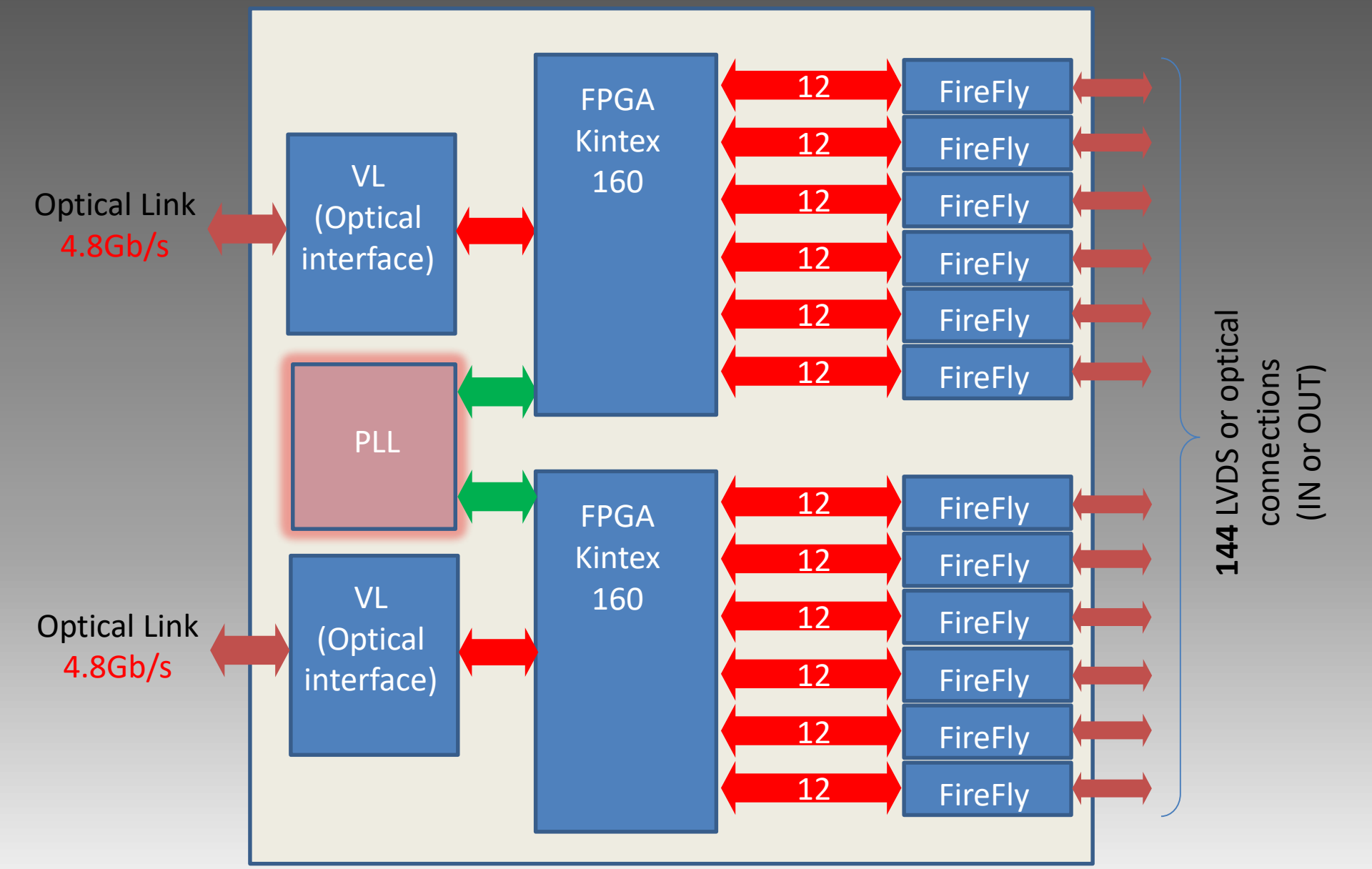
Summary on PANDA-DC development work

- We have 2 prototypes (1 working, 1 partially working), on which we can work on firmware development
- The work was so far progressing with long interrupts, but it will get accelerated in the coming months
- We are expecting 1 more device, hopefully the final one in 3 months. After successful verification we will produce the resting 9.
- All components are procured apart from the optical transceivers (Firefly), which need special order from Samtec in agreement with CERN to comply with VL and VL+. A MoU with CERN was signed for such an order.

A development work on the LVDS Data Concentrator



LVDS DC


Optical Link
4.8Gb/s
VL
(Optical
interface)
PLL
VL
(Optical
interface)
Optical Link
4.8Gb/s
FPGA
Kintex
160
FPGA
Kintex
160
12
FireFly
144 LVDS or optical
connections
(IN or OUT)

Short presentation and application

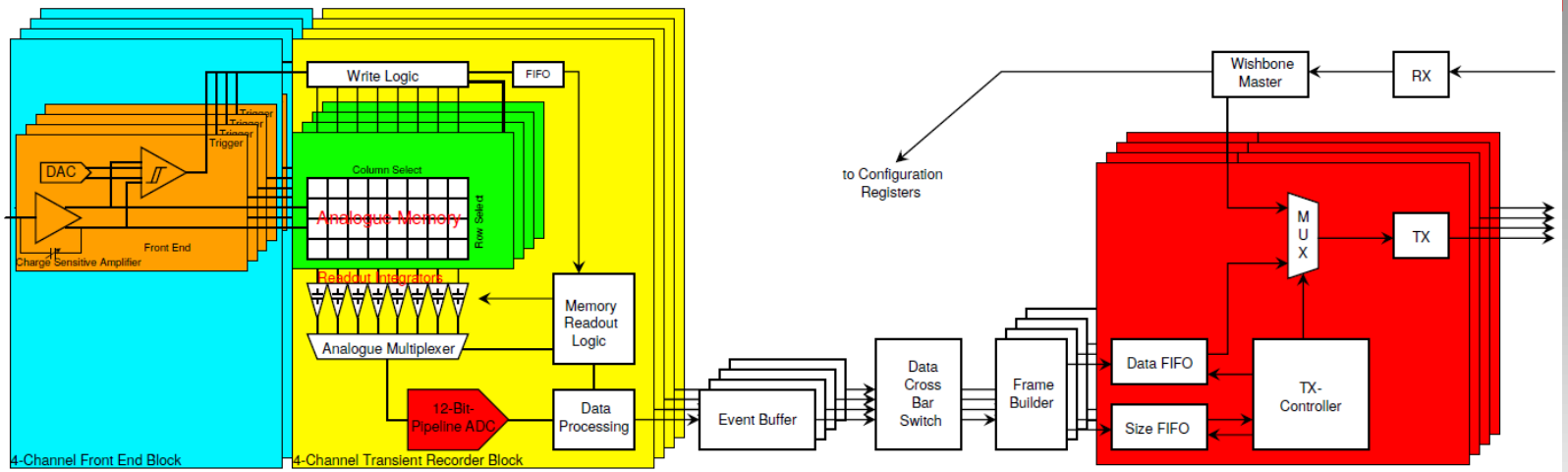
Readout interface using LVDS

- A broad interest arouse in utilizing LVDS lines for transporting data between front-end electronics and data collection systems
- LVDS are electrical signals and do not need any expensive and power consuming conversion to/from optical media
- The achievable data rate over LVDS is lower compared to optical, but is sufficient in many (majority) of applications

Application 1
EMC Barrel

- ~12000 crystals
- Each crystal is read-out by 2 APDs with 2 different gain channels each
- A CTR serving 4 crystals communicates over 4 LVDS lines
- -> a need for 12000 LVDS (digital) I/O for the readout.
- The signals are planned (?) to be transported via Samtech FireFly (ECUE-08)
- Data rate - 500Mbit/s, Coding - No

Below a schematic of a EMC Barrel readout ASIC (by Holger Flemming)



Short presentation and application

Application 2
Luminosity Monitor

- ~2500 channels
- The signals are planned to be transported via some twisted pair cables (?)
- Data rate? (~800 Mbit/s)
- Coding? (8B/10B)
- Preliminary tests shown positive outcome (Florian Feldbauer)

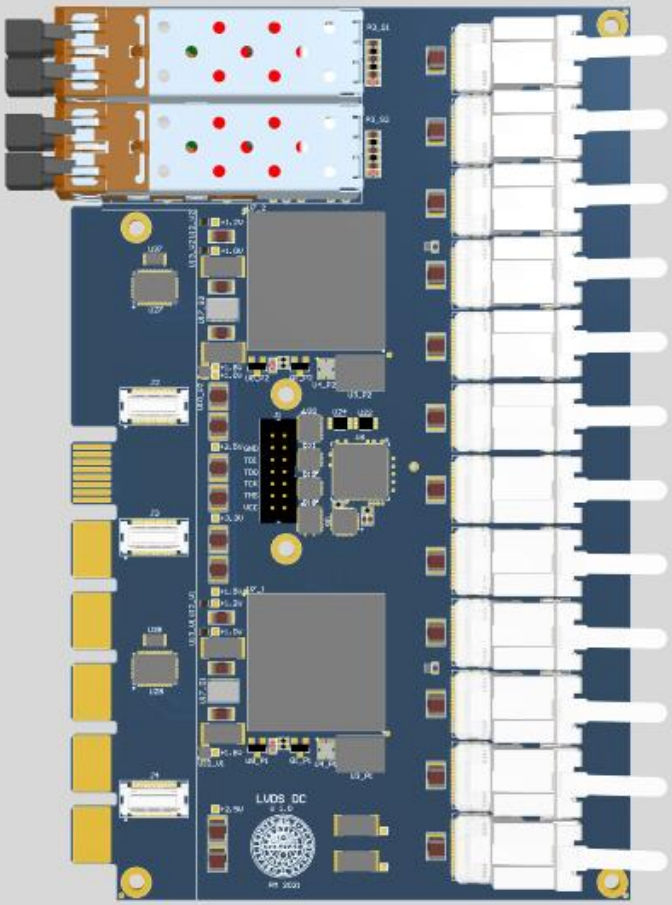
Application 3
Crystal Barrel (?)

Application 4
Other systems (?)

LVDS DC

A FireFly variant

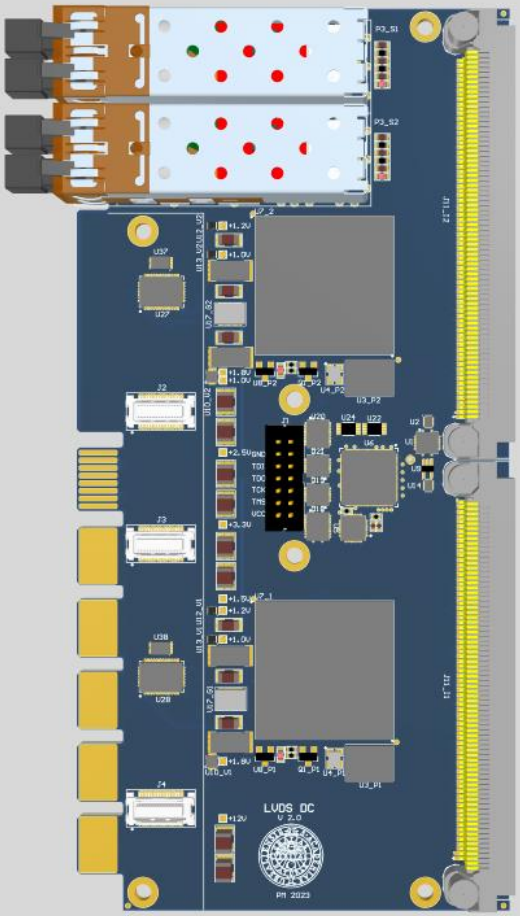
A single module with on-board FireFly transceivers



- FireFly modules are extremely fiddly to insert or remove. One can easily damage a module mechanically.
- The front becomes back – the module is inserted with the edge connector toward the back plane of a crate.
- Hardly service-able system

An EdgeRate variant

A module prepared for back-to-back FireFly interfacing over a back-plane

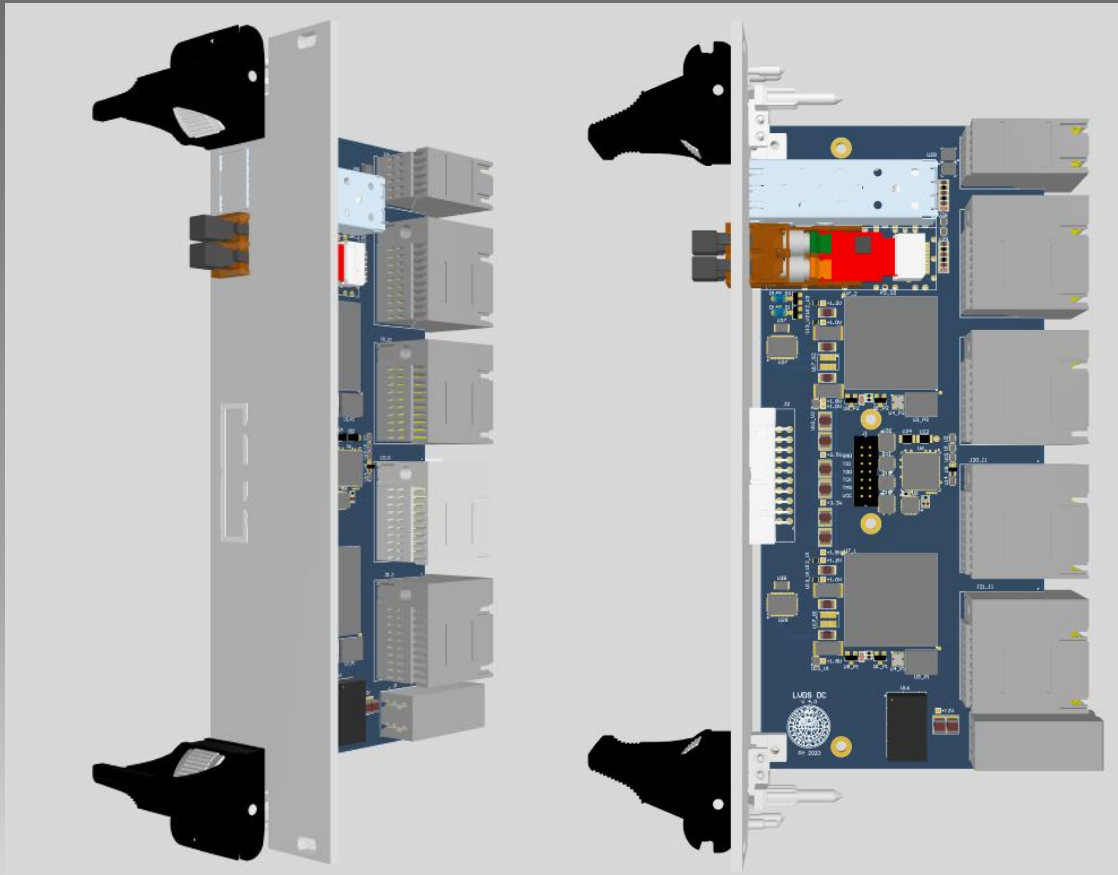


- EdgeRate 0.8 mm pitch connectors offer 300 pins. **288** are used for data.
  There is only **12** pins left for power and control. Too little...
- No guard separation between signals may lead to cross-talk – reducing data rate.
- The design is ready, however it's currently powered either from the front connector or by a dedicated mezzanine PS module. This could be subsitituted with a miniature **uModule** PS from TI and only use +12V as input.

LVDS DC

An ExaMAX variant

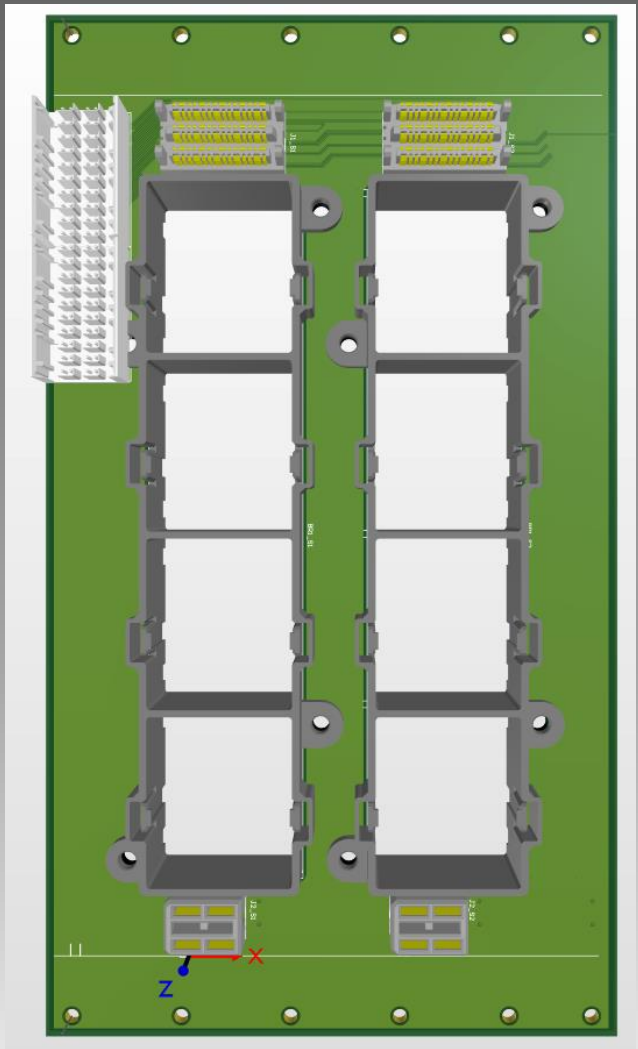
A module prepared for direct LVDS cable mating through a back-plane opening



- The module is **fully designed** and is powered by a uModule from +12V delivered from the back-plane.
- A monitoring system with +3.3V reference is distributed over the back-plane
- A number of control signals, JTAG programming and utility pins is available on a connector to be mated to the back-plane
- **Signal inputs are ESD protected**
- The module will fit in a customized Schroff mechanics
- The module is **8HP** (double width)

An ExaMAX variant

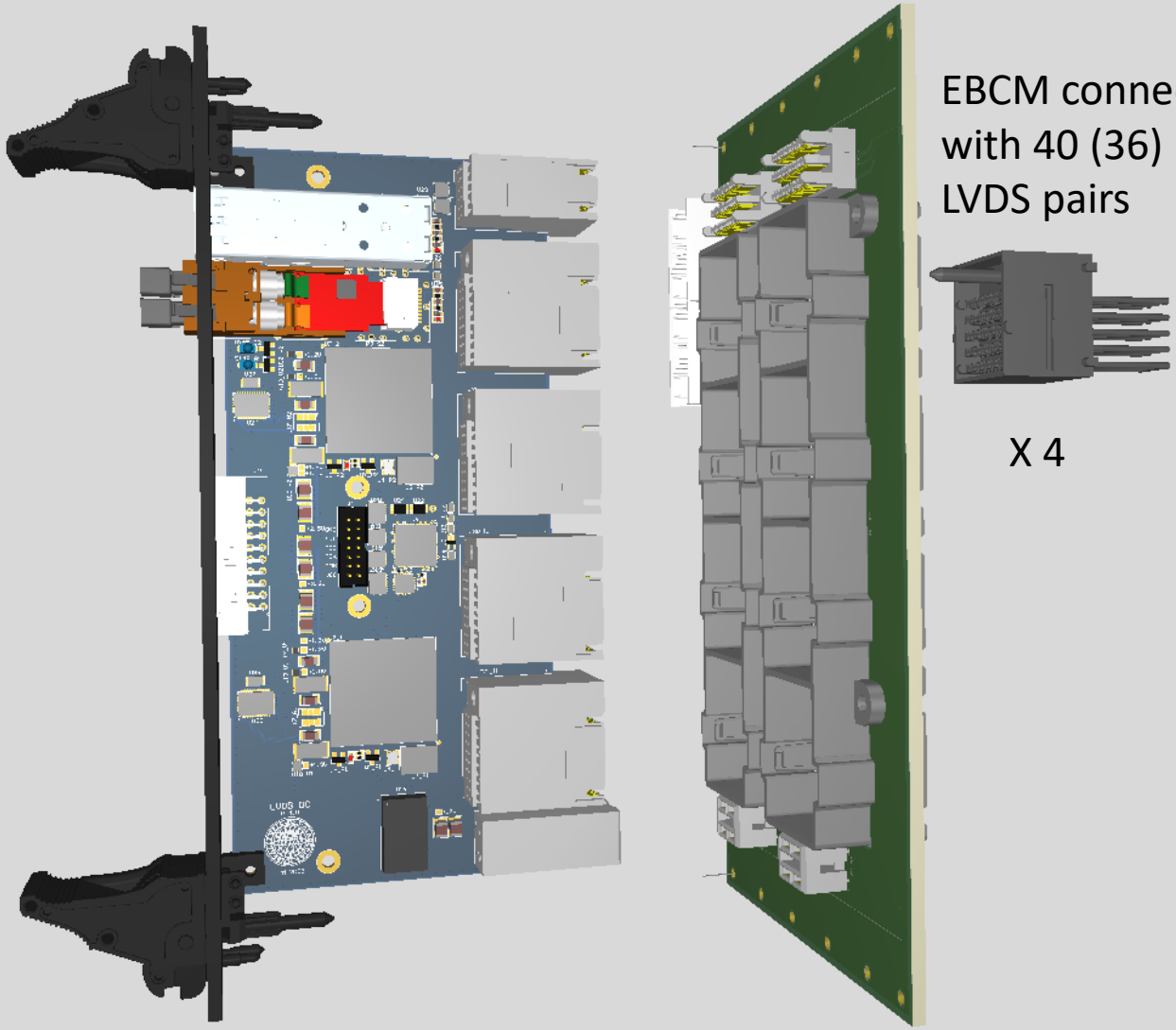
A two-slot back-plane



- A **10-slot** Back-Plane is **fully designed.** It will be presented later
- Here is a **2-slot** back-plane model for checking mechanical conditions.
- LVDS-DC slots are equiped with brackets. These hold cable connectors in place.
- On the left-hand side there is a slot for a Crate Controller. It will provide a possibility for configuration and control of the LVDS-DC modules in the crate. The Crate Controller will be **4HP** (standard width)

An ExaMAX variant

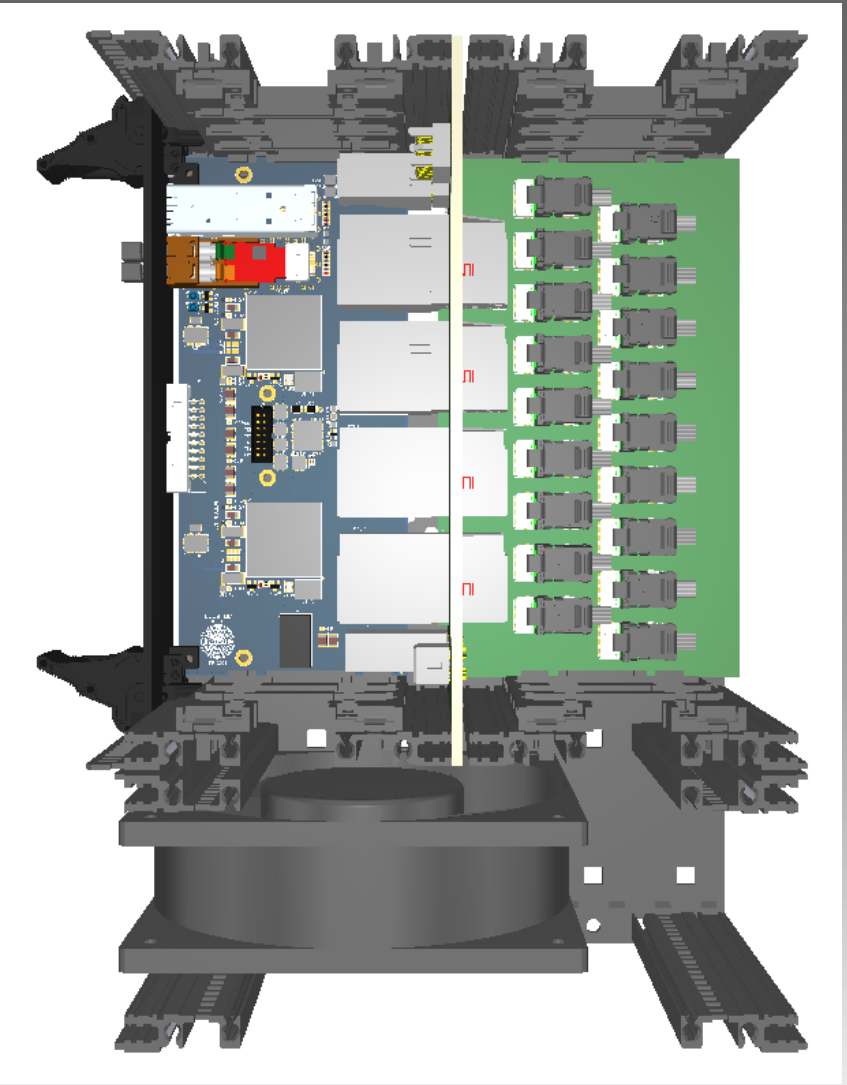
A module prepared for direct LVDS cable mating through a back-plane opening



- A 4-row 10 column EBCM connector can provide up to 40 LVDS pairs. Since our system is somewhat ECUE-12 oriented, we skip one column and only use 36 LVDS pais per connector.

An ExaMAX variant

A FireFly option for the ExaMAX system

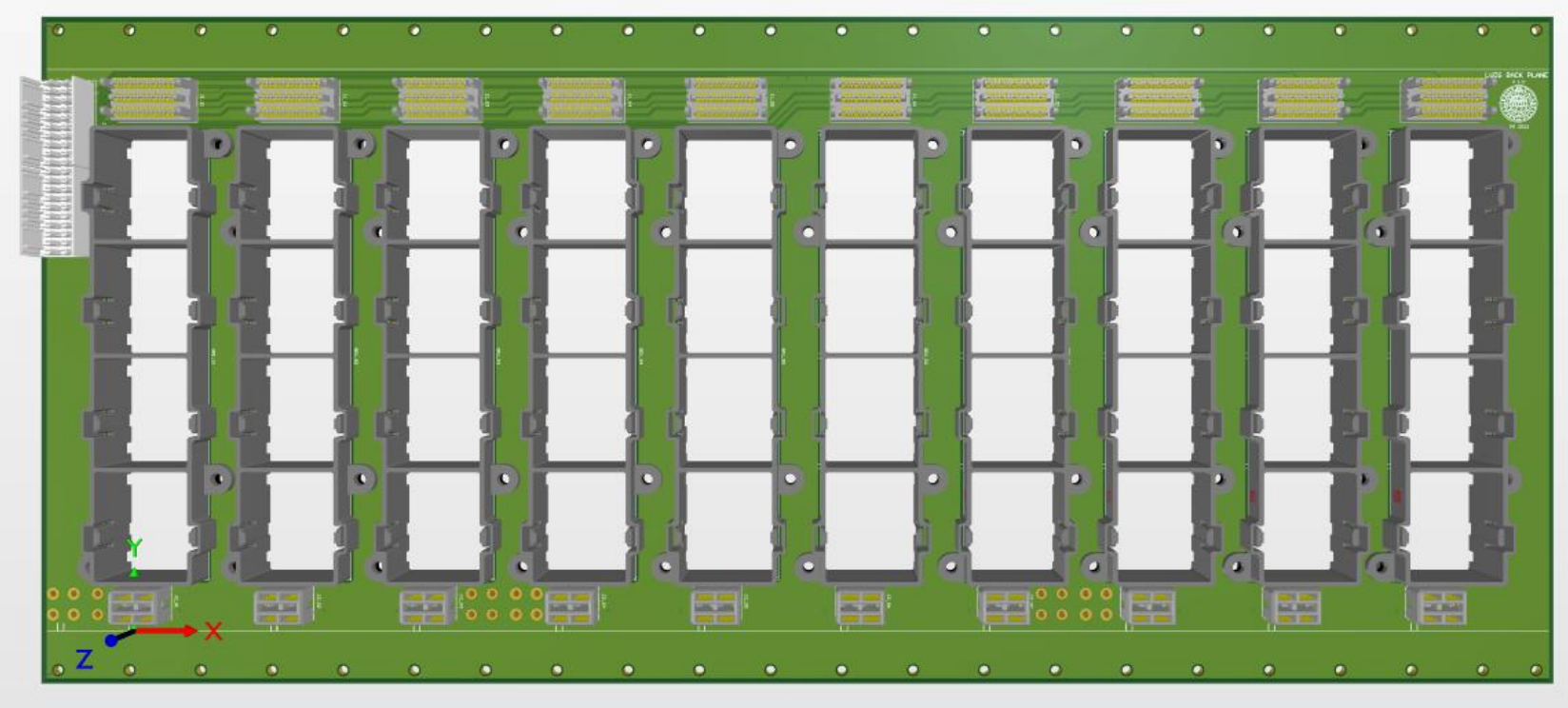


- The crate's rear compartment has rails for stable insertion of the FireFly carrier boards.
- The fan is 90 mm. The smaller fans, the more noisy.
- It seems that the rear compartment of the crate will need to be increased to fit power supplies below.
- The air-flow opening from below electronics is somewhat narrow...

LVDS DC

An ExaMAX variant

10-slot backplane for a 84HP (19”) crate

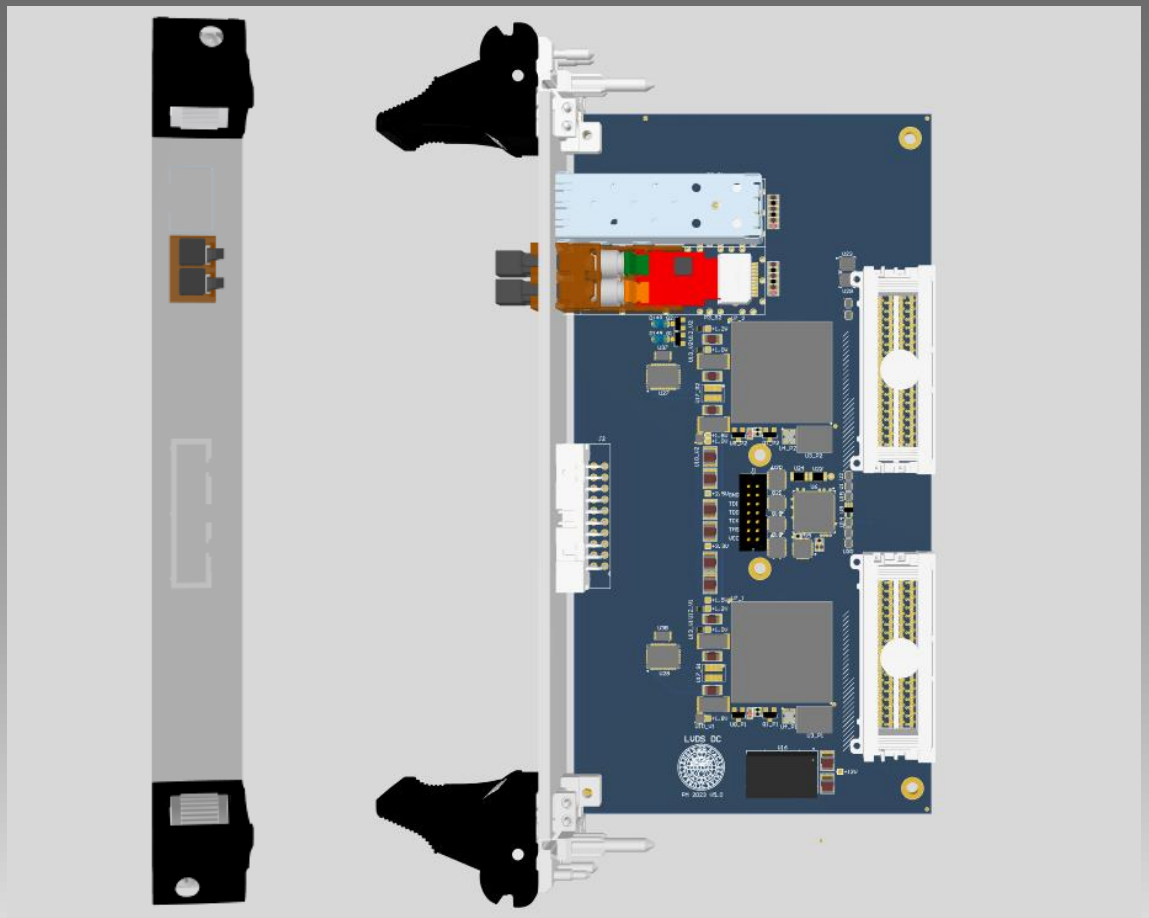


- The **Back-Plane** design is fully routed and **completed**
- It can suite both direct cable connection as well as FireFly carriers
- The **Crate Controller** design is **pending**

LVDS DC

An AcceleRATE variant

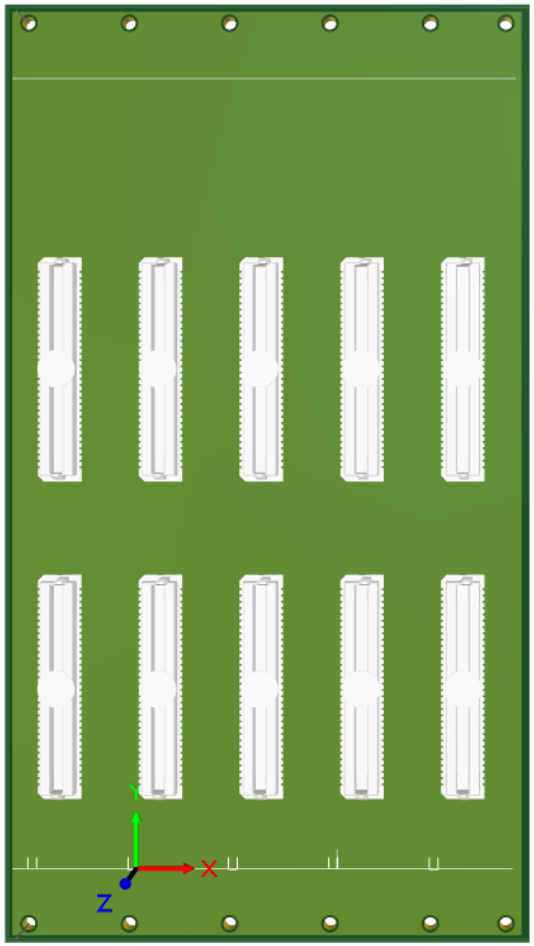
A high pin-density module for mating via a back-plane feed-through



- The module is **fully designed** and is powered by a uModule from +12V delivered from the back-plane.
- A monitoring system with +3.3V reference is distributed over the back-plane
- A number of control signals, JTAG programming and utility pins is available on a connector to be mated to the back-plane
- The module will fit in a customized Schroff mechanics
- The module is **4HP** (single width)

An AcceleRATE variant

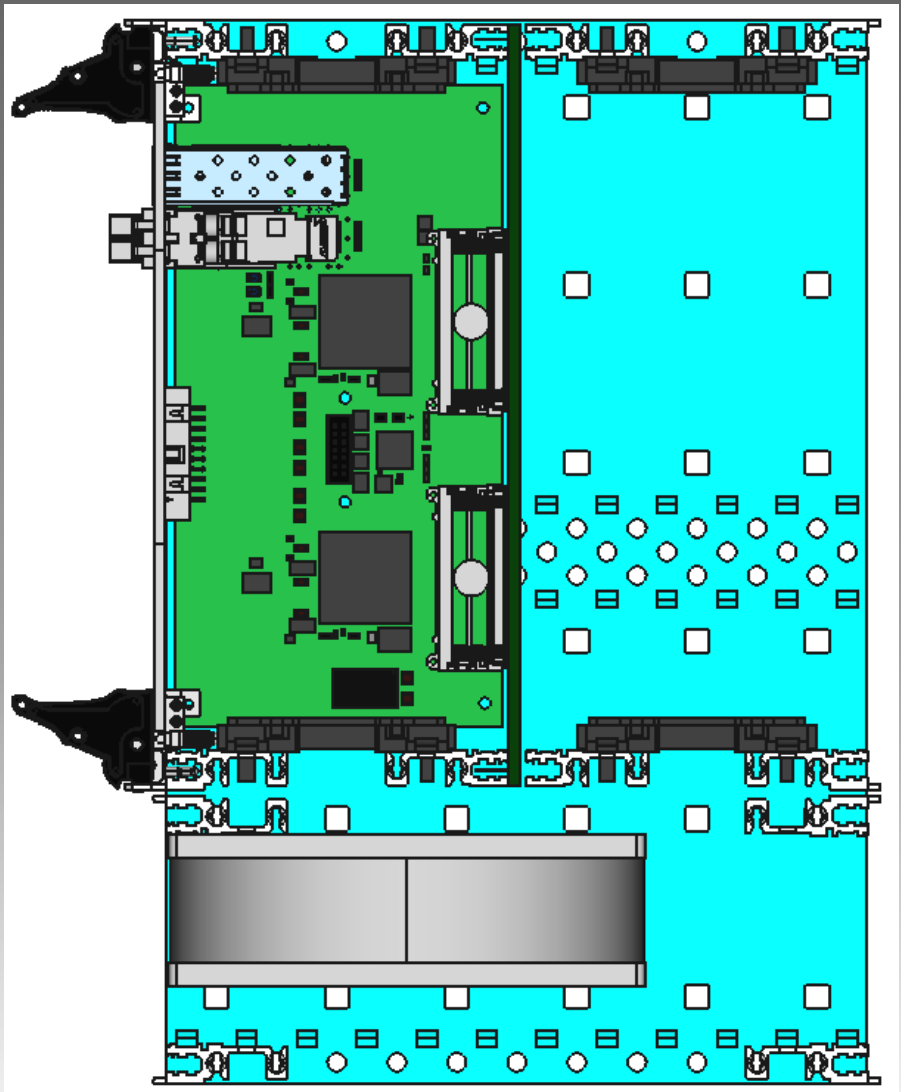
A four-slot back-plane



- Here is a **4+1 slot** back-plane model. The left-most is a controller slot.
- It is an empty design for checking mechanical conditions and adjust connector placement. No connections yet. The full design for 20+1 slot (84HP, 19”) **is pending**
- A Crate Controller design **is pending**

An AcceleRATE Crate mechanics

Crate construction

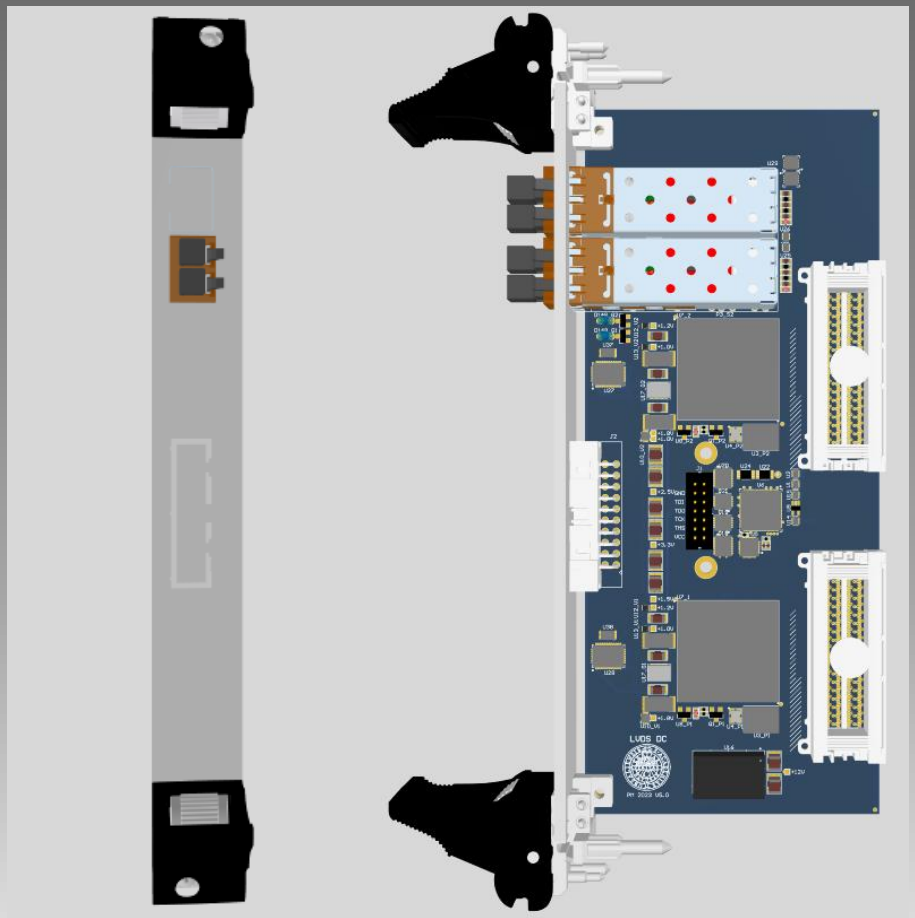


- The crate mechanical dimensions were elaborated in FreeCAD using STEP files provided by Schroff.
- The design and front panel models are available in STEP format.

A customized AcceleRATE variant

A right approach for the EMC Barrel?

No!



- During our meeting we came to the following conclusions:
- LVDS transceivers for EMC Barrel will be placed **inside** of the detector (in the backward region)
- One can expect **radiation** and a strong **magnetic field**
- The size matters
- No small on-board DC/DC
- Optical transceivers need to be **Versatile Link+** from CERN
- Custom crate mechanics providing space for **air-core** DC/DC modules

Summary and Conclusions

Summary (1)

In search for a perfect solution, 5 different versions of the LVDS-DC were designed.

- The on-board **FireFly** version is considered fiddly and not easily serviceable
- The **EdgeRATE** version is the simplest, but because of the pin shortage it should rather be considered as a mezzanine or as a part of a more robust module.
- The **ExaMAX** is a perfect solution for systems, where signals are distributed over individual cables, which then get aggregated at the input connector. Signals do not propagate over multiple connectors contributing to signal distorsions. Inputs are ESD protected. Due to bulky connectors the system does not offer the highest spatial channel density.
- The **AcceleRATE** version offers a double spatial channel density compared to ExaMAX. This solution would probably be the most appropriate for a system, where signals are distributed with FireFly (EMC Barrel).

Summary and Conclusions

Summary (2)

- The **ExaMAX** is a perfect solution for the **Luminosity** detector. One needs **20 modules** including spares.
- The **ExaMAX** will be used for the **EMC Barrel**, but it needs some more work in adapting it to the hostile environment. One needs **100-150 modules** including spares
- There is a consensus to use only one system (for service, documentation, spare parts etc), hence the risk is that the **Luminosity** detector may adopt the solution for the Barrel, despite if it's not optimal.

Thank You !