Status of the new LMD DAQ

PANDA CM 24/2

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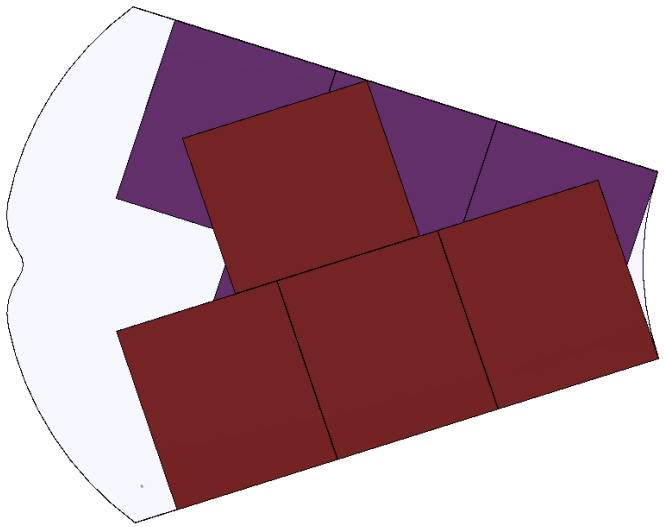
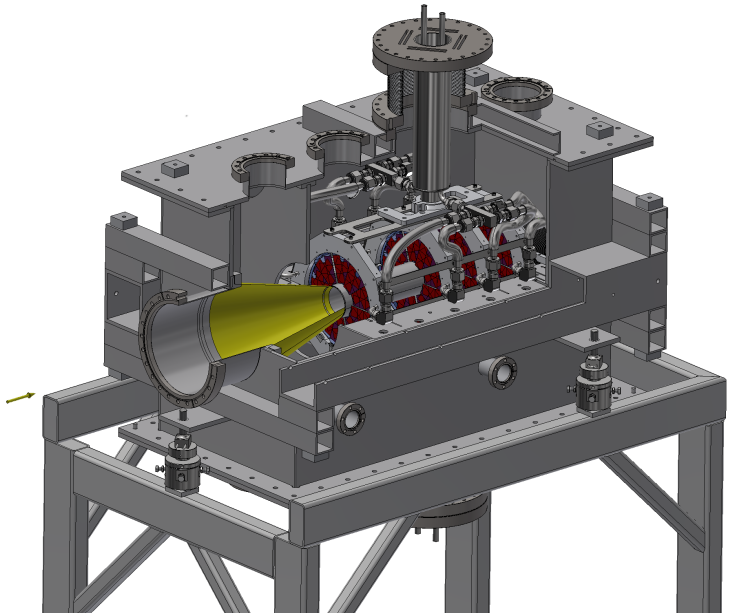
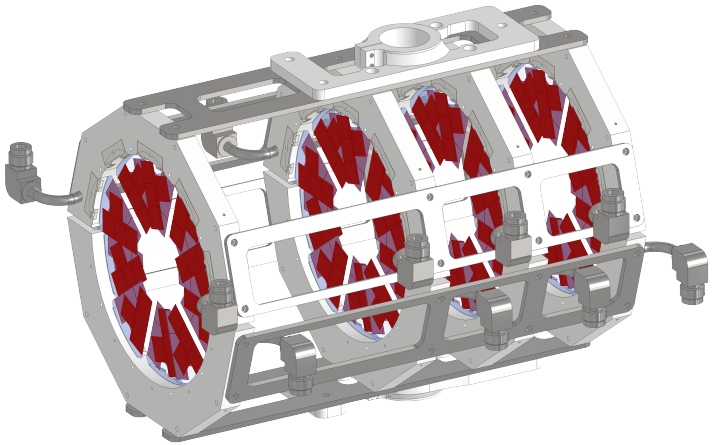
Luminosity Detector

- 320 MuPix chips
- Asynchronous LVDS readout
- Self triggered

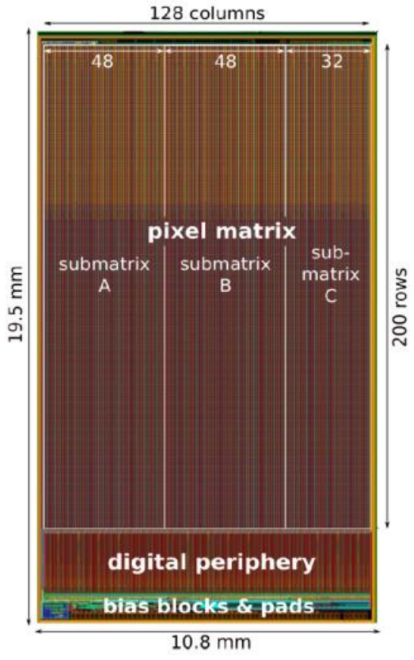






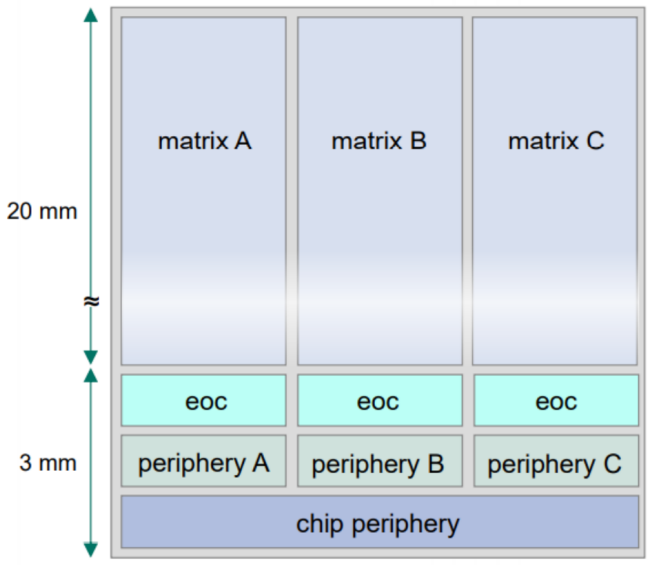
MuPix Sensors

MuPix8



- 128 × 200 pixels
- Physical size: $10.8 \times 19.5\,\mathrm{mm}^2$
- Active area: $10.2 \times 16.2\,\mathrm{mm}^2$

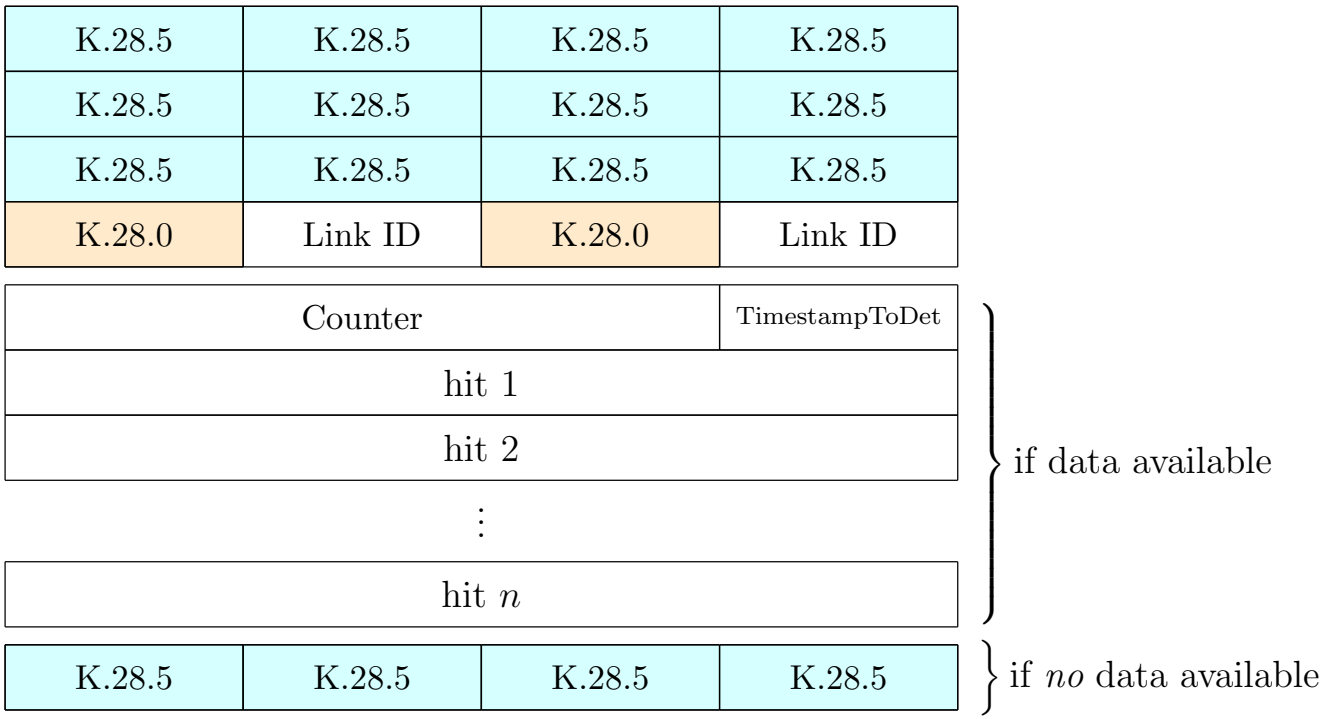
MuPix11



- 256 × 200 pixels
- Physical size: $20.7 \times 23.2\,\mathrm{mm}^2$
- Active area: $20.0 \times 20.5\,\mathrm{mm}^2$

MuPix8 Datagram

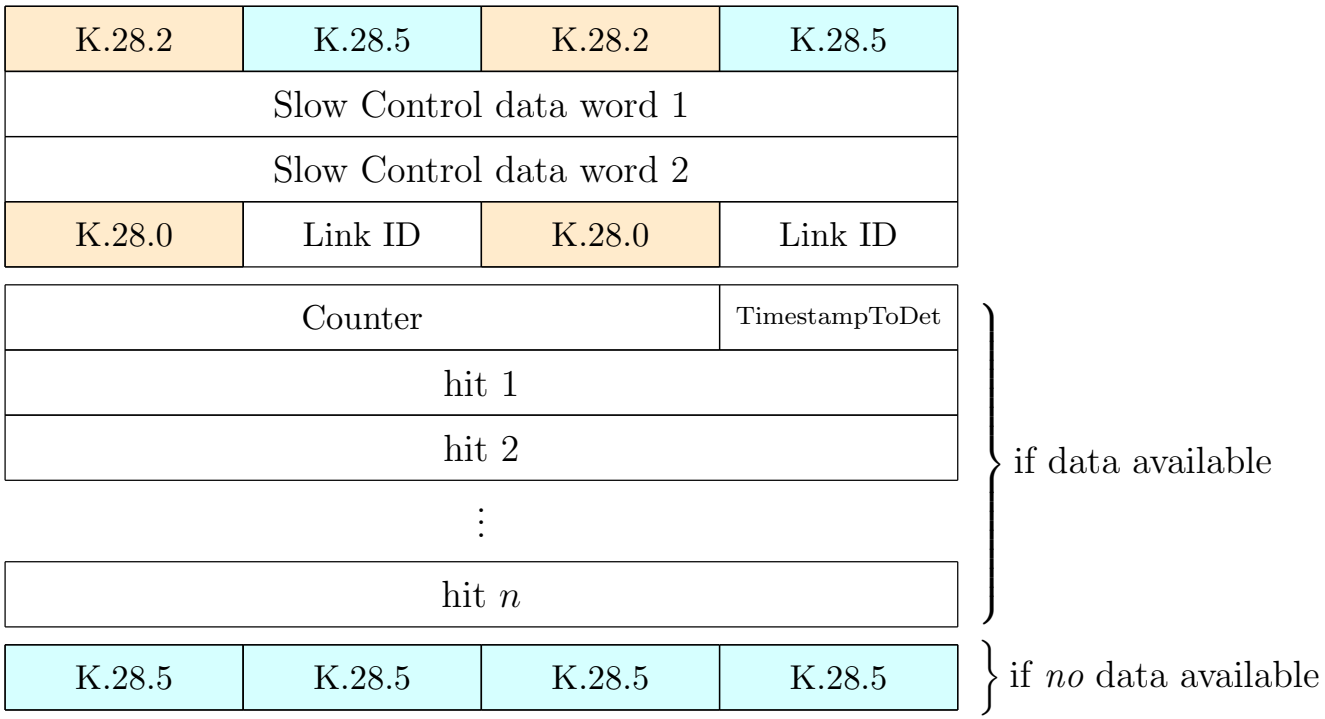
Continuous, asynchronous 8b10b encoded data stream from MuPix



Per readout cycle max 1 hit per column (max $n_{\text{cols(M)}}$ hits per frame)
K.28.5 “comma” word has unique bit sequence

MuPix11 Datagram

Continuous, asynchronous 8b10b encoded data stream from MuPix



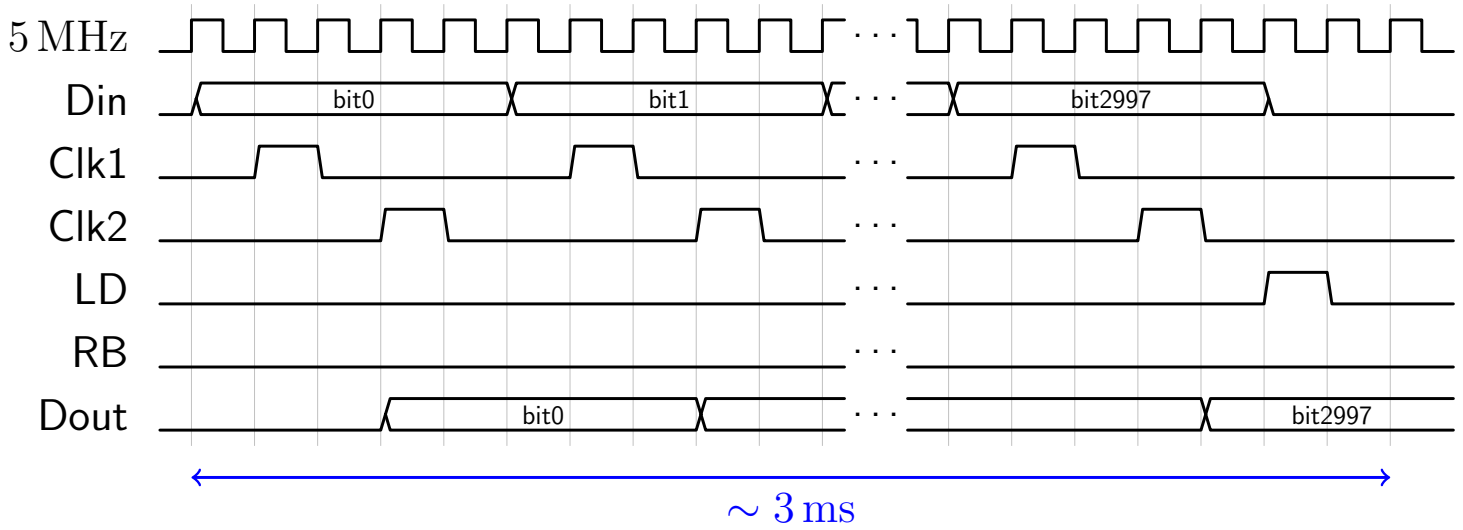
Per readout cycle max 1 hit per column (max $n_{\text{cols(M)}}$ hits per frame)
K.28.5 “comma” word has unique bit sequence
Slow Control data embedded in data stream!

MuPix8 Configuration

- Configuration realized with 2998 bit deep shift register
- Data needs to be send for each row ($200 \cdot 2998$ bit $\sim$ 600 kbit)
- Order of bits not “human readable” (e.g. R[2,0,1,3,4,5])
- Different length of individual registers (1, 2, 3, 4, 6 and 10 bit)

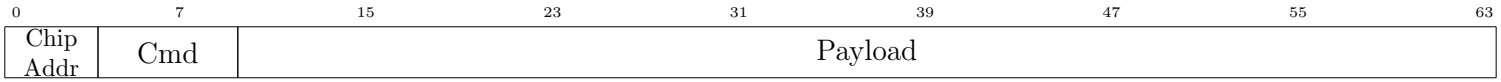
$\Rightarrow$ Build bitstream on PC rather then on FPGA

- On FPGA: State machine to pipe out bits and control signals (CLK1, CLK2, LD)
- 6 signals (4 could be shared) between MuPix and FPGA



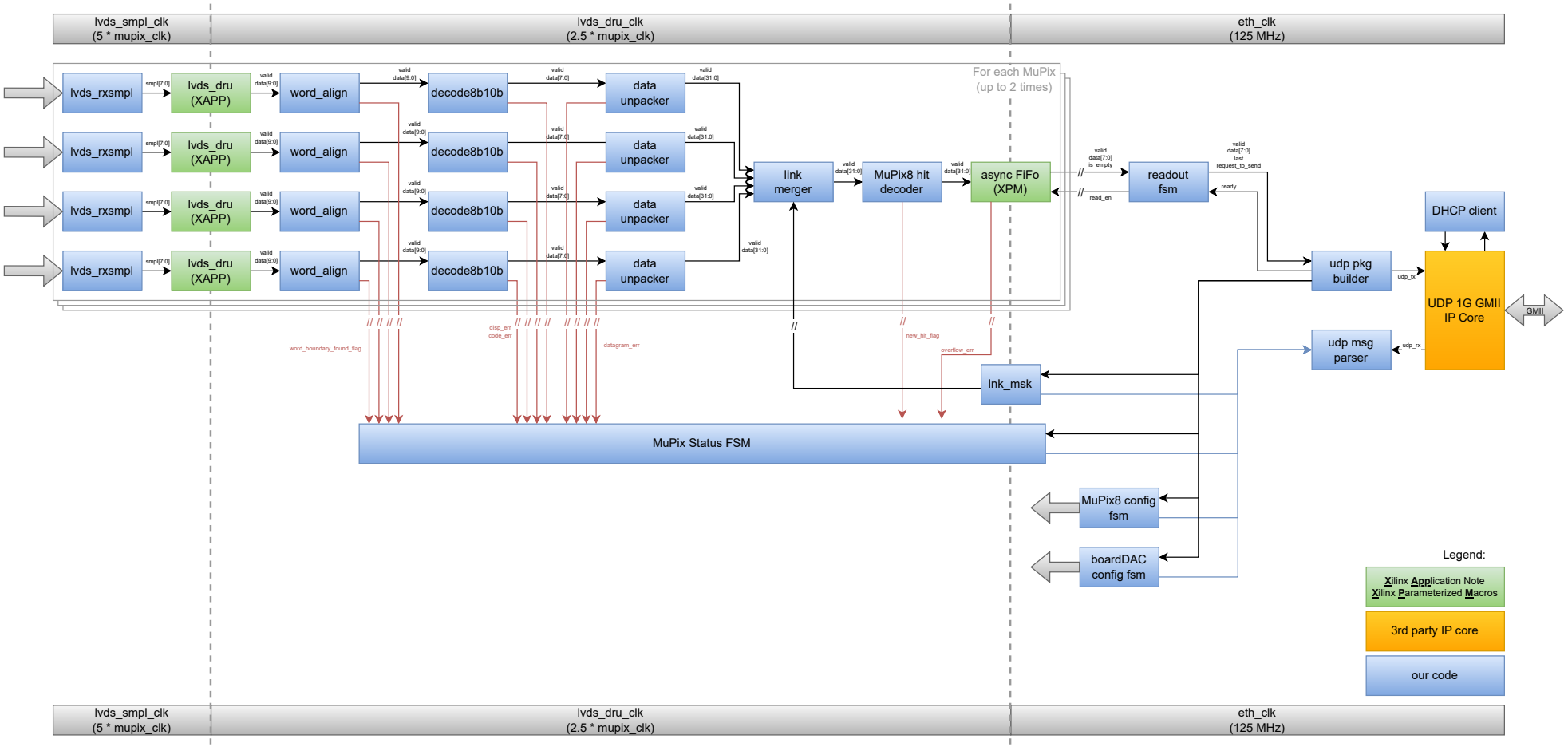
MuPix11 Configuration

- Only *one* differential pair for data transmission
- Up to 15 MuPix11 can be connected to one configuration bus

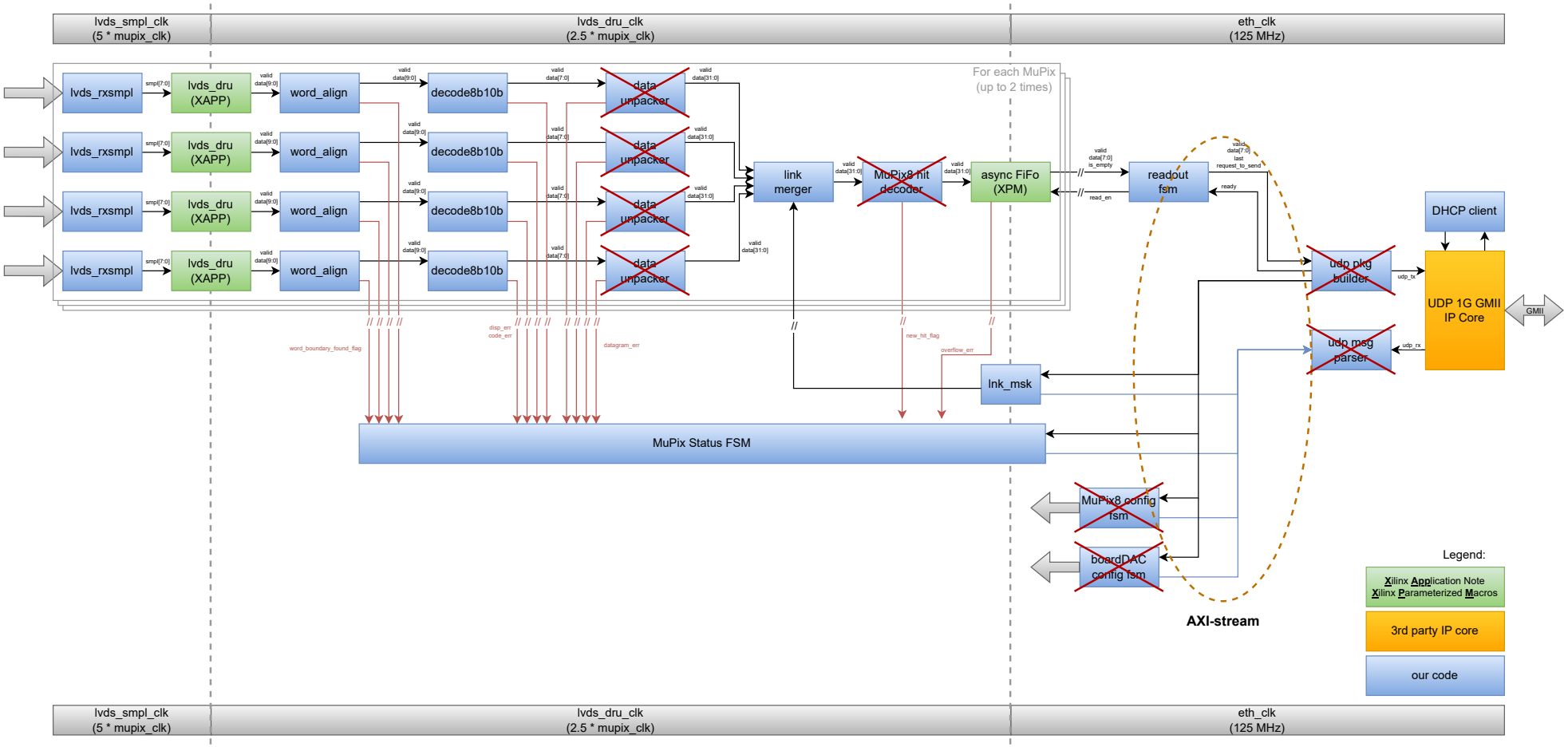


- Clock for sending data: $f_{SC} = \frac{f_{ref}}{8}$
- Configuration split into multiple register blocks
  Repeat “WriteXXX” command mulitple times to write complete register block
- Internal ADC for Voltage/Temp measurement
- All “replys” send back via data stream

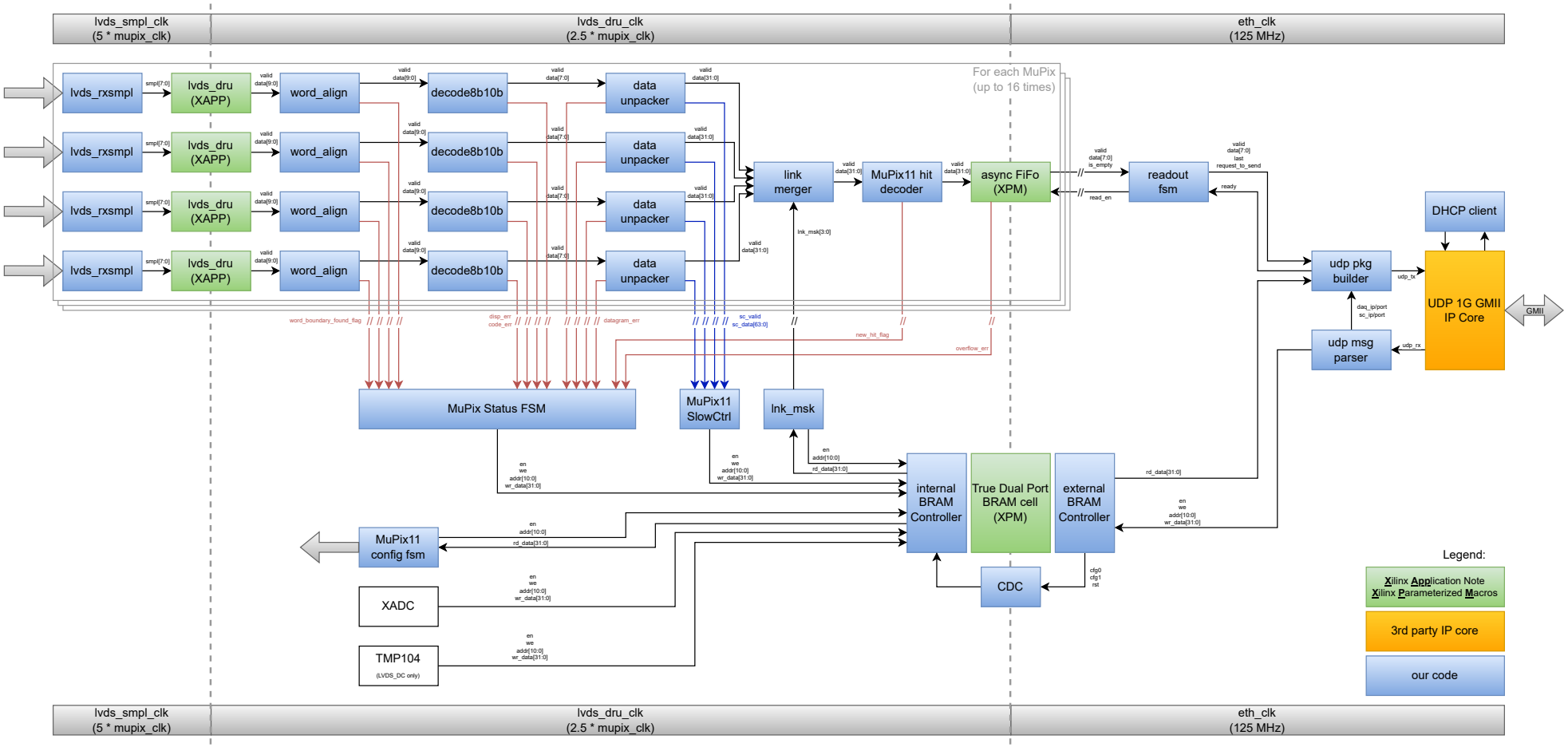
Block Diagram of Kintex 7 Firmware



Block Diagram of Kintex 7 Firmware

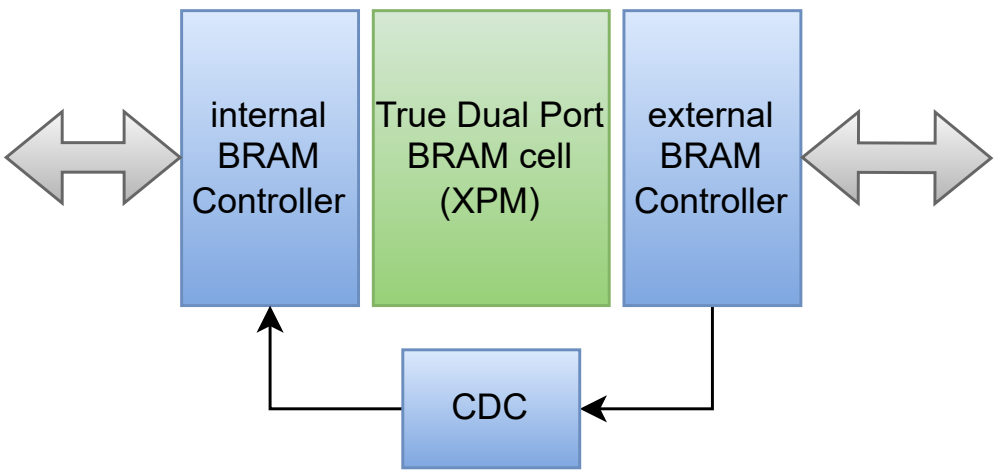


New Block Diagram of Kintex 7 Firmware



New Slow Control interface

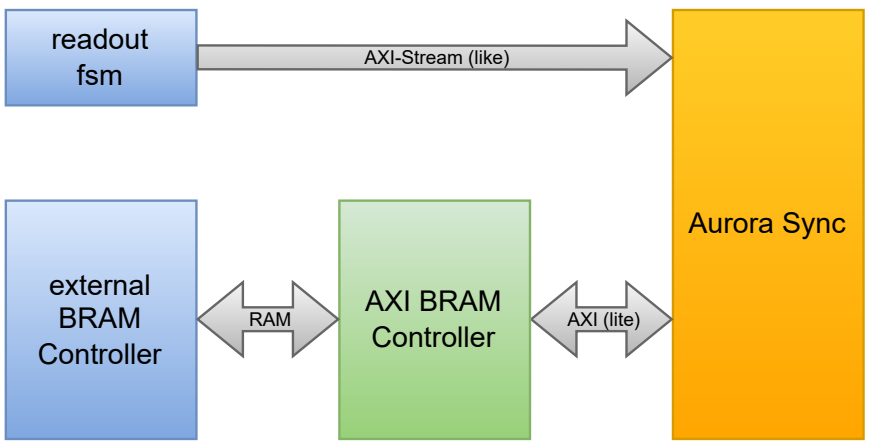
- Slow Control interface based on registers
- True Dual Port BRAM cell as storage (and for CDC)
- “external BRAM controller”: Access control (e.g. read-only, read/write)
  Counts MuPix11 configuration registers written
- “internal BRAM controller”: Round-Robin arbiter managing access of internal state machines to BRAM cell



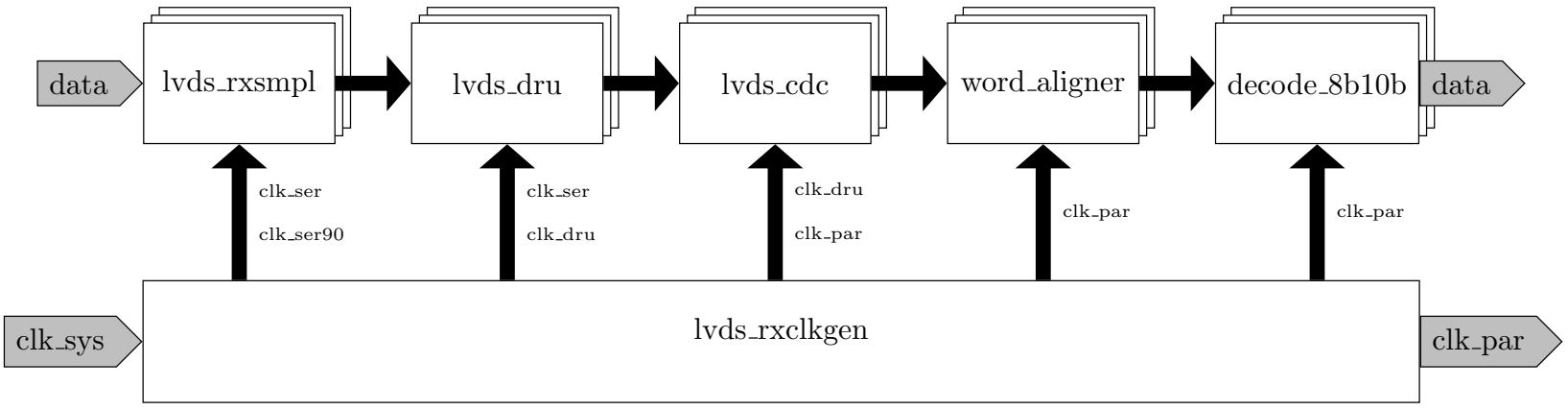
Summary: Modifications for MuPix11

- Rewritten Data Unpacker (extract Slow Control words)
- New MuPix11 Configuration state machine
- New Slow Control interface: Register based access with RAM interface

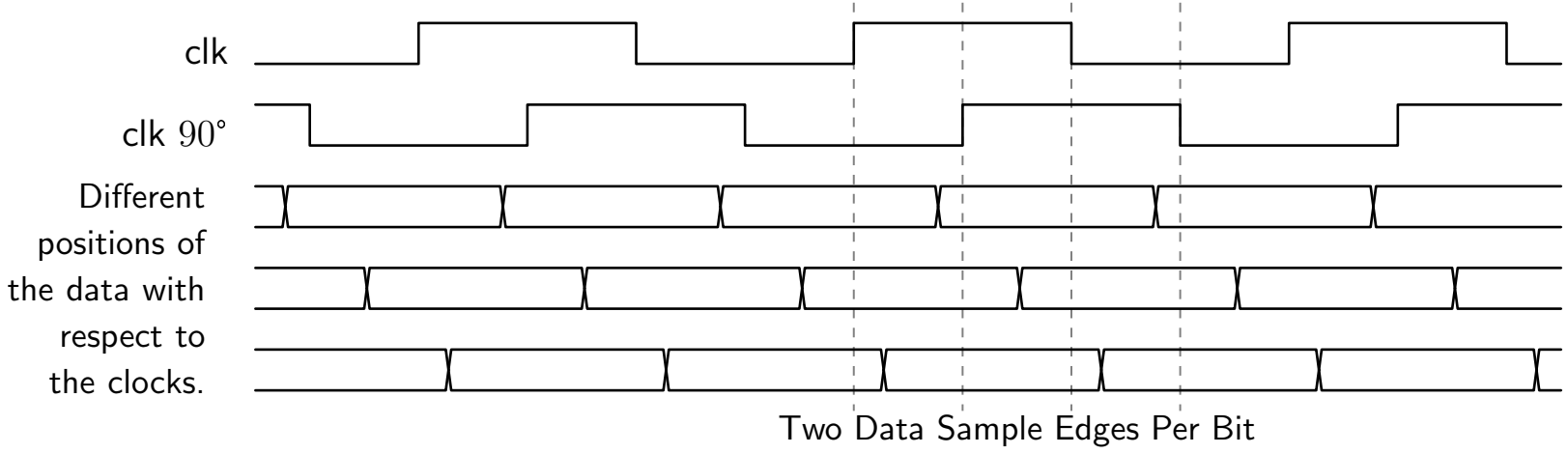
⇒ Should allow easy exchange of UDP interface with Aurora Sync



LVDS Receiver IP Core

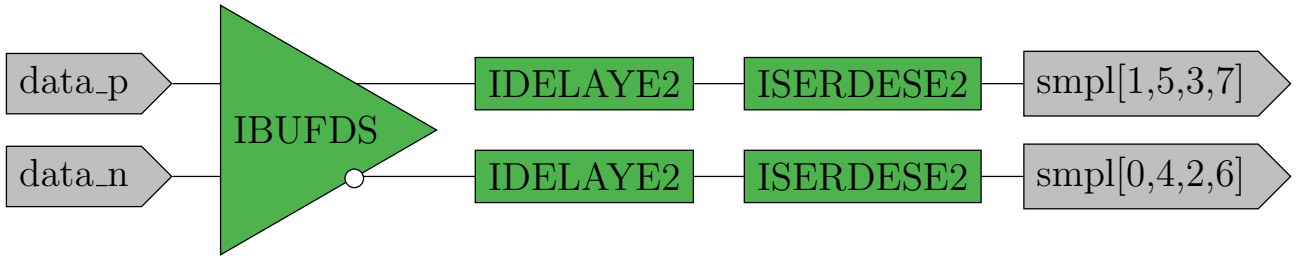


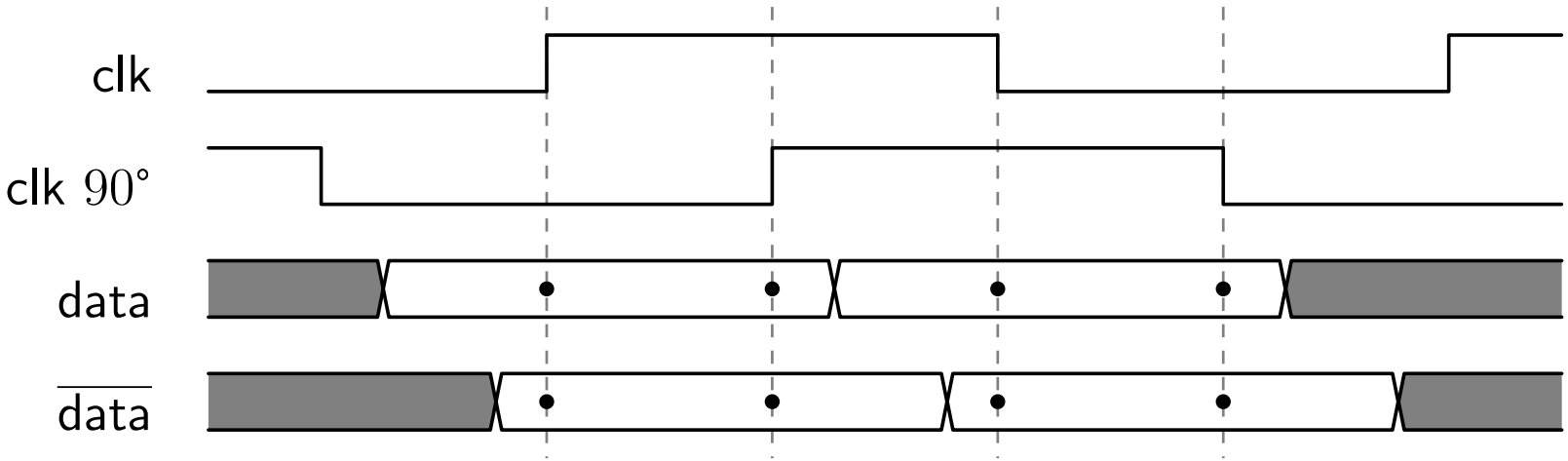
Sampling of asynchornous data bases on XAPP523:



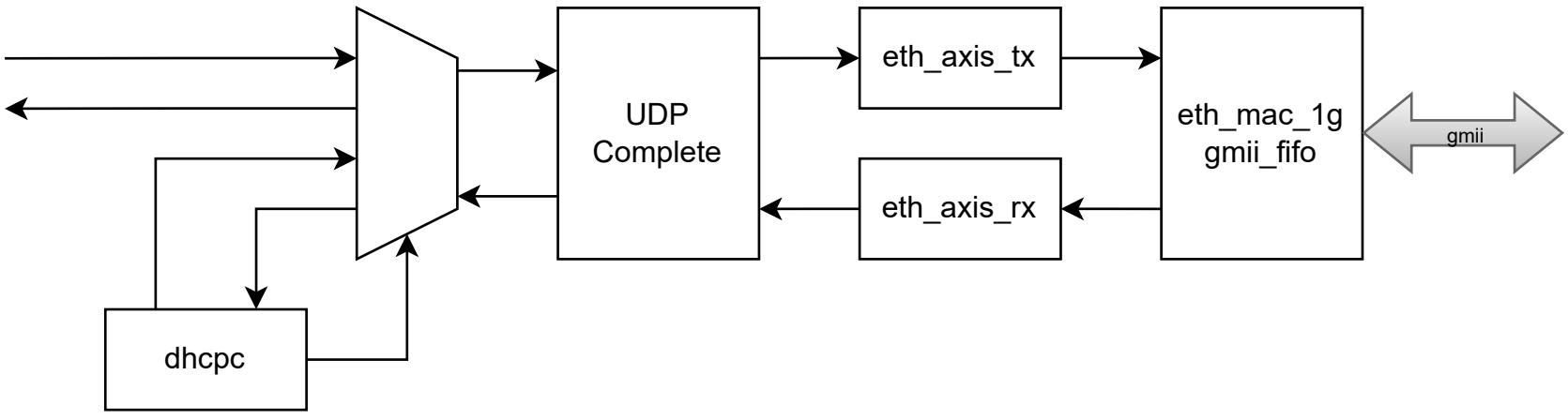
LVDS Receiver IP Core - Data Sampling

Use LVDS input buffer with differential output
Delay negative signal by 45°





UDP IP Core


UDP
Complete
eth_axis_tx
eth_axis_rx
eth_mac_1g
gmii_fifo
gmii
dhcpc