The Data Acquisition for the PANDA Phase-0 Experiment at MAMI

Oliver Noll

Helmholtz Institute Mainz

PANDA FEE/DAQ Workshop

PANDA Collaboration Meeting 24/2

Darmstadt

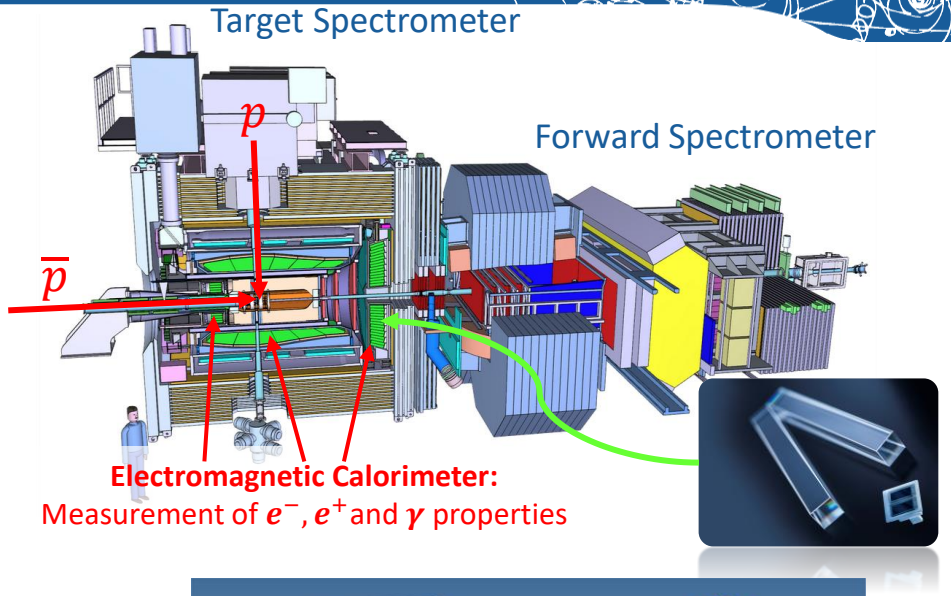
26.06.2024

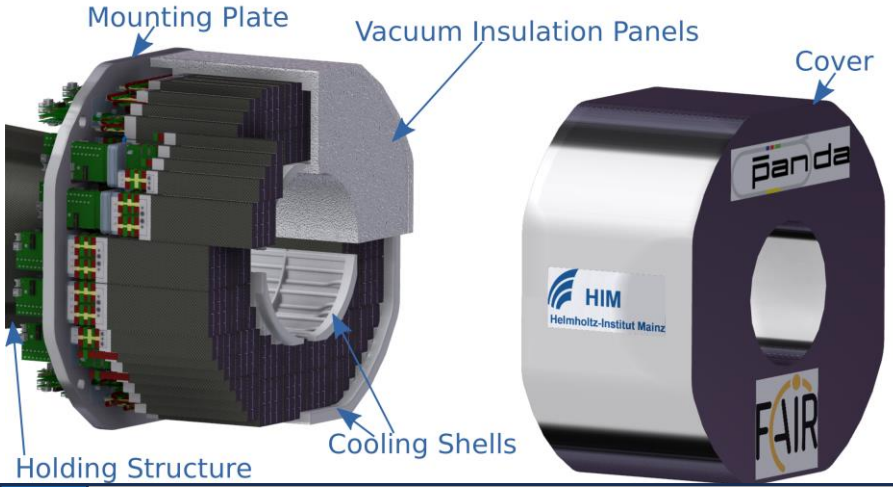
Outline

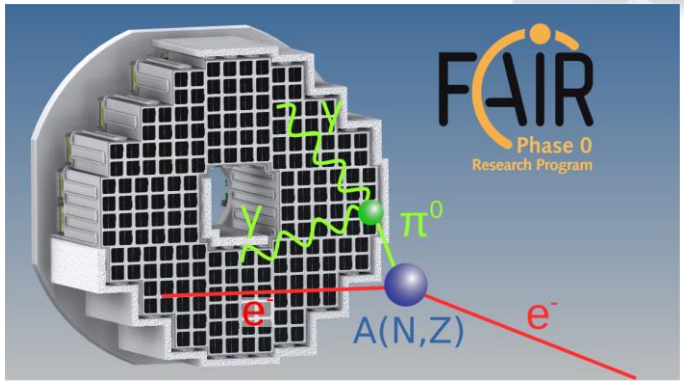
1. The PANDA Phase-0 Experiment at MAMI
2. The Data Acquisition Concept
3. Phase-0 Firmware for SADC
    1. Direct Line Messages
    2. Feature Extraction
    3. Time Sorted Hit Packaging and Triggered Readout
    4. Inter Chip Communication on SADC

FAIR, PANDA and FAIR Phase-0

- Facility for Antiproton and Ion Research (FAIR)
- **antiProton ANnihilation at DArmstadt (PANDA)**
  - **1.5 GeV/c – 15 GeV/c** ($\Delta p/p \sim 10^{-4}$)
  - Fixed target experiment
  - $\mathbf{2 \cdot 10^7}$ $\bar{p}p$ annihilations/second
  - Excellent particle identification
  - Radiation tolerance of the materials







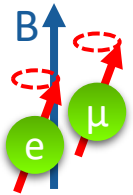
A FAIR Phase-0 Experiment at the Mainz Microtron

The $g_\mu - 2$-Puzzle

$g = \frac{\mu_s}{\mu_L} = \mathbf{2}$, point-like spin-$\frac{1}{2}$ particles (Dirac-Theory)

$a_l = \frac{g_l - 2}{2} = \mathbf{0}$, anomalous magnetic moment

Radiative corrections → $a_l \neq 0$



$$a_\mu^{\mathrm{SM}} = 0.00116591782(43)$$

$$a_\mu^{\mathrm{Exp.}} = 0.00116592061(41)$$

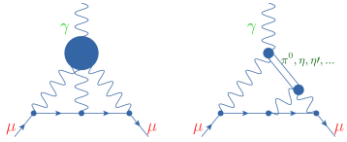
$4.2\,\sigma$

FermiLabs, 2021

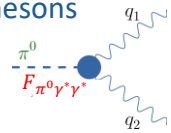
Standard Modell Calculation

$$a_\mu^{\mathrm{SM}} = a_\mu^{\mathrm{QED}} + a_\mu^{\mathrm{EW}} + a_\mu^{\mathrm{QCD}}$$

nonperturbative



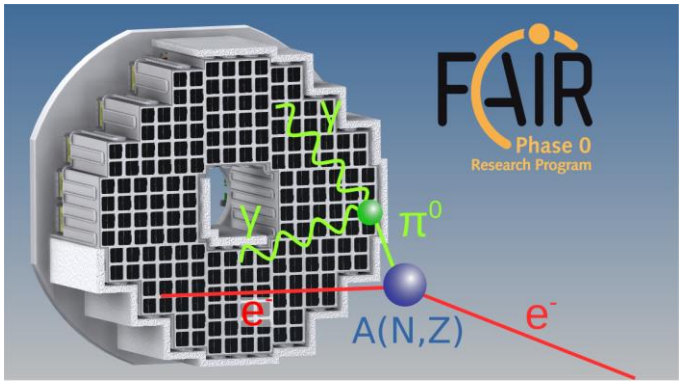
- Hadronic Light-by-Light scattering
- Huge contribution to uncertainty
- Pseudo scalar (PS) mesons π^0, η, η'



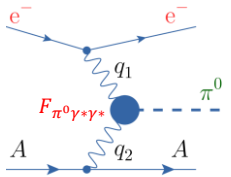
Data-driven approach

$$a_\mu^{HLbL,PS} = \int_0^\infty dQ_1 \int_0^\infty dQ_2 \int_{-1}^{1} d\tau\, w(Q_1, Q_2, \tau) F_{PS\gamma^*\gamma^*}(-Q_1^2, -(Q_1+Q_2)^2) F_{PS\gamma^*\gamma^*}(-Q_2^2, 0)$$

V. Pauk, M. Vanderhaeghen 2014, M. Hoferichter 2018

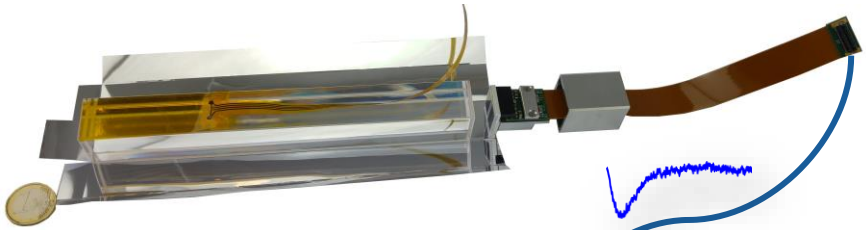


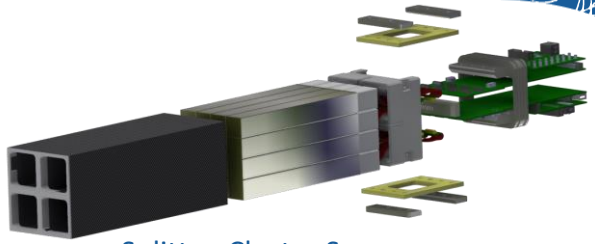
- FAIR Phase-0: FAIR detectors in stand-alone experiments
- PANDA backward calorimeter is completely developed ✓
- Measurement of the double virtual pion transition form factor (TFF) $F_{\pi^0\gamma*\gamma*}$ for spacelike momenta
- Primakoff electroproduction
- A1 experimental hall of Mainz Microtron
- Electron beam on highly charged target



Measurement of the Electromagnetic Transition Form Factor of the π^0 in the Space-Like Region via Primakoff Electroproduction. Letter of Intent, 2020

Signal Digitisation and Processing



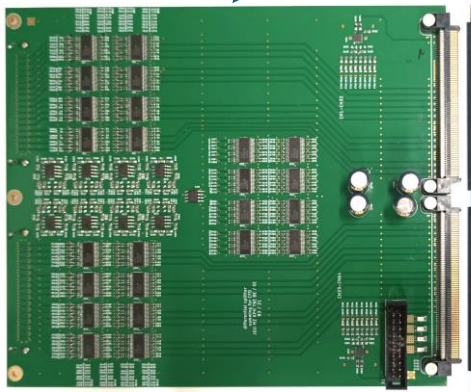


High Voltage and Control

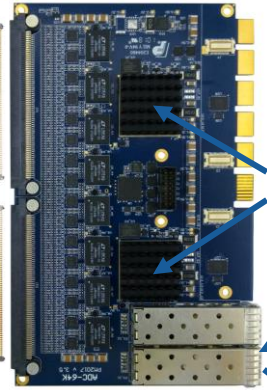
Amplification

Temperature Readout

Splitter, Cluster Sum



PANDA SADC

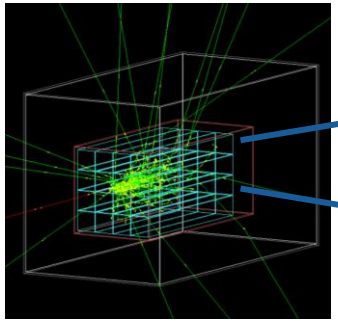


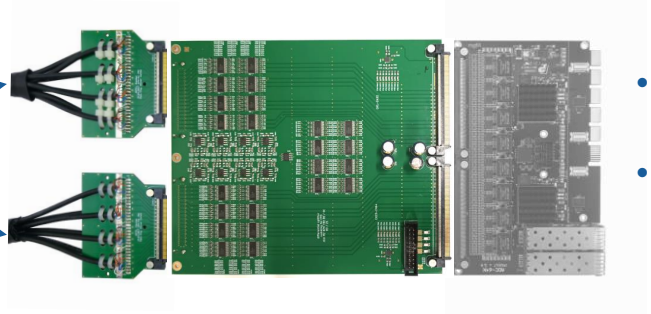
FPGAs

(E, T_0)

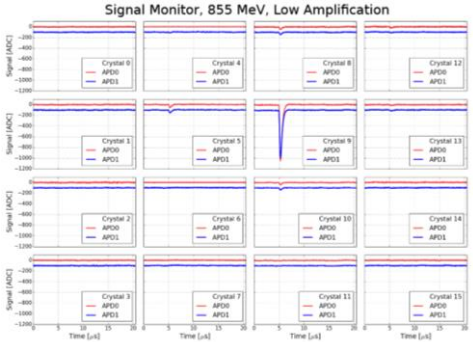
Detector → Amplification → Transmission → Cluster Trigger → ADC → FPGA → Data Concentrator → Compute Nodes

Analogue Cluster Trigger





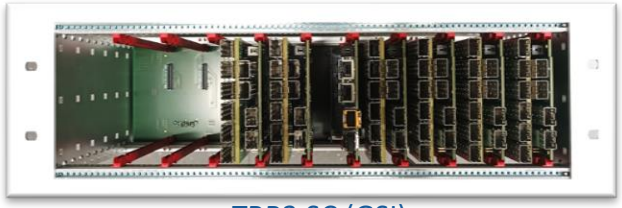
- Splitter, Backplane and CFD tested ✓
- Splitter boards and backplanes in production



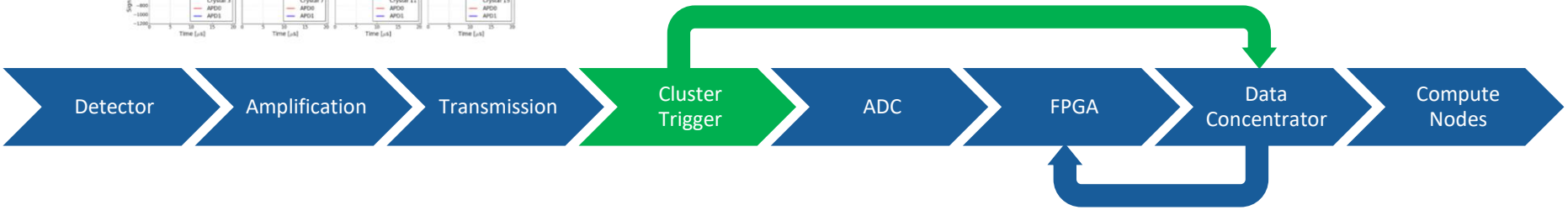
$\sum_{LG=0}^{7}$ → CFD

$\sum_{LG=8}^{15}$ → CFD

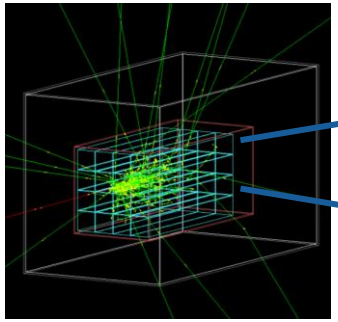
Analogue delay < 200 ns

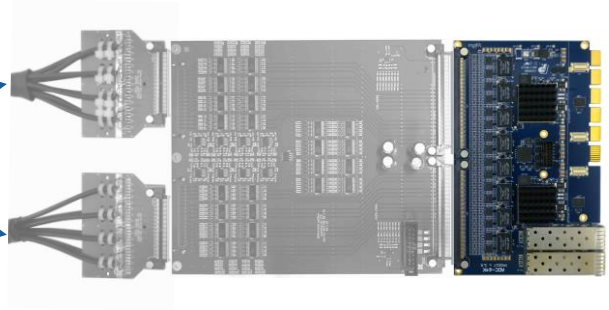


TRB3 SC (GSI)

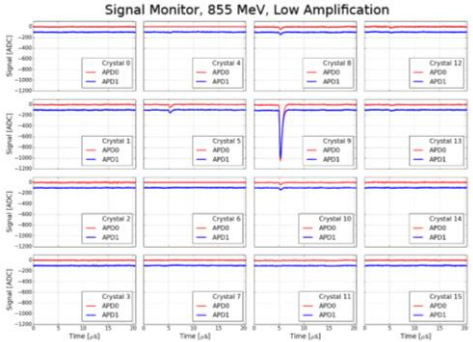


Data Concentrator and Clock/Trigger Distribution





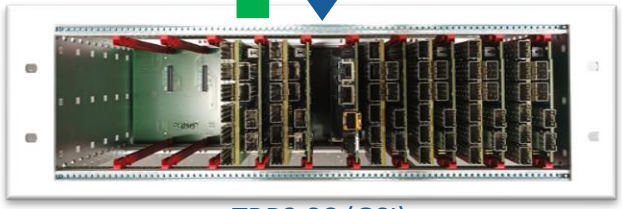
- Digital trigger implemented ✓



$\sum_{LG=0}^{7}$ → CFD

$\sum_{LG=8}^{15}$ → CFD

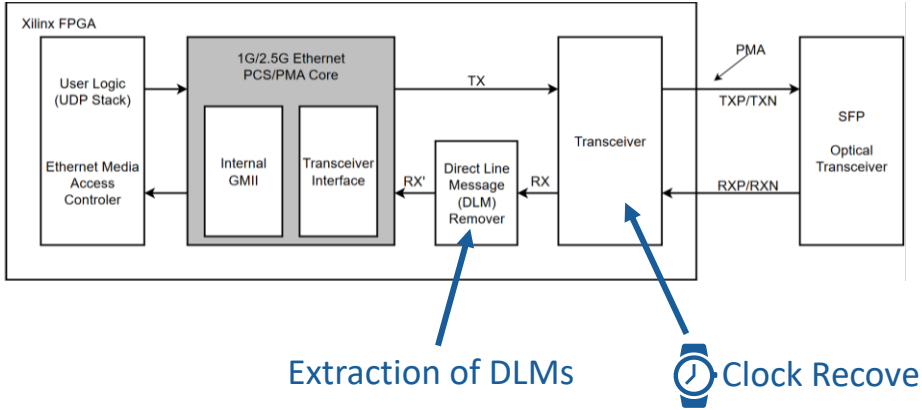
Throughput Time < 200 ns



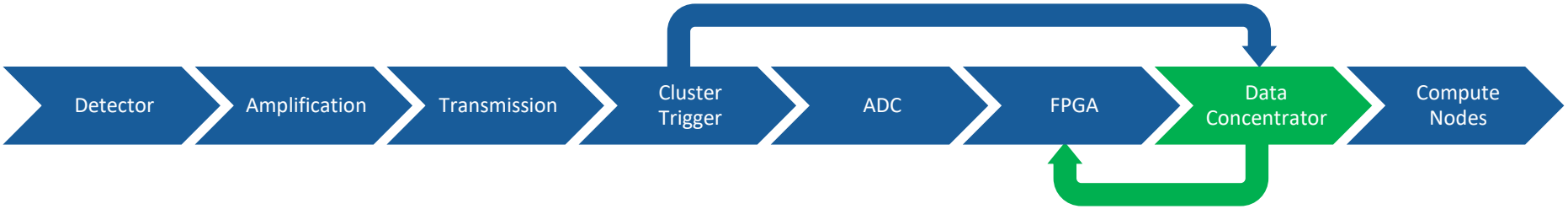
TRB3 SC (GSI)

Detector → Amplification → Transmission → Cluster Trigger → ADC → FPGA → Data Concentrator → Compute Nodes

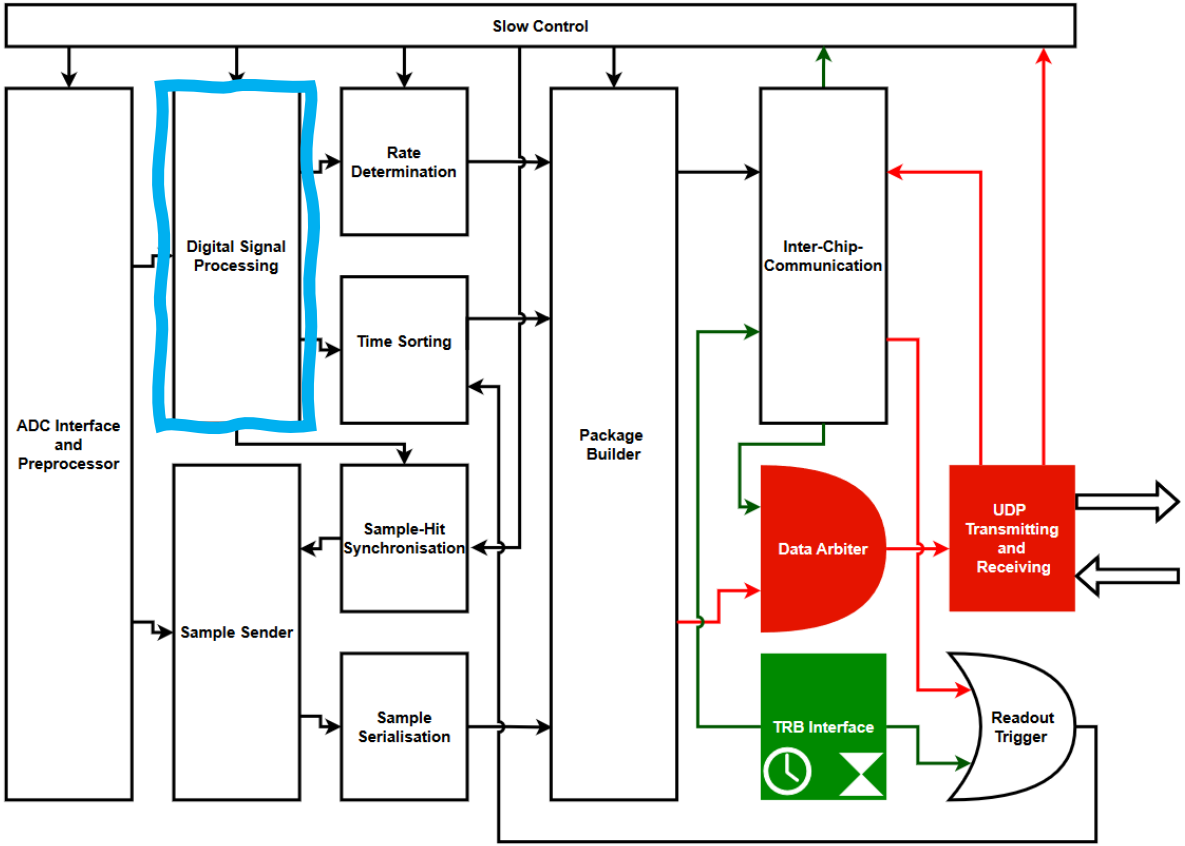
Direct Line Messages (DLMs)



- Need of defined and finite trigger propagation
- Network transport layer (4) is not “direct”
- Utilising control symbols within 8b/10b encoding
- Development of DLM protocol with Michael Böhmer (TU München)
- Many possibilities:
  - Arbitrary payload
  - Different trigger types
  - Synchronous resets
  - …
- Core features implemented on SADC ✓



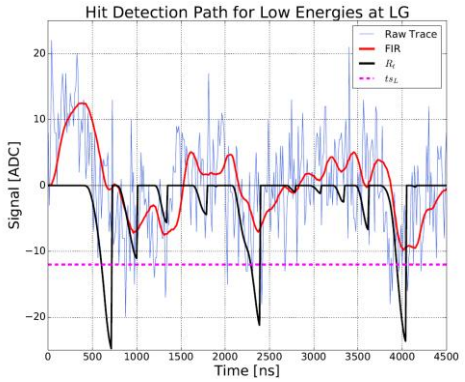
SADC Firmware



- Reminder of feature extraction methods
- PANDA EMC Session February 2024

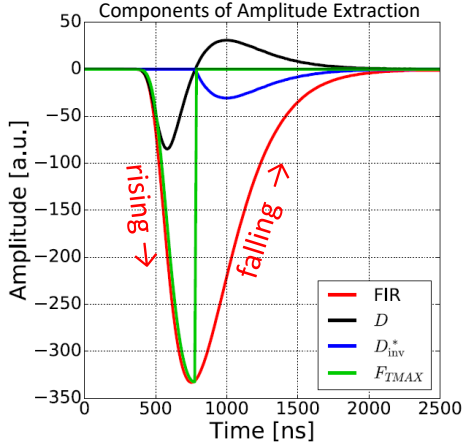
Digital Pulse Identification and Parameter Extraction on FPGA

Identification



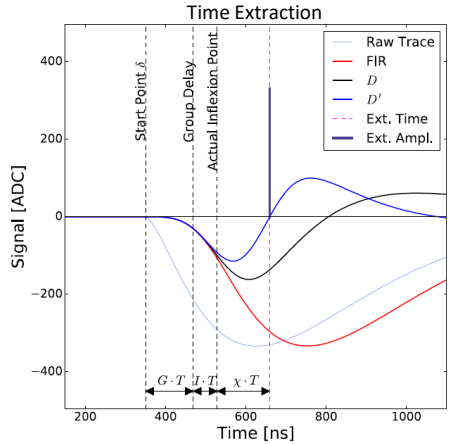
- FIR filter
- Extraction function
- Highly sensitive on pulse shape
- Improvement of detection efficiency (small energies!)

Digital Pulse Shaping



- Derivation → Integration
- Built-in baseline follower
- Elimination of falling edge
- Pileup detection and correction

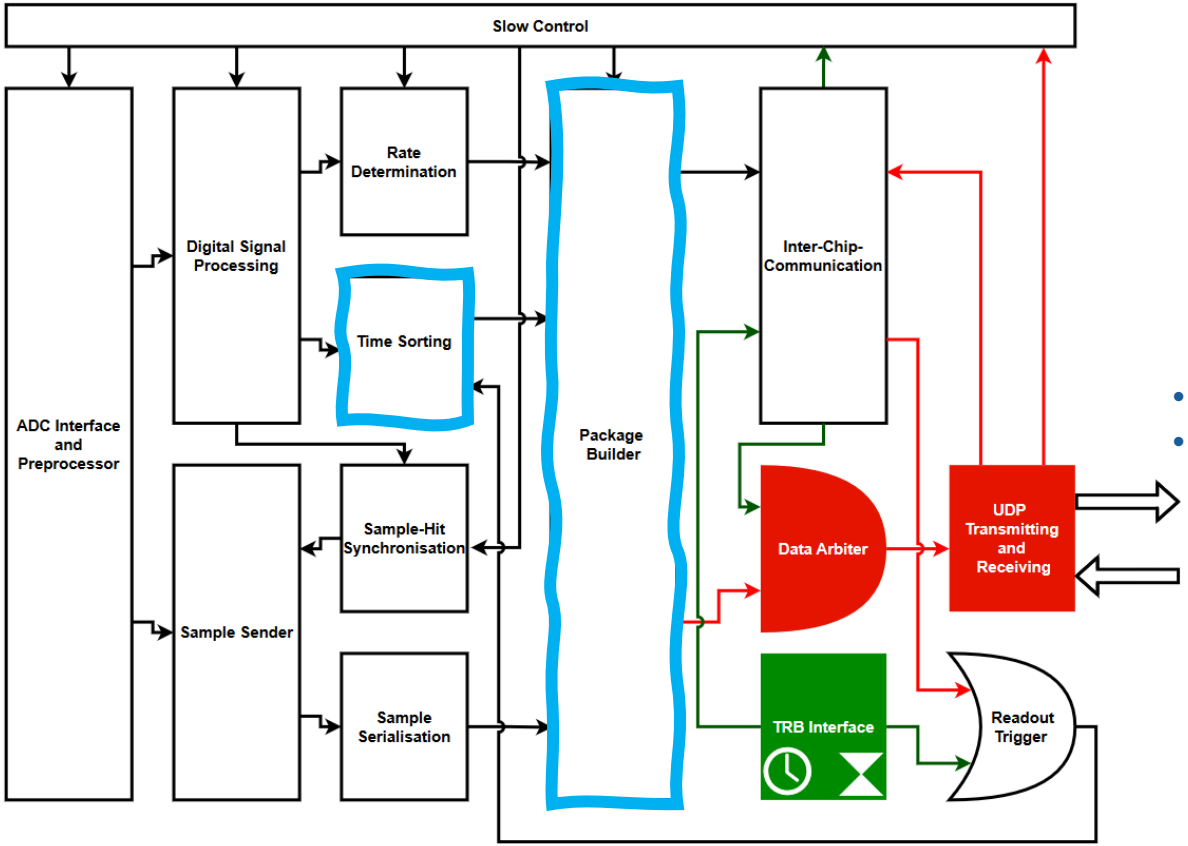
Time



- T_0 at inflexion point ($f''(x) = 0$)
- Discrete derivation → Interpolation

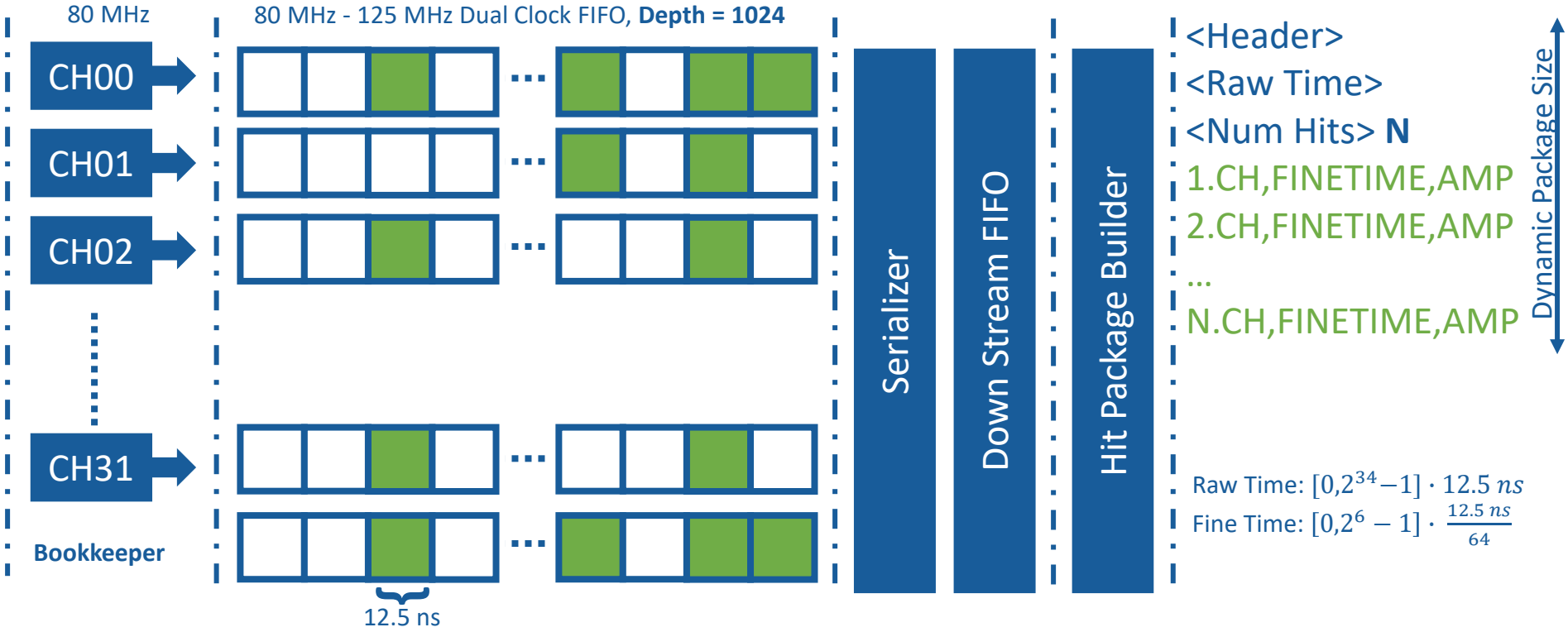
Detector → Amplification → Transmission → Cluster Trigger → ADC → FPGA → Data Concentrator → Compute Nodes

SADC Firmware



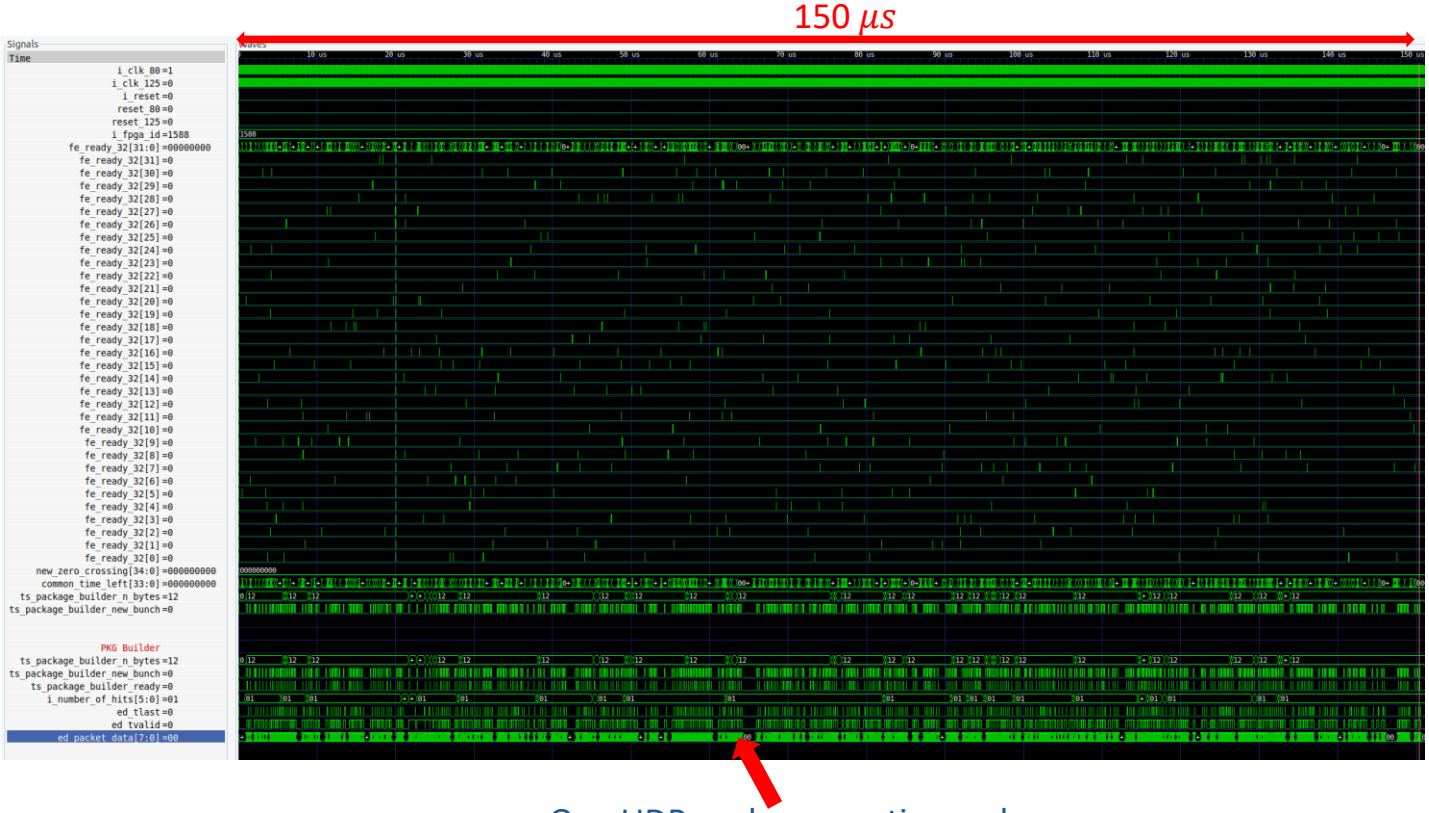
- Optimisation of time sorted hit packaging
- Implementation of triggered readout ✓

Time Sorted Hit Packaging on FPGA



Detector → Amplification → Transmission → Cluster Trigger → ADC → **FPGA** → Data Concentrator → Compute Nodes

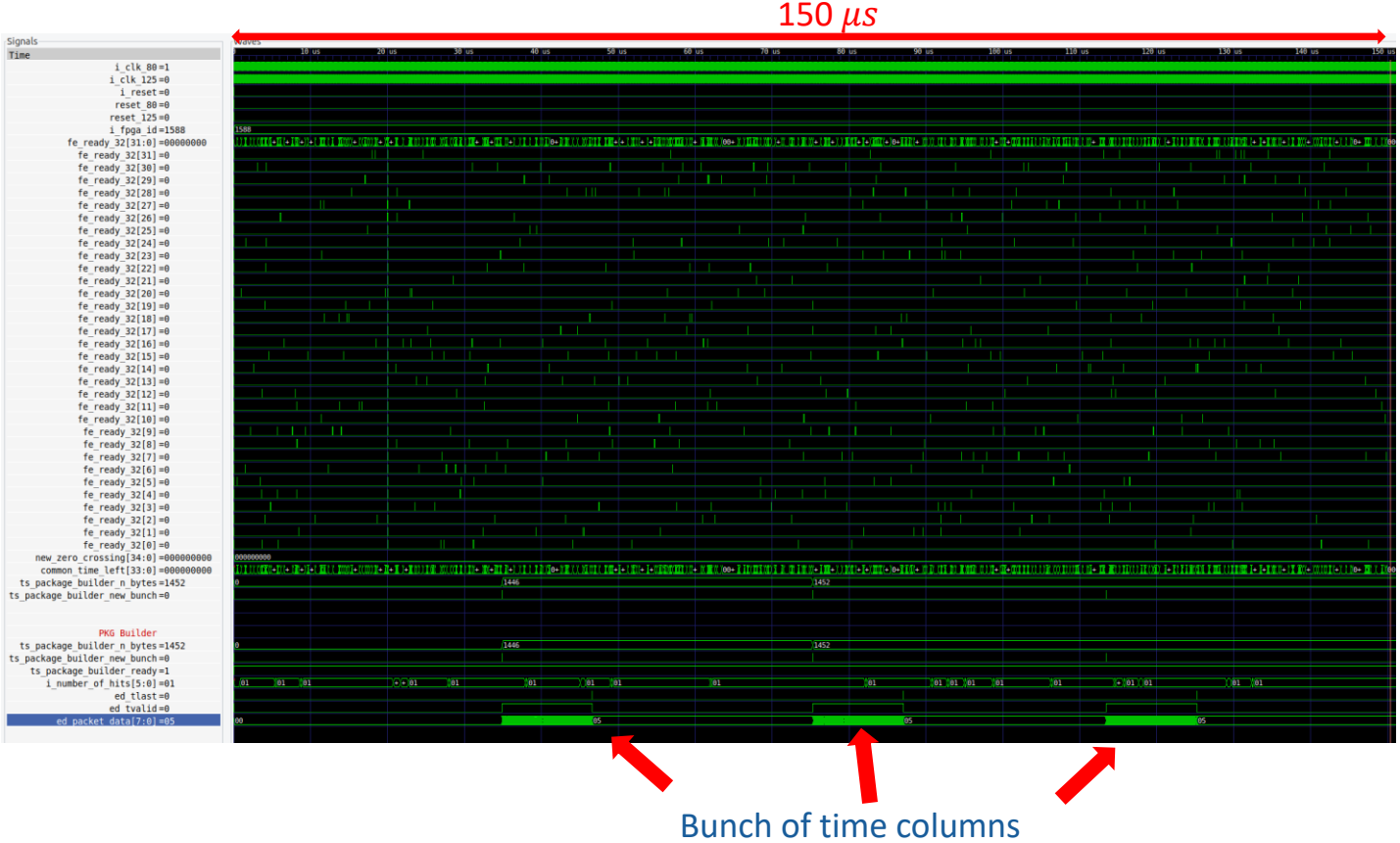
Time Sorted Hit Packaging on FPGA



One UDP package per time column

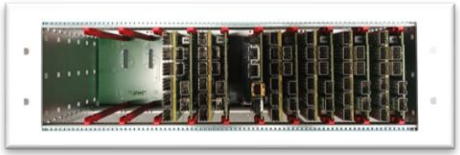
- Working and tested implementation
- Huge improvement for cluster building algorithm in analysis
- Busy TX lane

Time Sorted Hit Packaging on FPGA – Compression Mode



- Filling package with time columns up to UDP payload limit
- Or: timeout [0:65535] ns
- Timeout = 0 ns → former case
- Working and tested implementation
- Measured free streaming capability:
  - 310 kHz / channel
  - 19.84 MHz / SADC
  - Trace monitor
  - Rate monitor
  - Config monitor

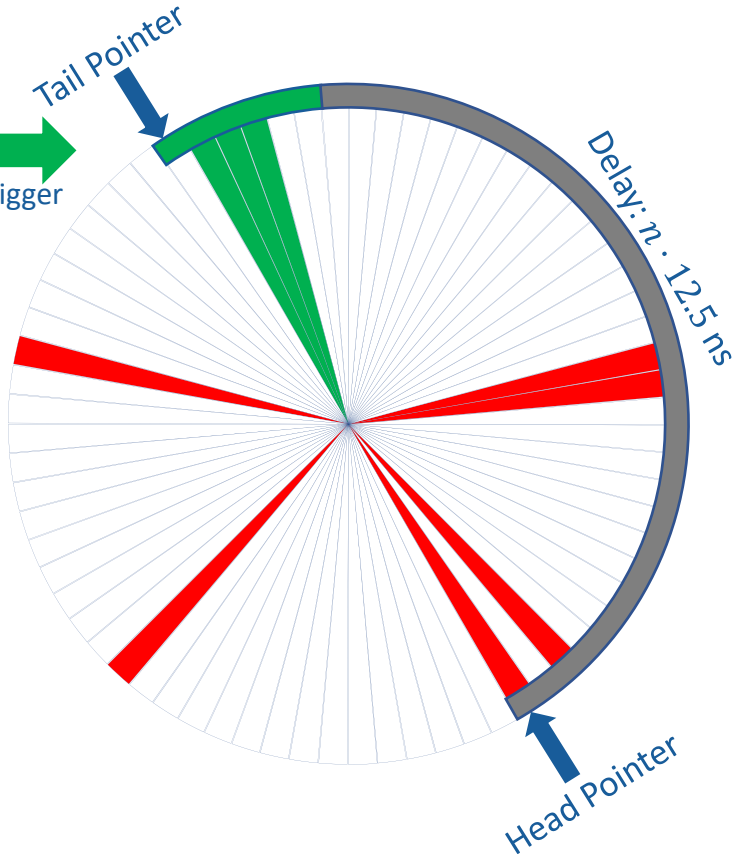
Time Sorted Hit Packaging on FPGA – Triggered Readout



Data Concentrator TRB3 SC (GSI)

DLM

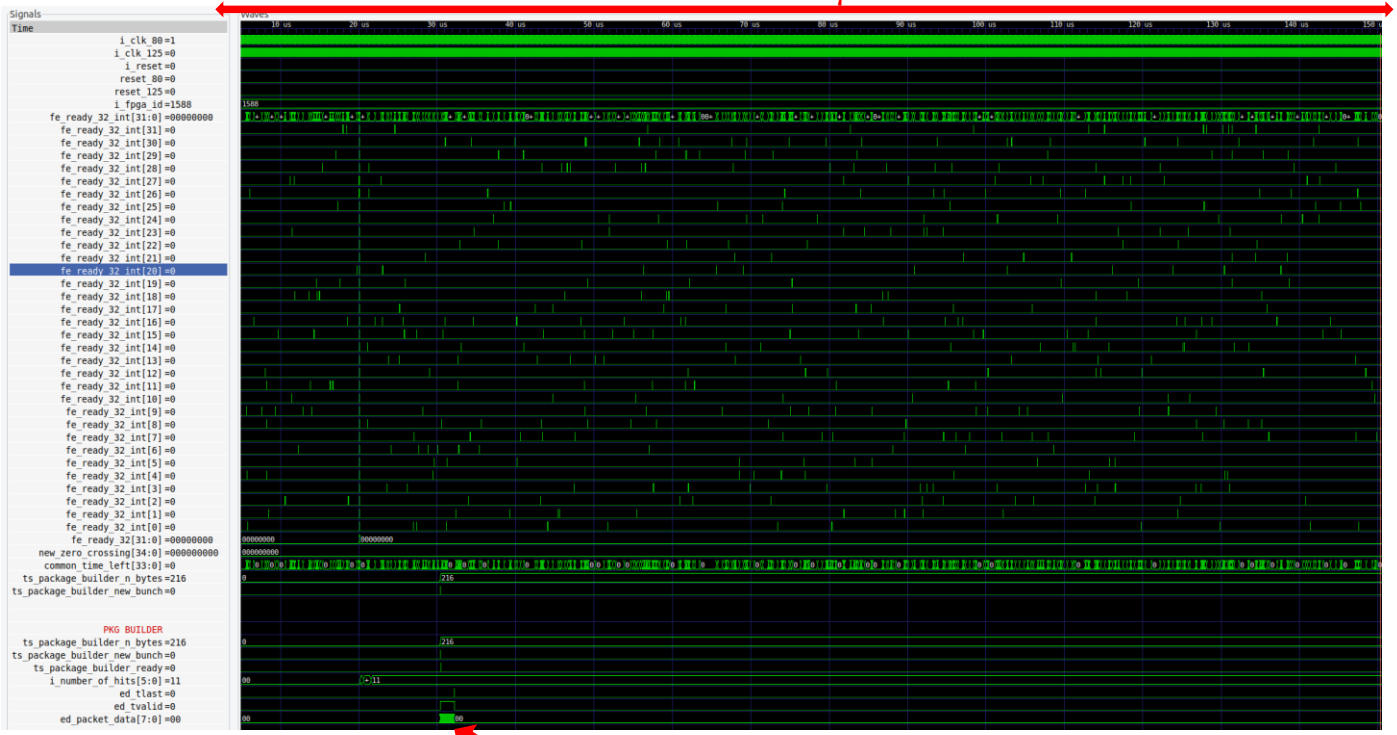
Readout Trigger



- Readout trigger from TRB3 SC
- Configurable delay on SADC (trigger → gate open)
- Configurable gate length on SADC

Time Sorted Hit Packaging on FPGA – Triggered Readout

150 μs

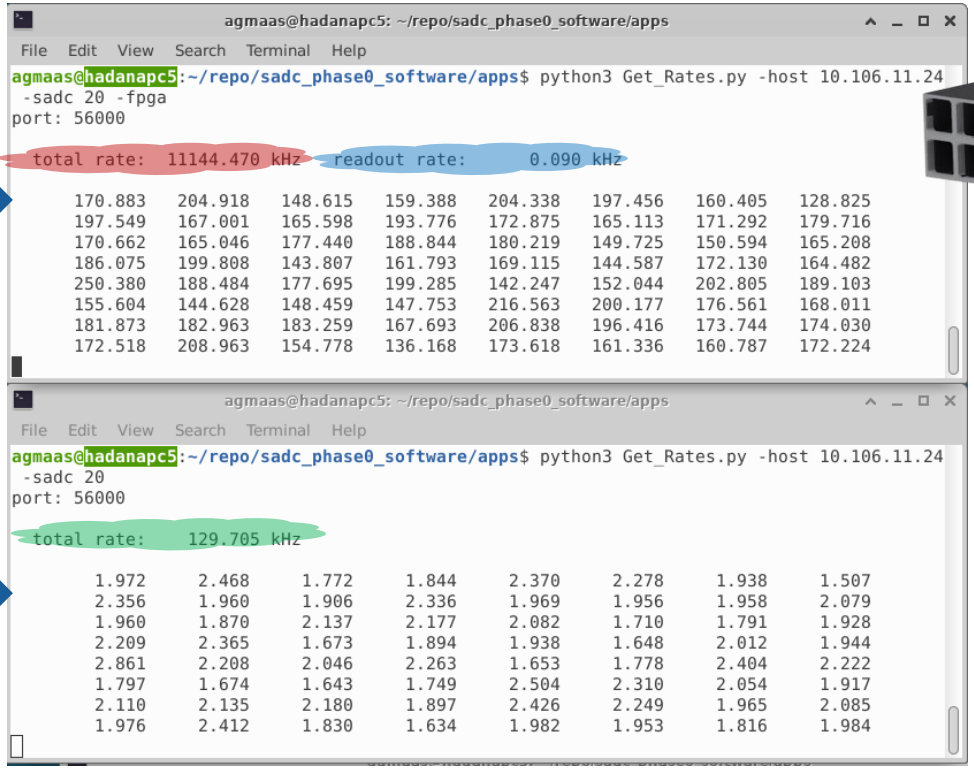


Bunch of time columns within 100 ns gate

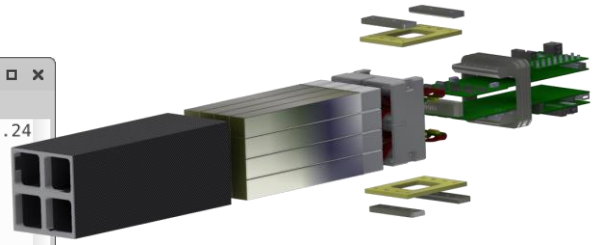
- Sending only time columns within gate after trigger
- Dramatically decrease of network load
- System is still internally “free streaming”

Time Sorted Hit Packaging on FPGA – Triggered Readout

SADC-Rate



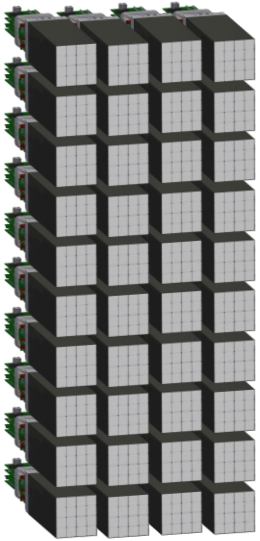
Receiver-Rate



- Sending only time columns within gate after trigger
- Dramatically decrease of network load
- System is still internally “free streaming”

PANDA Phase-0 Data Acquisition – Data Flow

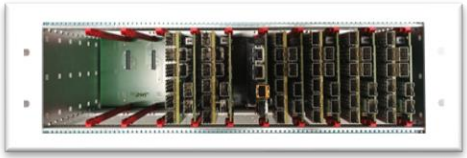
- 640 Crystals
- 1280 APDs



- 40 SADCs
- 2560 Channels

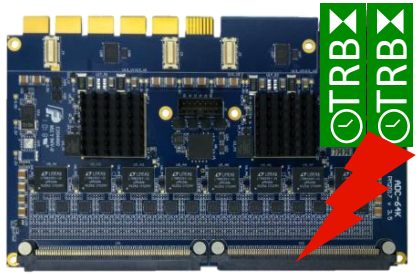
80 links

- TRB3 SC
  - Clock
  - Trigger



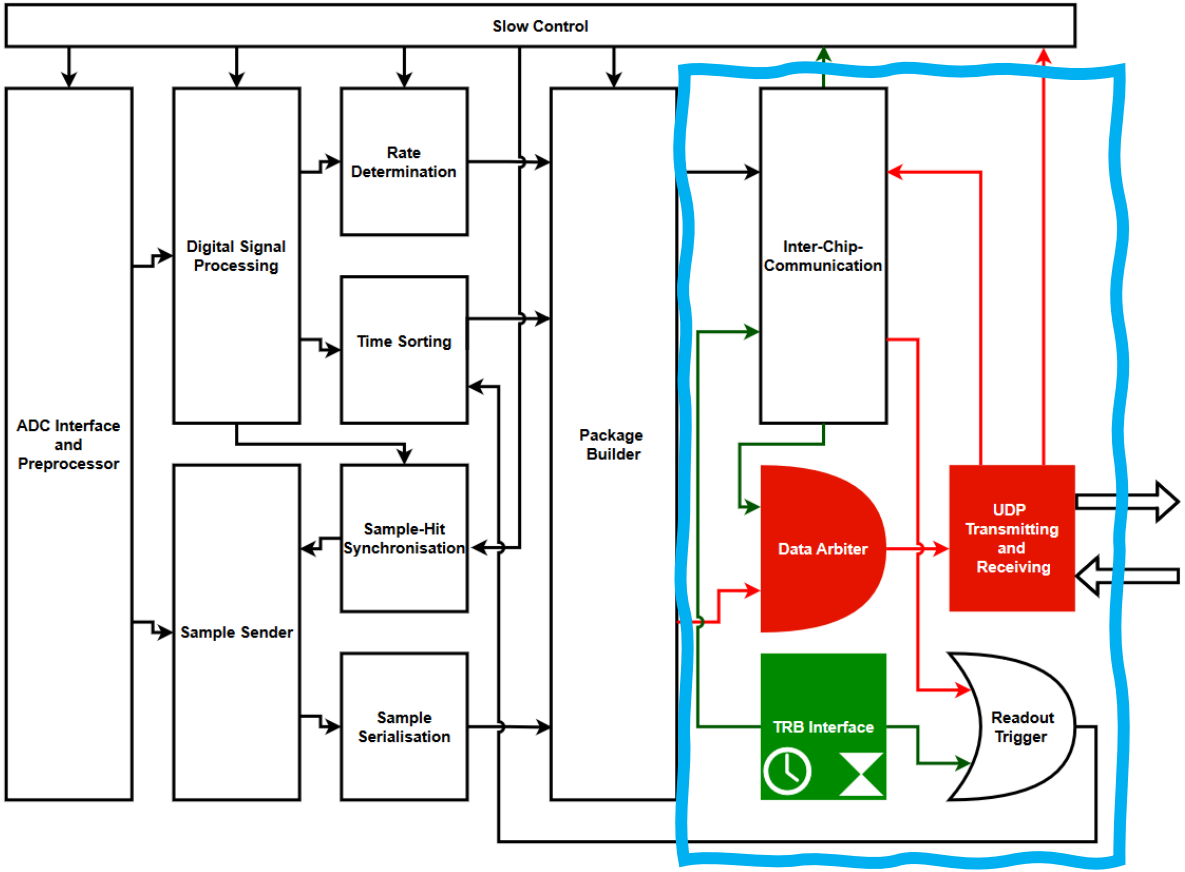
90 links

- One master board
- Nine slave boards with 10 links each
- But data transmitted via backplane at 1 Gbit/s

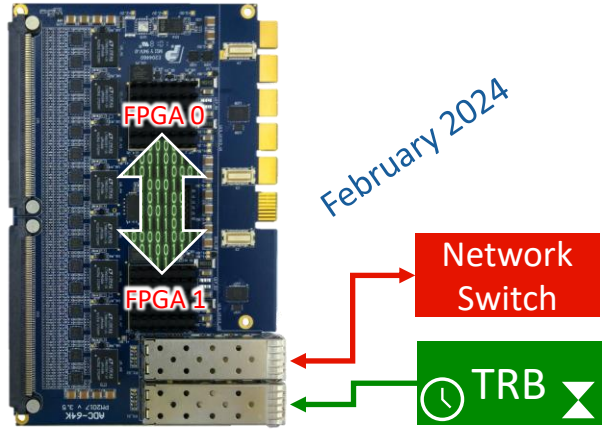


- Data of all SADCs can't flow over TRB backplane
- Are 80 links needed?

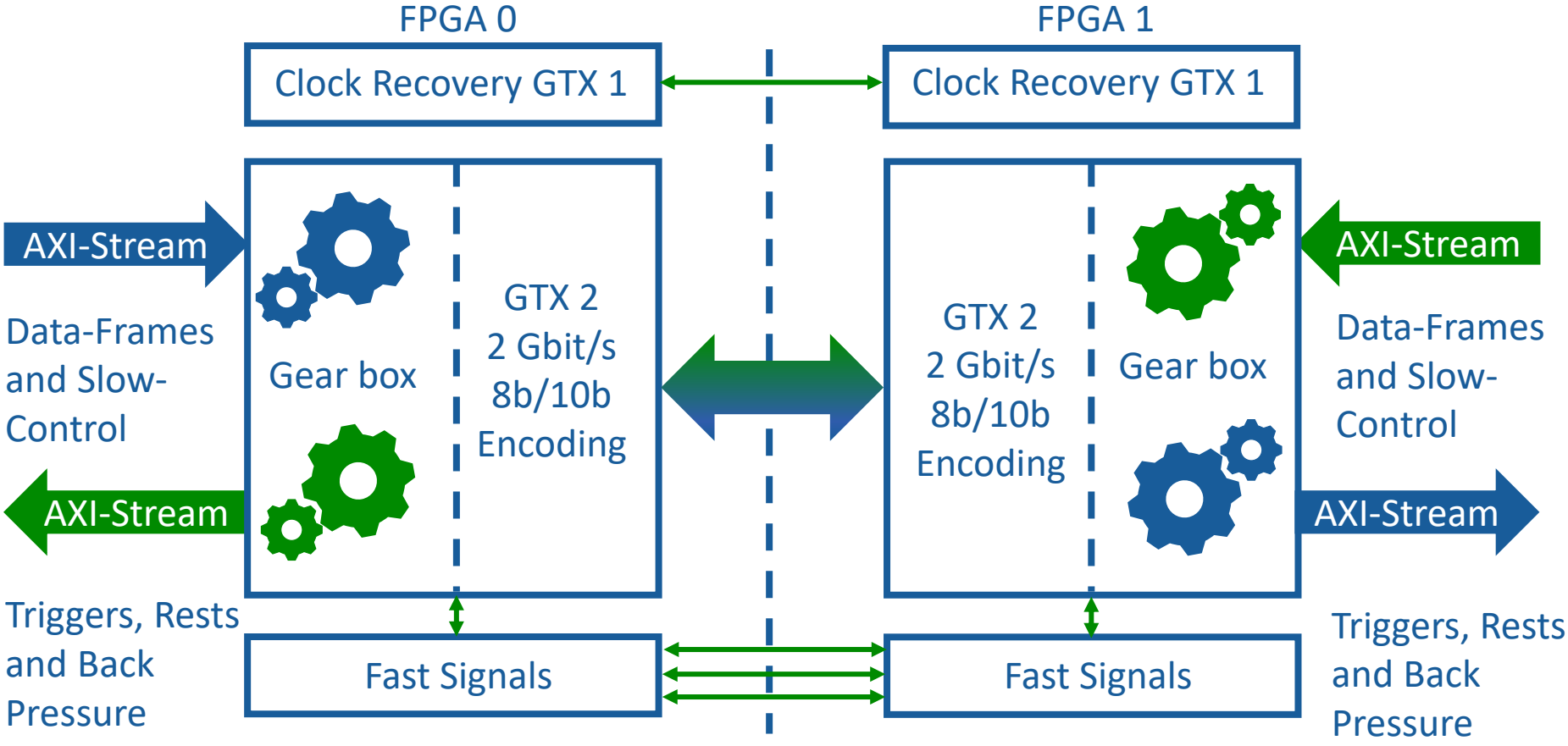
SADC Firmware



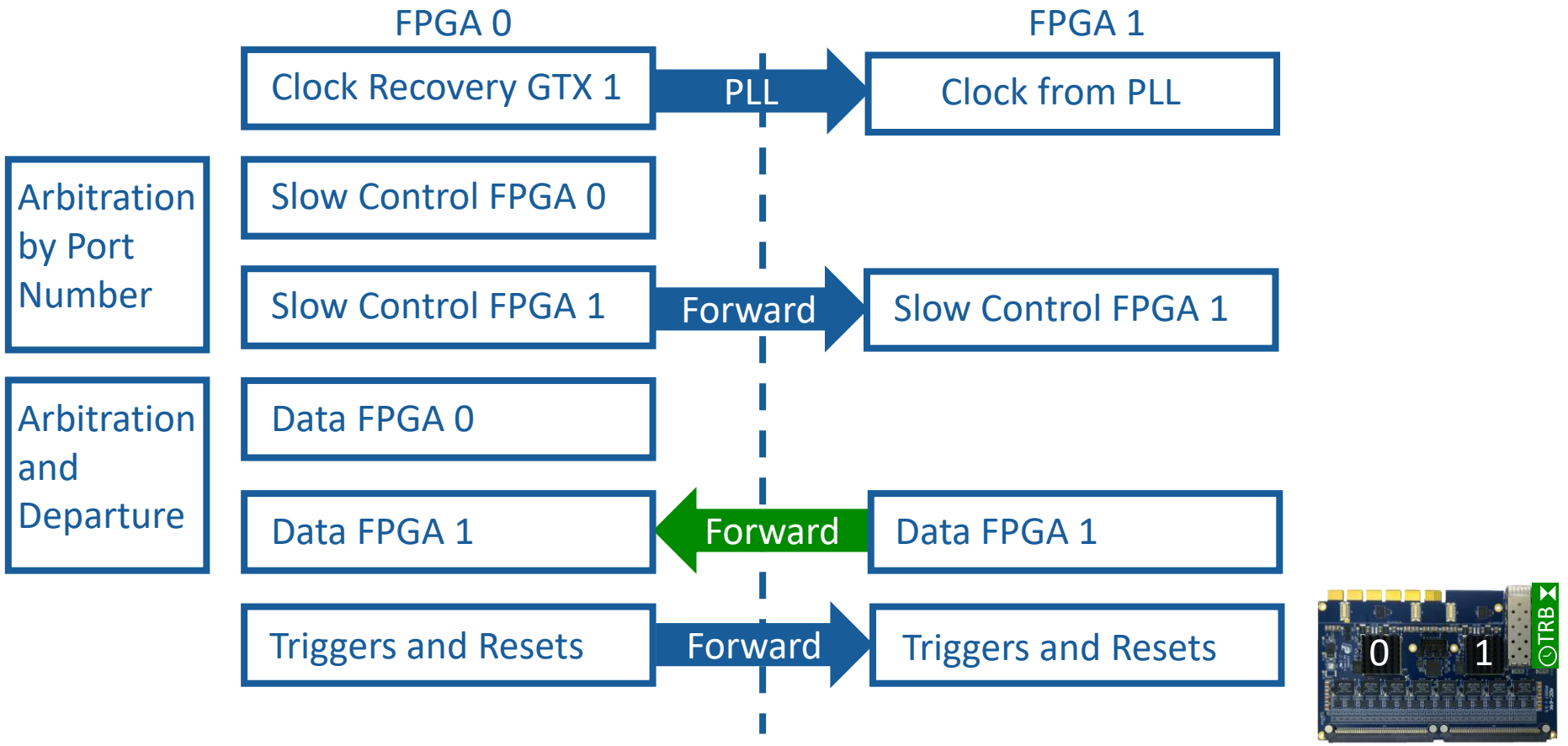
- Blocks in black: active on both FPGAs
- Block in green: active on FPGA connected to TRB3 SC
- Blocks in red: active on FPGA connected to network switch
- **Same firmware for both FPGAs**
- Behaviour is determined by GEO-Address and configuration



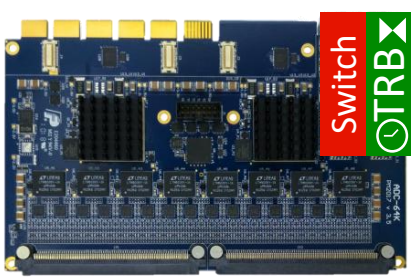
SADC Firmware – Inter Chip Communication

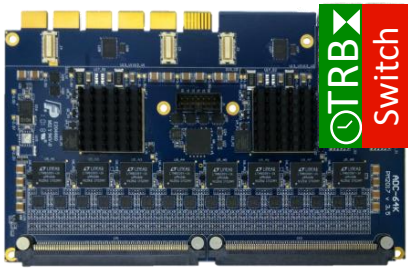


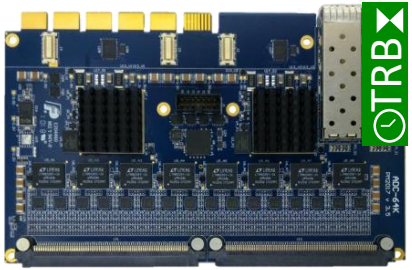
SADC Firmware – Inter Chip Communication Routing Example

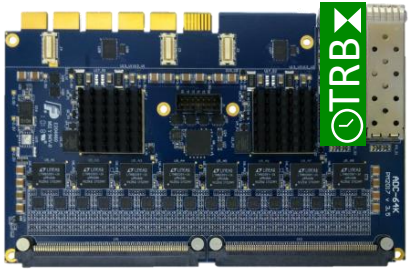


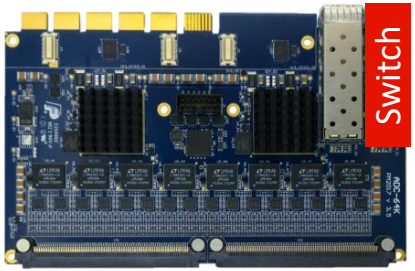
SADC Firmware – Inter Chip Communication

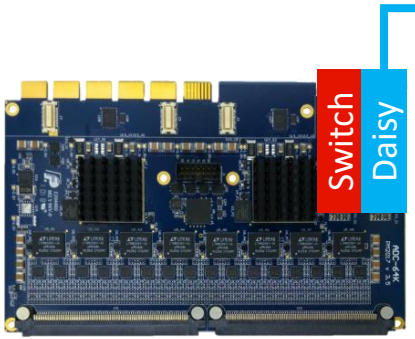


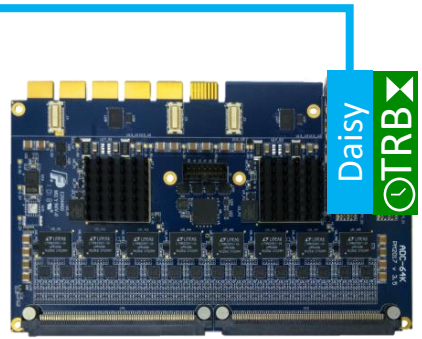






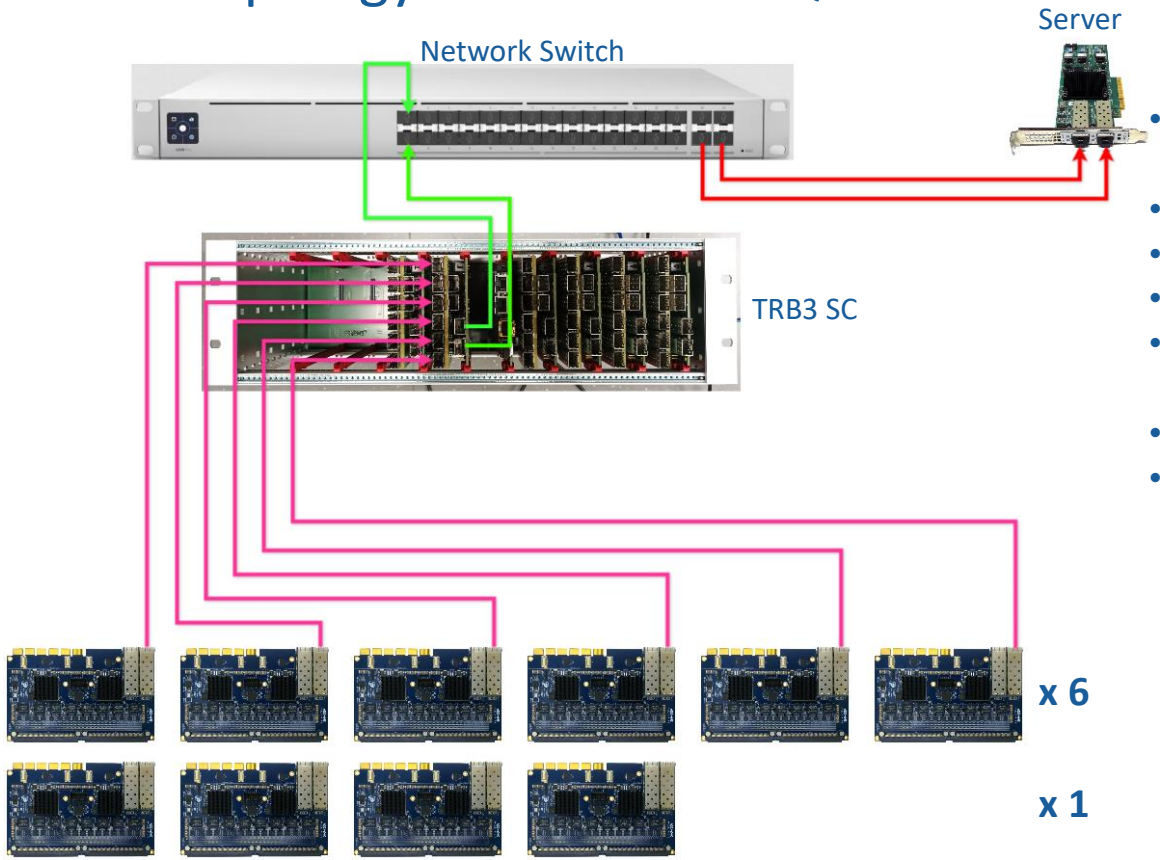






- Many routing possibilities
- Theoretically even at runtime…
- Load balancing (?)

Network Topology – Phase-0 DAQ

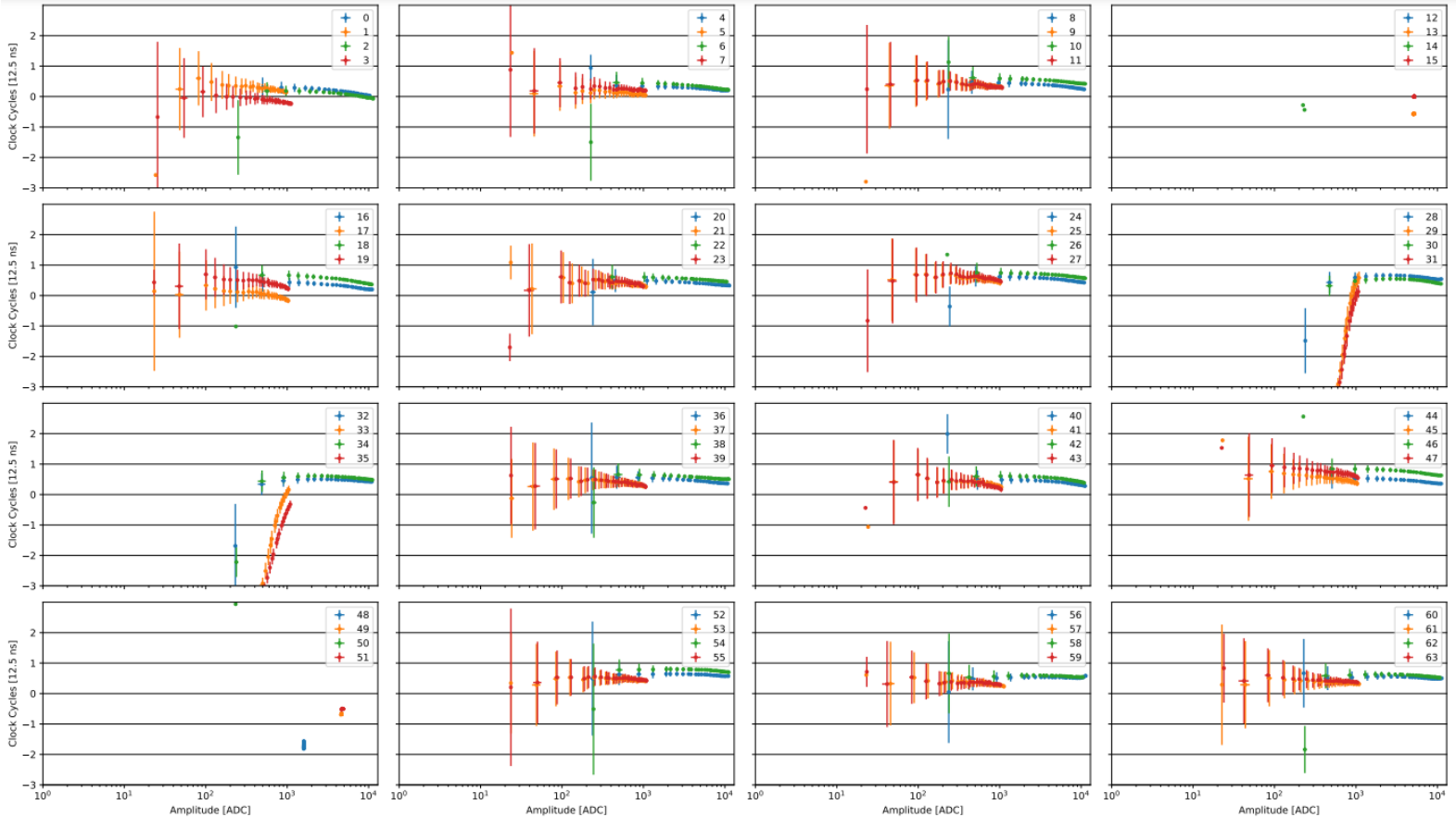


- Single link readout of SADCs
  - Free streaming: ~**150 kHz/Channel**
- Seven TRB slave cards
- Two uplinks per TRB slave
- Uplink addressing via VLAN ID
- Maximum bandwidth: 14 Gbit/s
  - Free streaming: ~**50 kHz/Channel**
- Two 10 Gbit/s uplinks to server
- Phase-0 conditions:
  - Event hit rate: **200 kHz/Channel**
  - Trigger rate: **100 kHz**
  - Gate width: **100 ns**
  - Rate reduction factor: **100**
  - Readout rate: **2 kHz/Channel**

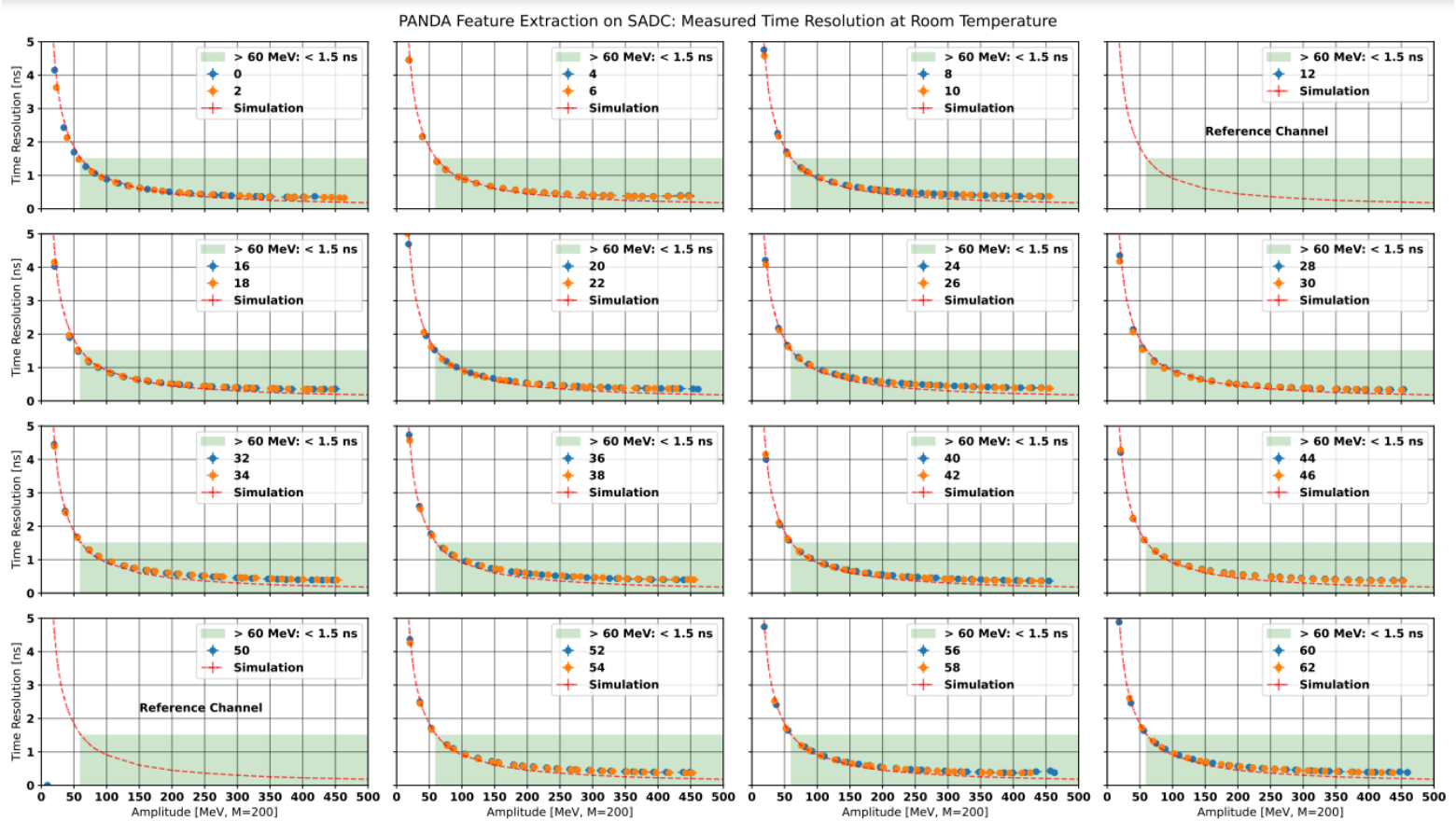
Phase-0 DAQ Status

- DAQ hardware is ready
- > 40 SADCs with unique DNA-ID (thanks to Gießen and single link readout)
- SADC Phase-0 firmware is finished
  - Feature extraction optimised on calorimeter signals (2020) ✓
  - All non-hit data at any time (traces, rates and config packages) (2021) ✓
  - Internal (auto) request modus for traces, rates and config packages (2023)
  - Time sorted hit packaging for efficient event building (2023) ✓
  - Hit package compression to optimise bandwidth consumption (2023) ✓
  - Clock recovery from TRB 3 SC (2023) ✓
  - Triggered readout via “Direct Line Messages” (TRB 3 SC) (2024) ✓
  - VLAN to optimise upstream capability (2024) ✓
  - Traces have timestamps to connect traces with hit data (new) ✓
  - Inter-Chip communication to optimise resource consumption (new) ✓
    - Arbitrary network topologies possible
    - Only one SADC firmware needs to be maintained
  - Trigger pipeline and gate generator for triggered readout (new) ✓
  - Gießen and Mainz joint venture beam time July 2024
    - Test Gießen detector with Mainz Phase-0 DAQ at A2
    - Complete Phase-0 readout chain

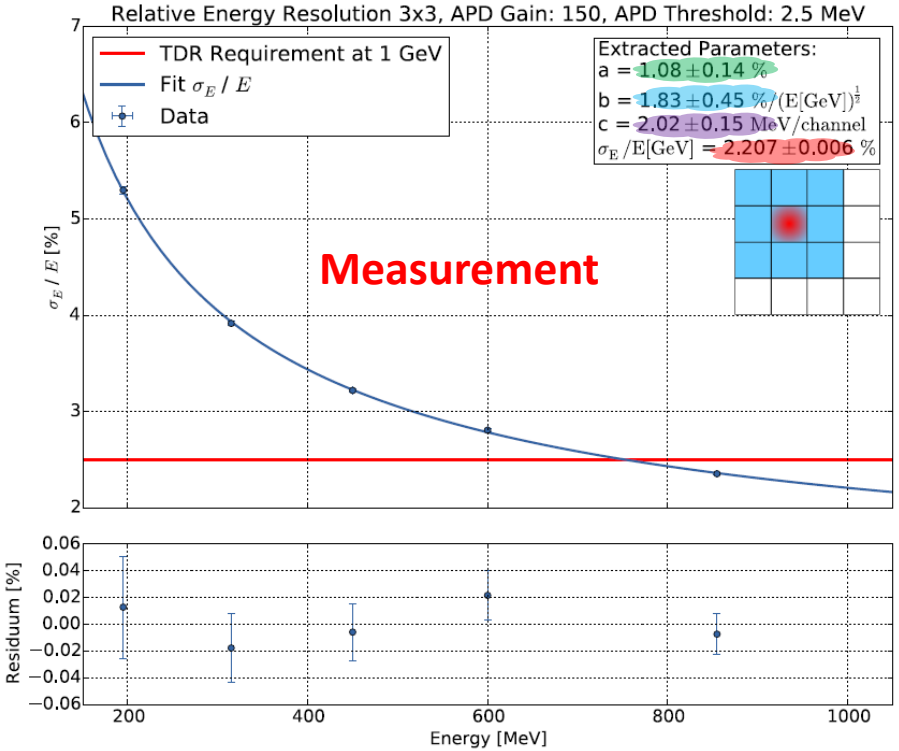
ADC Alignment and T0 Walk



Time Resolution at Room Temperature



Digital Pulse Identification and Parameter Extraction - Performance



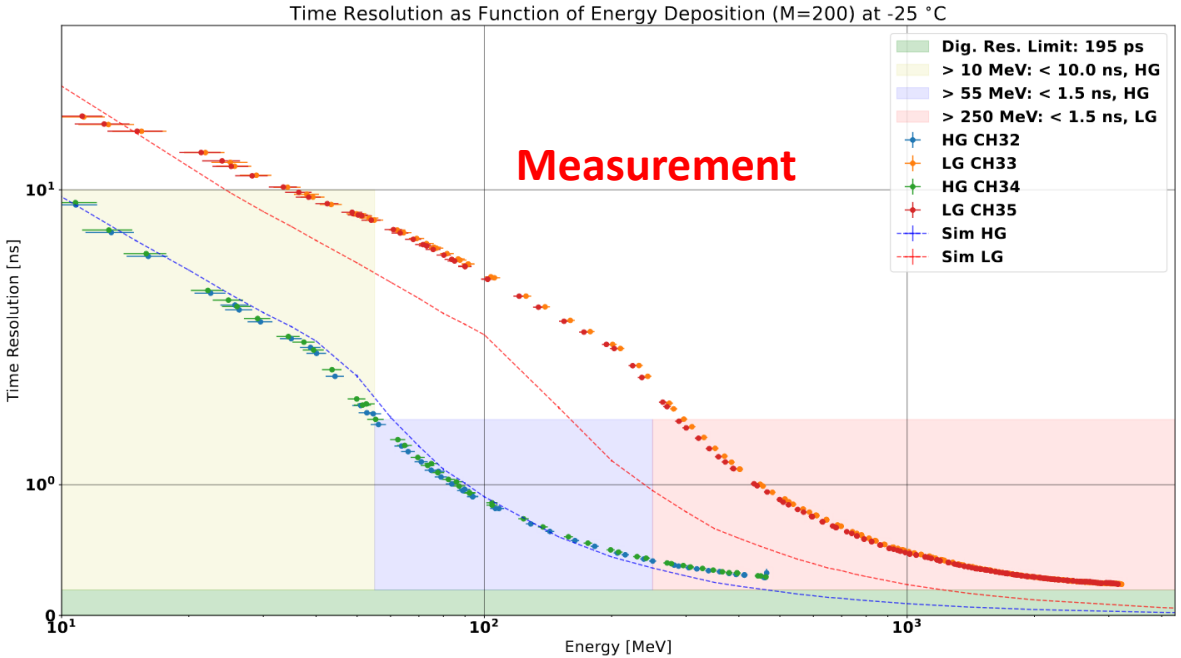
- Relative Energy Resolution (2018)

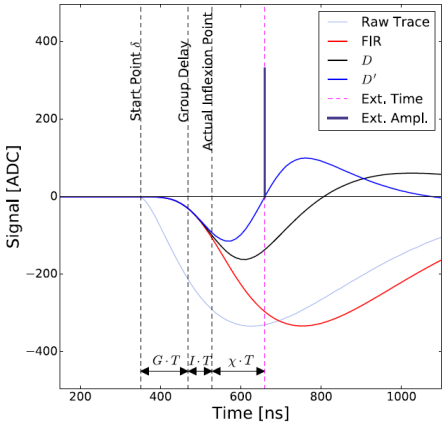
$$\frac{\sigma_E}{E} = \underbrace{a}_{\text{Constant}} \oplus \underbrace{\frac{b}{\sqrt{E}}}_{\text{Stochastic}} \oplus \underbrace{\frac{c}{E}}_{\text{Noise}} = \sqrt{a^2 + \frac{b^2}{E} + \frac{c^2}{E^2}}$$

PANDA Technical Design Report (TDR) requirements:

- $a_{\mathrm{TDR}} \leq 1\%$ ✓
- $b_{\mathrm{TDR}} \leq 2\,\frac{\%}{\sqrt{\mathrm{GeV}}}$ ✓
- $c_{\mathrm{TDR}} \leq 3\ \mathrm{MeV}$ ✓
- $\sigma_E/E(1\ \mathrm{GeV})_{\mathrm{TDR}} \leq 2.5\%$ ✓

Digital Pulse Identification and Parameter Extraction - Performance



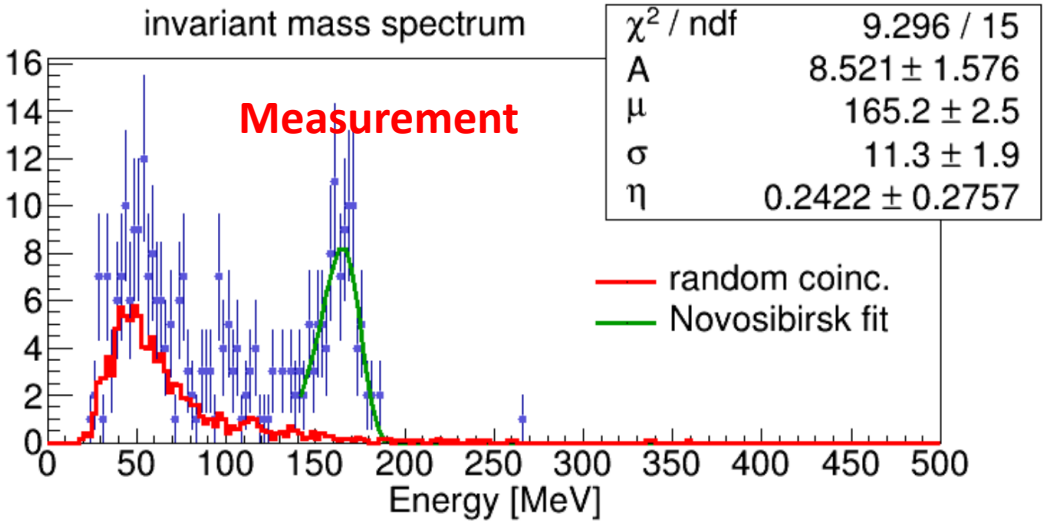


- Light pulser measurement (2024)
- Measurement in agreement with simulation (High Gain)
- Discrepancy between measurement and simulation for Low Gain due to digital resolution limitations
- But < 1 ns at the relevant region

Hit ready																	
Time left			i_0 (34-bit)														
Hit data	Amplitude (16-bit)					Dividend (10-bit)						Divisor (10-bit)					
Assignment	35	34	33	...	20	19	18	...	12	11	10	9	8	...	2	1	0

Table 1. Output of the digital signal processing unit of one ADC channel for one hit.

Digital Pulse Identification and Parameter Extraction - Performance



Back then:

- Measurement of neutral pion decay with two 4x4 prototypes in 2022
- Synchronisation with light pulser
- Energy calibration not optimal

Today:

- Now synchronisation with TRB3 SC
- Well calibrated subunits for Phase-0

Unique DNA-ID

```
##################################################################################################################
# This file was auto generated by sadc_data_logic/conf_from_dna/generate_levb_config.py                          #
# Config file name: config_mainz_mac.txt                                                                         #
# Time of creation: 21/06/2024 14:55:49                                                                          #
# Help: ernoll@uni-mainz.de                                                                                      #
##################################################################################################################

#SADC_No Interface  Interface_IP     SADC_MAC      SADC_IP         Default_Port FPGA1_ID FPGA2_ID VLAN_TCI Receiver_Server_port
00       ens4f0     192.168.030.001 cafebabe0001  192.168.030.011 50020        00       01       00       56000
01       ens4f0     192.168.030.001 cafebabe0002  192.168.030.012 50020        02       03       00       56000
02       ens4f0     192.168.030.001 cafebabe0003  192.168.030.013 50020        04       05       00       56000
03       ens4f0     192.168.030.001 cafebabe0004  192.168.030.014 50020        06       07       00       56000
04       ens4f0     192.168.030.001 cafebabe0005  192.168.030.015 50020        08       09       00       56000
05       ens4f0     192.168.030.001 cafebabe0006  192.168.030.016 50020        10       11       00       56000
06       ens4f0     192.168.030.001 cafebabe0007  192.168.030.017 50020        12       13       00       56000
07       ens4f0     192.168.030.001 cafebabe0008  192.168.030.018 50020        14       15       00       56000
08       ens4f0     192.168.030.001 cafebabe0009  192.168.030.019 50020        16       17       00       56000
09       ens4f0     192.168.030.001 cafebabe000a  192.168.030.020 50020        18       19       00       56000
10       ens4f0     192.168.030.001 cafebabe000b  192.168.030.021 50020        20       21       00       56000
11       ens4f0     192.168.030.001 cafebabe000c  192.168.030.022 50020        22       23       00       56000
12       ens4f0     192.168.030.001 cafebabe000d  192.168.030.023 50020        24       25       00       56000
13       ens4f0     192.168.030.001 cafebabe000e  192.168.030.024 50020        26       27       00       56000
14       ens4f0     192.168.030.001 cafebabe000f  192.168.030.025 50020        28       29       00       56000
15       ens4f0     192.168.030.001 cafebabe0010  192.168.030.026 50020        30       31       00       56000
16       ens4f0     192.168.030.001 cafebabe0011  192.168.030.027 50020        32       33       00       56000
17       ens4f0     192.168.030.001 cafebabe0012  192.168.030.028 50020        34       35       00       56000
18       ens4f0     192.168.030.001 cafebabe0013  192.168.030.029 50020        36       37       00       56000
19       ens4f0     192.168.030.001 cafebabe0014  192.168.030.030 50020        38       39       00       56000
20       ens4f0     192.168.030.001 cafebabe0015  192.168.030.031 50020        40       41       00       56000
21       ens4f0     192.168.030.001 cafebabe0016  192.168.030.032 50020        42       43       00       56000
22       ens4f0     192.168.030.001 cafebabe0017  192.168.030.033 50020        44       45       00       56000
23       ens4f0     192.168.030.001 cafebabe0018  192.168.030.034 50020        46       47       00       56000
24       ens4f0     192.168.030.001 cafebabe0019  192.168.030.035 50020        48       49       00       56000
25       ens4f0     192.168.030.001 cafebabe001a  192.168.030.036 50020        50       51       00       56000
26       ens4f0     192.168.030.001 cafebabe001b  192.168.030.037 50020        52       53       00       56000
27       ens4f0     192.168.030.001 cafebabe001c  192.168.030.038 50020        54       55       00       56000
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38       ens4f0     192.168.030.001 cafebabe0024  192.168.030.049 50020        76       77       00       56000
39       ens4f0     192.168.030.001 cafebabe0025  192.168.030.050 50020        78       79       00       56000
40       ens4f0     192.168.030.001 cafebabe0027  192.168.030.051 50020        83       84       00       56000
41       ens4f0     192.168.030.001 cafebabe0028  192.168.030.052 50020        85       86       00       56000
```
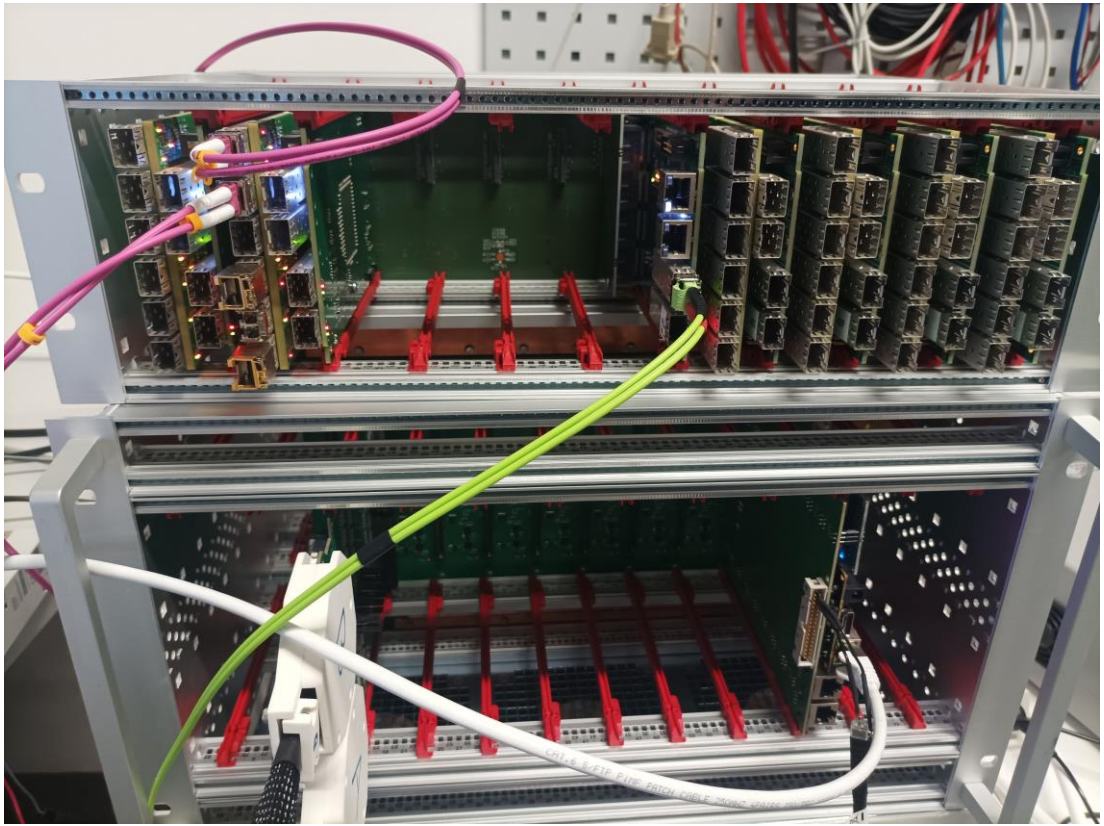

Configurable | **Defined by DNA-ID** | **Configurable**

Splitter, Backplane, CFD and TRB3 SC



Backplane, Controller and SADC