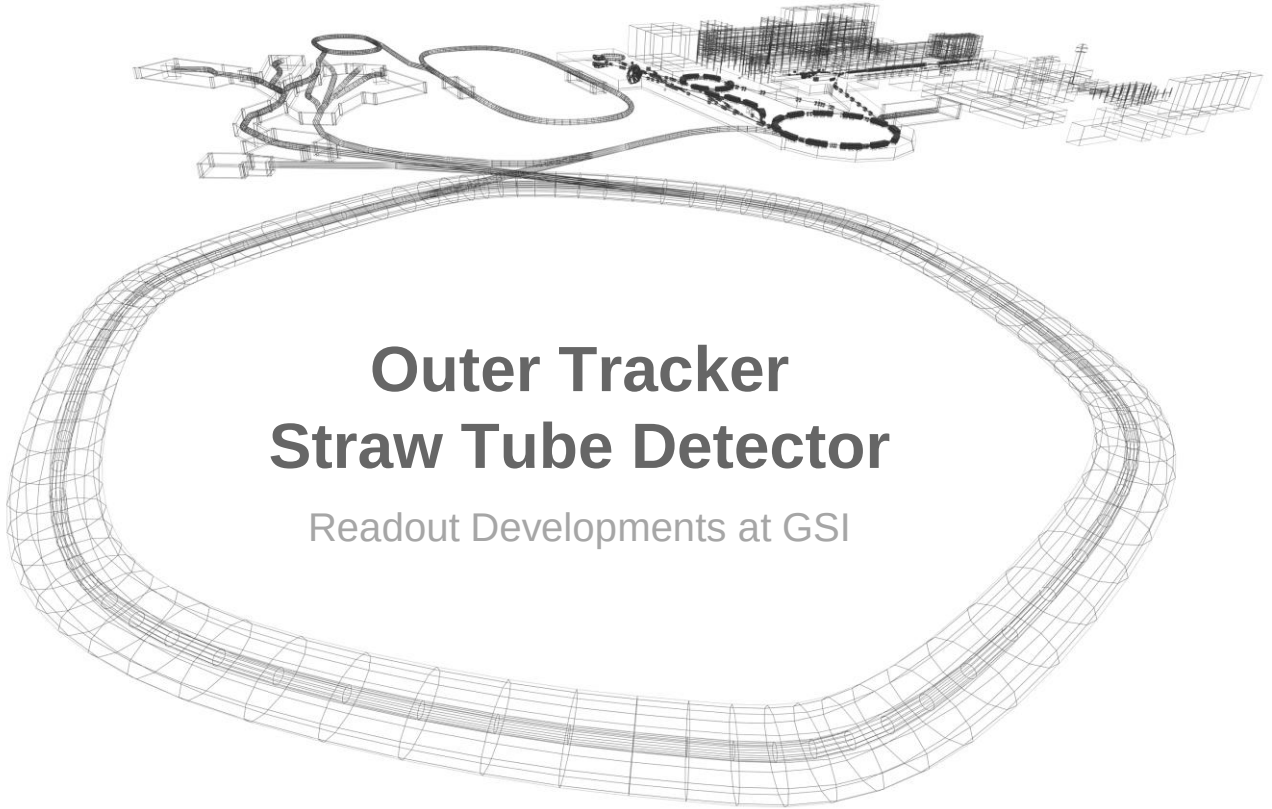
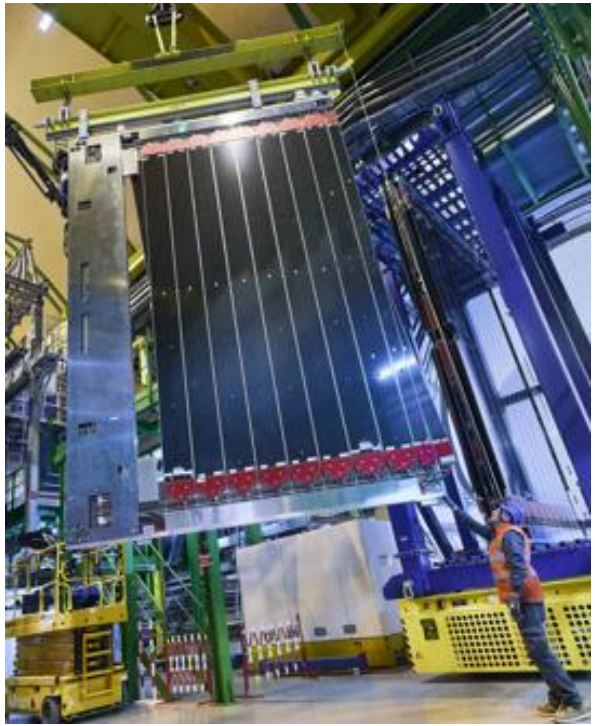


Outer Tracker
Straw Tube Detector

Readout Developments at GSI

Luca Schramm (GSI / TU Darmstadt)

LHCb/CERN donated the formidable Outer Tracker straw-tube detector to PANDA / GSI / FAIR



One of 12 frames, 5x6 m^2, with 4352 straws in 18 modules. (Photo courtesy: LHCb)

Outer Tracker straw-tube brief specs

Straw tube
- Diameter, length: 5 mm, 2.4 m
- Anode wire: 25µm at 1550 V
- Gas mix: $Ar/CO_2/O_2$

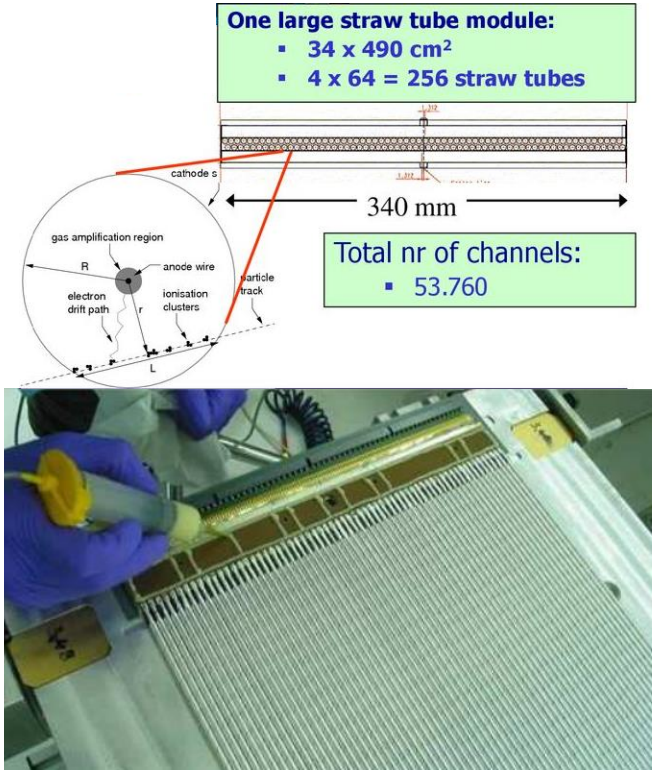
Module
- Independent upper and lower parts
- Each part has 2 staggered layers of 64 tubes
- Singe sided readout
- Front-end electronics on each end of module

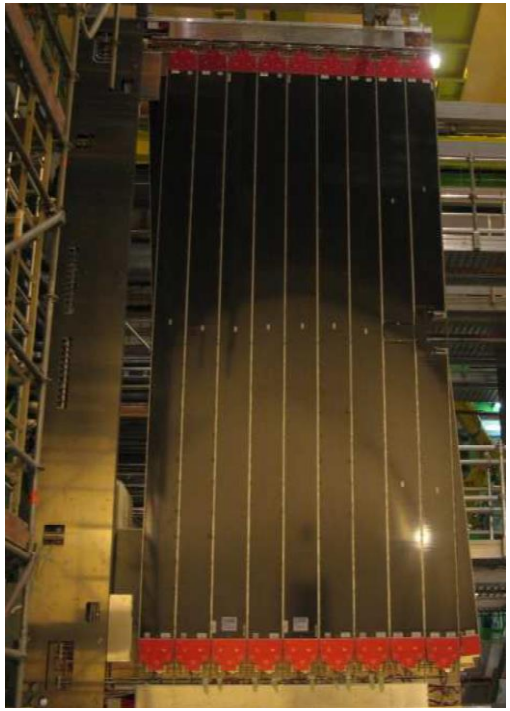
Whole Detector
- 53,760 straw tubes, 216 modules, 432 FEE
- Area coverage: 5 x 6 m^2 x12 planes

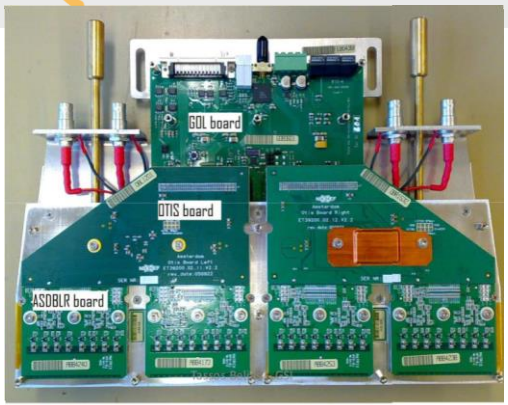
Performance at LHCb (Run1&2)
- ε ~ 98%, σ ~ 170 µm
- δp/p ~ 0.4% (2-100 GeV tracks)

Whole OT in transport frame, 7x5.5x3.5 m^3, 24t, arrival at GSI, Aug. 25, '23. (Photo courtesy: GSI)

Outer Tracker Detector Elements

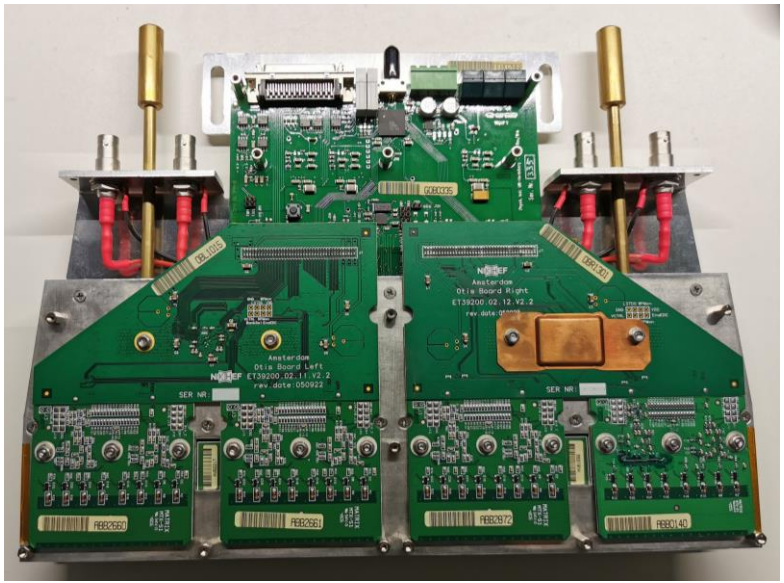






Straw-tubes in a module (left), modules on frame 5x6 m² (middle), FEE Box open (right) (Photos courtesy: LHCb)

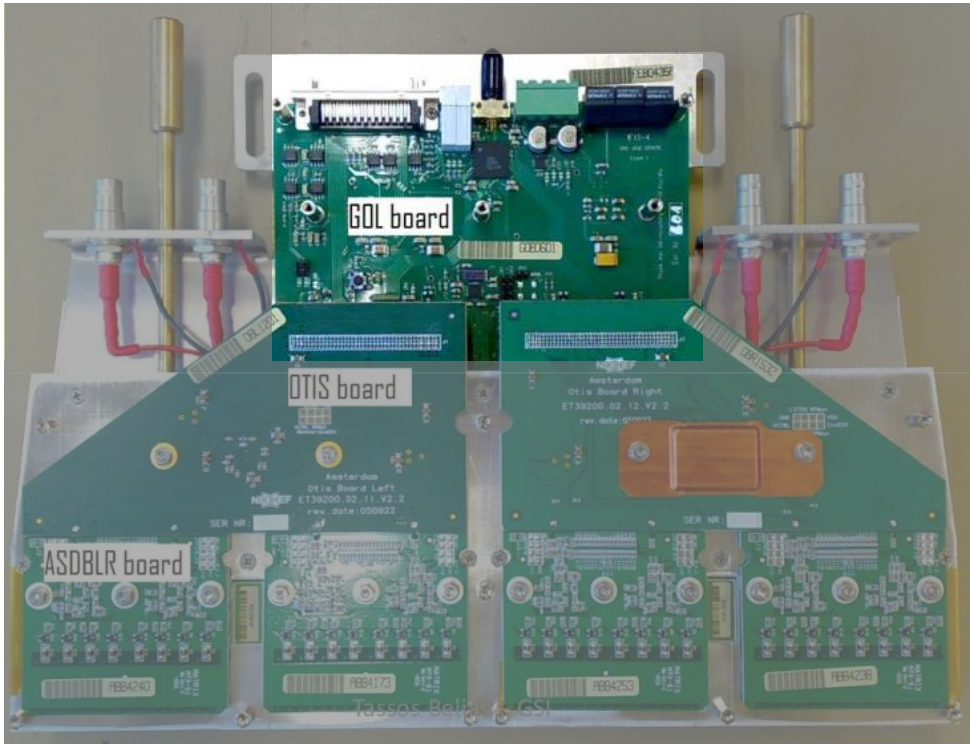
Outer Tracker FEE modules



View inside the FEE Box, front side (left) and back side (right).

Outer Tracker FEE Boards of LHCb

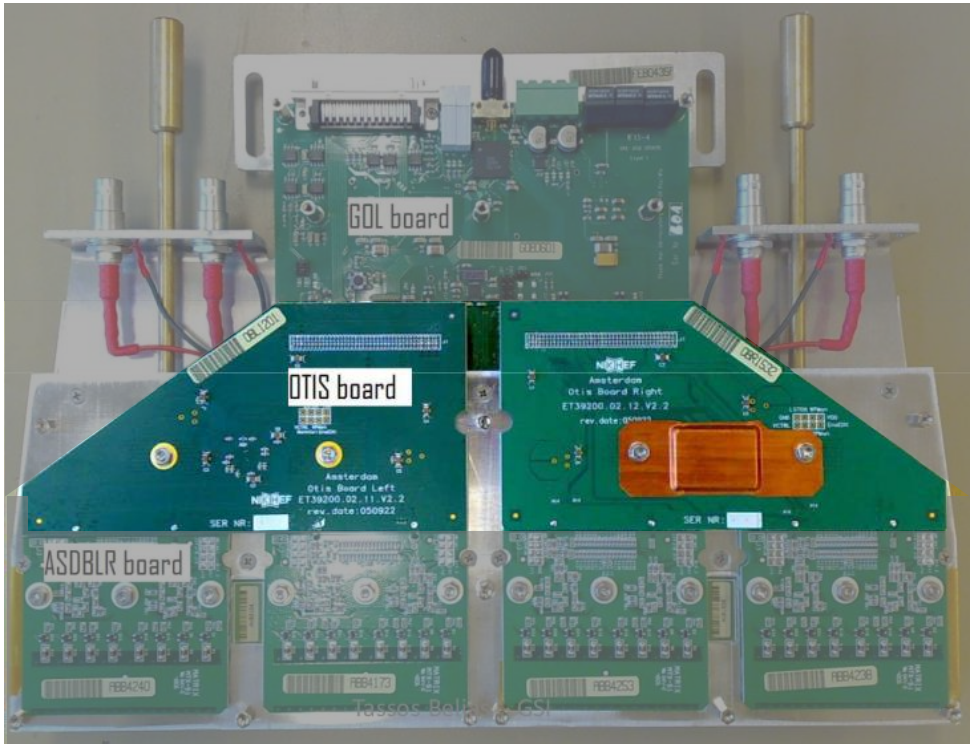
- *GOL*/Auxiliary board (1x) that reads out the OTIS boards of a Front End box. The GOL serializes the time information and sends it to the off-detector electronics through a 1.6 Gbit/s optical link.
- OTIS boards (4x) for time measurement, that each take the output of two ASDBLR boards. The OTIS board has a 32 channel TDC-chip that digitizes the hit signal time wrt the LHC Bunch Crossing.
- *ASDBLR* boards (8x) with ASICs connect to the HV boards to amplify the signals received from these. A board contains two ASDBLR ASICs, that is two 8-channel *A*mplifier-*S*haper-*D*iscriminator with ion-tail cancellation and *B*ase*L*ine *R*estoration. (Designed for ATLAS TRT Readout)
- *High Voltage* boards, (hidden behind the aluminium chassis) plug into a module's feed-through board. Distribute HV to 128 anode wires and pass the straw signals to the ASICs.



FEE Box boards on one side & another set of same boards on the other side.

Outer Tracker FEE Boards of LHCb

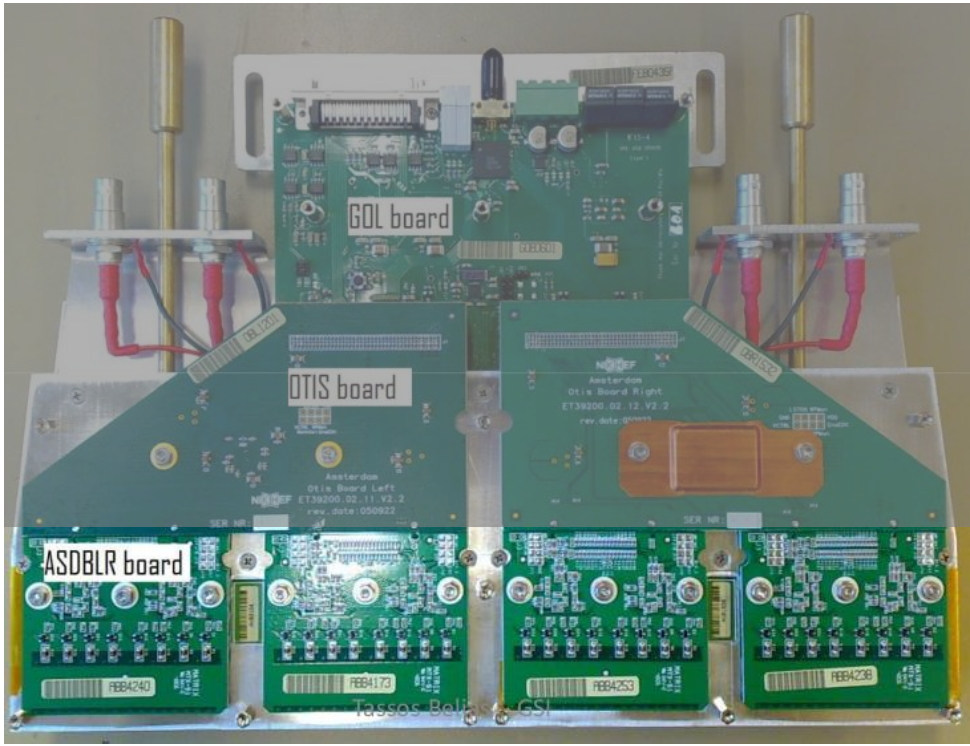
- *GOL*/Auxiliary board (1) that reads out the OTIS boards of a Front End box. The GOL serializes the time information and sends it to the off-detector electronics through a 1.6 Gbit/s optical link.
- OTIS boards (4) for time measurement, that each take the output of two ASDBLR boards. The OTIS board has a 32 channel TDC-chip that digitizes the hit signal time wrt the LHC Bunch Crossing.
- *ASDBLR* boards (8) with ASICs connect to the HV boards to amplify the signals received from these. A board contains two ASDBLR ASICs, that is two 8-channel *A*mplifier-*S*haper-*D*iscriminator with ion-tail cancellation and *B*ase*L*ine *R*estoration. (Designed for ATLAS TRT Readout)
- *High Voltage* boards, (hidden behind the aluminium chassis) plug into a module's feed-through board. Distribute HV to 128 anode wires and pass the straw signals to the ASICs.



FEE Box boards on one side & another set of same boards on the other side.

Outer Tracker FEE Boards of LHCb

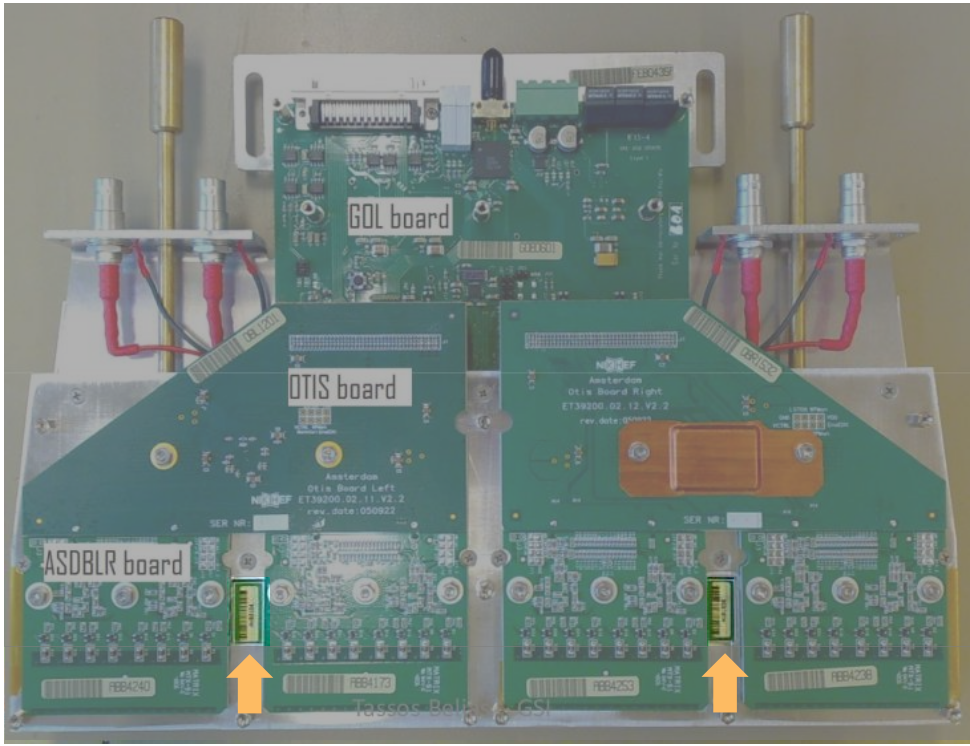
- *GOL*/Auxiliary board (1) that reads out the OTIS boards of a Front End box. The GOL serializes the time information and sends it to the off-detector electronics through a 1.6 Gbit/s optical link.
- OTIS boards (4) for time measurement, that each take the output of two ASDBLR boards. The OTIS board has a 32 channel TDC-chip that digitizes the hit signal time wrt the LHC Bunch Crossing.
- *ASDBLR* boards (8) with ASICs connect to the HV boards to amplify the signals received from these. A board contains two ASDBLR ASICs, that is two 8-channel *A*mplifier-*S*haper-*D*iscriminator with ion-tail cancellation and *B*ase*L*ine *R*estoration. (Designed for ATLAS TRT Readout)
- *High Voltage* boards, (hidden behind the aluminium chassis) plug into a module's feed-through board. Distribute HV to 128 anode wires and pass the straw signals to the ASICs.



FEE Box boards on one side & another set of same boards on the other side.

Outer Tracker FEE Boards of LHCb

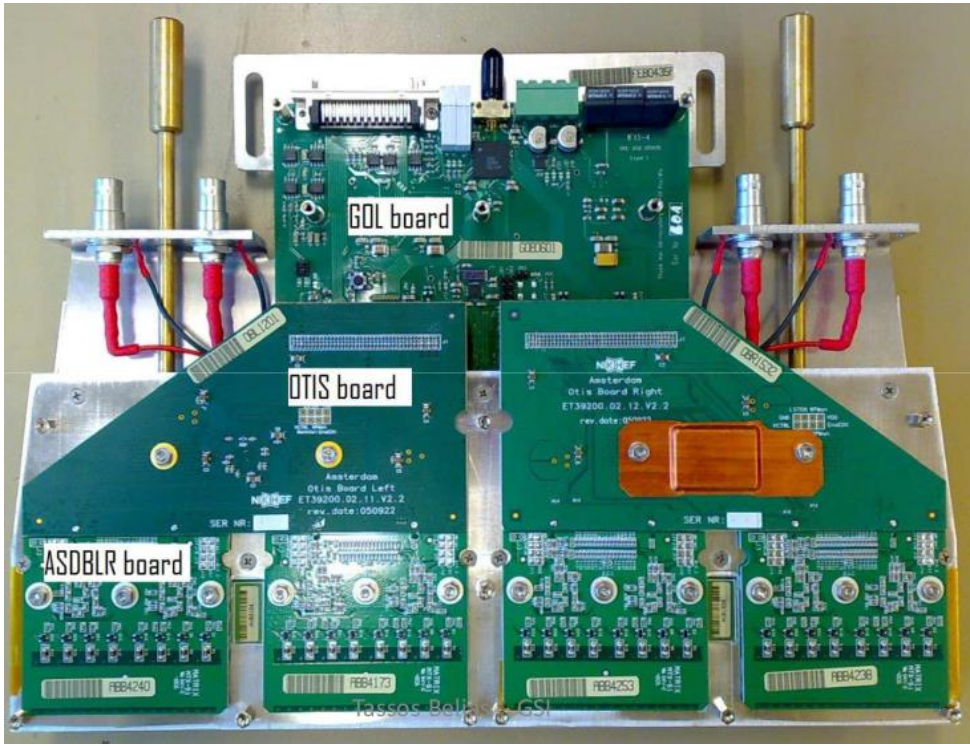
- *GOL*/Auxiliary board (1) that reads out the OTIS boards of a Front End box. The GOL serializes the time information and sends it to the off-detector electronics through a 1.6 Gbit/s optical link.
- OTIS boards (4) for time measurement, that each take the output of two ASDBLR boards. The OTIS board has a 32 channel TDC-chip that digitizes the hit signal time wrt the LHC Bunch Crossing.
- *ASDBLR* boards (8) with ASICs connect to the HV boards to amplify the signals received from these. A board contains two ASDBLR ASICs, that is two 8-channel *A*mplifier-*S*haper-*D*iscriminator with ion-tail cancellation and *B*ase*L*ine *R*estoration. (Designed for ATLAS TRT Readout)
- *High Voltage* boards, (hidden behind the aluminium chassis) plug into a module's feed-through board. Distribute HV to 128 anode wires and pass the straw signals to the ASICs.



FEE Box boards on one side & another set of same boards on the other side.

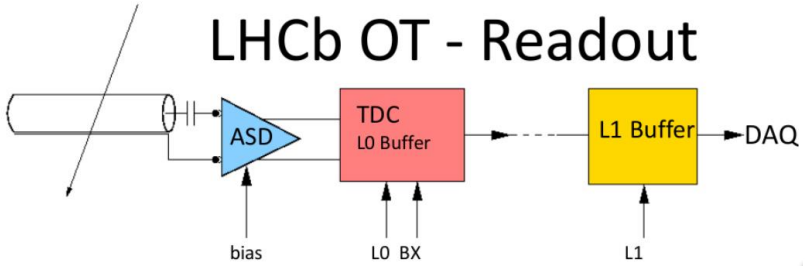
Outer Tracker FEE Boards of LHCb

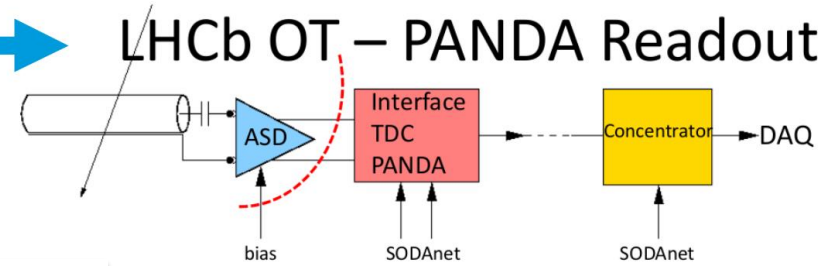
- *GOL*/Auxiliary board (1) that reads out the OTIS boards of a Front End box. The GOL serializes the time information and sends it to the off-detector electronics through a 1.6 Gbit/s optical link.
- OTIS boards (4) for time measurement, that each take the output of two ASDBLR boards. The OTIS board has a 32 channel TDC-chip that digitizes the hit signal time wrt the LHC Bunch Crossing.
- *ASDBLR* boards (8) with ASICs connect to the HV boards to amplify the signals received from these. A board contains two ASDBLR ASICs, that is two 8-channel *A*mplifier-*S*haper-*D*iscriminator with ion-tail cancellation and *B*ase*L*ine *R*estoration. (Designed for ATLAS TRT Readout)
- *High Voltage* boards, (hidden behind the aluminium chassis) plug into a module's feed-through board. Distribute HV to 128 anode wires and pass the straw signals to the ASICs.

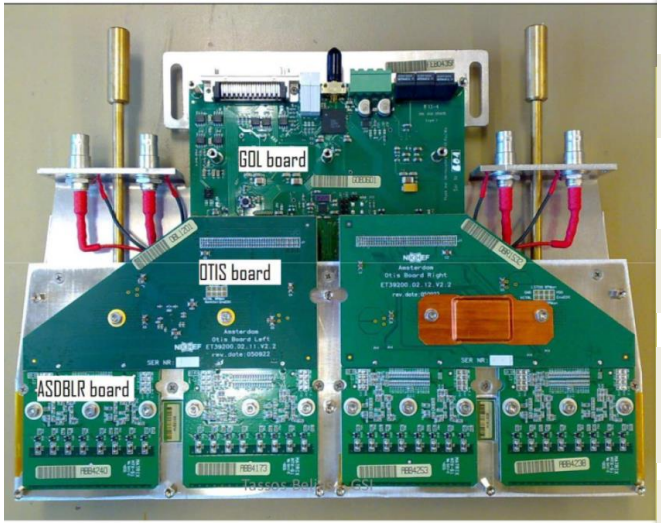


FEE Box boards on one side & another set of same boards on the other side.

OT Readout – Changes for PANDA Readout





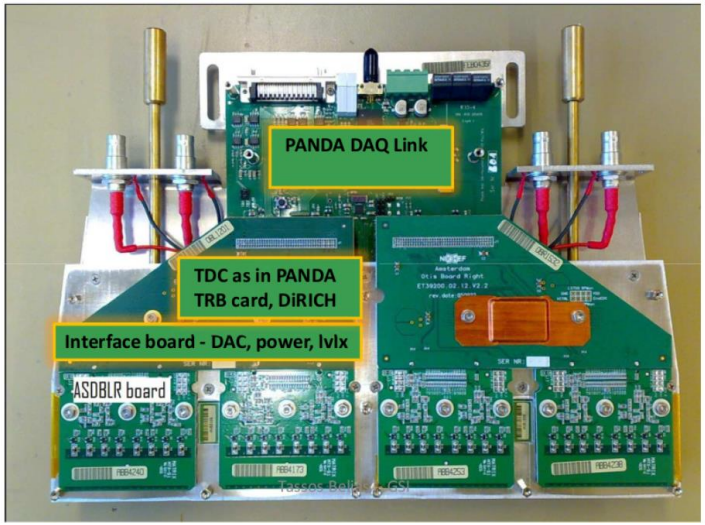


1 optical link,
1.28 Gbit/s

4 OTIS TDC chips,
32 ch/chip

16 ASDBLR chips,
8 ch/chip
(2 chips/board)

Input: 128 channel

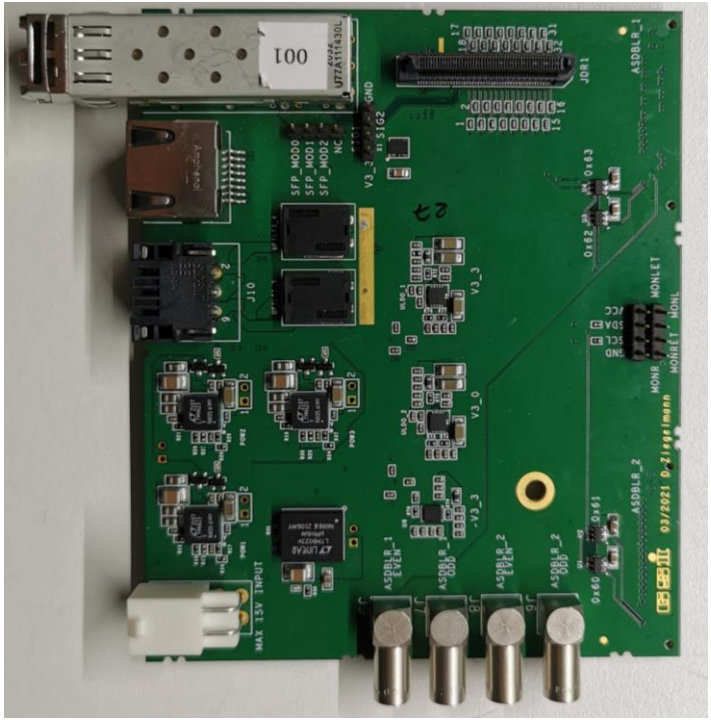


Interface board – Design at GSI

Requirements for Interface board:

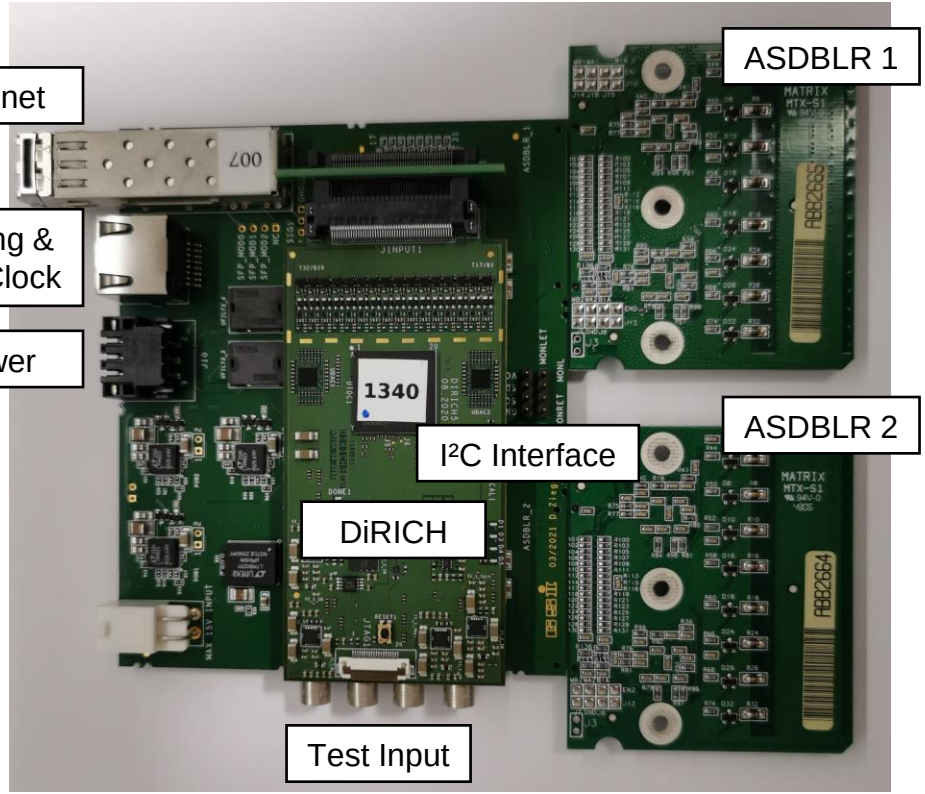
- Interconnect ASDBLR with DiRICH (TDC)
- Power and Controls

  for ASDBLR (2x) and DiRICH (1x)
- Pass ASDBLR digital signals to DiRICH
- Clock In & Data Out from DiRICH
- Send test signals directly to ASDBLR
- V.1 → easily monitor and measure signals



Interface board v.1

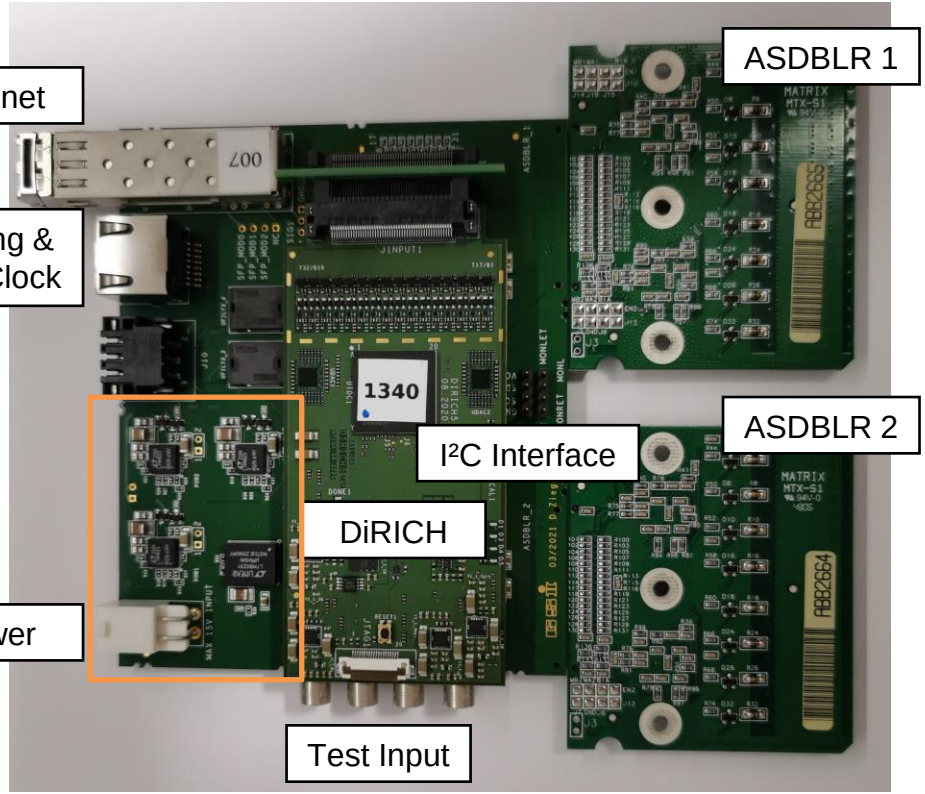
Interface board – ASDBLR to DiRICH



- TRBnet
  - Communication & datatransfer
- Timing & ext. Clock
  - 200 MHz on-board clock available
- I²C Interface
  - DAC programming → ASDBLR thresholds
- Test Input
  - Directly pass pulses to ASDBLR
- Power
  - 2 possibilities:
    - 4 voltages by lab powersupply
    - Voltages created on-board by DCDC converter

Interface board v.1 with mounted DiRICH and ASDBLRs

Interface board – ASDBLR to DiRICH



- TRBnet
  - Communication & datatransfer
- Timing & ext. Clock
  - 200 MHz on-board clock available
- I²C Interface
  - DAC programming → ASDBLR thresholds
- Test Input
  - Directly pass pulses to ASDBLR
- Power
  - 2 possibilities:
    - 4 voltages by lab powersupply
    - Voltages created onboard by DCDC converter

Interface board v.1 with mounted DiRICH and ASDBLRs

Interface board – Signals and Rates Tests

Threshold tests:

- ASDBLR (I²C Interface) and DiRICH (TRBnet) thresholds can be set

First hit rate tests:

- Input test pulse (up to 100 kHz)
- Check hit rates in DiRICH TDC

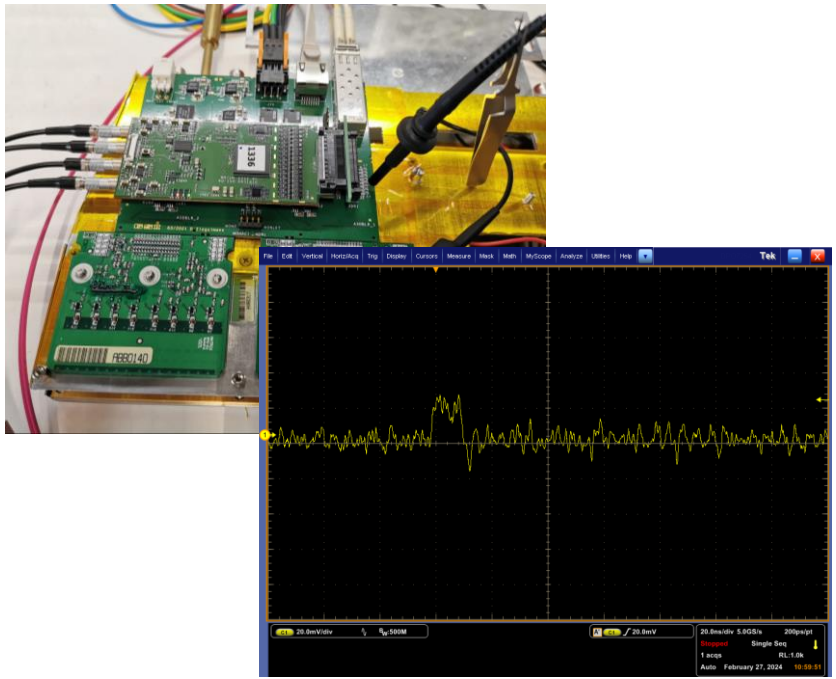
➡ Match both thresholds to reduce noise

Reg	Channel	1336	1340	c001
	Channel group	3 2 1 0 or or or or of of of of	3 2 1 0 or or or or of of of of	3 2 1 0 or or or or of of of of
c000	0	0	0	0
c001	1	110677	0	0
c002	2	105919	0	0
c003	3	105452	0	0
c004	4	106931	0	0
c005	5	111841	0	0
c006	6	106213	0	0
c007	7	122852	0	0
c008	8	121717	0	0
c009	9	134862	0	0
c00a	10	115531	0	0
c00b	11	132476	0	0
c00c	12	117525	0	0
c00d	13	137557	0	0
c00e	14	120359	0	0
c00f	15	121341	0	0
c010	16	116631	0	0
c011	17	133866	0	0
c012	18	127428	0	0
c013	19	135952	0	0
c014	20	115391	0	0
c015	21	119742	0	0
c016	22	117390	0	0
c017	23	129697	0	0
c018	24	114872	0	0
c019	25	135475	0	0
c01a	26	114882	0	0
c01b	27	124014	0	0
c01c	28	114649	0	0
c01d	29	130688	0	0
c01e	30	122147	0	0
c01f	31	130652	0	0

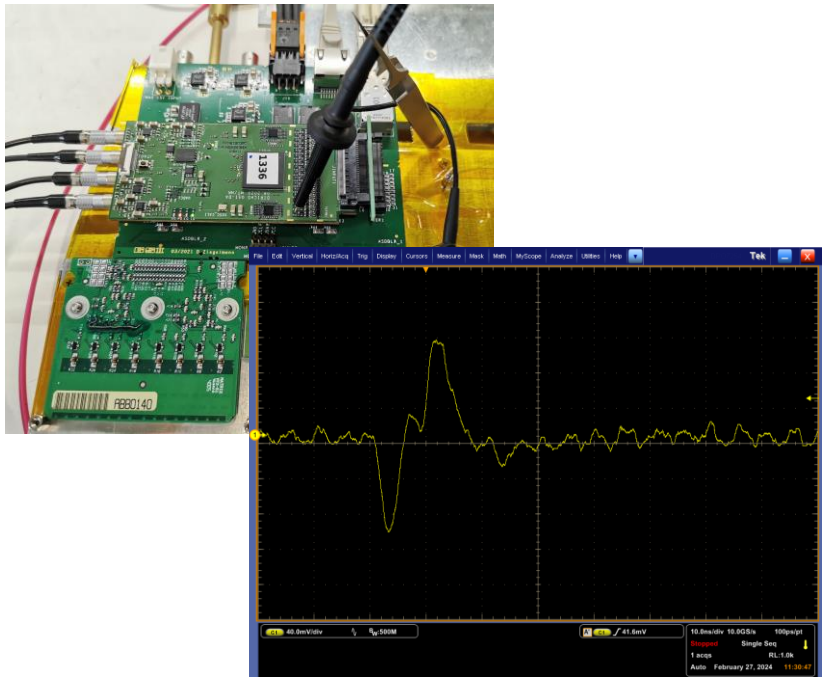
TRBnet HitRegister for one DiRICH

Interface board – Signals and Rates Tests

Signals from ASDBLR



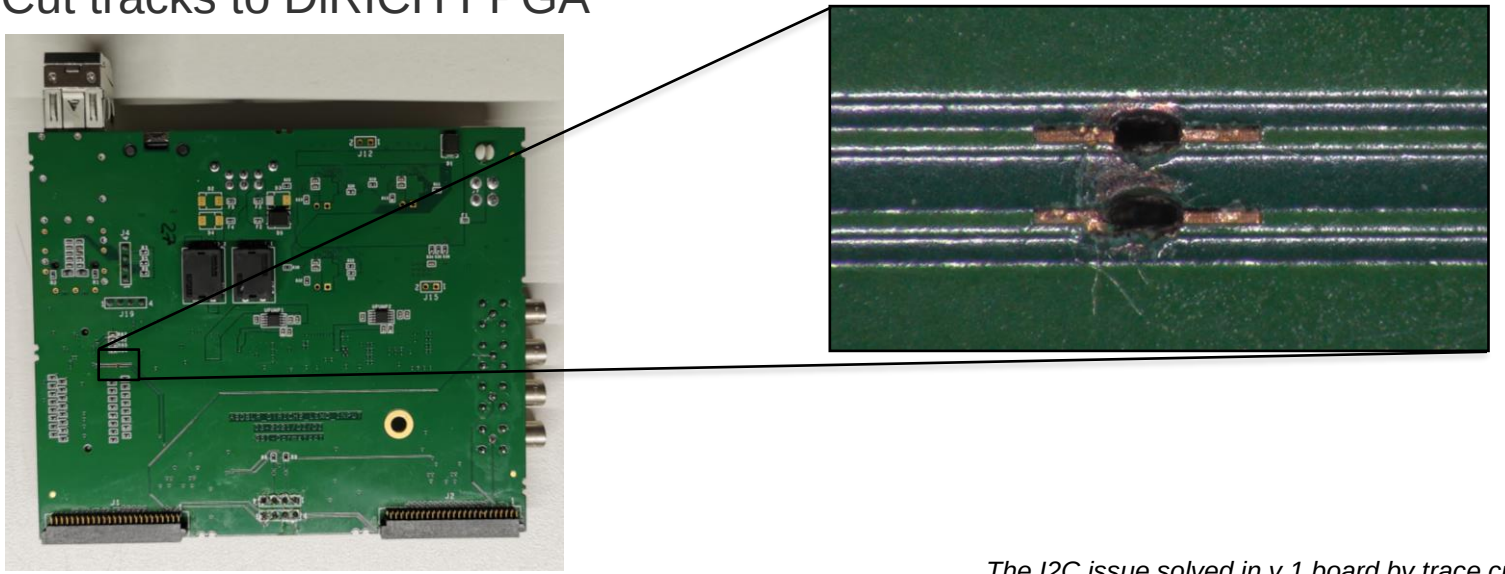
Signals after DiRICH amplifier



Scope screenshots and probe setup

Interface board – Debugging and challenges

- Timing: RJ45 input mismatched compared to CTS output
  - ➡ Manually corrected
- ASDBLR thresholds: I²C unstable while DiRICH mounted
  - ➡ Cut tracks to DiRICH FPGA



The I2C issue solved in v.1 board by trace cut-through

OT PANDA Readout Crate

Readout setup

- Capacity up to 8 DiRICH per TRB3 peripheral (32ch./DiRICH)
- TRB3 Crate
- 6 TRB3sc
  - 1 CTS (Central trigger system)
    - SFP-AddOn-v2
    - RJ45 AddOn Board
  - 1 master
  - 4 peripherals

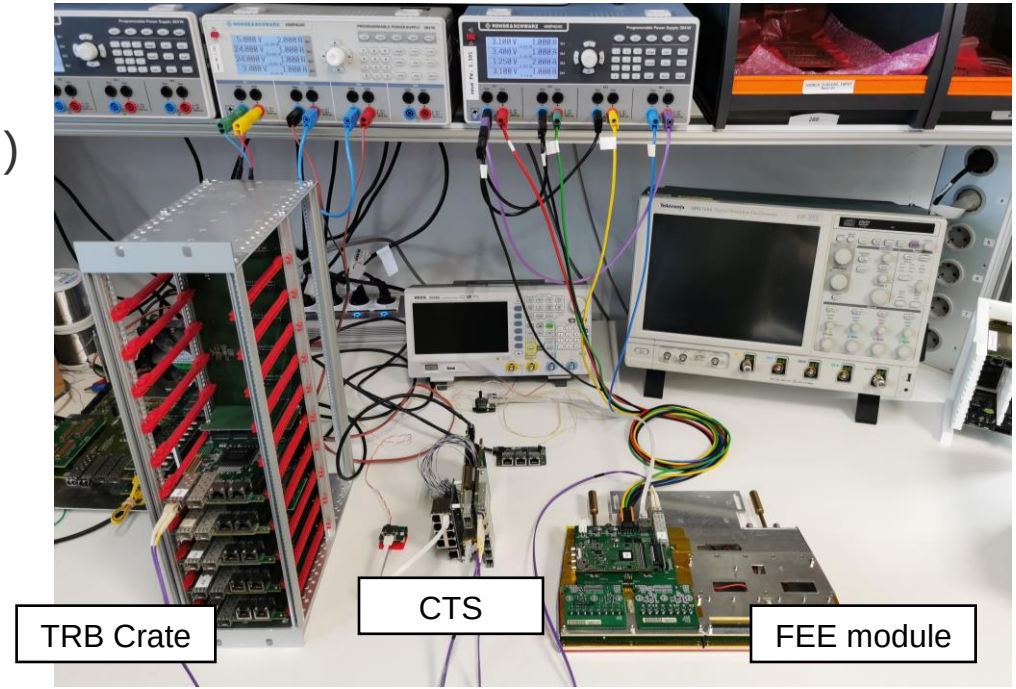
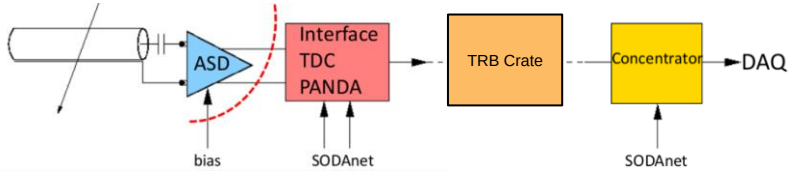


Photo of crate and all components

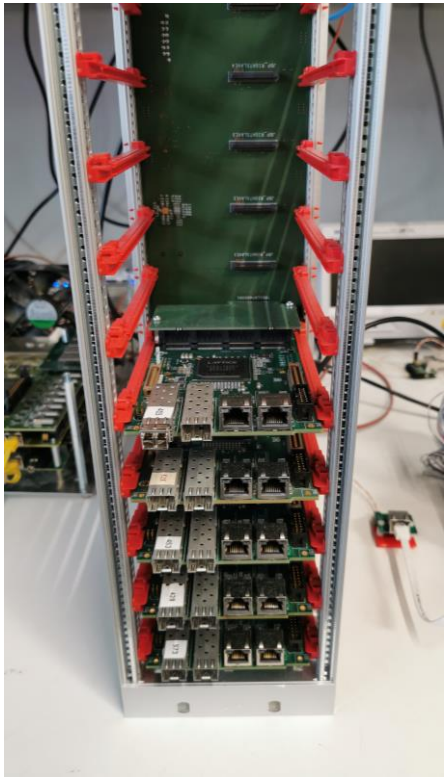
OT PANDA Readout – Next Steps

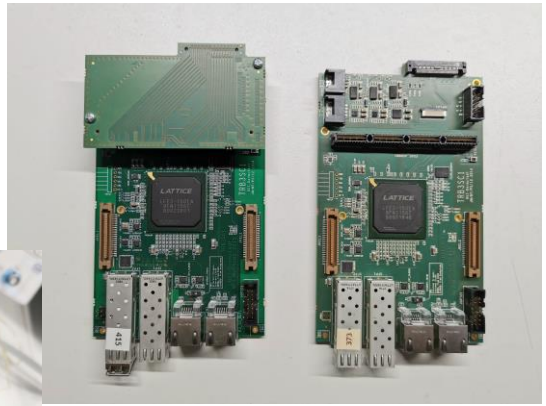
- Continue testing, check and debug interface board → design of version 2
- Progress with available ASDBLR boards on straw-tube modules
- Further integration with DAQ
- Use of Data Concentrator

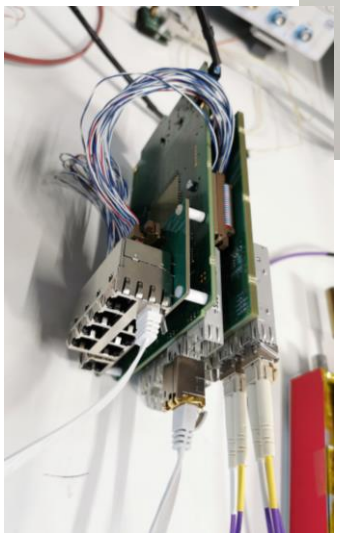


- Common DAQ Clock Source
- Build and use more readout crates for test in labs and in beam-lines
- … have fun and enjoy the system!

Back-up – TRB system







TRB Crate front/back view, TRB3sc in CTS/master/slave setup

Back-up – half-sized FEE module

Outer Tracker (half-sized) FEE module