PANDA MVD electronics developments in Torino

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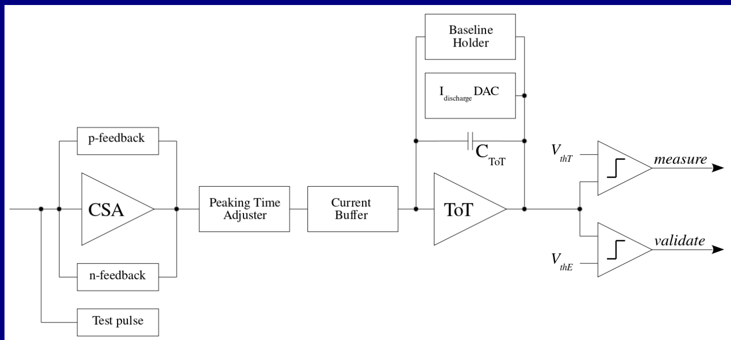
SSDs readout requirements

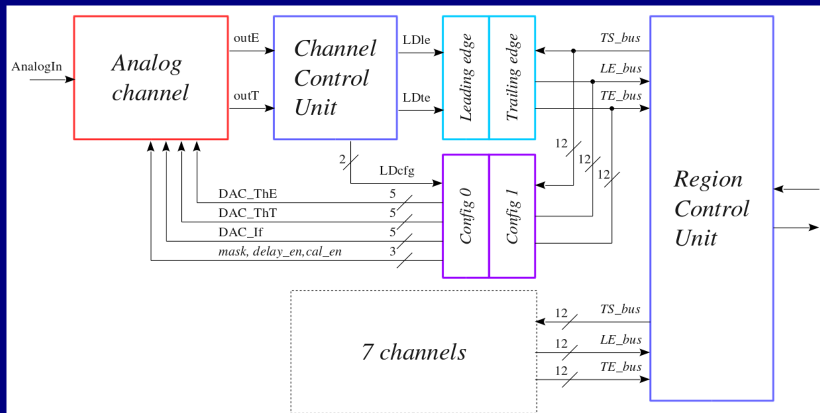
Specification	Min	Max	Unit
Channels per chip	64		
ToA (pk-pk)		6.25	ns
ToA (r.m.s.)		1.8	ns
Charge resolution	8		bits
Input charge	1	40	fC
Input capacitance	2	17	pF
Max rate per strip		40	kHz
Noise		1500	e^-
Preamp peaking time	50	$\geq$ 100	ns
Reference clock		160	MHz
Power consumption		256	mW
Radiation tolerance		20	kGy
Chip dimensions	4.5×3.5		mm^2
Pads position	On two sides only		

ToASt analog channel



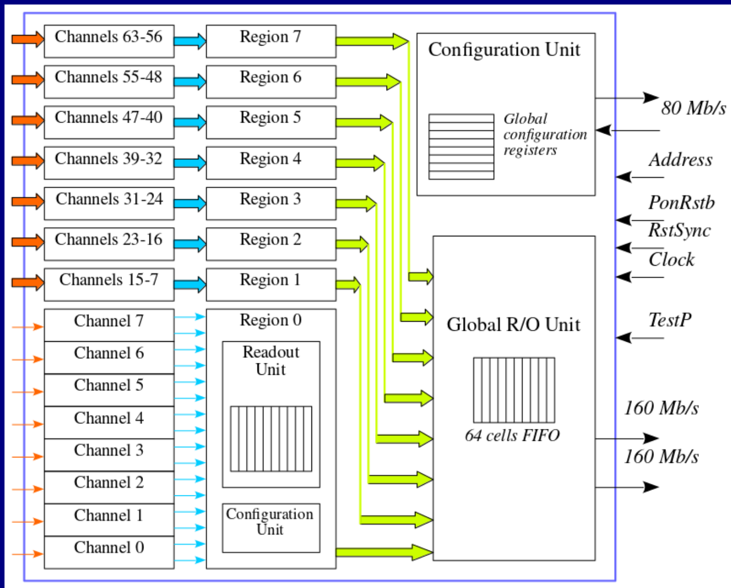
- CSA with selectable input signal polarity, gain ≈ 5 mV/fC
- Shaper with adjustable peaking time
- Current buffer
- Test pulse injection via integrated capacitor
- ToT stage with programmable discharge current
- Low frequency feedback to set baseline
- Two comparators with independent thresholds
- Local DACs for threshold and discharge current fine tuning

ToASt channel schematic

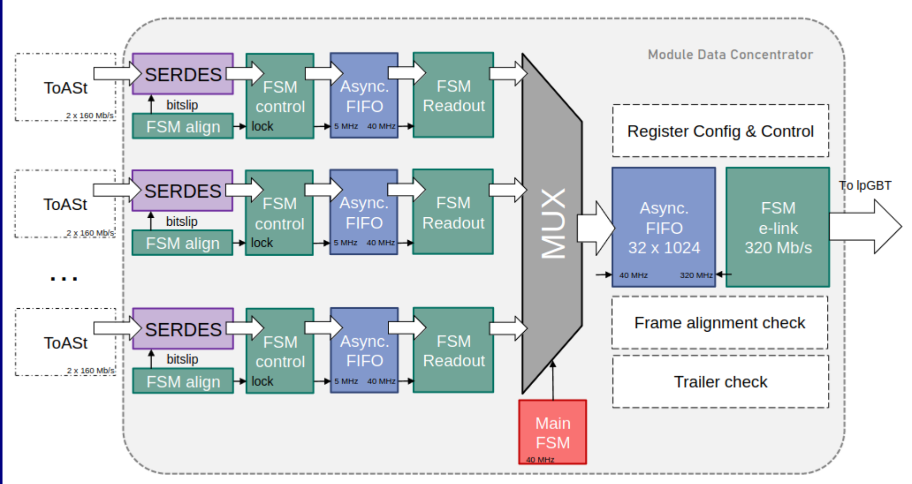


- Common time reference : 12 bits time stamp distributed to all channels
- Time stamp are Gray-encoded
- LE and TE registers latch time stamp at comparator rising/falling edges

ToASt architecture

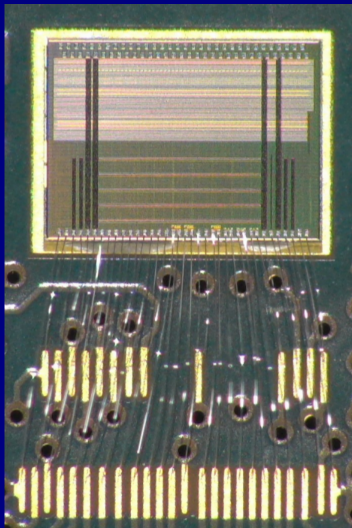


Data concentrator



→ *Details in M. Caselle presentation later in this session*

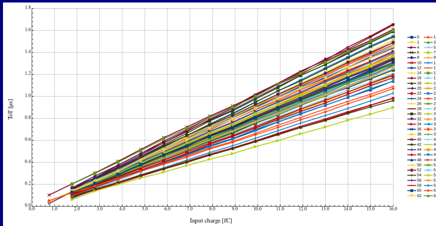
ToASt version 1



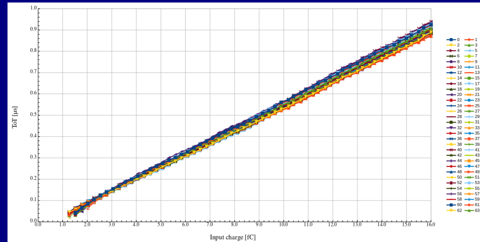
- CMOS 110 nm technology
- Digital-on-top design flow
- Die size : 3.24×4.41 mm^2
- Left pads pitch (on two rows) : 63 μm
- Right pads pitch : 90 μm
- Three power domains : analog, digital, digital pads *(all supply voltages at 1.2 V)*
- One external analog reference ($V_{BG} = 600$ mV)
- SLVS driver/receivers
- TMR protected digital logic *(using CERN TMRG tool)*

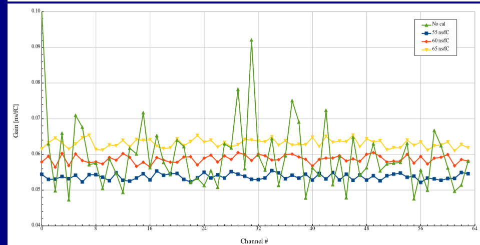
Measurement - transfer function

Before calibration



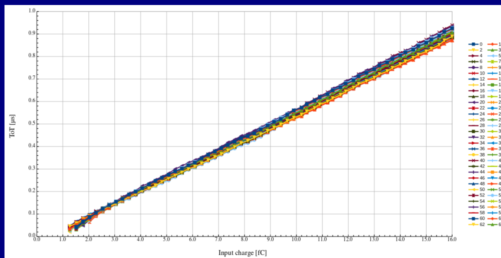
After calibration (gain & offset)

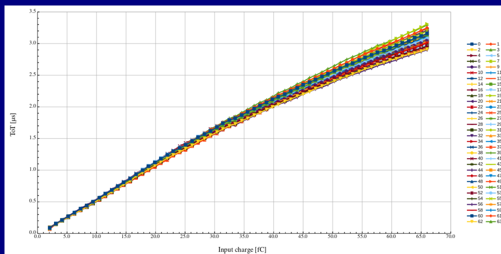




- Fully functional at 160 and 200 MHz
- Calibration reduces gain spread from 12% to 1.7% and offset spread reduced from 30% to 5.8%
- Power consumption : 180 mW @1.2 V

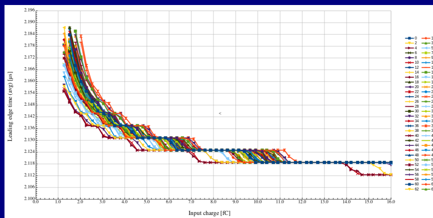
Measurement - test pulse ranges

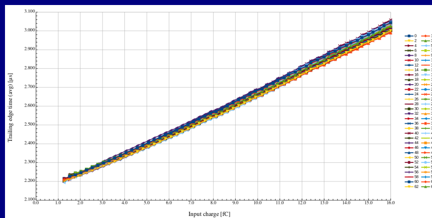


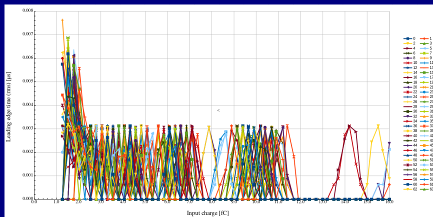


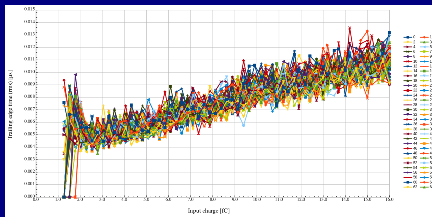
- Test pulse input with internally programmable amplitude via 6+1 bit internal DAC.
- Two test pulse ranges *(the +1 bit)* :
  - Normal range : up to 16 fC, step 0.25 fC
  - Extended range : up to 66 fC, step 1.03 fC
- Non linearity (rms) <0.64% in the 2÷16 fC range

Measurement - leading and traling edge



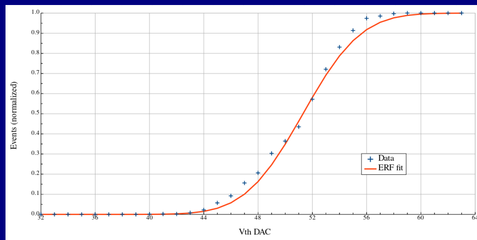


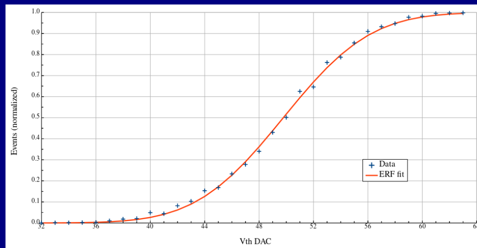




- Test : test pulses synchronous with reset
- Events per channel : 100
- Time bin : 6.25 ns

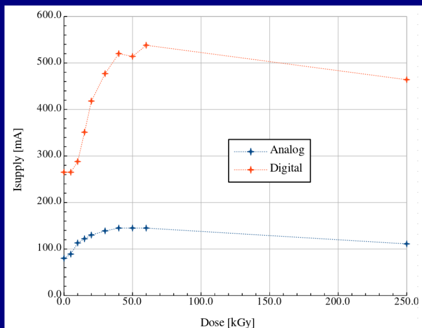
Measurement - noise

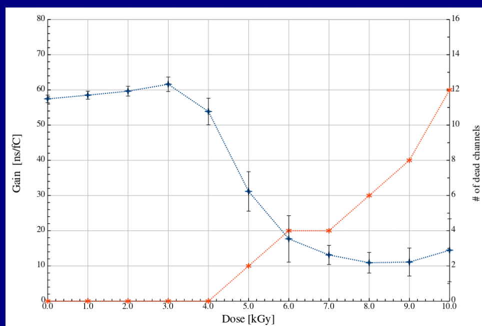




- S-curve obtained with channel threshold scan
  - Test pulse resolution and global threshold resolution too coarse
  - Baseline resolution gives similar results but with fewer points
- Conversion from DAC codes to input charge from simulations
- No input capacitance
- Average noise : 0.034 fC (211 e^-)
- Maximum noise : 0.05 fC (312 e^-)

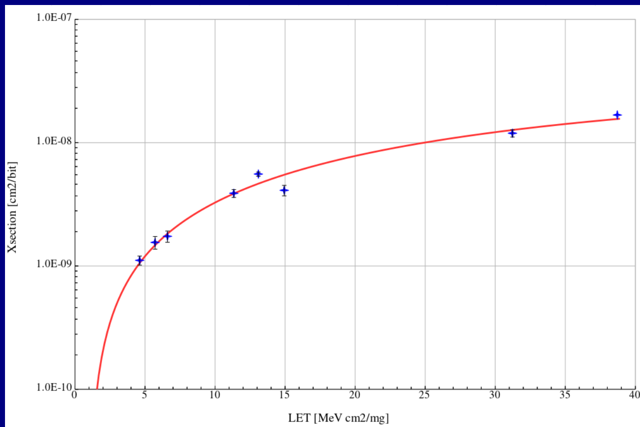
TID test *(@ University of Padova)*





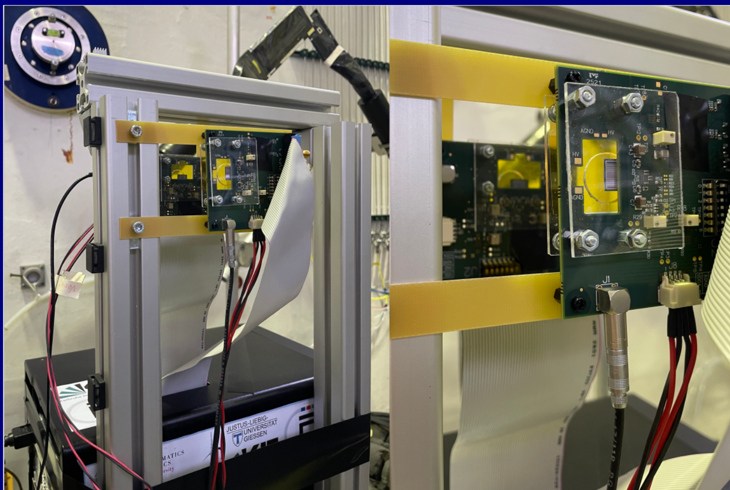
- Digital interface still working after 250 kGy
- Power consumption increase after 10 kGy (expected : leakage current in MOS)
- Gain drop after 4 kGy (unexpected)
- Full recovery after high T annealing
- Problem traced back to leakage current in analog switches
  - Enclosed layout has been adopted for switches in ToASt v2

SEU test *(@ INFN LNL SIRAD facility)*



- Ion fluence $\sim 5 \cdot 10^7$ per ion
- Estimated cross section for 200 MeV protons : 3×10^{-15} cm^2
- Hadron flux 5×10^6 hadrons/(cm$^2 \times$s) $\rightarrow 9.3 \times 10^{-2}$ errors/(h chip)
- Only 1$\rightarrow$0 errors observed - triplication error found in the Verilog code

Beam test at COSY - experimental set-up



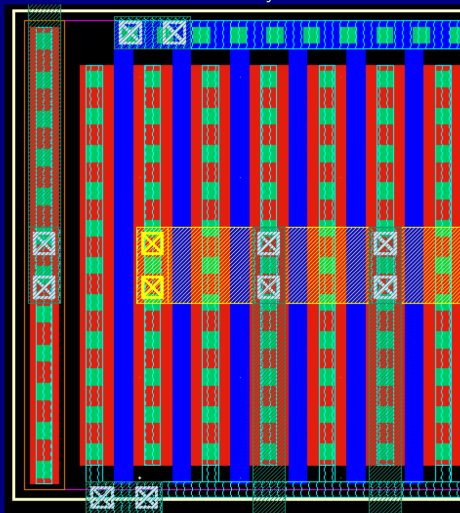
→ *Details in H.G. Zaunick presentation later in this session*

Changes from v1 to v2 - 1

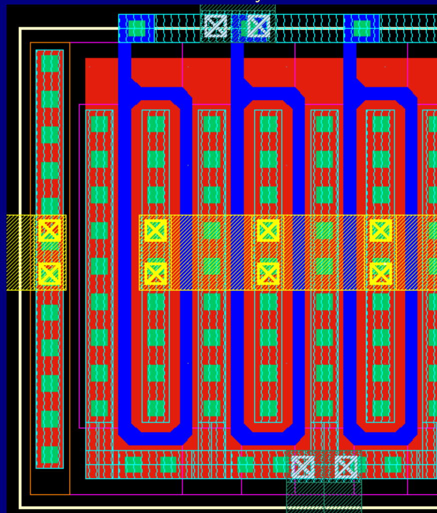
- Die size : $3.24 \times 4.41\ mm^2 \rightarrow 3.24 \times 4.59\ mm^2$
- Same pinout as v1
- Reference voltage generated by internal bandgap
  - V_{BG} pin still present for filtering
  - Internal bandgap can be disabled (GCR2[11])
- Enclosed layout for analog switches
  - It should solve the analog functionality issue
  - It will not solve the power supply increase issue
- Channel DACs threshold voltage resolution has been increased from 5 to 6 bits.
  - Range bits for these two DACs has been moved to CCR0[9:8].

Enclosed layout

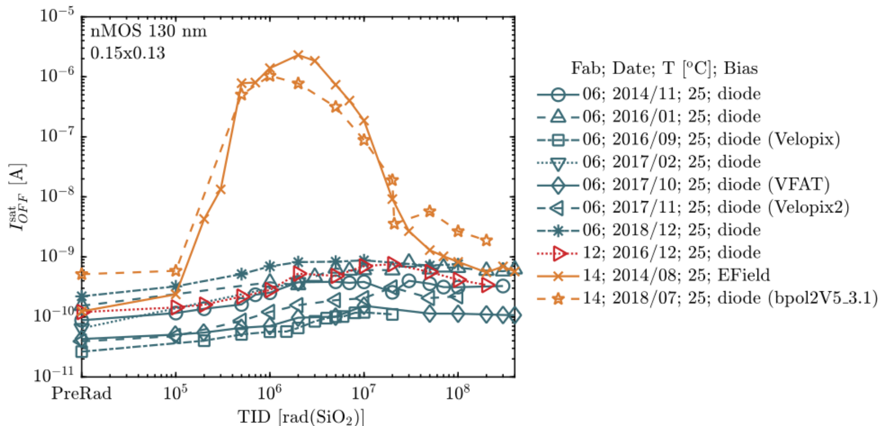
Standard layout



Enclosed layout



Leakage current variability



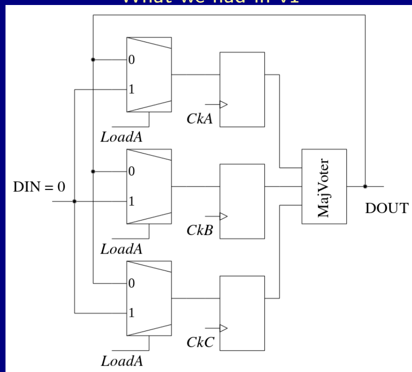
F.Faccio et al., Variability of the TID response of transistors in <*omiss*> 130nm technology

Note : We do not have data for our 110 nm technology.
These are the closest ones I could find.

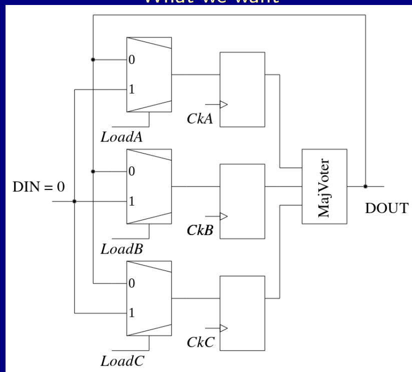
Changes from v1 to v2 - 2

- Full review of the digital part
  - Change in synthesis tool to avoid TMR removal
  - Improvement in triplication structure
  - New TMR design guidelines from CERN

What we had in v1



What we want



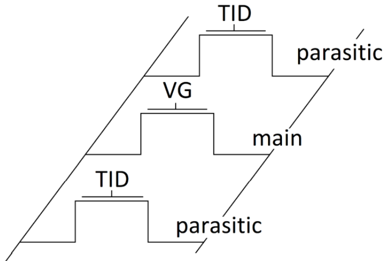
Design status and plans

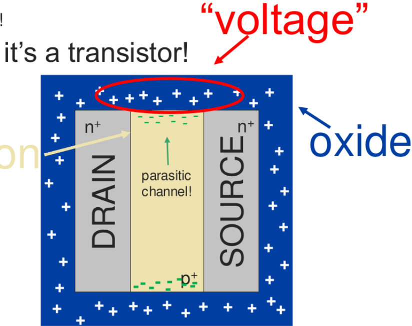
- ToASt v1 fully functional
  - Extensively tested in lab at 160 and 200 MHz
  - Beam test results very promising, work ongoing
  - Issues in radiation tolerance found, corrected in v2
- ToASt v2 submitted on February 26th 2024
  - delivery expected on August 5th 2024
- Same test board as v1
  - minor changes in the software are required
- Beam time requested to LNL in 4Q2024 for v2 SEU test

Spare slides

MOS intrinsic parasitic transistor

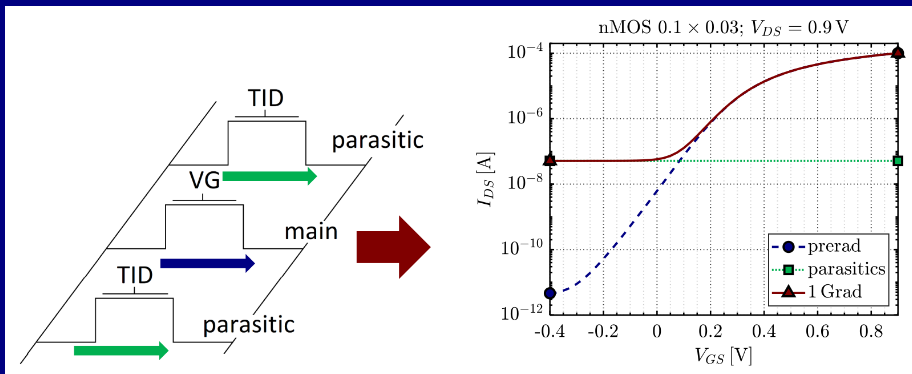
positive charge attracts electrons ->**problem only in nMOS**!





G. Borghello, Radiation effects on 28nm CMOS technology

Radiation induced leakage current



G. Borghello, Radiation effects on 28nm CMOS technology

Note : I_{DS} values are for a 28 nm technology.