A high time resolution and high dynamic range ASIC for the micro vertex detector in the PANDA experiment

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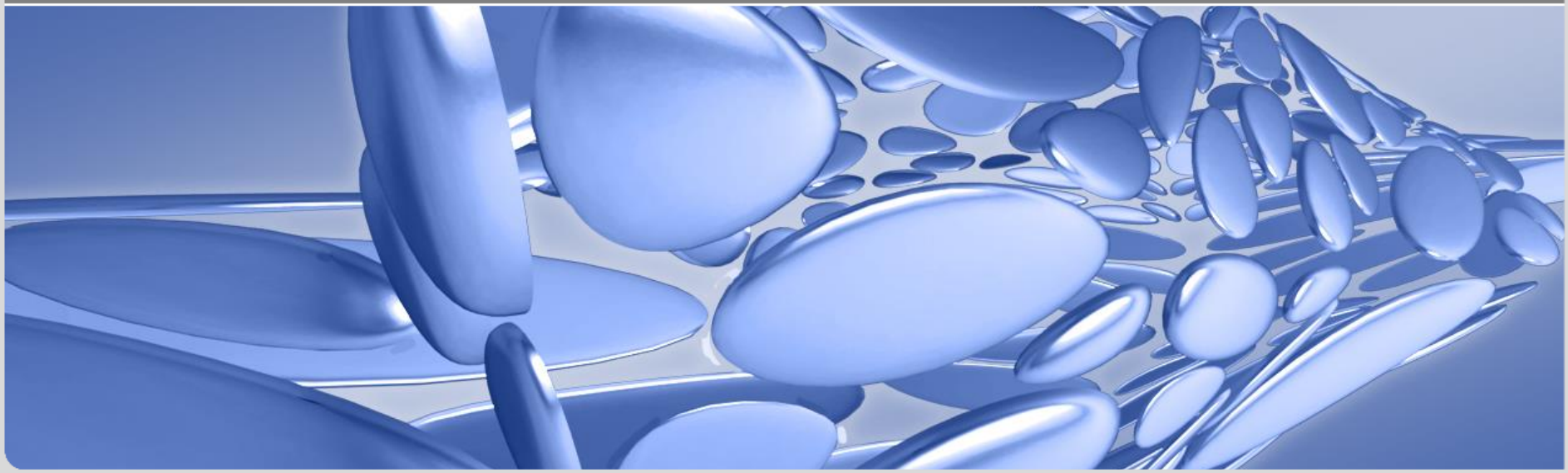
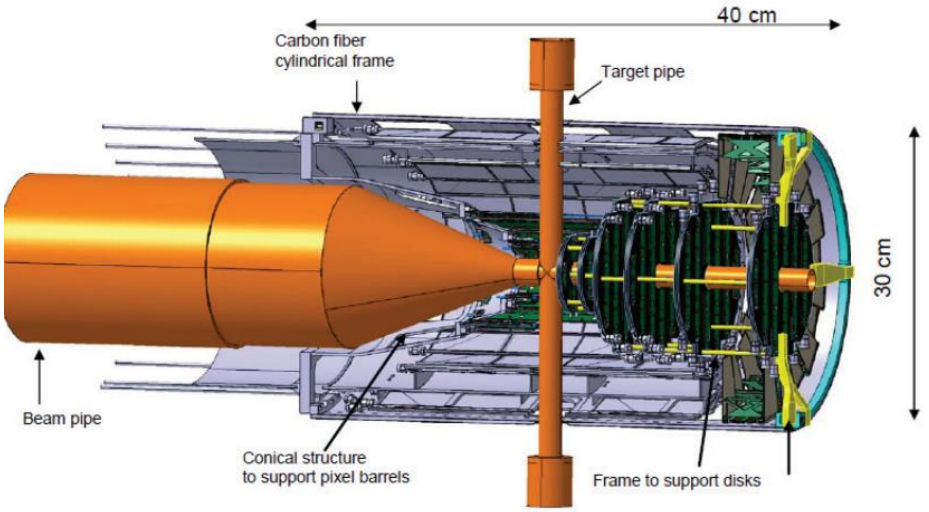


PANDA Micro Vertex Detector

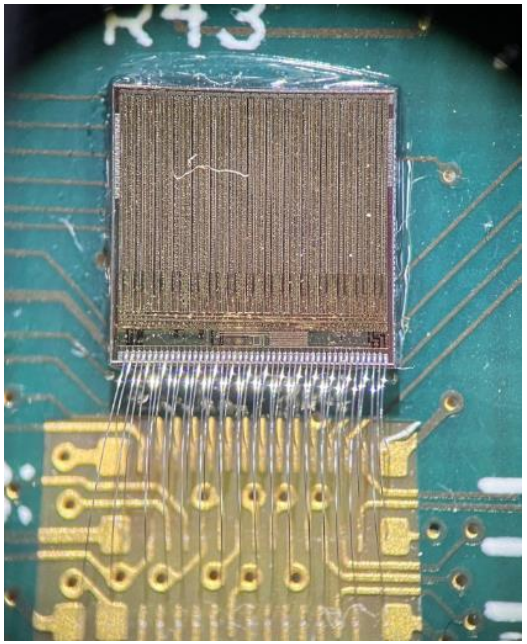
- The PANDA detector is composed of several subdetectors
- The Micro Vertex Detector (MVD) is a tracking device for charged particles. It is the innermost sub-detector system of the target spectrometer
- Main tasks of the MVD are:
  - High vertex resolution for primary and secondary vertices of short-lived particles
  - Improvement of momentum resolution
  - Additional input for particle identification

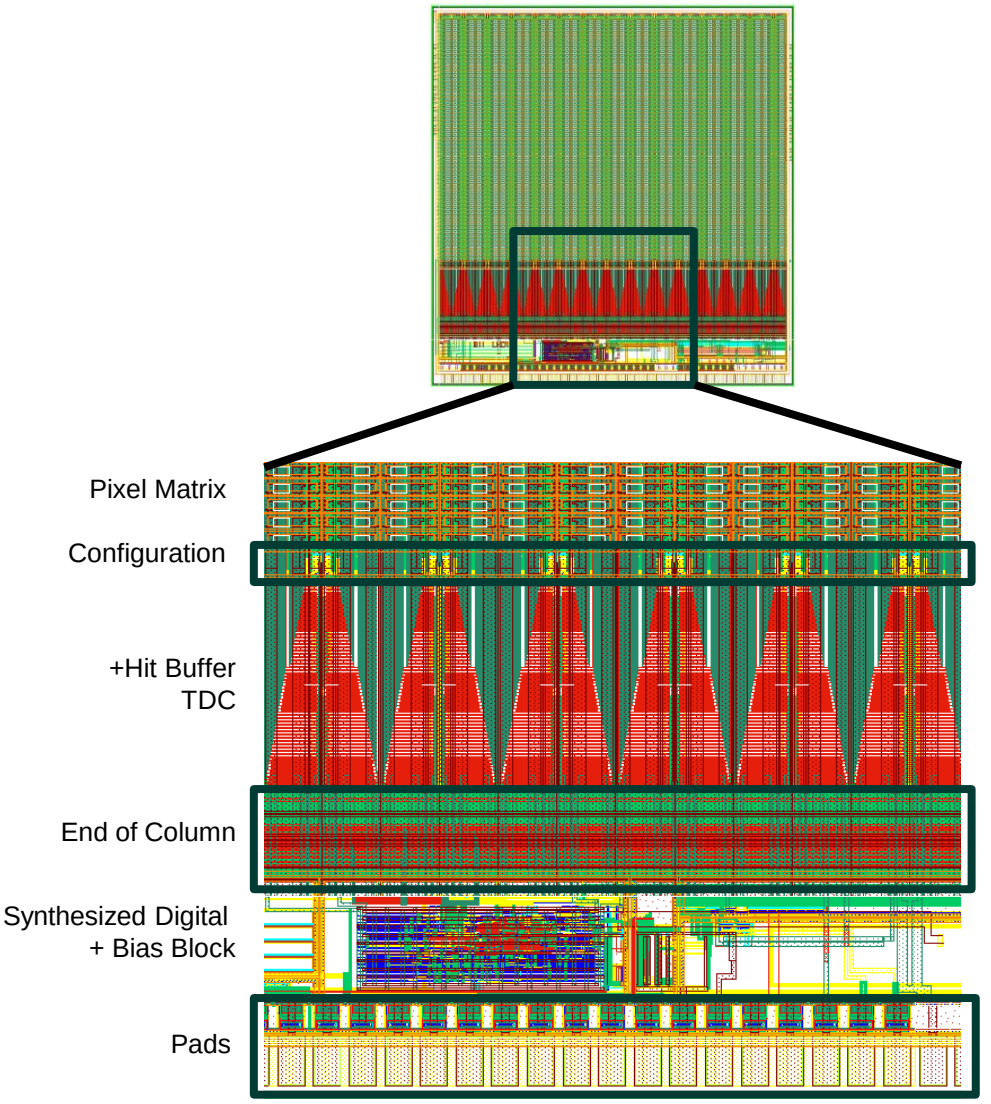
- High time resolution of 1ns RMS enables efficient track reconstruction and possibly particle identification by time of flight
- Energy resolution in wide dynamic range 100ke with 100e noise for dE/dX measurements and particle identification
- Pixel size: 80 µm x 80 µm
- Chip size: 1 cm x 2 cm



Chip Architecture

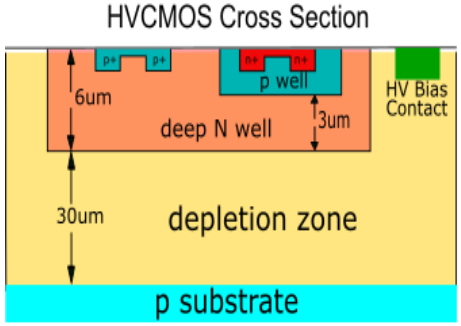
- HVCMOS 180 nm technology with MPW run
- Chip Size: ~ 5 mm x 5 mm
- Pixel Matrix: 29 columns x 62 rows
- Pixel Size: 50 µm x 165 µm
- Configuration register
- Readout Cell
- End of Column
- Synthesized Digital
- Bias Block
- Pads

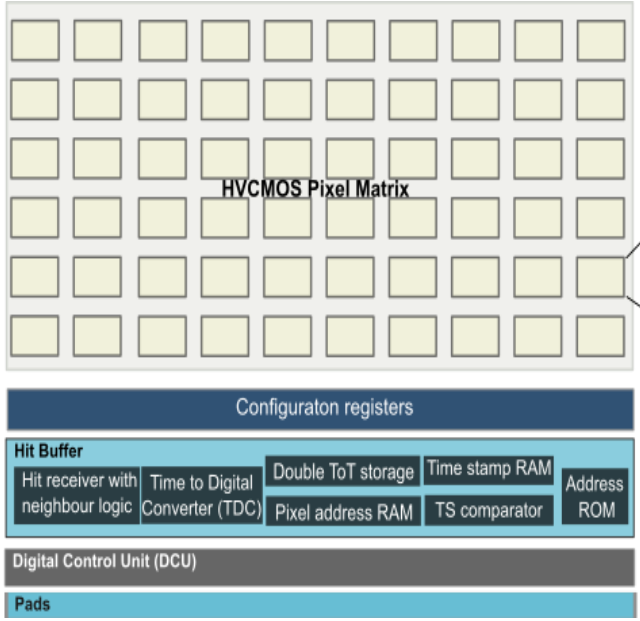


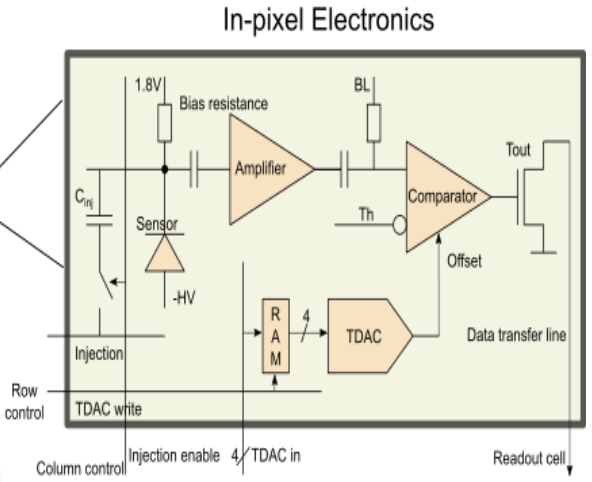


HVCMOS Technology

- HVCMOS Sensor, a new generation of particle detectors
- Commercial technology, not expensive
- The sensor and readout electronics in the same die
- Use external negative bias voltage
- Pixel is based on a deep n well with electronics inside, isolated against HV
- Charge collection by drift
- Substrates from 300Ωcm to ~20kΩcm
- Good time resolution, detection efficiency and radiation tolerance
- Can be thin
- Radiation tolerant technology, further increased by special design
  - Radiation tolerant PMOS transistors
  - Deep submicron
  - Guard Ring
  - Shielding

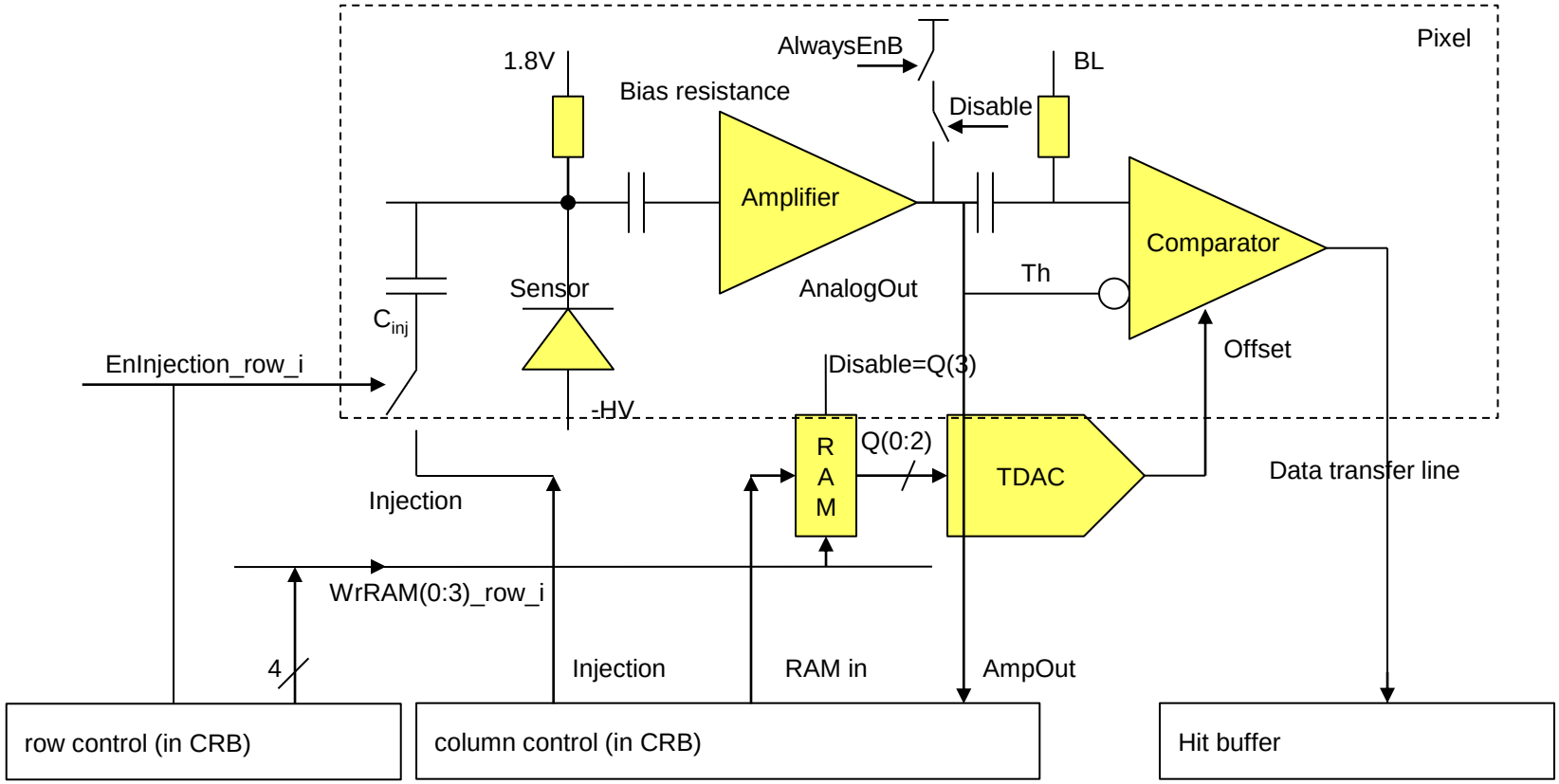






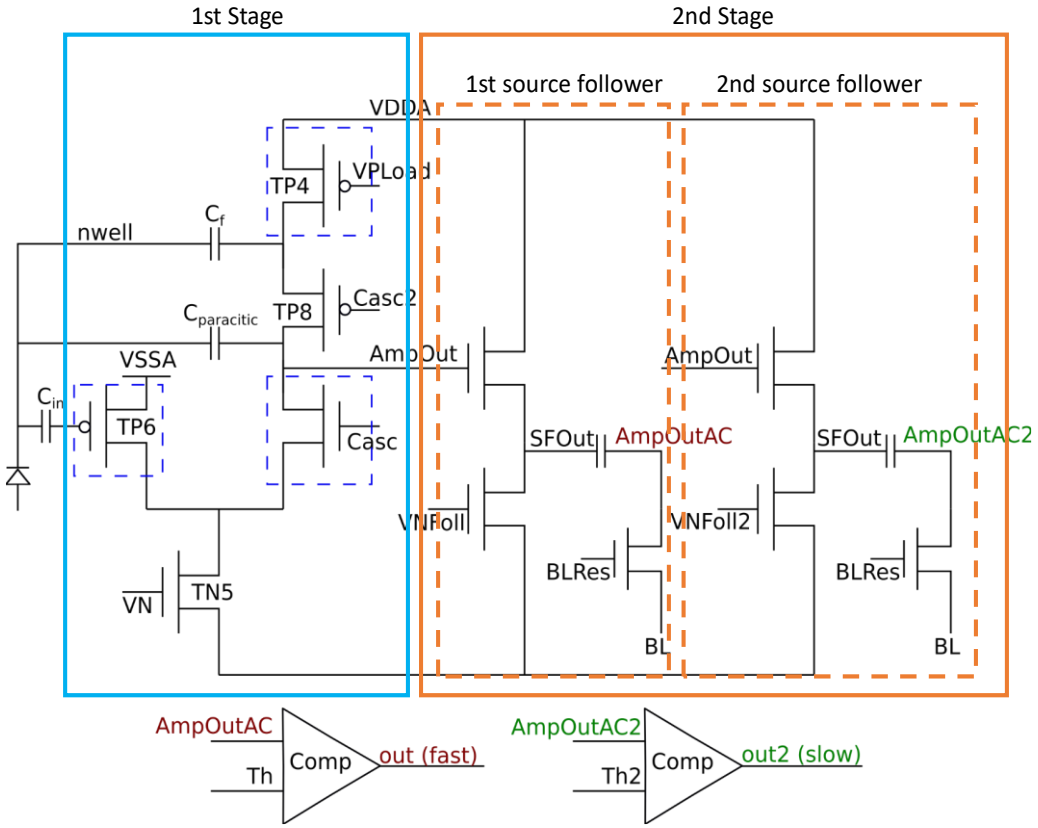
Pixel Electronics

- Charge sensitive amplifier with variable gain
- Feedback circuit
- Two comparators
  - Fast comparator: enable accurate time measurement
  - Slow comparator: enable precise amplitude measurement



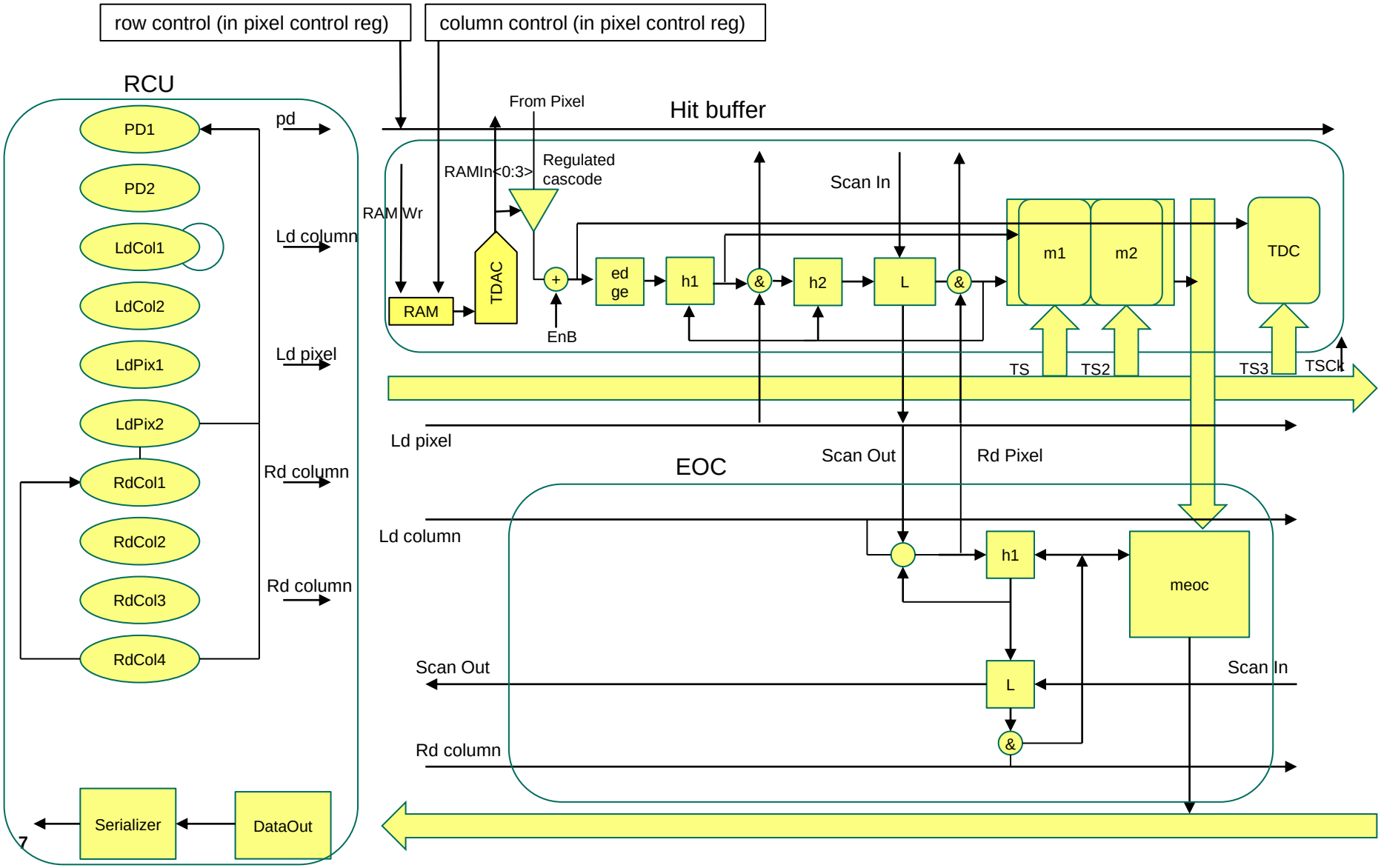
Pixel Electronics

- The first stage is a standard folded cascode amplifier
  - Implement variable gain
- The second stage are the two source followers
  - It provides fast time constant and voltage level shifting
  - The bias current of the second source follower is smaller than that of the first
  - The second source follower acts as a low pass filter
- Each pixel has two comparators and two readout channels



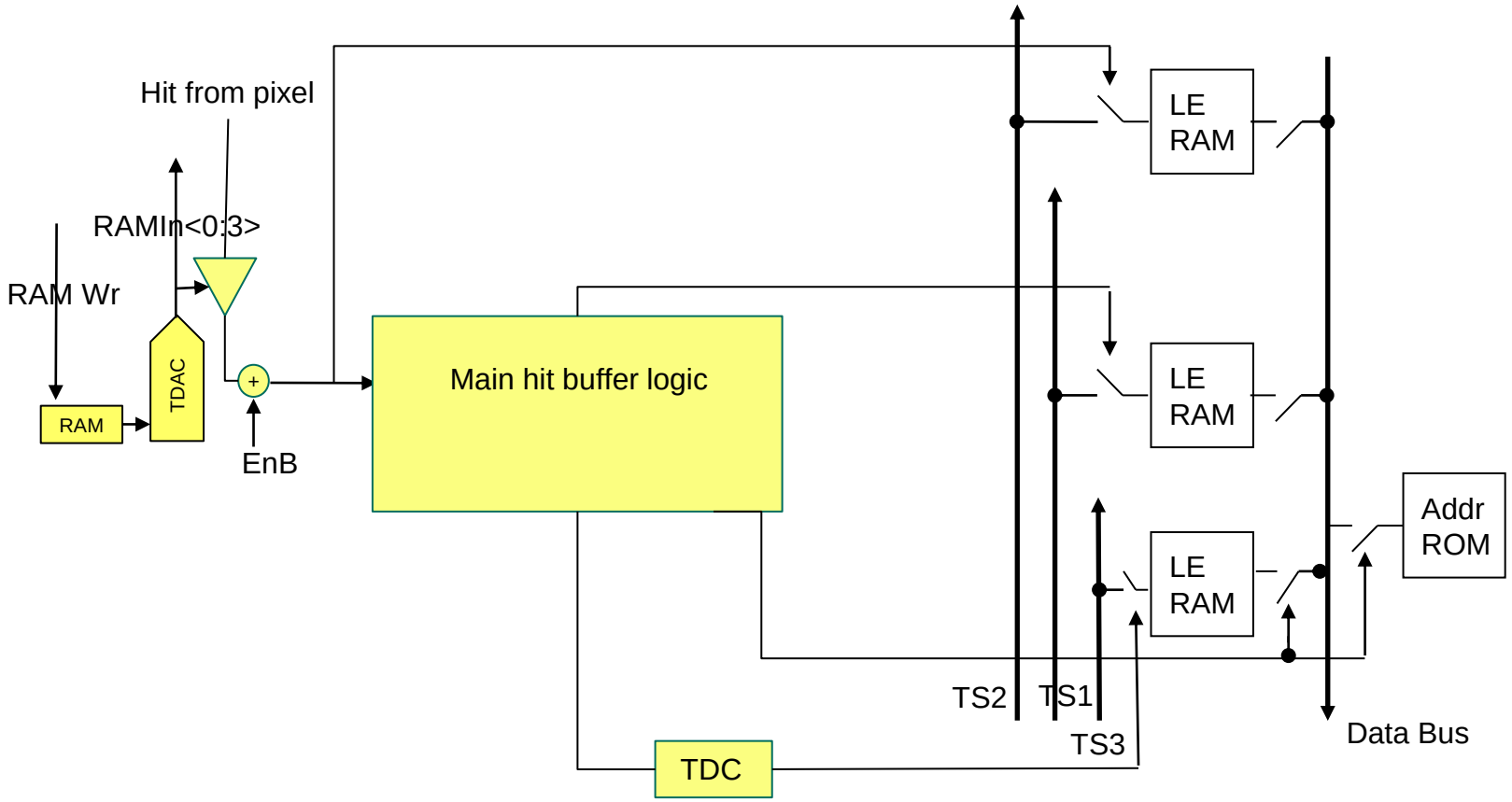
Readout control unit

- Hit Buffer, End of Column, Readout Control Unit



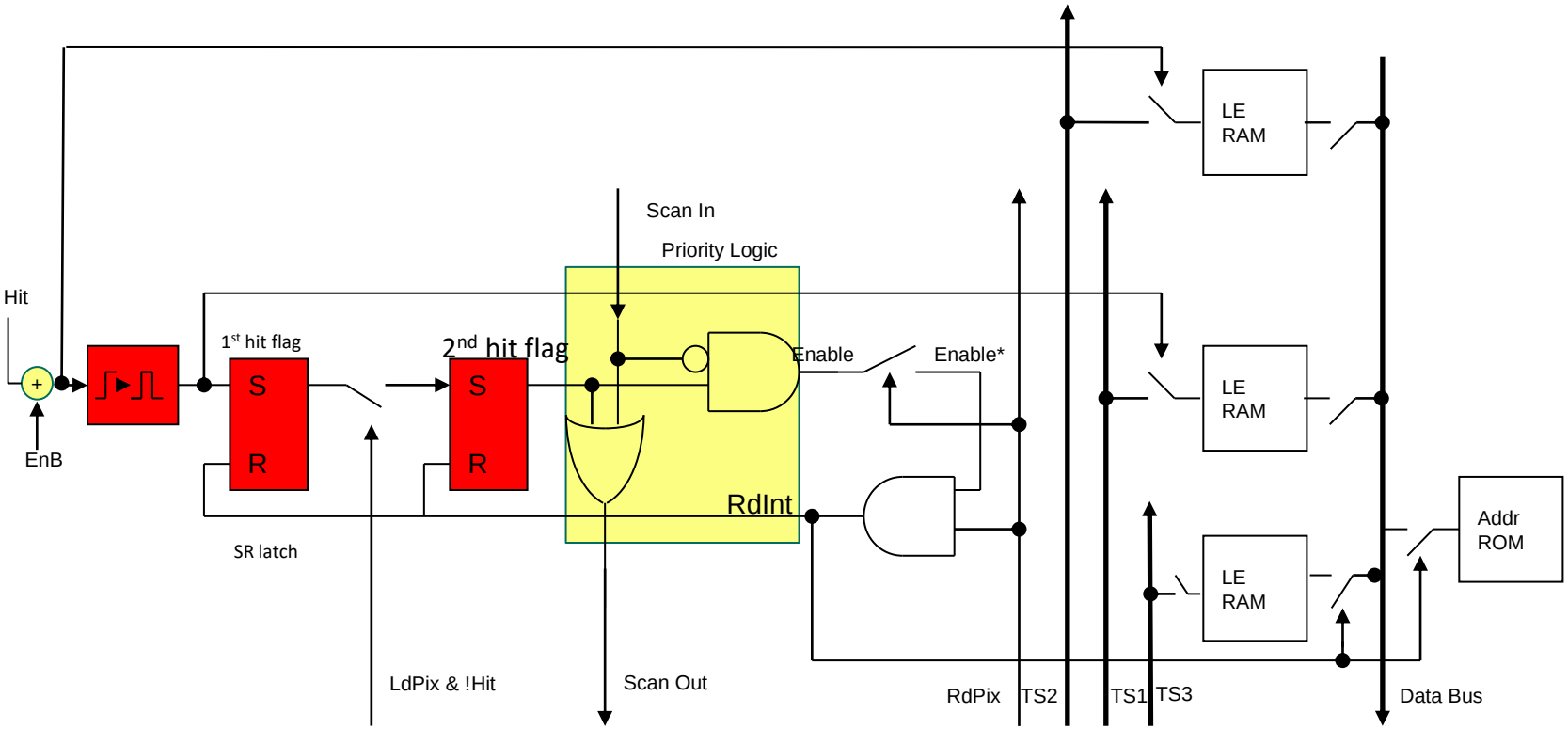
Hit buffer

- Hit buffer logic
  - RAM cell
  - 4-bit Tune DAC
  - Regulated cascode receiver
  - Time to digital converter
  - Main hit buffer logic



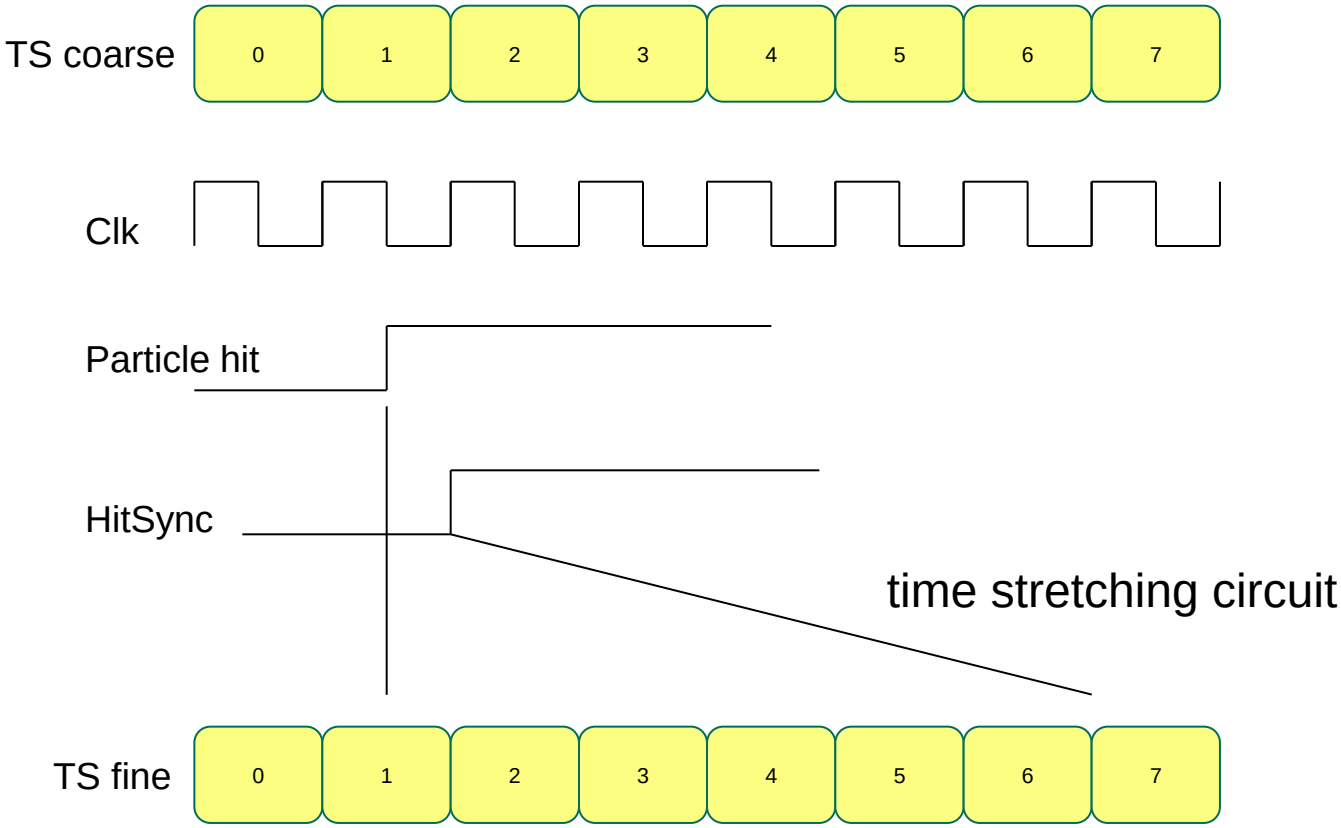
Hit buffer

- Main hit buffer
  - Edge detector
  - Priority logic
  - Address ROM cells
  - Time stamp RAM cells



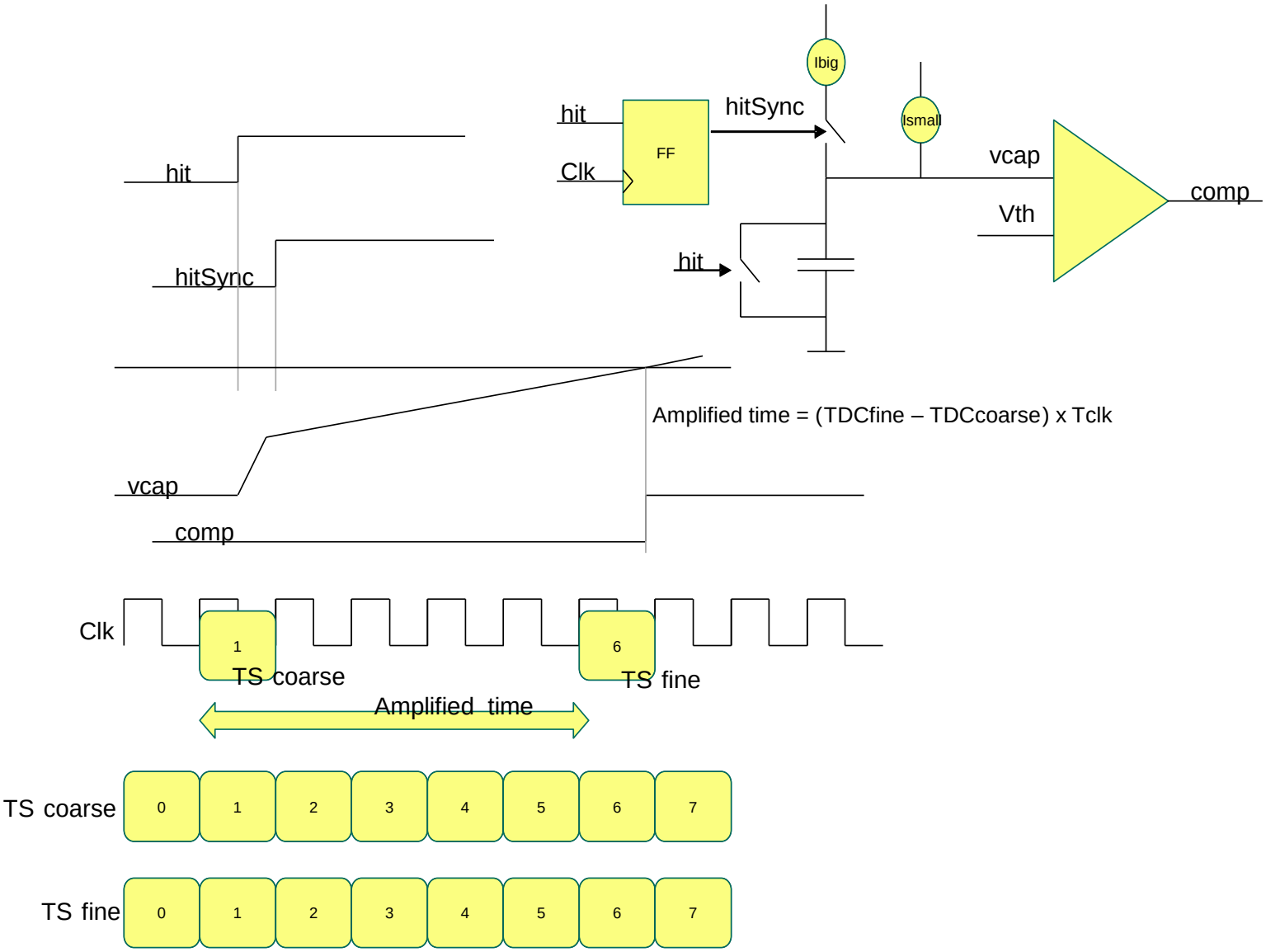
Time to Digital Converter

- Time to digital converter
- The hit time is measured by storing two time stamp values
- Two time stamp counters run with the same period of 10ns and could be reset synchronously



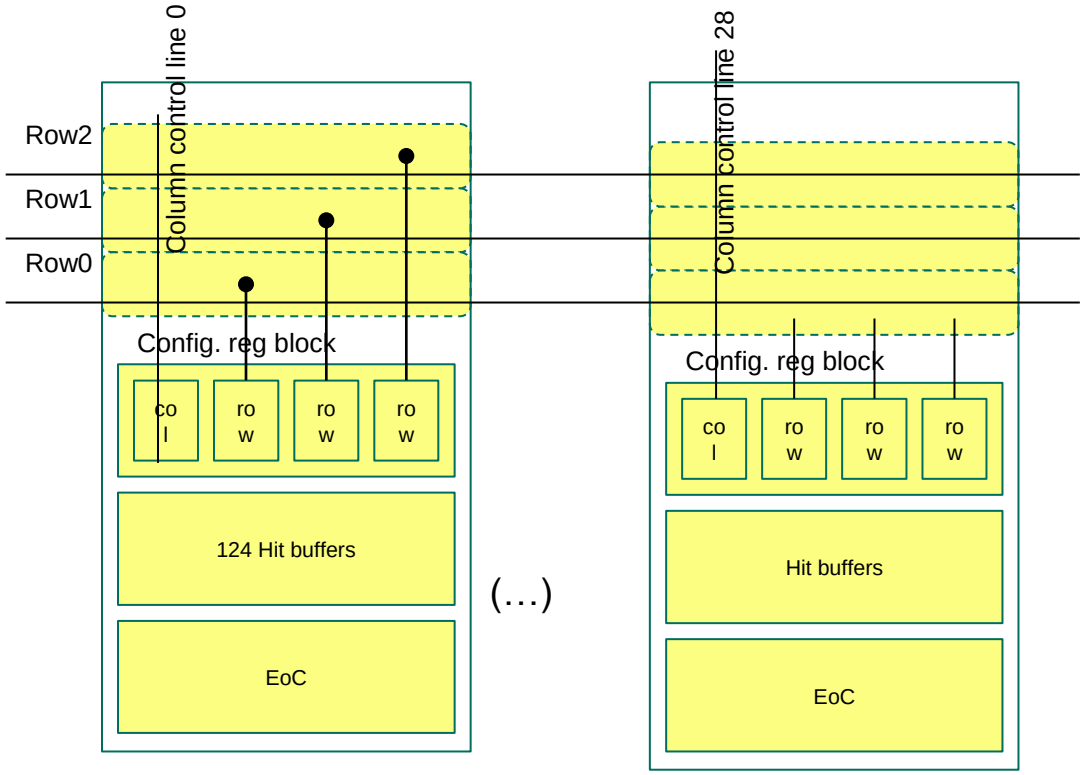
Time to Digital Converter

- Our circuit



End of Column

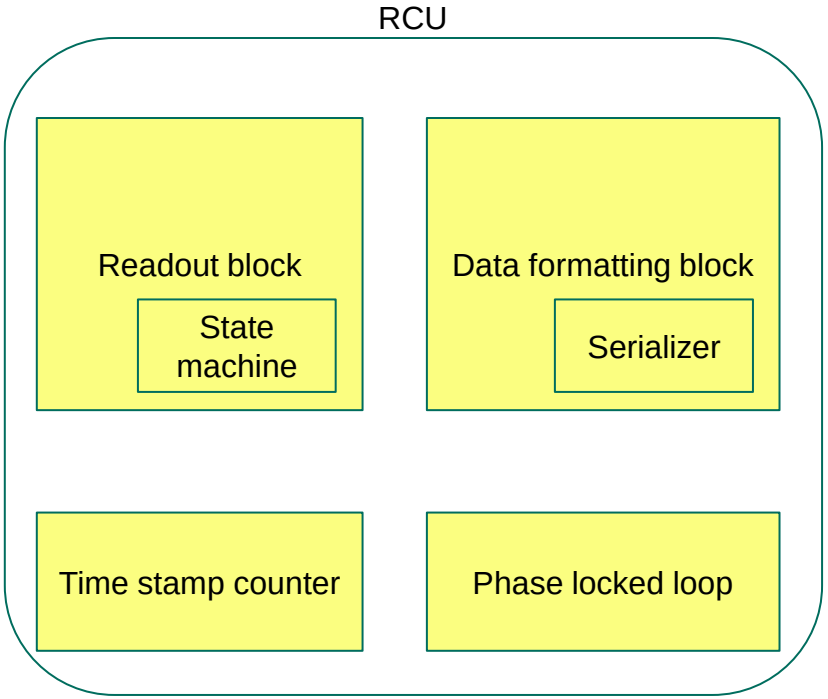
- Data for each event has 55 bits
  - Coarse time stamp (20 bits TS1)
  - Energy measurement (10 bits TS2)
  - Fine time stamp (7 bits TS3)
  - Row Address (10 bits)
  - Column Address (8 bits)
- The time stamp frequency: 100MHz
- TS1 uses two 10-bit counters, one clocked with positive edge and the other with the negative edge



Readout control unit

- Readout block, data formatting block, time stamp counter, Phase locked loop

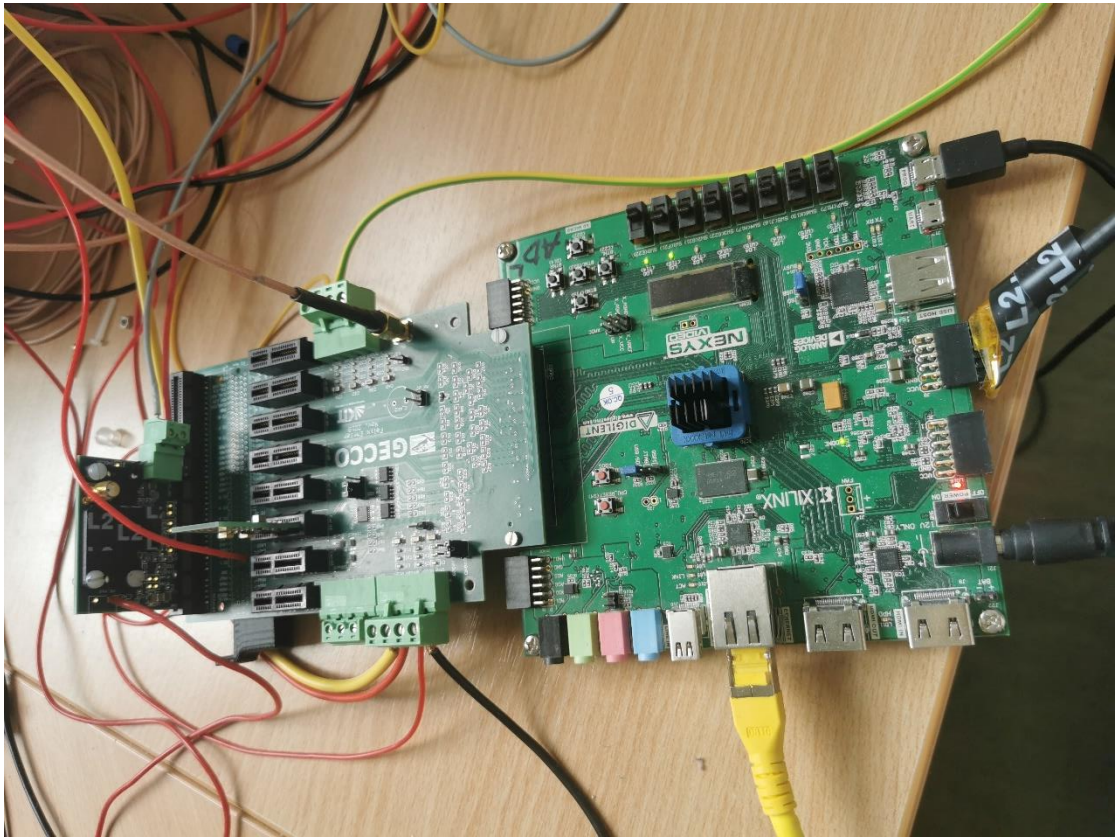
- Readout block comprises a state machine
- Data formatting block performs 8-bit to 10-bit conversion and transmits the data serially
- Serializer is based on a binary tree, and transmits a bit on the rising and falling output clock edge
- PLL input clock of 250 MHz and output clock of maximal 800 MHz
- Maximal data rate: 1.6Gbps



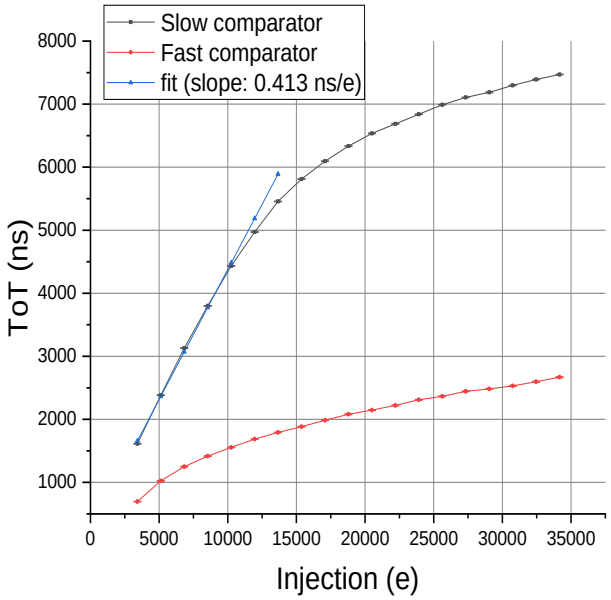
Measurement system

- Test system

- Signal source for measurements is a test signal circuit – a capacitor placed in every pixel
- The test circuit is calibrated with radioactive source

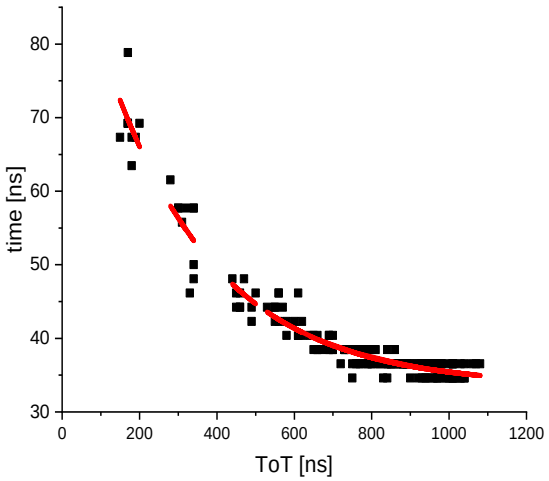


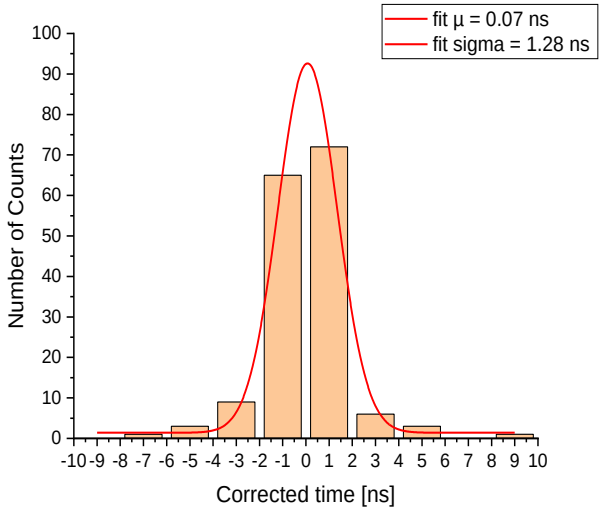
- Pulse width measurement
- The pulse width of slow signal is larger than the fast signal. The sigma value for slow channel is smaller, leading to significantly larger SNR.
- Energy resolution with SNR>1000 possible, the maximum signal limited by the injection circuit



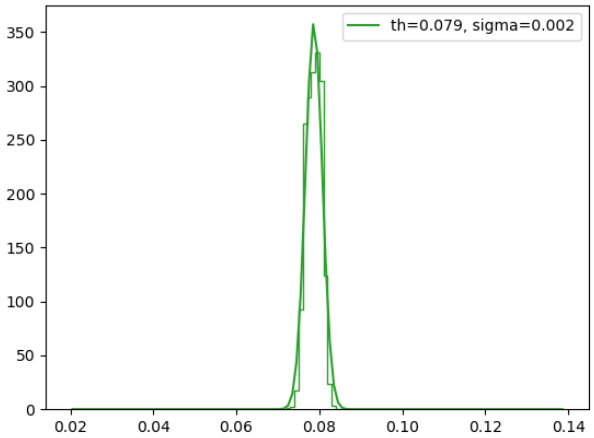
- For 32ke amplifier does not saturate, maximum signal limited by injection circuit
- The average ToT noise is about 48 ns for slow comparator. Its gain can be obtained by fit and it is 0.413 ns/e. If we divide the ToT by gain, we obtain the noise in electrons as 116 e.

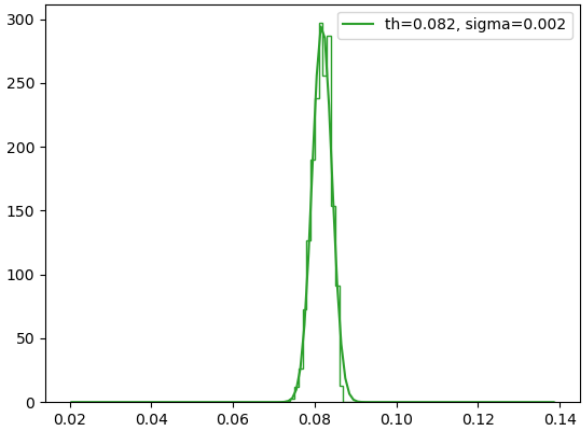
- Comparator response time and pulse width
- The time of threshold crossing is smaller when measured ToT is larger. Exponential function has been fitted to the data and it is used for the time walk correction.
- Time resolution <1ns should be possible





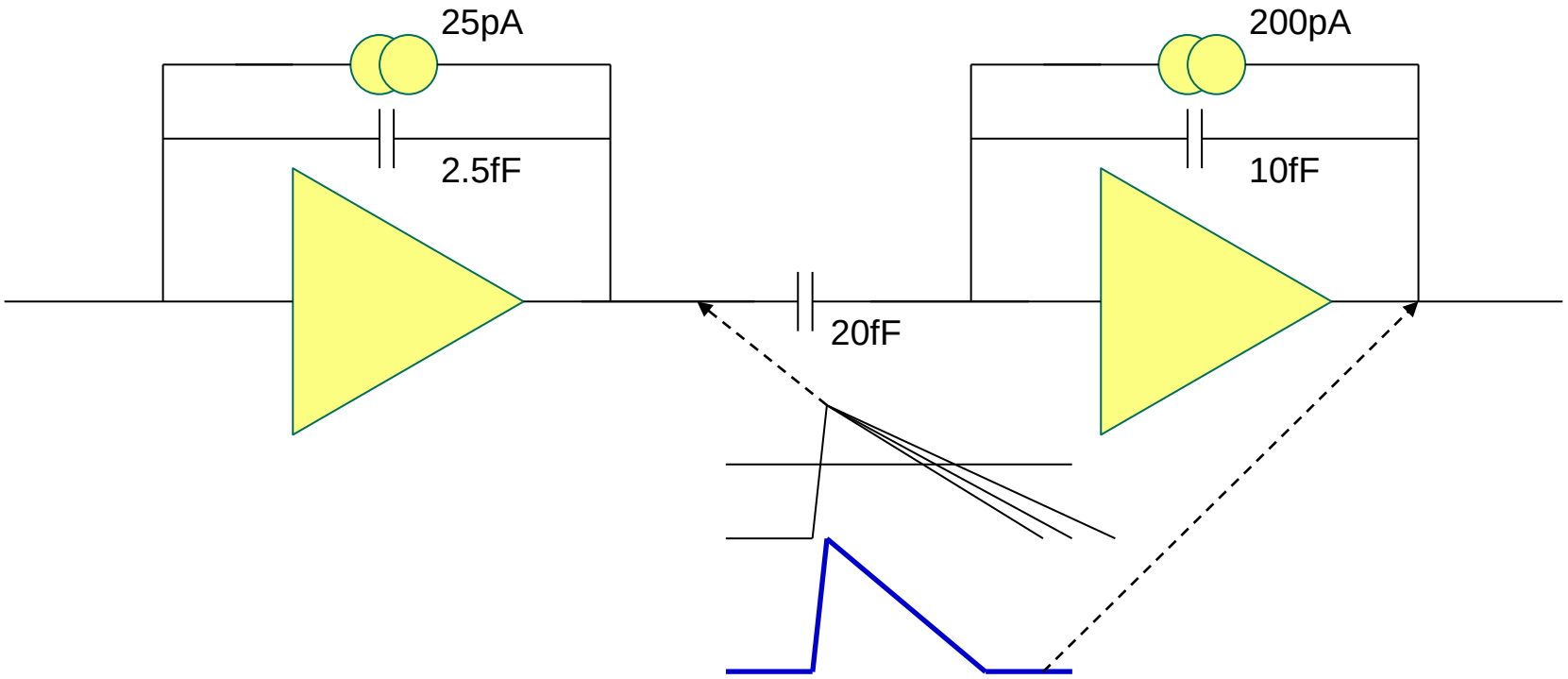
- Threshold dispersion is <60e, both comparators can be tuned





Outlook

- Planned design improvements include:
  - reduce detector capacitance, reduce noise
  - optimize layout design
- Next prototype (named MiniPANDA), with 80 µm x 80 µm pixel size has been completed.
  - Uses two stage amplifier and one comparator
  - Second amplifier improves energy resolution by TOT
  - Uses deep p-well and isolated amplifier
  - Test system ready, results soon
- Following testing of the MiniPANDA ASIC, the full-size sensor will be designed.




thank you