



Hardware Acceleration
LAB



PANDA FEE/DAQ Workshop

DAQ session

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Panda Collaboration Meeting 24/2

24.06.2024



5 years ago

Concepts for PANDA DAQ system

PANDA DAQ problems

- Constant shortage of manpower
- Slow, expensive and risky hardware development cycles
- Many custom hardware components, standards, protocols
 - In fact similar boards: many links, powerful FPGA, differences in memory, clocking, system interfaces
- Time-scale, time-shifts, delays

DAQ-related work packages: Hardware
(R&D, design, testing, production and screening)

- Data-collector board based on EMC digitizer (part of FEE, required by LUMI, EMC (Hit-detection ASIC), other subsystems?) - 7 py
- prototyping, principle investigations (Bochum) - 7 py
- hardware design (Uppsala?) - 7 py
- production screening (Uppsala?) - 7 py
- Data Concentrator - 1 py
- (core of the DAQ, used for the burst-building) - 7 py
- hardware design (Uppsala) - 7 py
- prototype testing/bugging (?) - 7 py
- production screening (Uppsala?) - 7 py
- Compute Node - 7 py
- design/testing/production (HEP) - 7 py
- HPC interface - 7 py
- design/testing/production (KIT?) - 7 py

DAQ-related work packages: Firmware
(R&D, design, testing)

- SODANET - 1 py
- support, development (???) - 0.5 py
- DAQ-accelerator interface (???) - new py
- Framework for data-handling IP cores and communication protocols - 7 py
- development / testing / deployment (???) - 7 py
- Data-processing algorithms - 7 py
- Event-building (???) - 0.5 py
- Burst-building (???) - 7 py
- Tracking (Lancaster) - 7 py
- FW tracking (Krakow) - 7 py
- EMC Clustering, support (???) - 7 py

DAQ-related work packages: Software
(R&D, design, testing)

- DAQ functionality (so far only SODANET protocol) (???)

Mosaic of custom elements

- Hardware
 - Subsystems FEE
 - Data Concentrators
 - SODANet distribution
 - Compute Nodes
 - High-Flex cards
- Protocols
 - Subsystem internal
 - SODANet
 - Raw 8/10b
 - InfiniBand
- Systems, interfaces
 - Standalone
 - ATCA
 - AMC
 - PCIe

Push-Only Readout

4 (MVD) + 16 (STT) + 20 (BDIRC) + 9 (EDIRC) + 0.6 (BTOF) + 12.7(EMC) + 24(FwTracker) = **86.3 Gbit/s**

Compute Nodes -5 ATCA modules

High-flex readout card PC → InfiniBand to HPC

M. Kavatsyuk

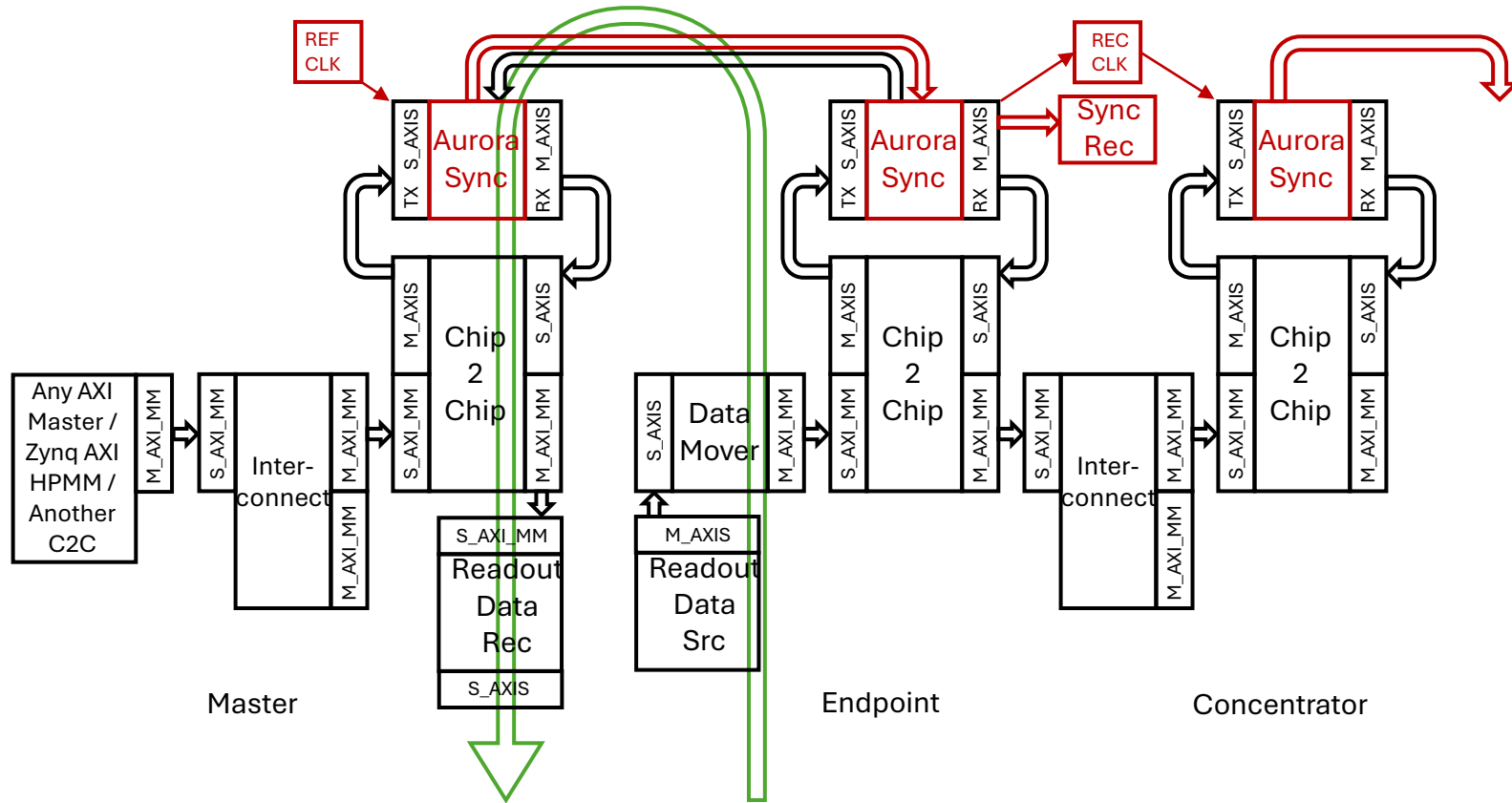
9 December 2019, Kraków

Now

- Subdetector subsystem specific readouts continue stable development
- Multitude of parallel developments
 - Multiple SADC firmware sets
 - ...
 - Complete TRB-based systems
 - ...
 - At least 3 implementations of GbE
 - ...
 - Data Concentrators with Kintex and Zynq
 - E.t.c...
- Prototype system based on Aurora-Sync
 - Set of components to build complete synchronous DAQ on Xilinx platforms
 - Prototype set up but not yet evaluated

Aurora Sync

- Regular Aurora GT enhanced with synchronous mode
 - Synchronization pulse and clock distribution
 - No external PLL required
 - All Xilinx GT families
 - Platform independent (Xilinx FPGA and GT required)
- Logic components architecture
 - Master (clock and sync pulse source)
 - Endpoint (sync receiver, data source)
 - Concentrator (Endpoint, data agregator, Eth gateway)
- AXI-based infrastructure
 - Stream to memory-mapped converters
 - Facilitated IP integration
 - Suitable for preprocessing in HLS
 - Native control and monitoring (petalinux with memory R/W operations)
- 10G Eth UDP from the Concentrators
 - To be processed by the online servers



However

- Considering:
 - Timescale for PANDA
 - PANDA Satellite activities
 - Integration with CB-ELSA, CBM, AMBER, A1, ... required
- **Focus on optimizing the subsystems and integration**
- **Explore new solutions and technologies**
- **Search for synergies**

- **Search for future-proof solutions**
- **Easy to maintain, upgrade**
- **Supported by the community or well-established in the industry**

- Physics and the detector design (almost) didn't change
 - E.g. PANDA EMC TDR published in 2008
- Technology keeps progressing
 - E.g GPU 1.3 TFLOPs in 2008 vs 35 TFLOPs in 2020 vs 82 TFLOPs in 2022

The DAQ session

09:00	DAQ intro <i>AUD</i>	<i>Grzegorz Korcyl</i> 09:00 - 09:10
	CBM DAQ overview <i>AUD</i>	<i>David Emschermann</i> 09:10 - 09:40
	CRI firmware <i>AUD</i>	<i>Dr Wojciech Zabolotny</i> 09:40 - 10:10
10:00	NestDAQ <i>AUD</i>	<i>Ken Suzuki</i> 10:10 - 10:40
11:00	Coffee <i>AUD</i>	10:45 - 11:15
	CB-ELSA DAQ system <i>AUD</i>	<i>Jan Hartmann</i> 11:15 - 11:55
12:00	PANDA-Phase0 Mainz DAQ <i>AUD</i>	<i>Oliver Noll</i> 11:55 - 12:15
	AMBER DAQ <i>AUD</i>	<i>Igor Konorov</i> 12:15 - 12:35
	Status of the Kintex Data Concentrator <i>AUD</i>	<i>Pawel Marciniewski</i> 12:35 - 12:55
13:00	Status of the Zynq Data Concentrator <i>AUD</i>	<i>Olena Manzhuira</i> 12:55 - 13:15