Hardware Acceleration
LAB

PANDA FEE/DAQ Workshop
DAQ session

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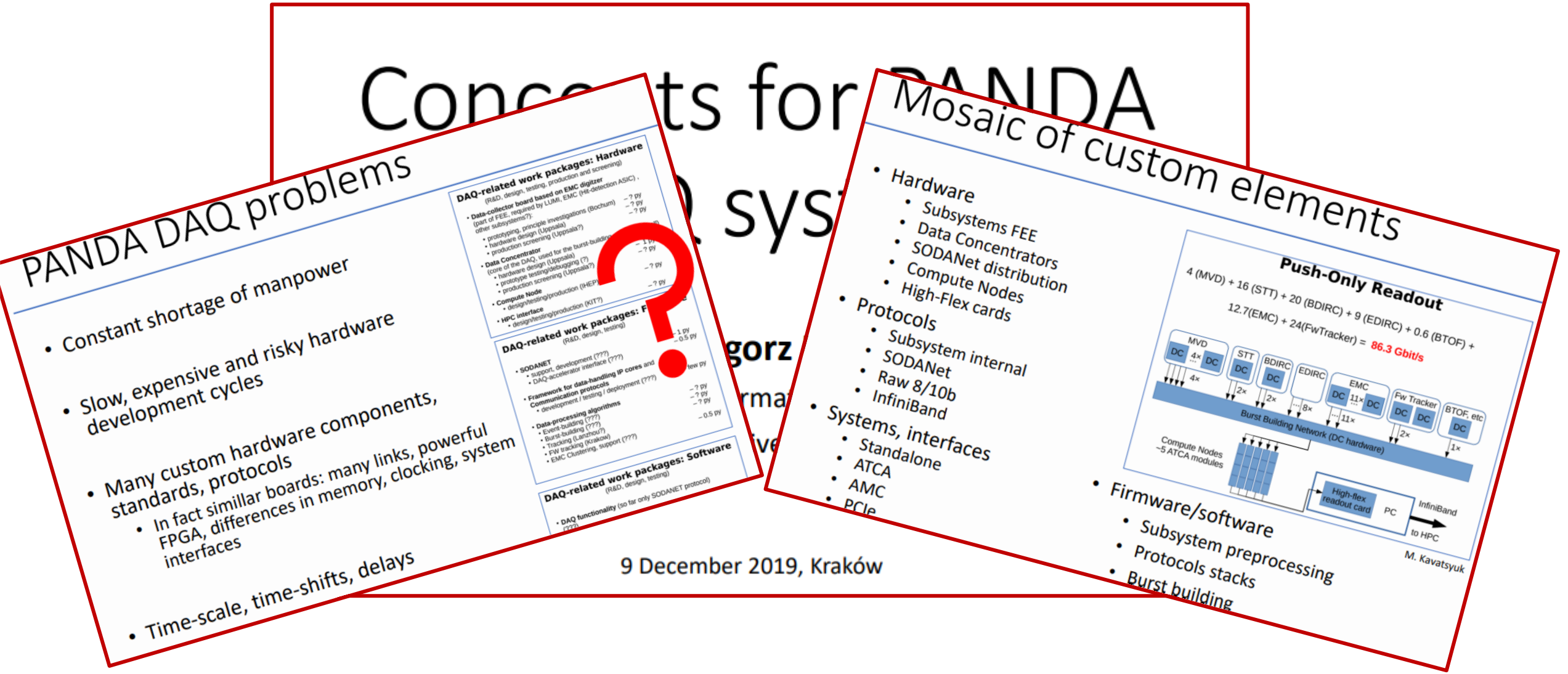
Panda Collaboration Meeting 24/2

24.06.2024

5 years ago


PANDA DAQ problems
Constant shortage of manpower
Slow, expensive and risky hardware development cycles
Many custom hardware components, standards, protocols
In fact simillar boards: many links, powerful FPGA, differences in memory, clocking, system interfaces
Time-scale, time-shifts, delays
DAQ-related work packages: Hardware
DAQ-related work packages: Software
Mosaic of custom elements
Hardware
Subsystems FEE
Data Concentrators
SODANet distribution
Compute Nodes
High-Flex cards
Protocols
Subsystem internal
SODANet
Raw 8/10b
InfiniBand
Systems, interfaces
Standalone
ATCA
AMC
Push-Only Readout
4 (MVD) + 16 (STT) + 20 (BDIRC) + 9 (EDIRC) + 0.6 (BTOF) +
12.7(EMC) + 24(FwTracker) = 86.3 Gbit/s
Burst Building Network (DC hardware)
Compute Nodes ~5 ATCA modules
High-flex readout card
PC
InfiniBand
to HPC
Firmware/software
Subsystem preprocessing
Protocols stacks
Burst building
M. Kavatsyuk
9 December 2019, Kraków

Now

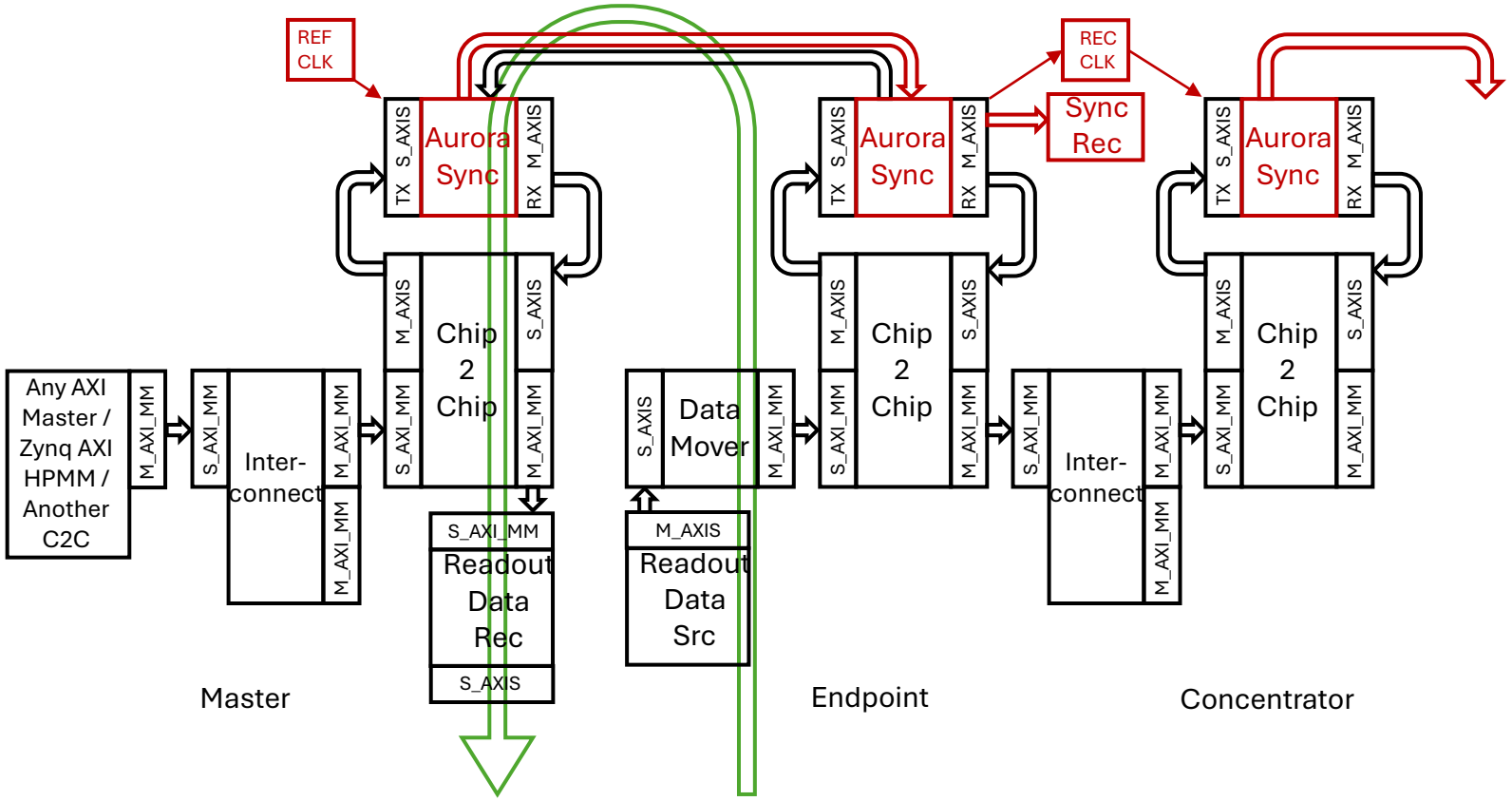
- Subdetector subsystem specific readouts continue stable developement

- Multitude of parallel developments
  - Multiple SADC firmware sets
  - …
  - Complete TRB-based systems
  - …
  - At least 3 implementations of GbE
  - …
  - Data Concentrators with Kintex and Zynq
  - E.t.c…

- Prototype system based on Aurora-Sync
  - Set of components to build complete synchronous DAQ on Xilinx platforms
  - Prototype set up but not yet evaluated

Aurora Sync

- Regular Aurora GT enhanced with synchronous mode
  - Synchronization pulse and clock distribution
  - No external PLL required
  - All Xilinx GT families
  - Platform independent (Xilinx FPGA and GT required)
- Logic components architecture
  - Master (clock and sync pulse source)
  - Endpoint (sync receiver, data source)
  - Concentrator (Endpoint, data agregator, Eth gateway)
- AXI-based infrastructure
  - Stream to memory-mapped converters
  - Facilitated IP integration
  - Suitable for preprocessing in HLS
  - Native control and monitoring (petalinux with memory R/W operations)
- 10G Eth UDP from the Concentrators
  - To be processed by the online servers



However

- Considering:
  - Timescale for PANDA
  - PANDA Satellite activities
    - Integration with CB-ELSA, CBM, AMBER, A1, … required

- **Focus on opitimizing the subsystems and integration**
- **Explore new solutions and technologies**
- **Search for synergies**

- **Search for future-proof solutions**
- **Easy to maintain, upgrade**
- **Supported by the community or well-established in the industry**

- Physics and the detector design (almost) didn’t change
  - E.g. PANDA EMC TDR published in 2008
- Technology keeps progressing
  - E.g GPU 1.3 TFLOPs in 2008 vs 35 TFLOPs in 2020 vs 82 TFLOPs in 2022

The DAQ session