

# Module and ladder characterization and burn-in tests of the STS for the CBM experiment

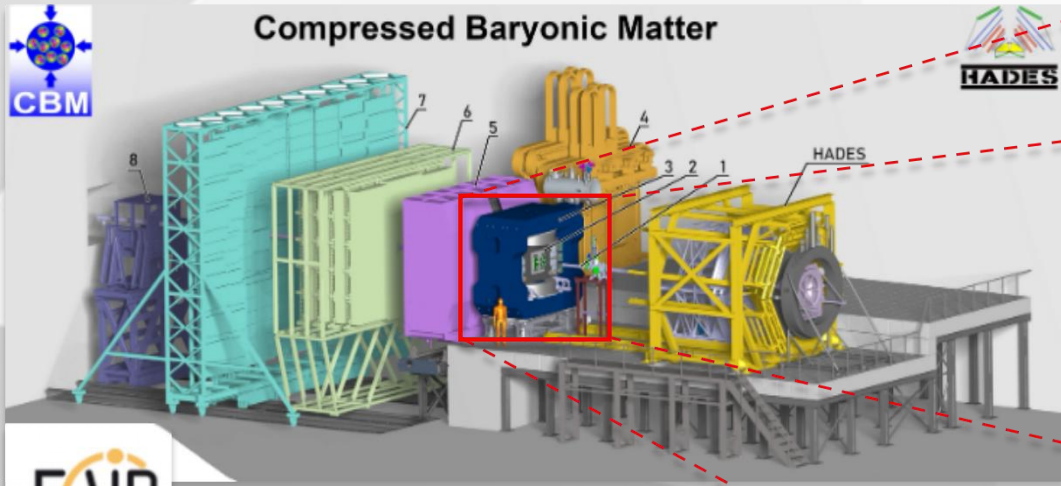
FAIRNESS 2024

L.M. Collazo Sánchez<sup>1,2</sup>, A. Rodríguez Rodríguez<sup>2</sup>, D. Rodríguez Garcés<sup>1,2</sup>, M. Teklishyn<sup>2</sup>  
for the CBM Collaboration

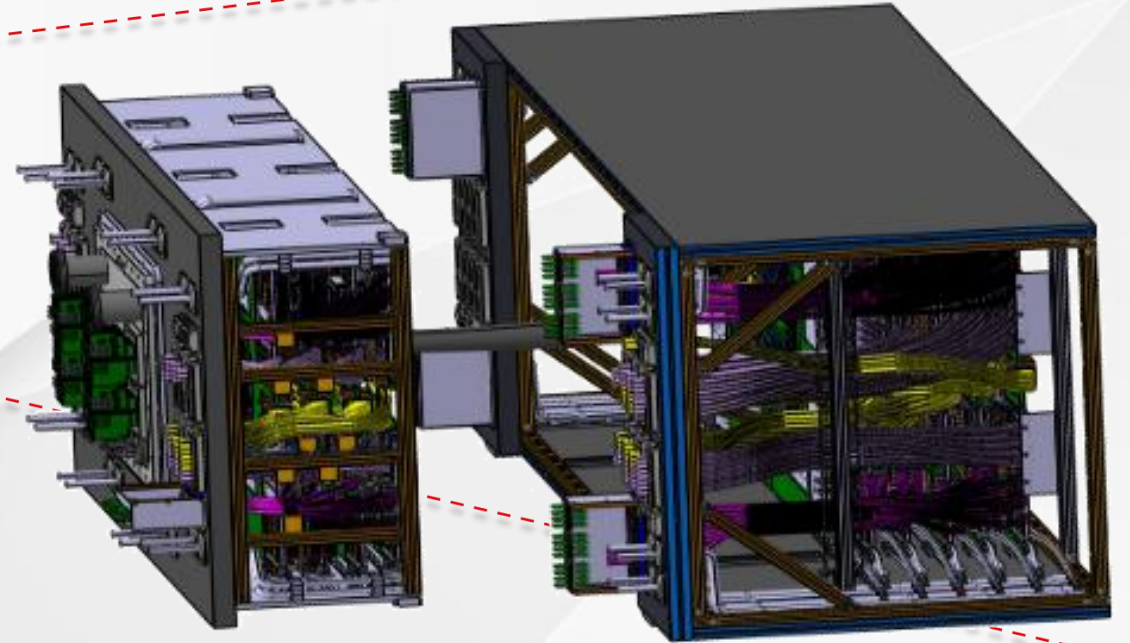
<sup>1</sup>Goethe-Universität (Frankfurt), <sup>2</sup>GSI (Darmstadt)

September 26<sup>th</sup>, 2024

# The CBM experiment - STS



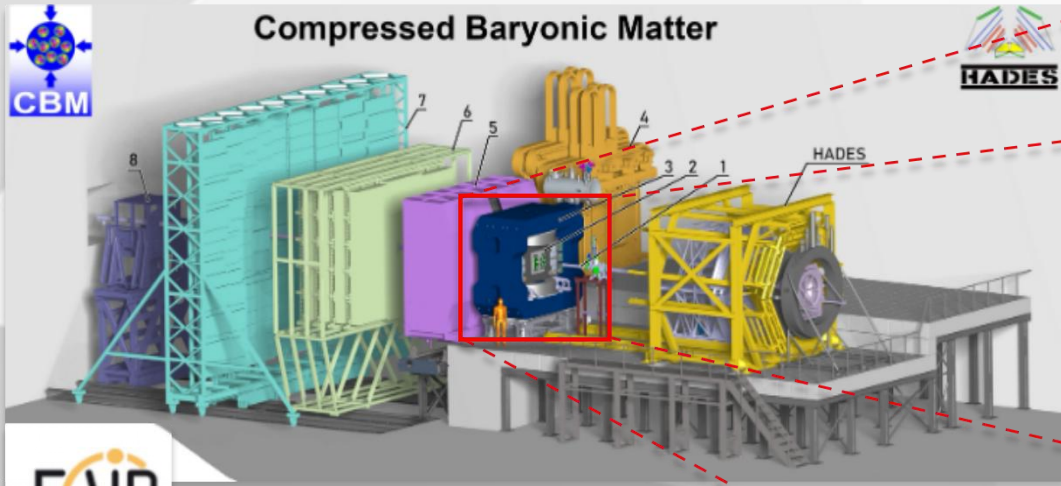
## The STS Silicon Tracking System



The **CBM** experiment intends to explore the QCD phase diagram in the region of high baryon densities using high-energy nucleus-nucleus collisions.

- The measurements will be performed at beam-target interaction rates up to 10 MHz.
- Maintaining material budget within 2 – 8%  $X_0$ .
- High granularity, spatial, and timing precision.

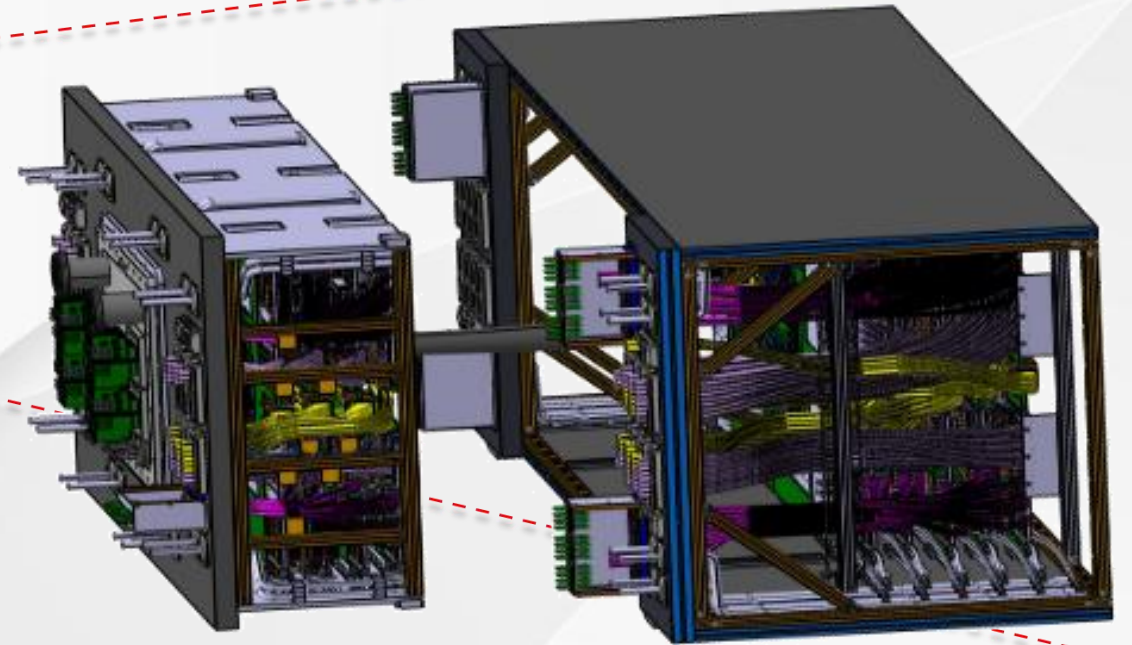
# The CBM experiment - STS



The **CBM** experiment intends to explore the QCD phase diagram in the region of high baryon densities using high-energy nucleus-nucleus collisions.

- The measurements will be performed at beam-target interaction rates up to 10 MHz.
- Maintaining material budget within 2 – 8%  $X_0$ .
- High granularity, spatial, and timing precision.

## The **STS** Silicon Tracking System



- A novel integration approach was employed where the read-out electronics are placed outside of the sensitive volume.

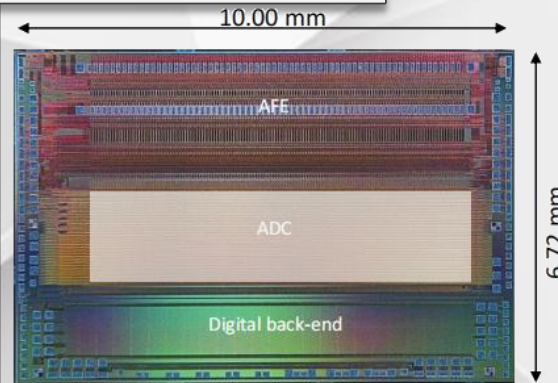
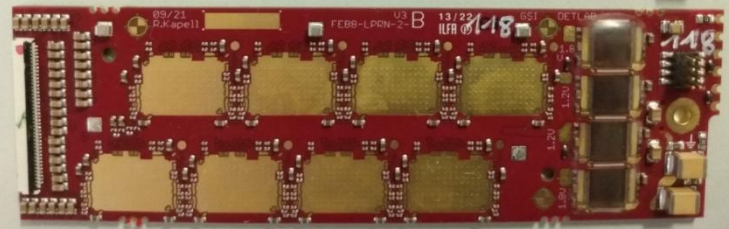
# CBM - STS module

STS detector consists of **876** DSDM micro-strip modules.

Each double-sided silicon strip sensor is connected via a stack of low-mass microcables to two Front-End Boards (FEBs).



Each FEB has eight custom-designed STS-XYTER ASIC (SMX).

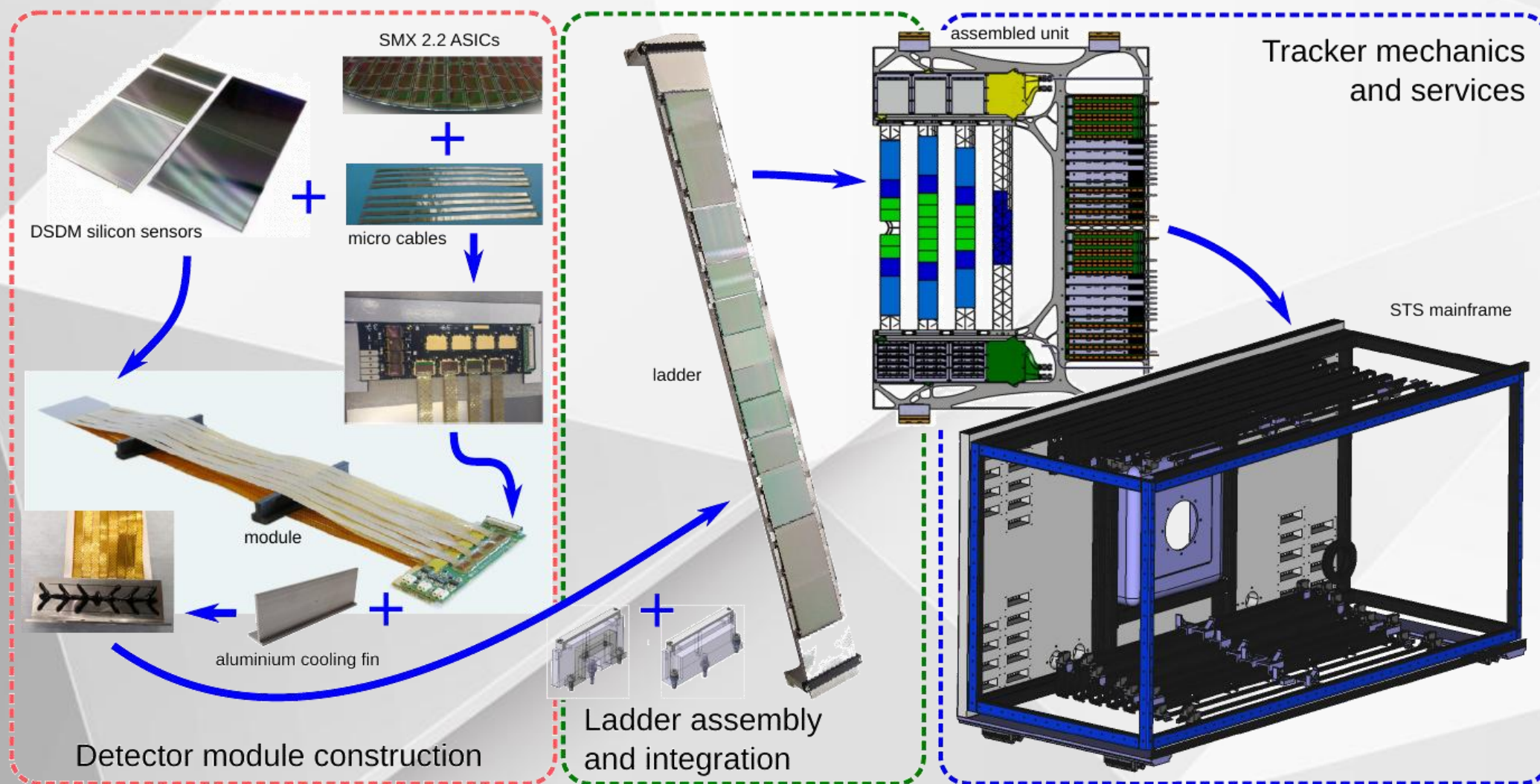


The STS-XYTERv2 ASIC under the microscope.

After module assembly, a 2.7 mm thick aluminum cooling shelf is glued (STYCAST) between FEBs. Necessary step to ensure proper cooling of the FEB (Average power dissipation per FEB  $\sim 11$  W).



# STS assembling sequence and structure



- **40** C Frames in STS
- Each C Frame contains between two and four ladders

- Each Ladder carries up to 10 modules
- In total STS will be built with **106** ladders and **876** modules

# Module and ladder characterization

## Module Assembly



STS has started the module series production

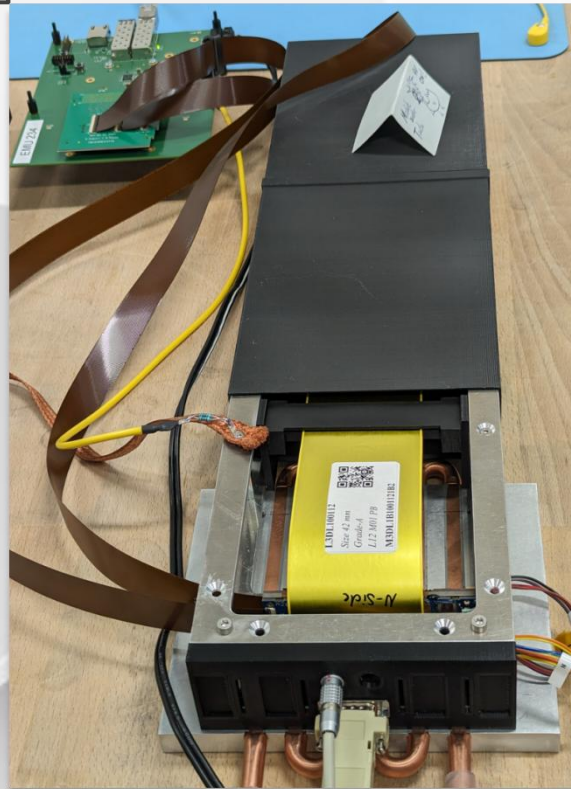
Produced: 264 (30% of total)  
Tested: 181 (20.6% of total)  
Assembled in Ladder: 26

# Module and ladder characterization

Module Assembly

Reverse bias  
voltage scan

Electrical and  
functional test



STS has started the module  
series production

Produced: **264** (30% of total)  
Tested: **181** (20.6% of total)  
Assembled in Ladder: **26**

# Module and ladder characterization

Module Assembly

Reverse bias voltage scan

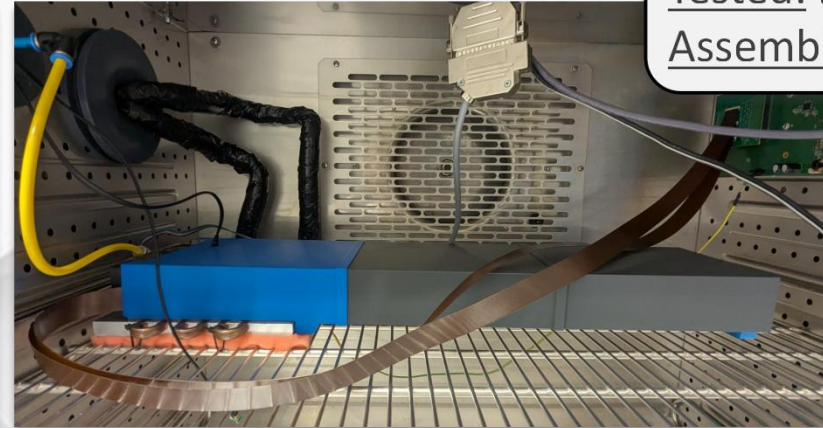
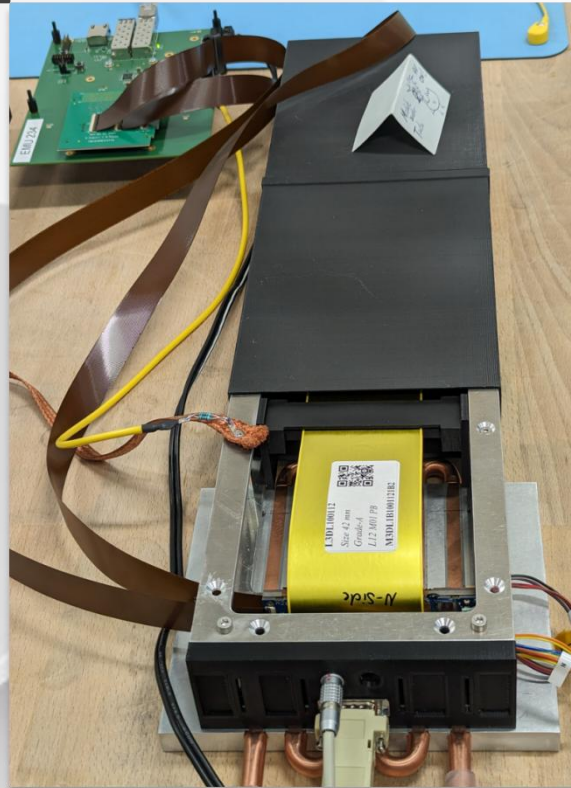
Electrical and functional test

Thermal Test (Burn-in)



STS has started the module series production

Produced: **264** (30% of total)  
Tested: **181** (20.6% of total)  
Assembled in Ladder: **26**





# Module and ladder characterization

Module Assembly

Reverse bias voltage scan

Electrical and functional test

Thermal Test (Burn-in)

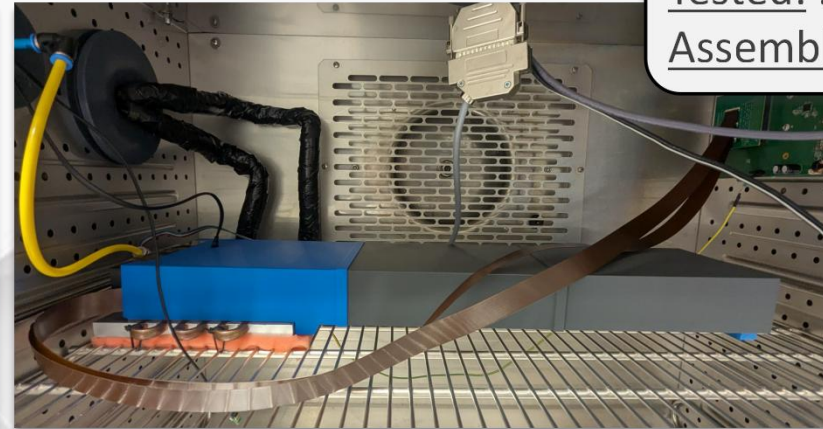
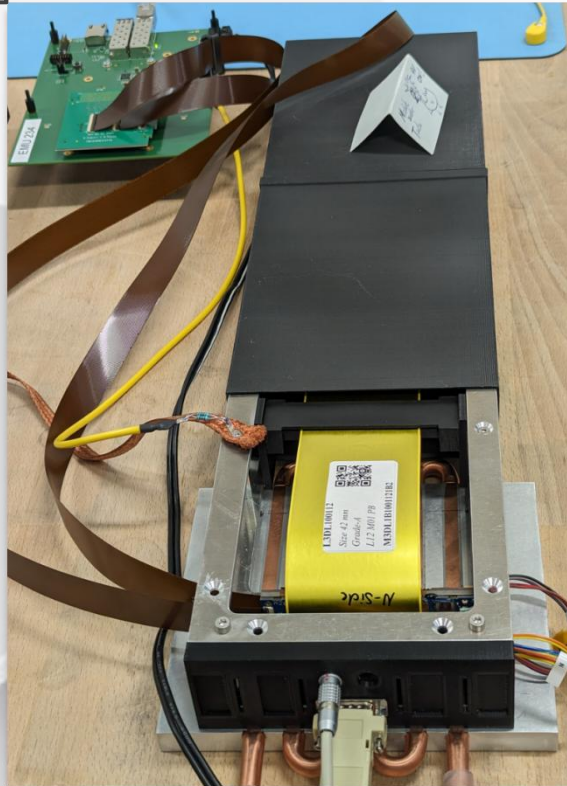
Ladder Assembly

Ladder Testing

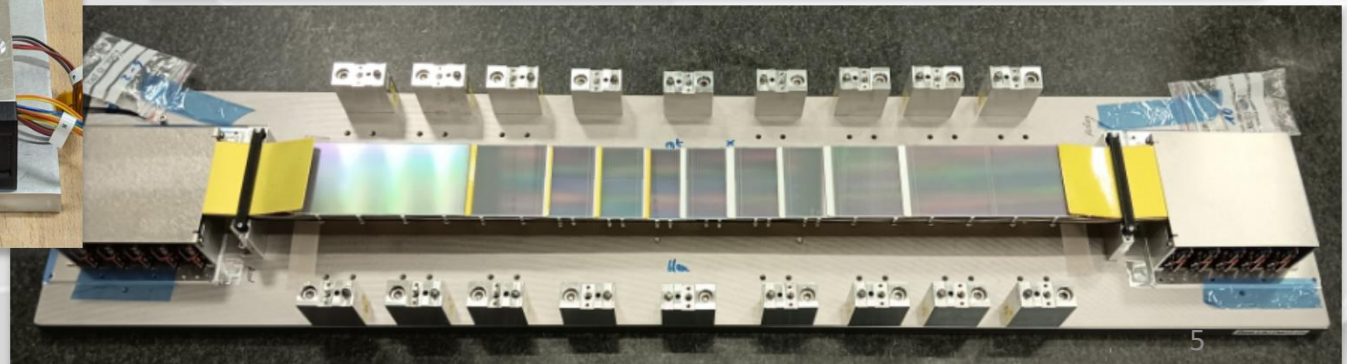


STS has started the module series production

Produced: **264** (30% of total)  
Tested: **181** (20.6% of total)  
Assembled in Ladder: **26**



Quality Assurance grade ready for Ladder Assembly



# Module and ladder characterization

Module Assembly

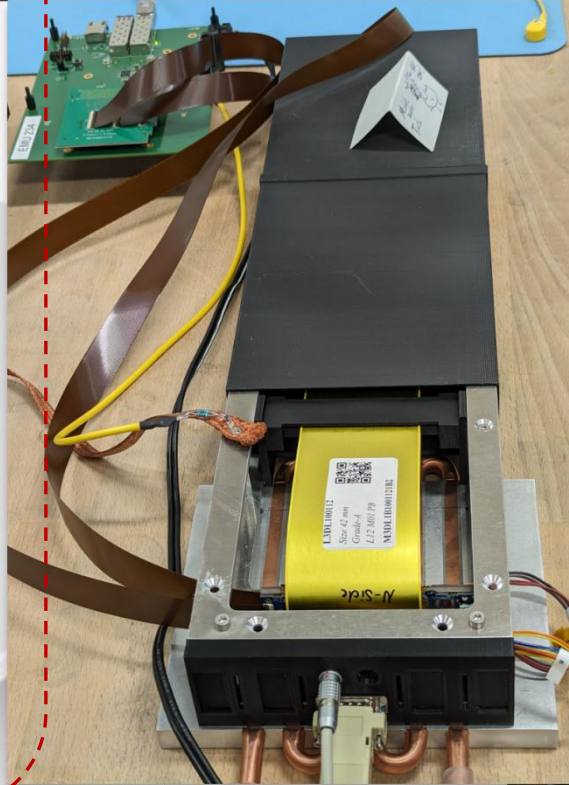
Reverse bias voltage scan

Electrical and functional test

Thermal Test (Burn-in)

Ladder Assembly

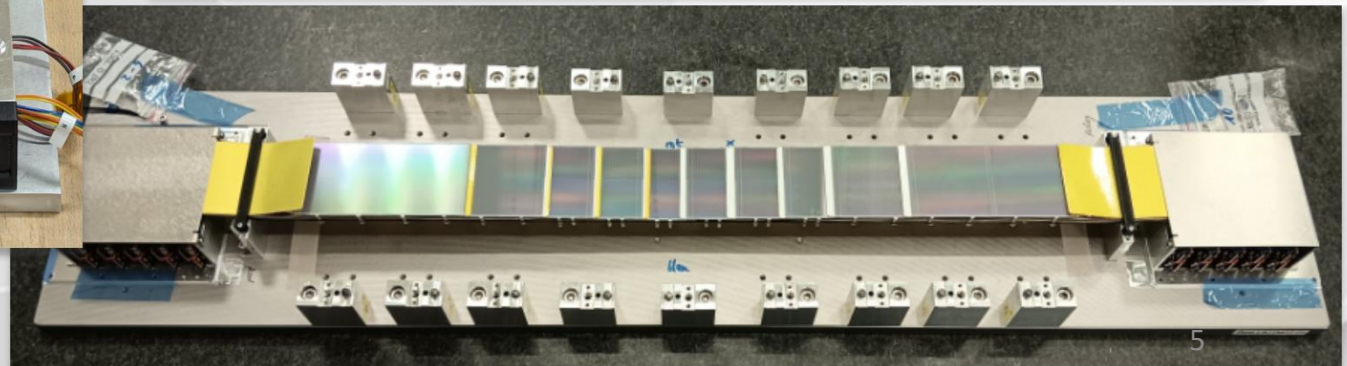
Ladder Testing



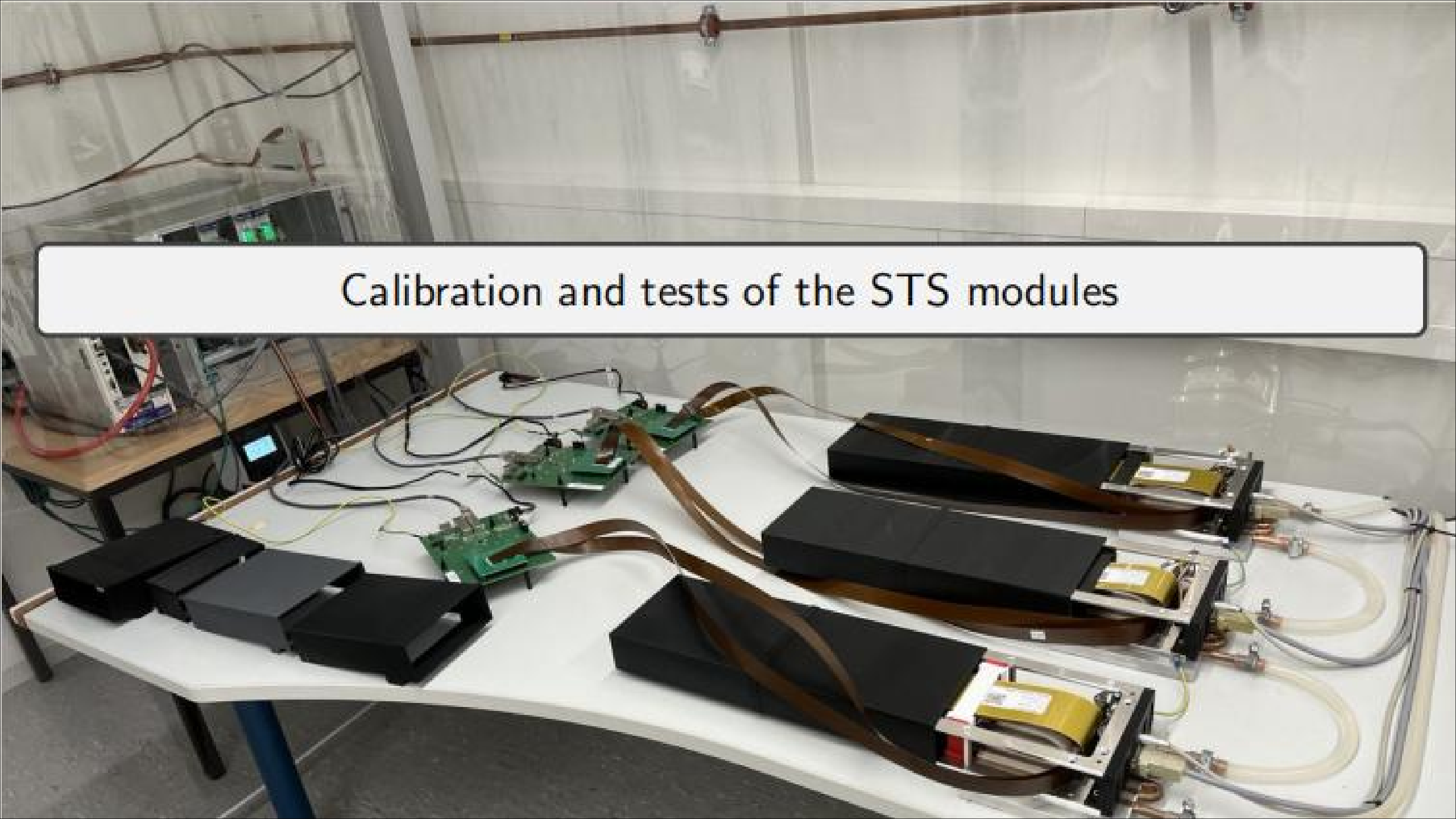
STS has started the module series production

Produced: **264** (30% of total)  
Tested: **181** (20.6% of total)  
Assembled in Ladder: **26**

Quality Assurance grade ready for Ladder Assembly



## Calibration and tests of the STS modules



# How do we test the modules?

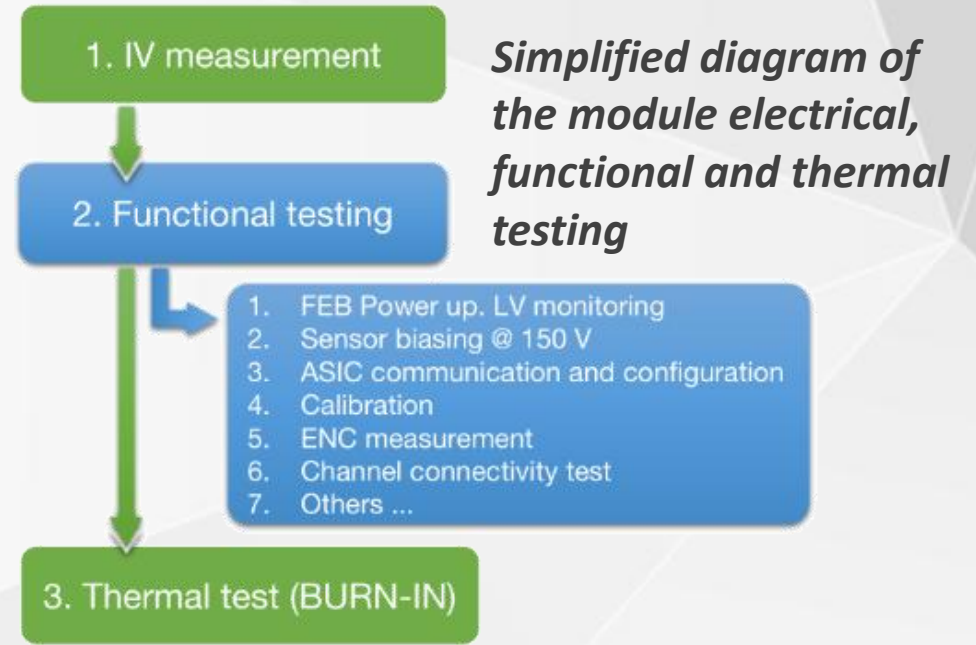
## Module Testing & Burn-in

First step:

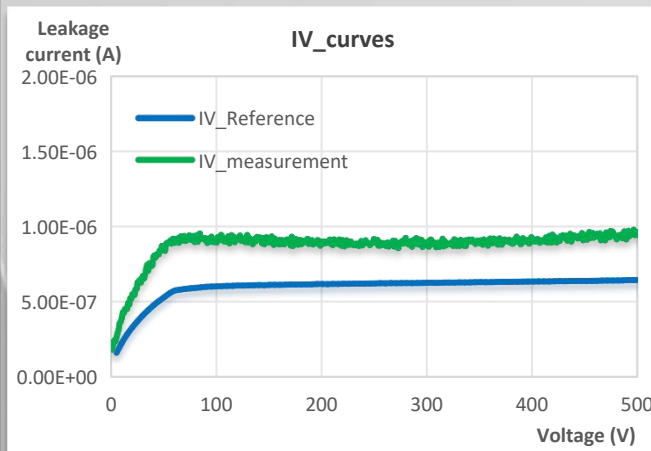
- Placing the module in a carrier

Main objectives of Module Testing:

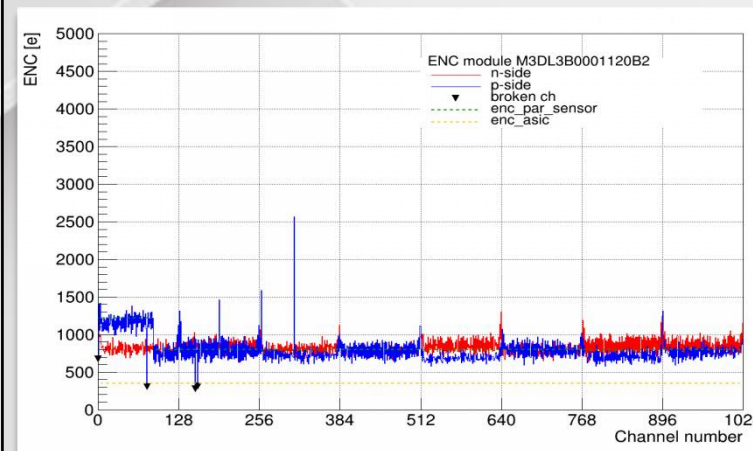
- Evaluate modules functional operation
  - Sensor current-voltage characteristic (IV)
  - Calibrate the Front-End Electronics (FEE)
  - Estimate noise level
- Evaluate the thermal performance of the full assembly object at the final operational temperatures



### Reverse bias voltage scan

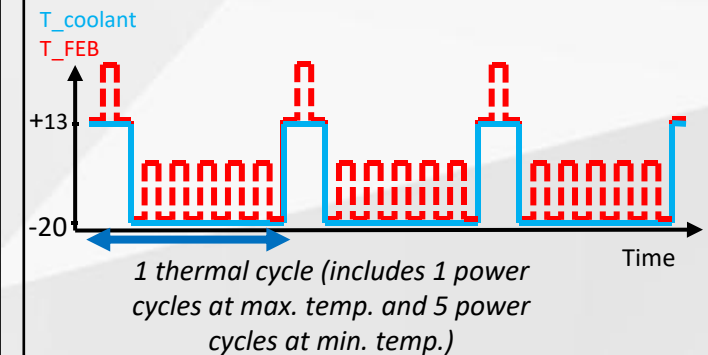


### Electrical & Functional Tests



### Burn-in

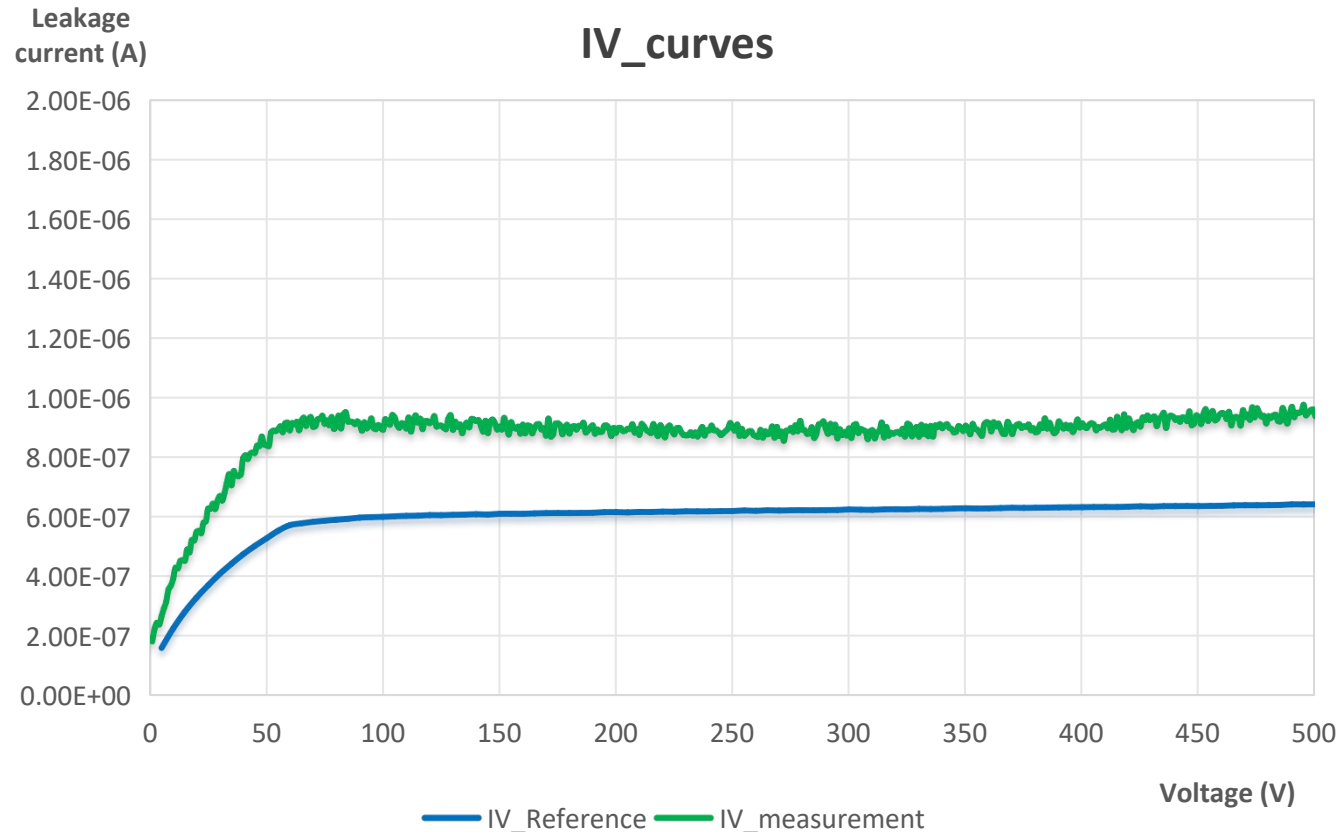
STS operation temperature:  $-20^{\circ}\text{C}$



# Voltage scan

## Module Testing

### Reverse bias voltage scan



One IV setup:

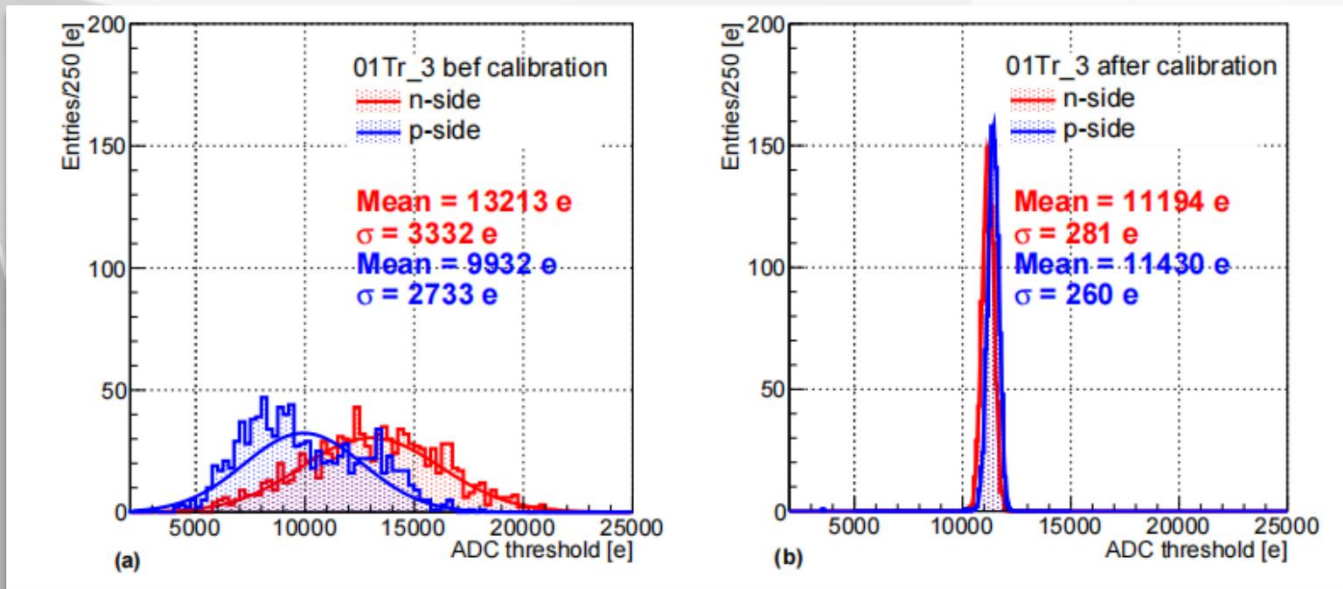
- a module / every 25 min
- It allows to compare the measurements with the results of the Electrical Inspection.
- A sensor is assigned to a given position in the detector according to the particle flux that it will receive in operation so that the best grades will go to the region of higher exposure to particle, and the sensor is biased depending on the assigned grade.
- Edge cleaning and thermal treatment for modules identified with an early breakdown. Possibility to recover modules with IV issues due to high humidity.

# Functional performance

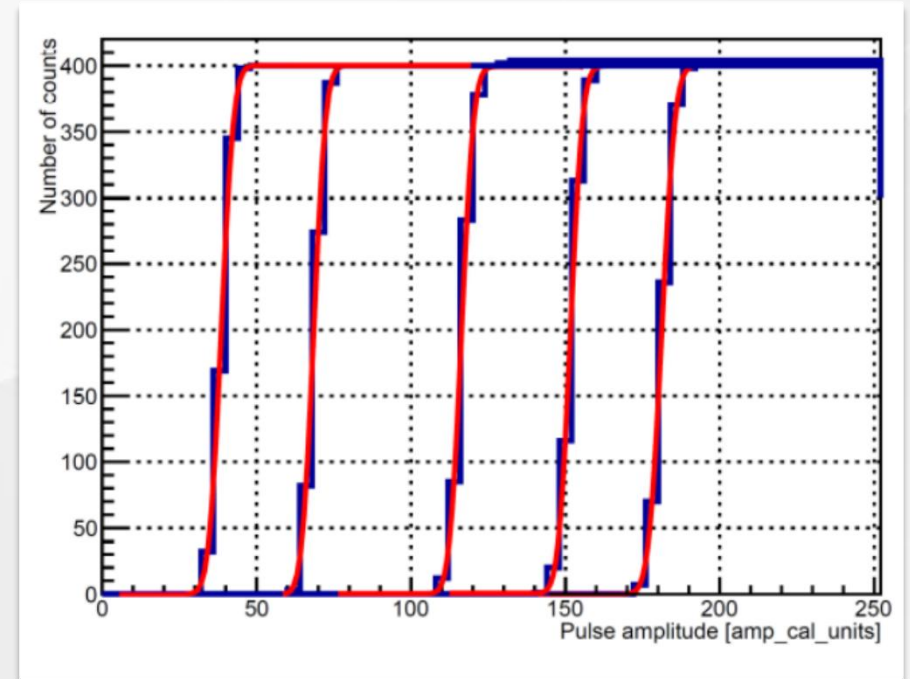
## Module Testing

### Functional Tests

- Three modular testing setups:
  - The possibility to study a module with issues while continuing with regular series testing



**Comparison of the ADC threshold distribution before (a) and after (b) charge calibration.**



- The response function of each discriminators in a channel are fitted with erfc.
  - mean represents the effective discriminator threshold
  - $\sigma$  represents the ENC value in units of the internal pulse generator

# Functional performance

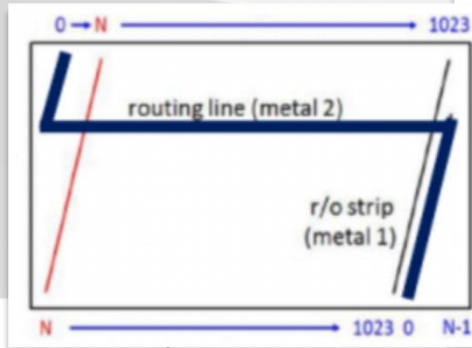
## Module Testing

### Functional Tests

- Check ASICs functionalities:
  - downlinks, uplinks
  - ASIC potentials VDDM, temperature
- Module ADC calibration
- ENC performance
- Identification of broken channels

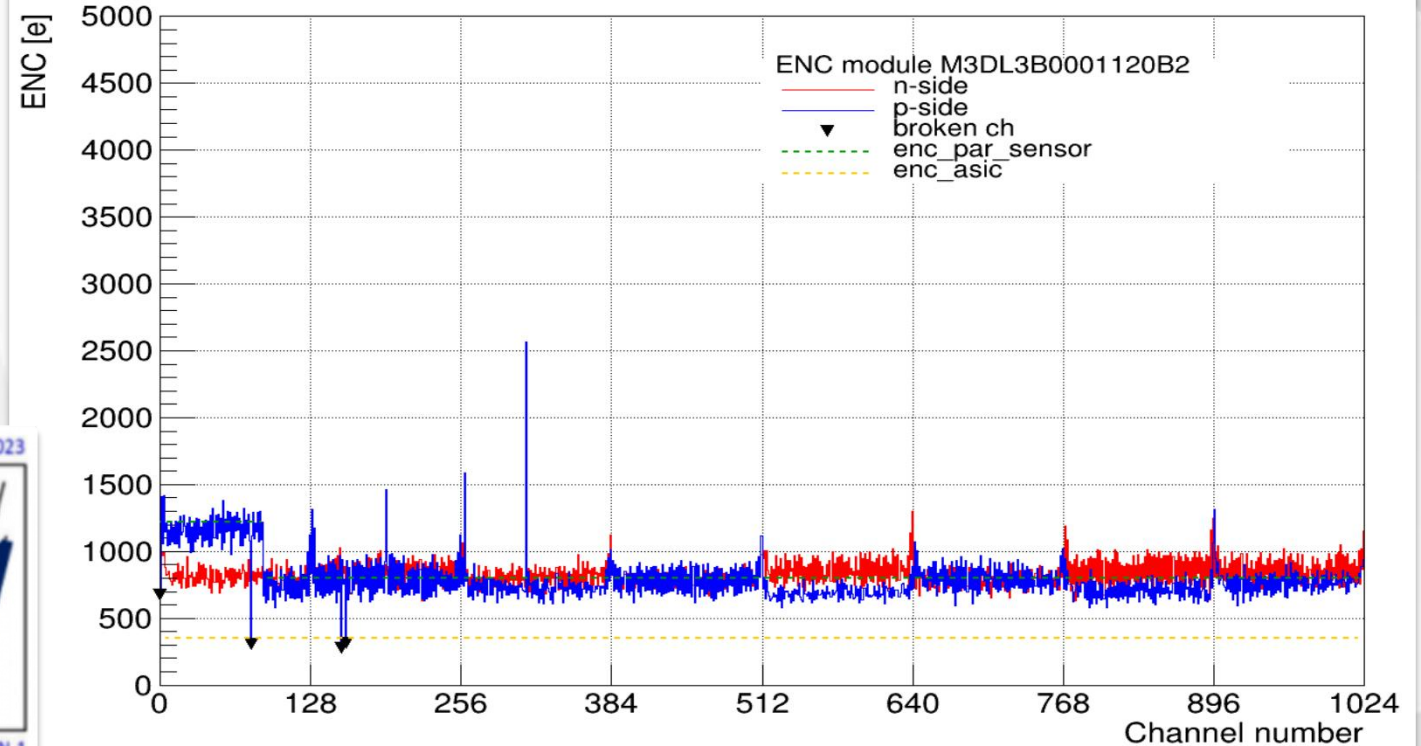
Z-strip: 17 pF extra from the double metal routing

[Panasenko, I., Ph.D. diss., Univ. of Tübingen, 2022.](#)



$$ENC = \left[ \underbrace{L_{\text{sensor}} \cdot 1.02 \frac{\text{pF}}{\text{cm}}}_{\text{sensor}} + \underbrace{L_{\text{cable}} \cdot 0.38 \frac{\text{pF}}{\text{cm}}}_{\text{microcable}} \right] \cdot 25 \frac{e}{\text{pF}} + \underbrace{350 e}_{\text{ASIC}}$$

[Rodríguez, A., Nucl. Instrum. Meth. A 1058 \(2024\)](#)



Equivalent Noise Charge (ENC) derived from an S-curves scan in every channel, where the discriminator response is evaluated in a pulse amplitude scan

# Thermal stress test

## Burn-in

### Burn-in Test

#### Test parameters:

The **temperature** ranges:

[-20,15] in LAUDA chiller, and [-15, 20] in BINDER climatic chamber

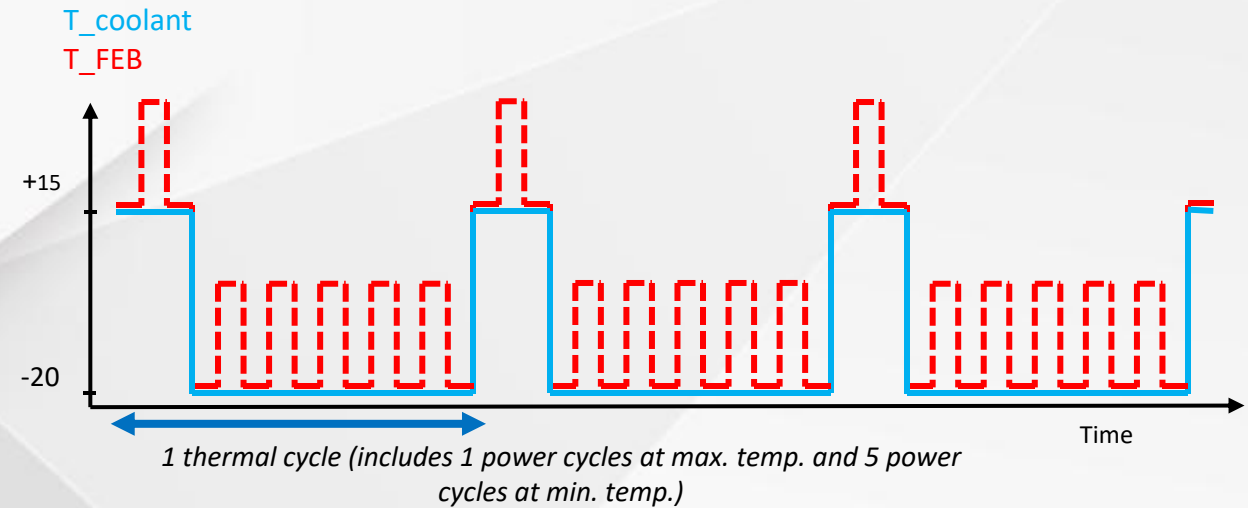
**Thermal cycles:** 3 thermal cycles

**Power-ups at low temp:** 5 per thermal cycle

**Power-ups at high temp:** 1 per thermal cycle

Two burn-in setups:

- two module / 6.5h



STS operation temperature:  $-20^{\circ}\text{C}$

Continuous nitrogen gas flows inside the module enclosure



A photograph showing three people in white lab coats in a laboratory setting. They are gathered around a piece of equipment. A prominent red sign is attached to the equipment, containing safety instructions. The scene is brightly lit, and the background shows typical laboratory equipment and a whiteboard.

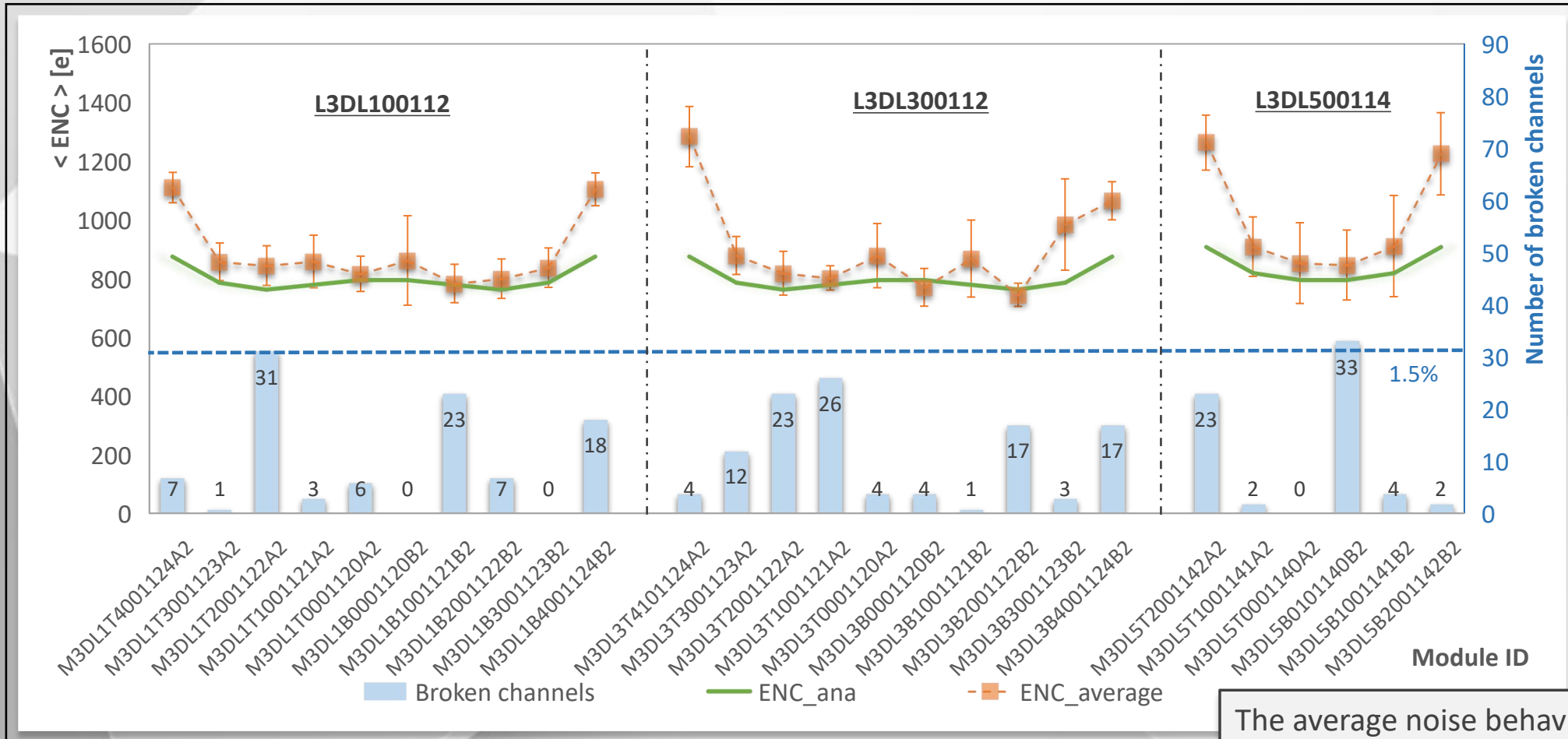
HV SWITCHED OFF??

-> Otherwise:  
Crate has to be switched off  
before opening!!

QA for series module production

# Module characterization

## Module Testing results for the first three assembled ladders



The average noise behavior is consistent with the sensor size, and the number of broken channels for each module is in agreement with our acceptance criterion.

# Thermal stress test

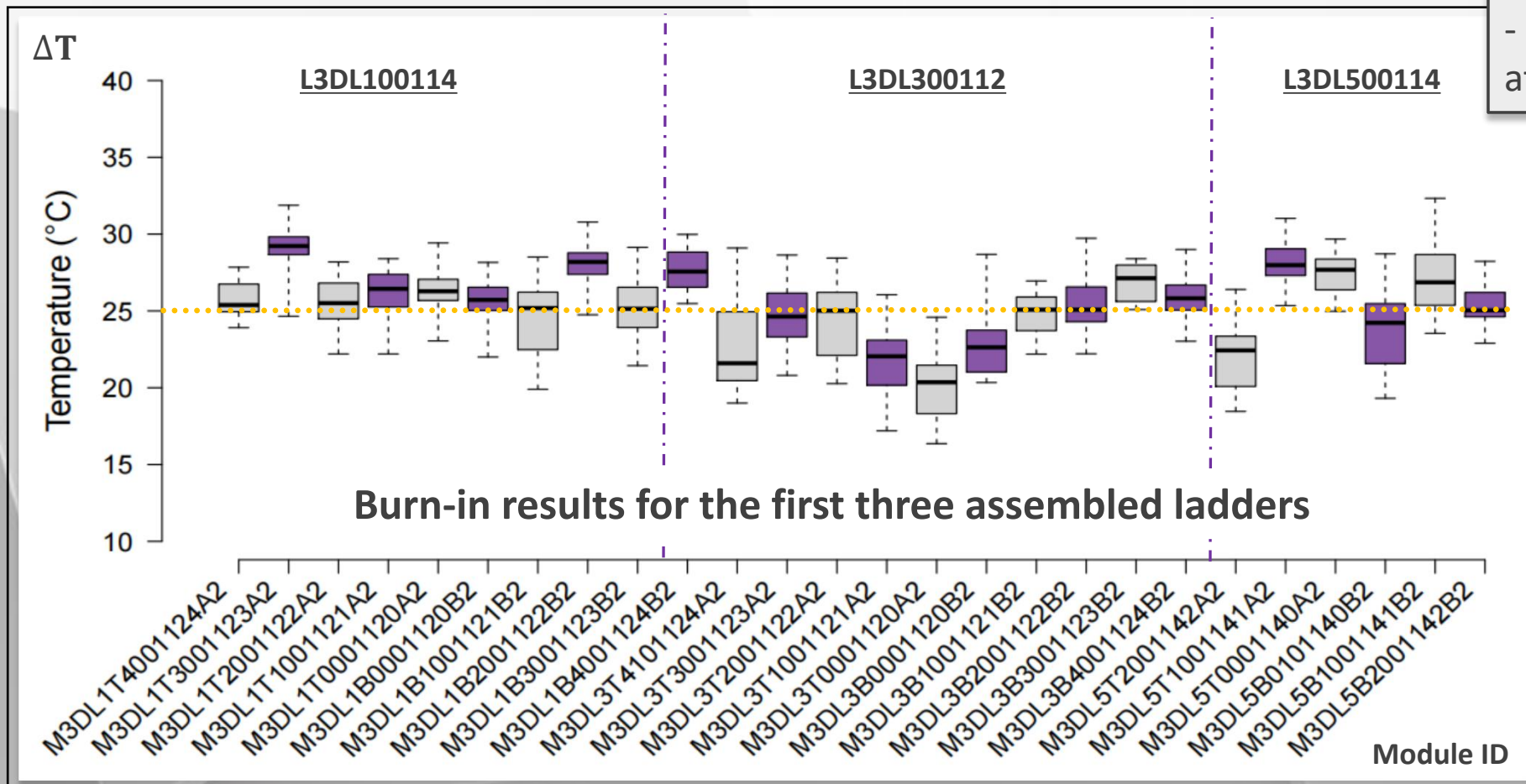
## Module Burn-in results

Overall results: 150 / 150 modules **OK**

16 ASICs per module  $\approx$  2400 functional ASICs

### What data do we collect?

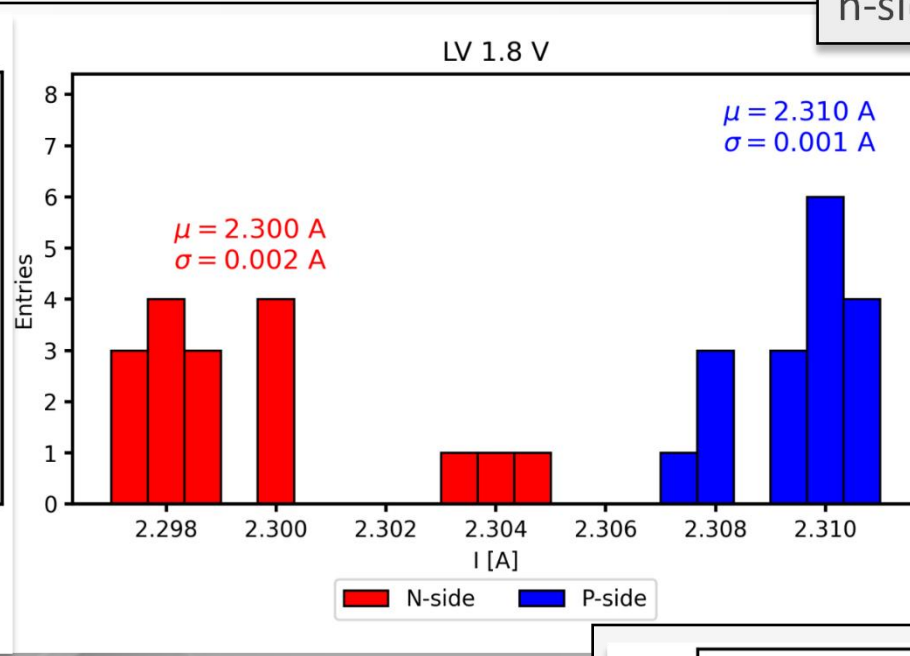
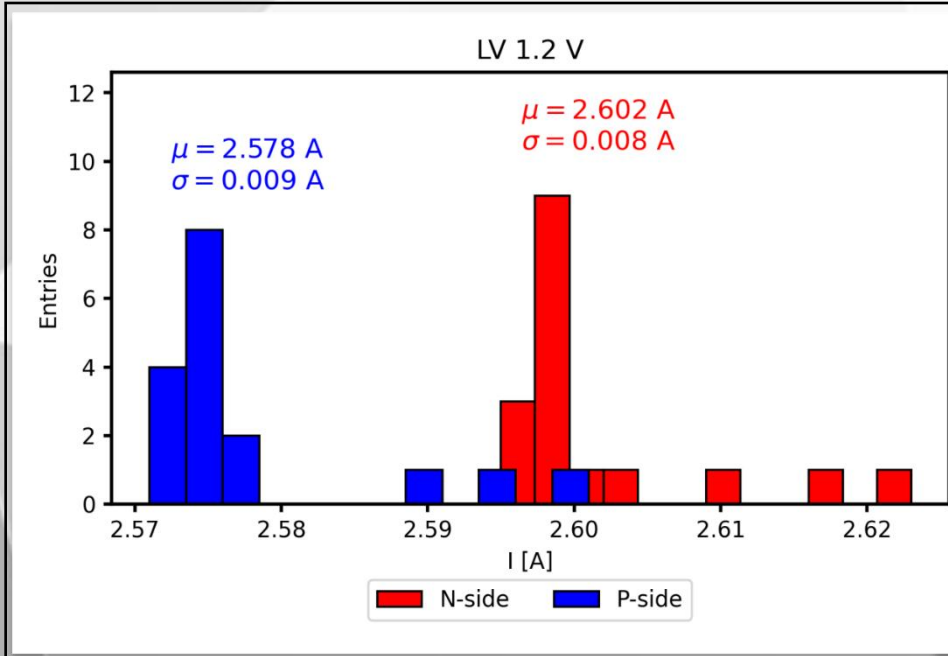
- Power consumption
- Temperature
- Operation potentials in FEE
- Number of broken channels after thermal stress test



# Thermal stress test

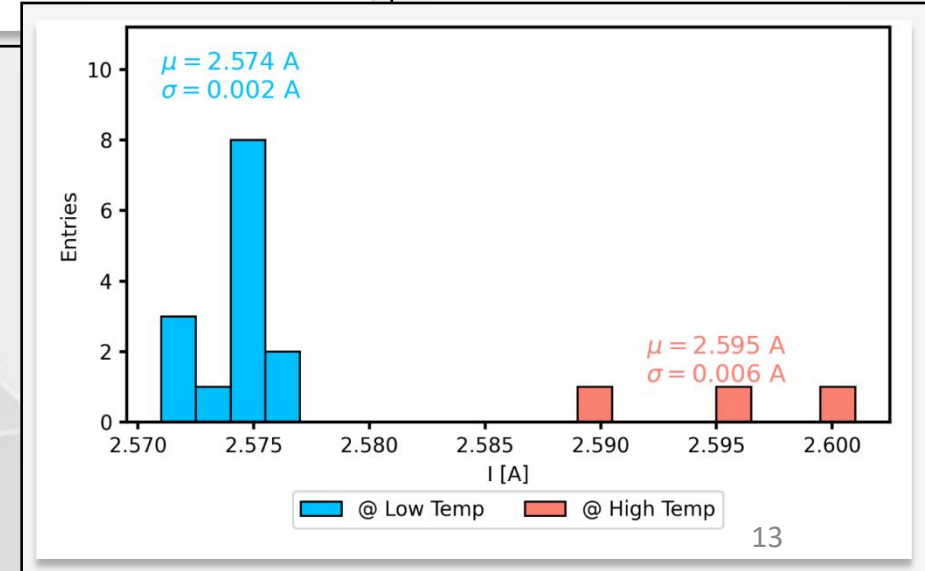
## Power consumption during Burn-in test

FEB power dissipation  
n-side: 10.9 W p-side: 10.9 W



### FINDINGS:

- Differences in current consumption between p and n-side for each power line are below 50 mA.
- Current consumption at room temperature and operating temperature (-20 C) is quite similar.

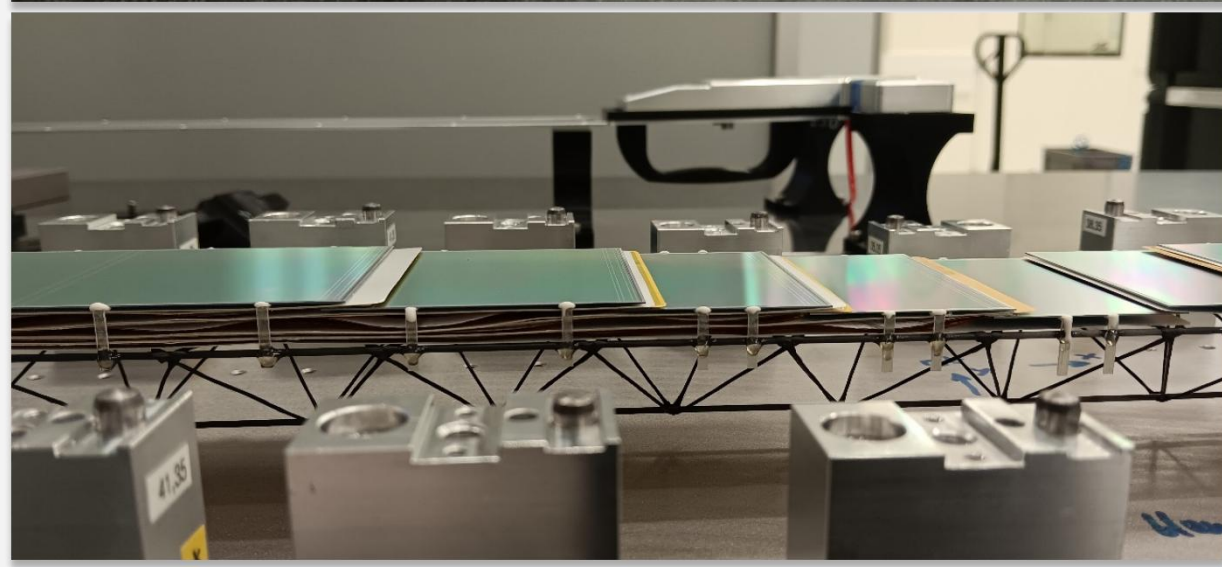
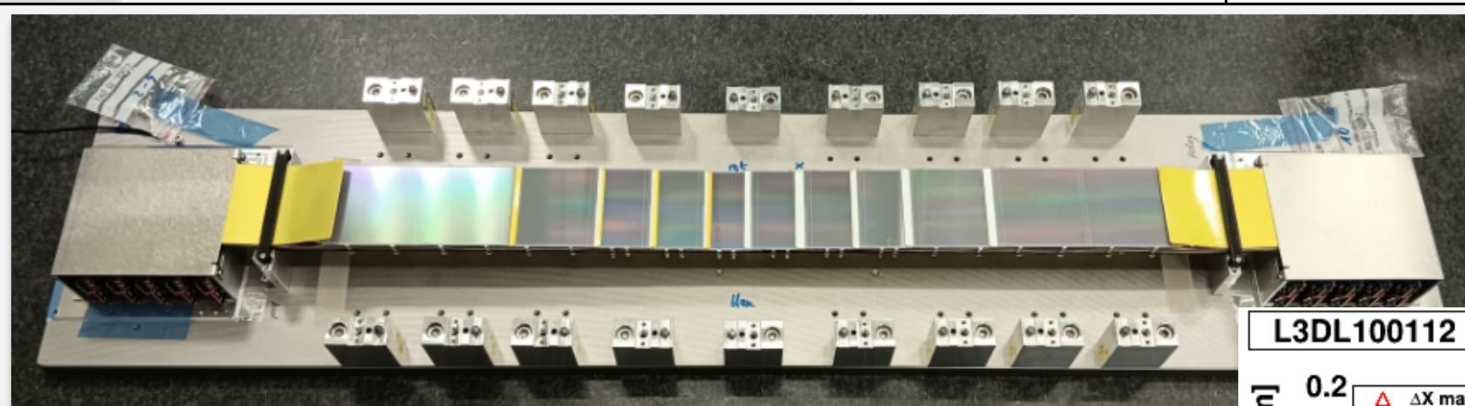


Experience with first ladders



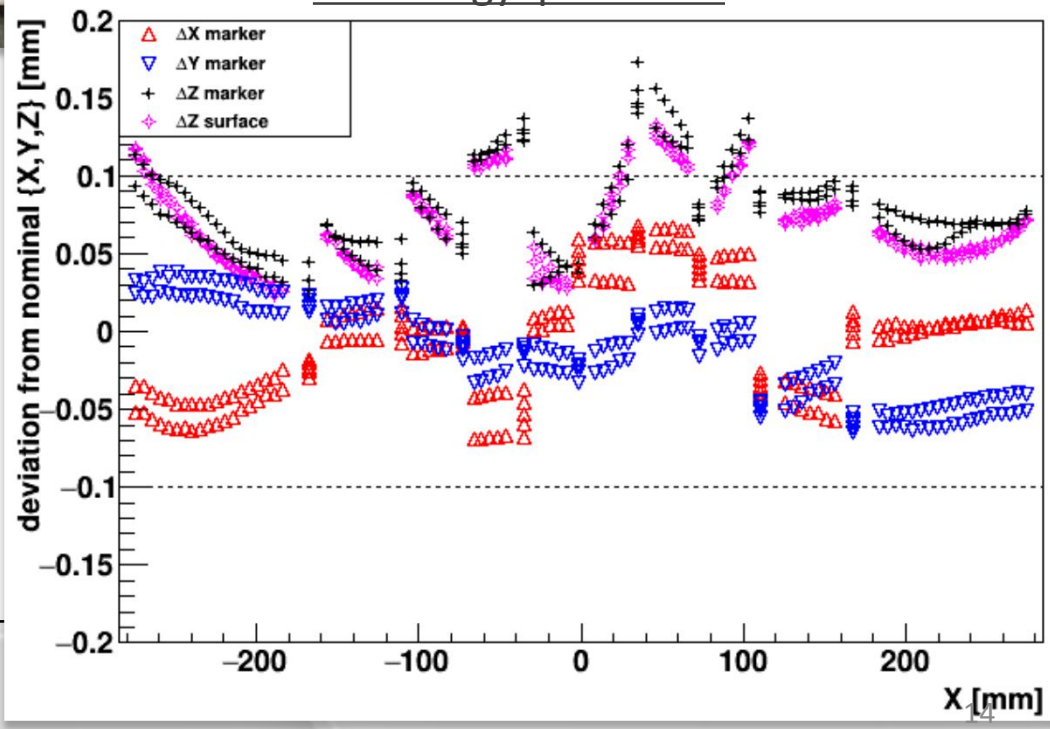
# Ladder assembly

## Ladder Assembly:



L3DL100112

Metrology precision  $\sim 5 \mu\text{m}$



# Ladder characterization

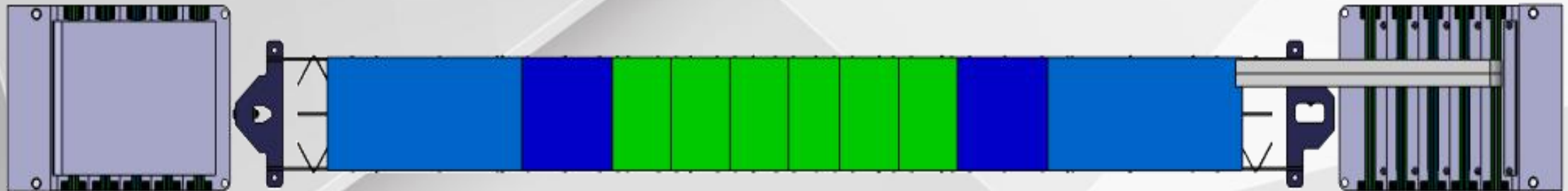
## The construction and setting up of a Ladder test box:

Features of the Ladder test box:

- Modular design: can test all types of STS ladders
- Light tight, EMI protection
- Integrate LV, HV, data readout and cooling interfaces.

The test and characterization of the ladder started with the first of series fully assembled ladder: L3DL300112 (Ladder type 12, holding 10 modules with different form factors):

- - 6 modules built from  $4.2 \times 6.2 \text{ cm}^2$  sensors (Electrical grade B, i.e., EOL biasing up to 350 V)
- - 2 modules built from  $4.2 \times 6.2 \text{ cm}^2$  sensors (Electrical grade C, i.e., EOL biasing up to 250 V)
- - 2 modules built from  $12.4 \times 6.2 \text{ cm}^2$  sensors (Electrical grade C, i.e., EOL biasing up to 250 V)

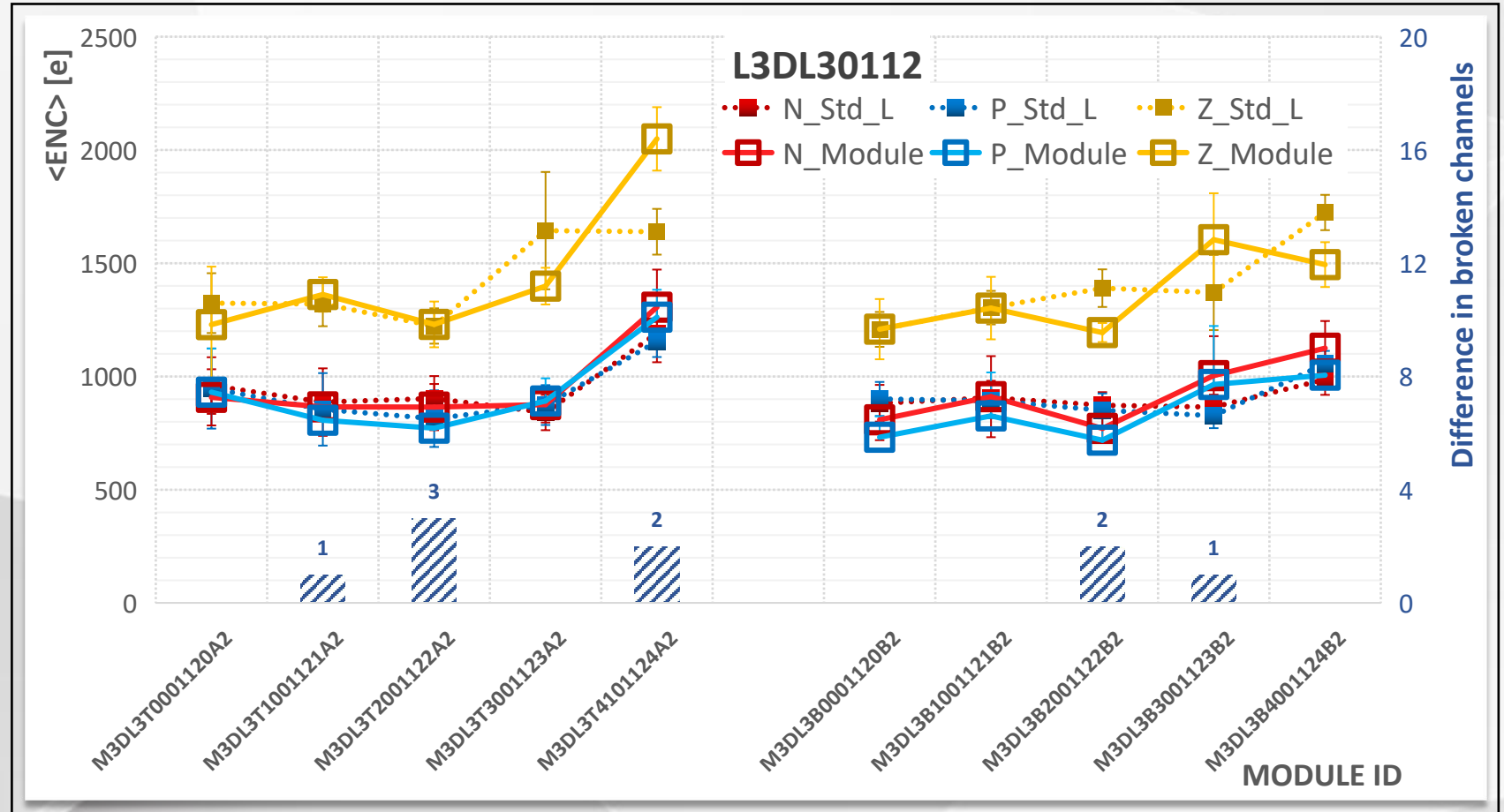
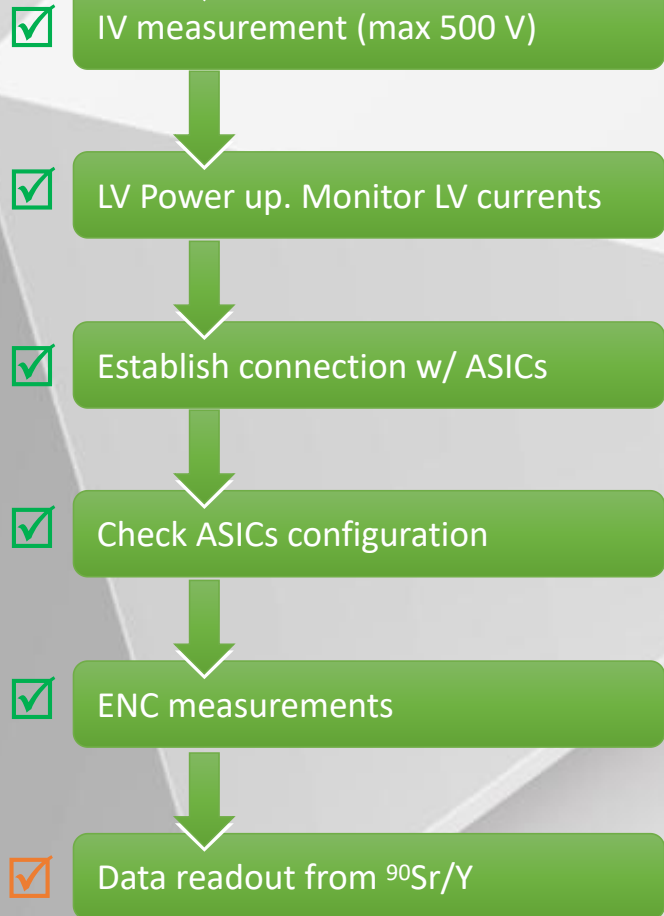


CAD drawing of a Ladder 12 type.

# Ladder characterization

## Testing sequence and status

Ladder in Test box

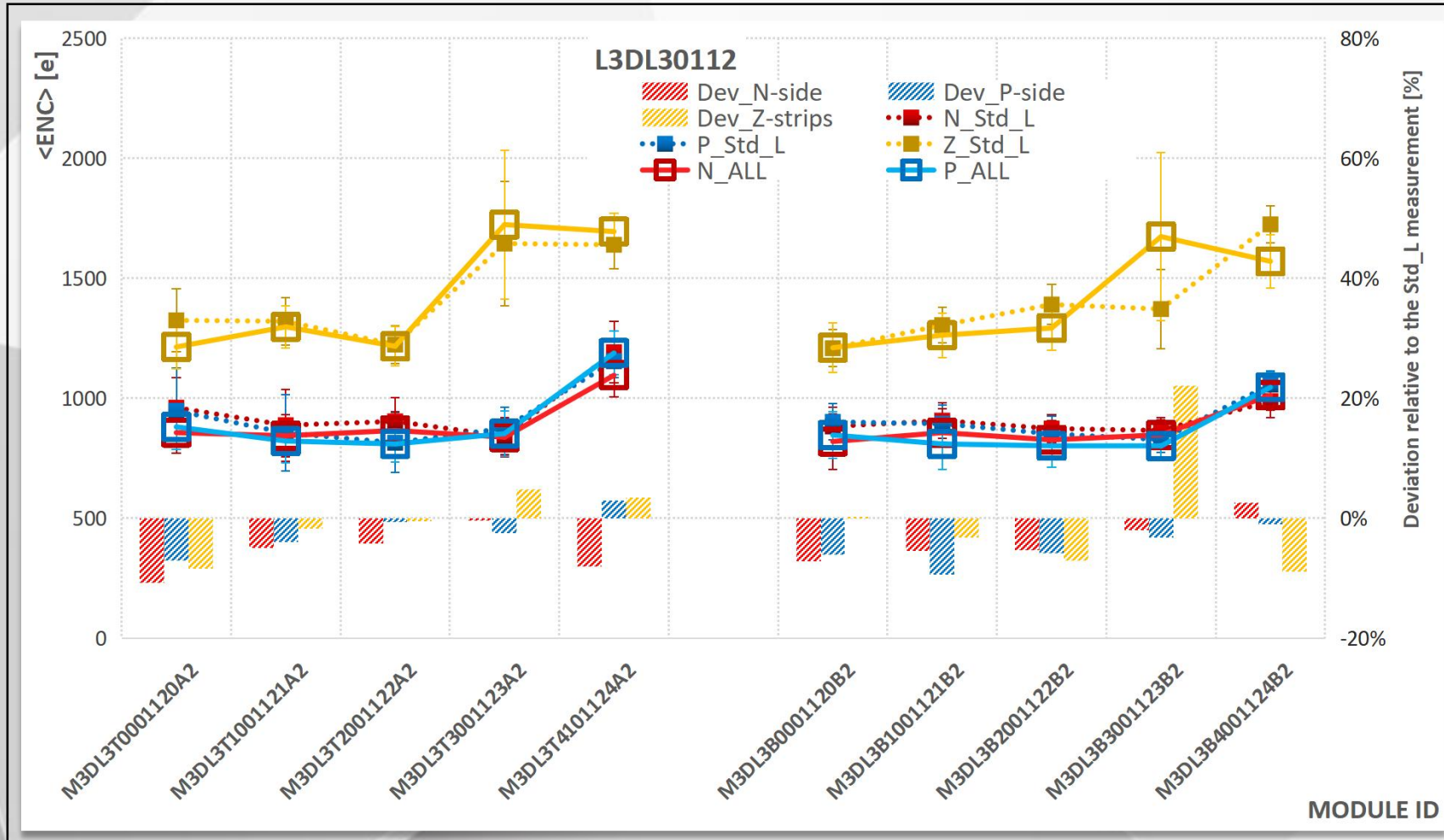


- Direct comparison of ENC measurements between each individual module in the ladder with its previous tests at "Module testing".
- The number of broken channels suffered a very small deterioration during the assembly procedure.



# Ladder characterization

## ENC characterization for each module in the ladder



The large percentual deviation in the Z-strips of module B3 appeared after reworking the position of the microcables.

- Comparison of the module's ENC measured mounted onto the ladder in two different stages:
  - **Std\_L** refers to the standalone biasing and operation of 1 module
  - **ALL** refers to the simultaneous biasing and configuration of all modules

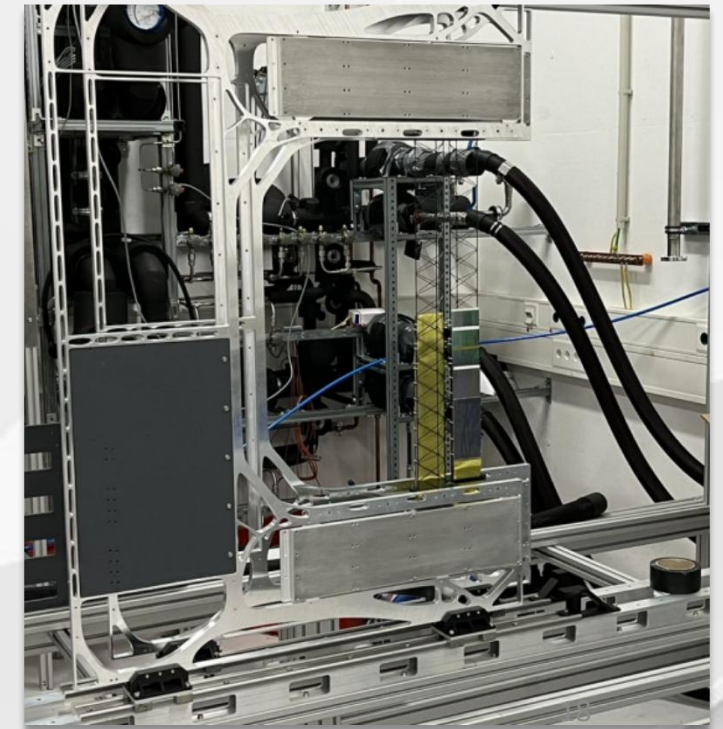
# Module and ladder characterization and burn-in tests

## CONCLUSIONS

- The test and characterization of fully assembled modules is fundamental to ensure reliable performance, improve their operation, and correctly interpret the collected data in the final detector.
- The burn-in test identifies potential weaknesses and evaluates the robustness of the electronics and functionality of the whole module under realistic operational conditions.
- The ladder test ensure that the module proper functionality and performance are preserved.

## What are the next steps in the assembly?:

- Each ladder will be placed in the corresponding C Frame
- It will be integrated with the final components: Cooling interfaces, Readout boards, Power boards, LV, HV and data cables.
- C frames will be tested to ensure proper operation.
- Each C Frame will be mounted in the mainframe, and further tests are foreseen.
- Transported to the CBM cave, where it will be finally operated.





***THANKS***