xTCA Compliant Compute Node design for PANDA experiment

Z. A. LIU

TrigLab, IHEP Beijing

Panda DAQ Meeting, Paris, France

Sept.11 2012

Outline

- Review
- Status
  - New AMC(xFP V3) design
  - ACAB design
  - Joint test of xFP and ACAB
- Future plan
- Summary

Short Summary of xTCA development

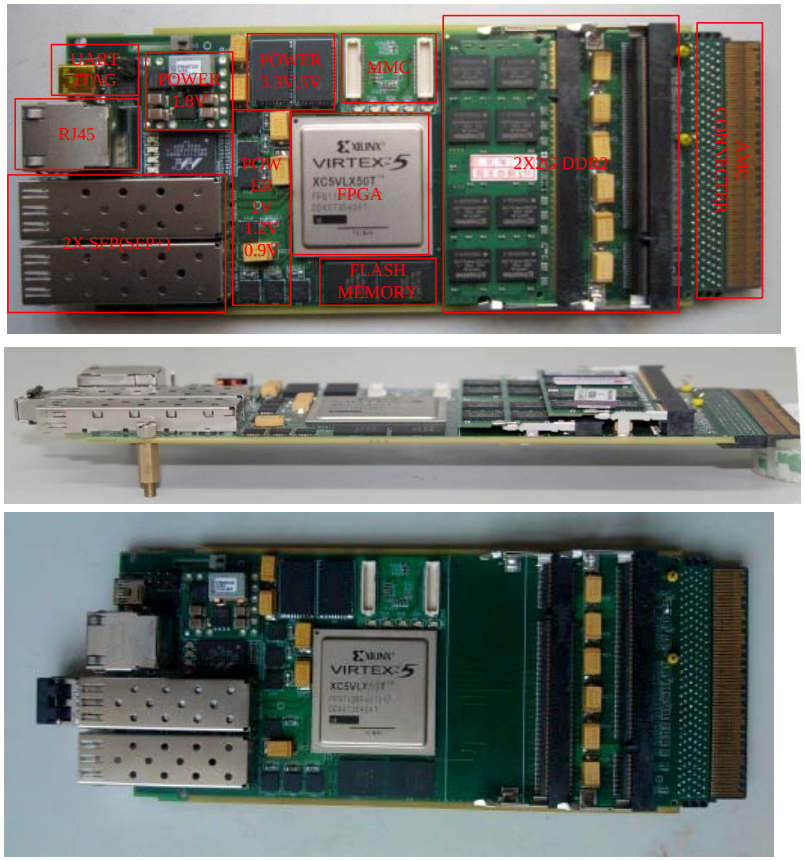
at Rauischholtzhausen, Germany

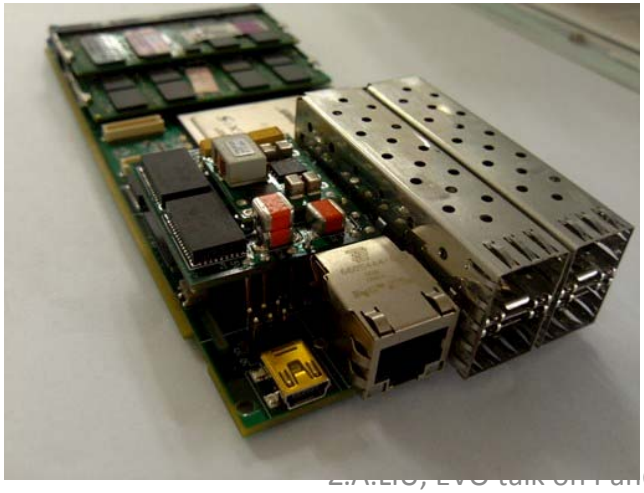
Apr. 12-13 2012

- xTCA activities going well at IHEP
- CN Development for PXD
  - Carrier Board is going
  - AMC is in good shape
    - Soldering problem lost a week
- CN development for SVD DATCON
  - Well planned after detailed discussion
  - No key problem foreseen now
  - AMC with 4 SFP almost in hand
- Development smoothly in General

AMC Board development

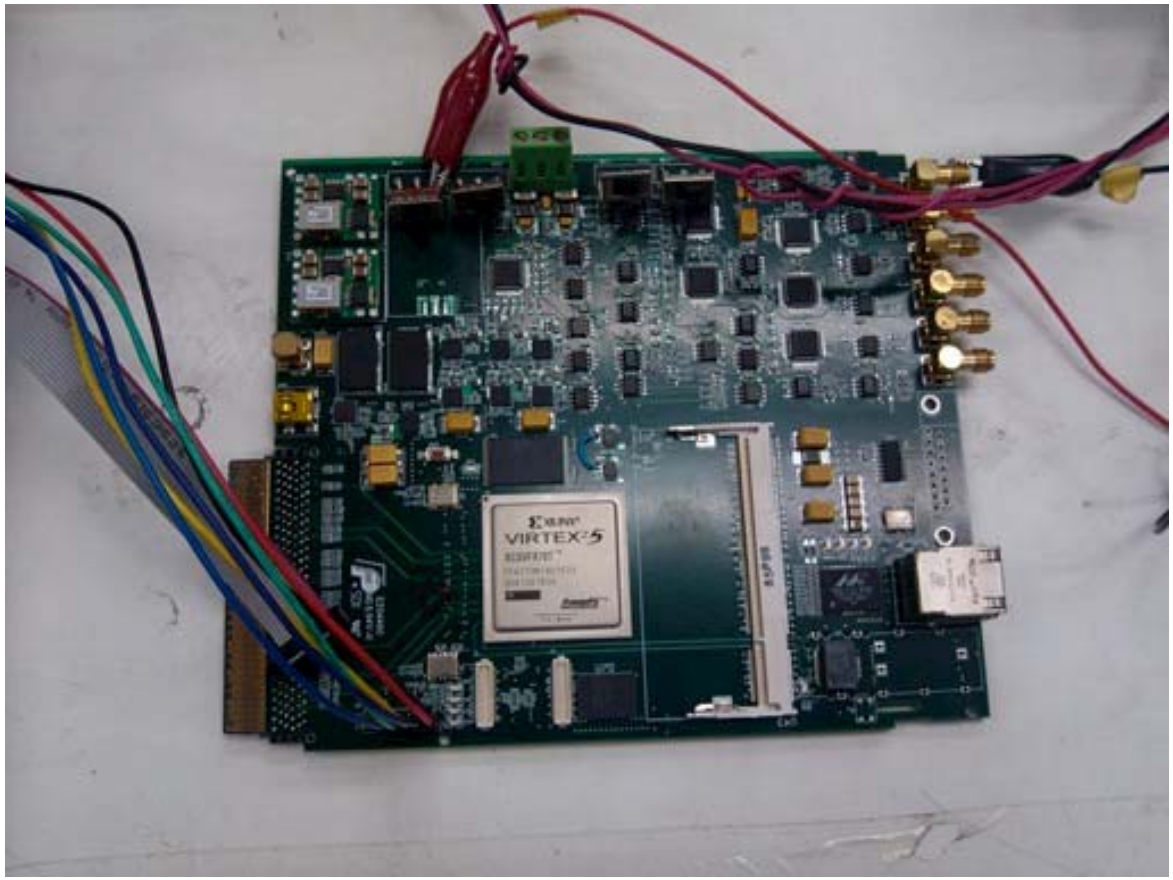
- Single width AMC card
  - FPGA XC5VFX50t without PPC
    - 2 x 3Gbps ports, 4G DDR2
  - FPGA XC5VFX70t with PPC
    - 2 x 3Gbps ports, 4G DDR2
    - 2 x 4Gbps ports, 4G DDR2
    - 4 x 4Gbps ports, 4G DDR2





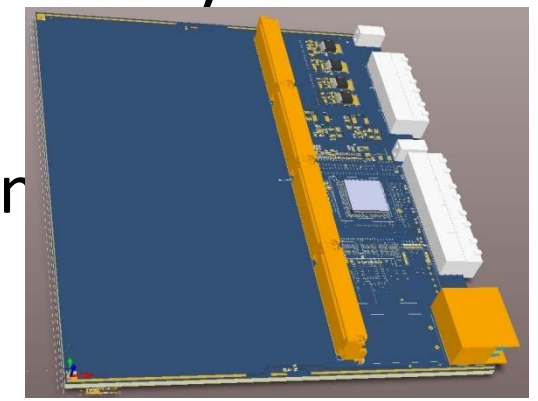
Carrier Board development (2)

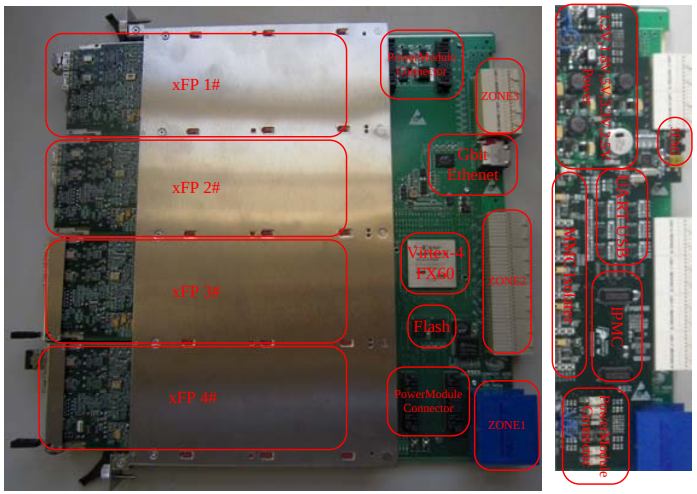
- Double width AMC card
  - Designed for BESIII Luminosity Monitor

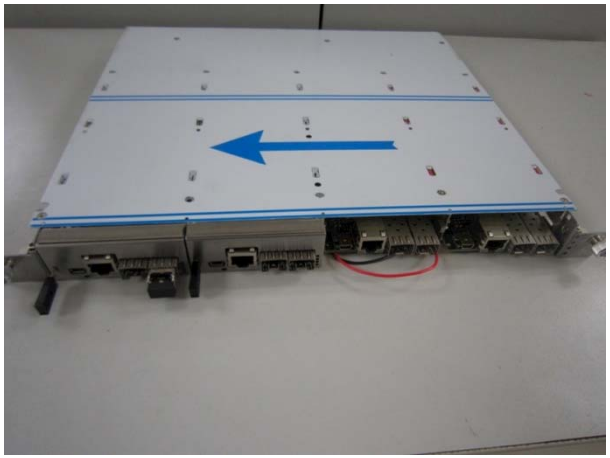


Carrier Board Development

- ACAB-AMC Carrier ATCA Board(xTCA term)
  - PS board ready in April
  - V4 on carrier board changed in May/Jun
  - Ch. Difinition

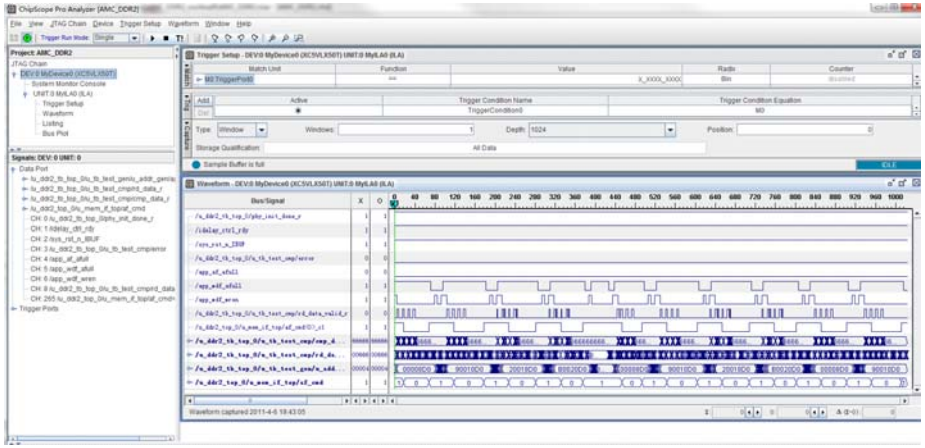


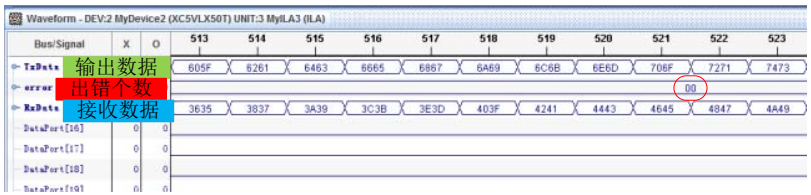




AMC Testing

- Optical link（Ver. 1/2/3)
  - 3.125/4Gbps
    - Tested about 24/1 hour with pseudo random data
    - Estimated BER < 8.6X10e-15/ < 8.6X10e-14





DDR2 test

◆ Single DDR2 test(Ver.1/Ver.2)

DDR2	Clock	R/W speed
DDR2_A	200M	400MHz
DDR2_B	167M	334MHz

DDR2	Clock	R/W speed
DDR2_A	167M	334MHz
DDR2_B	167M	334MHz

◆Double DDR2 joint test(Ver.1/Ver.2)

DDR2	clock	R/W speed
DDR2_A_B	167M	334MHz

DDR2	clock	R/W speed
DDR2_A_B	167M	334MHz

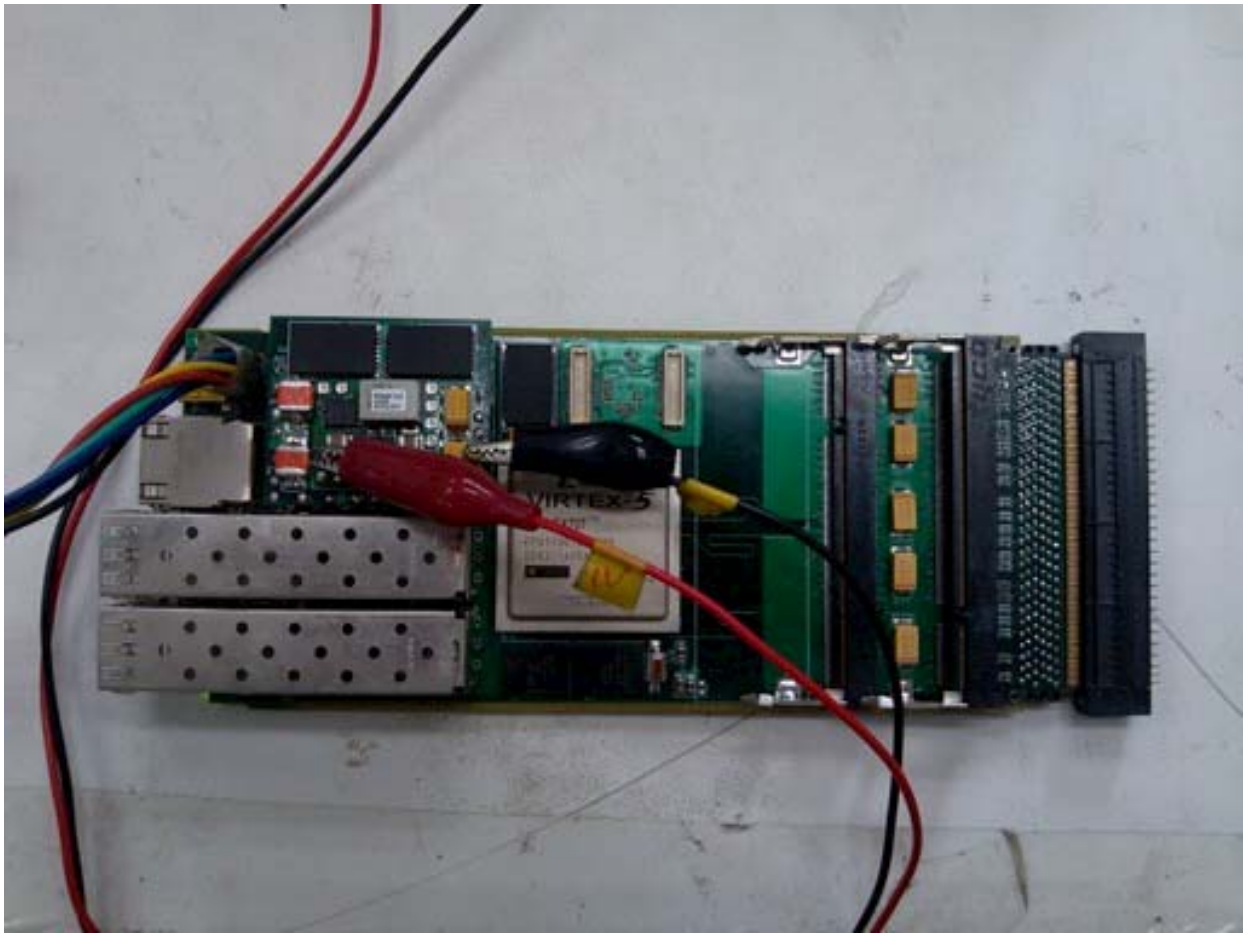
◆Single and Double DDR2 joint test(Ver.3)

DDR2	Clock	R/W speed
DDR2_A	200M	400MHz
DDR2_B	200M	400MHz

DDR2	clock	R/W speed
DDR2_A_B	200M	400MHz

Backplain testing

- RX/Tx9 4Gbps 2hours 0 err-> reliable



Joint Test with AMC and ACAB

- We DID have problem with Carrier Board development both in
  - Jtag chain Downloading
    - FPGA on Carrier board
    - FPGA on AMC boards
  - Data way inter AMC cards

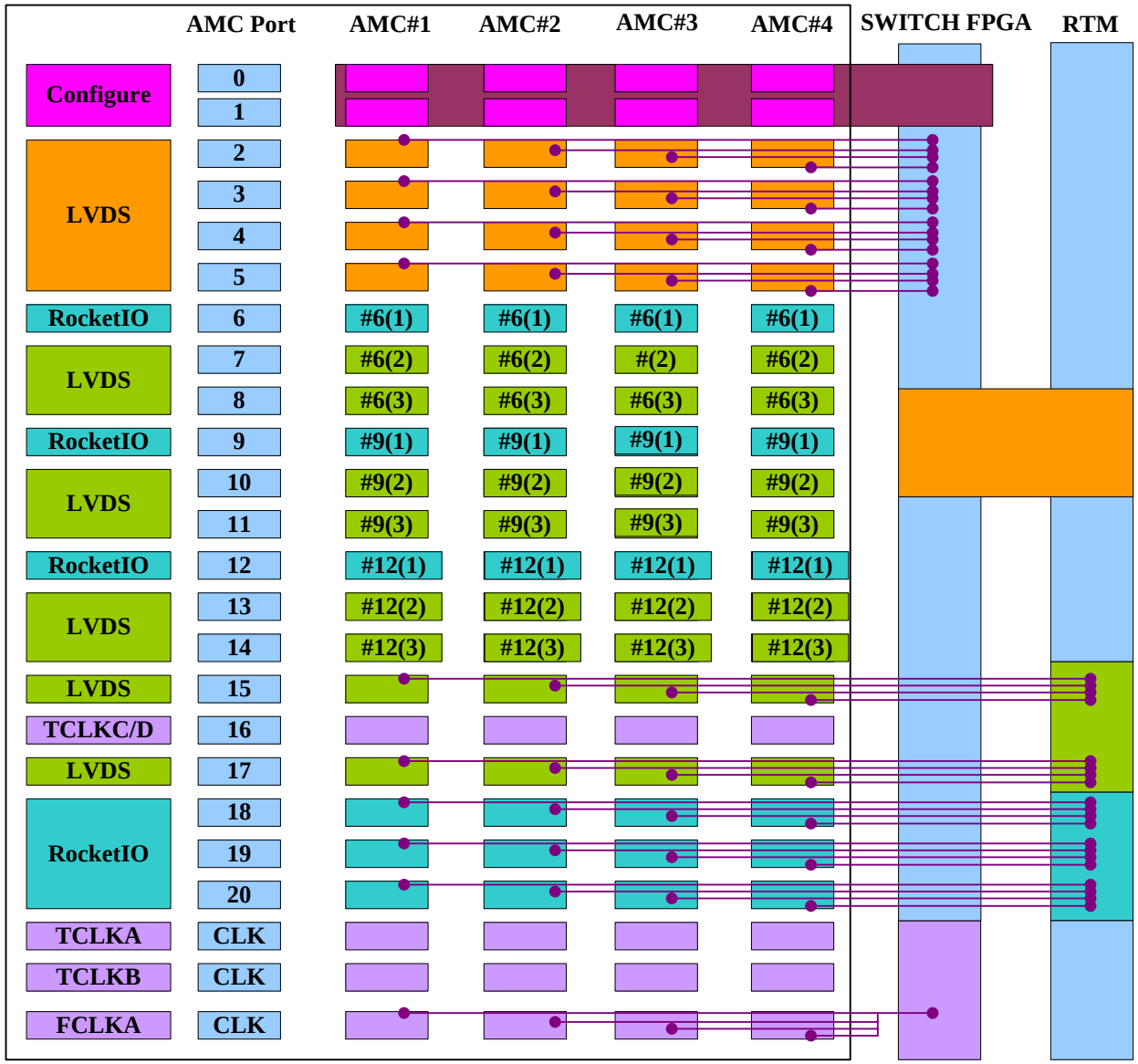
Problems encountered

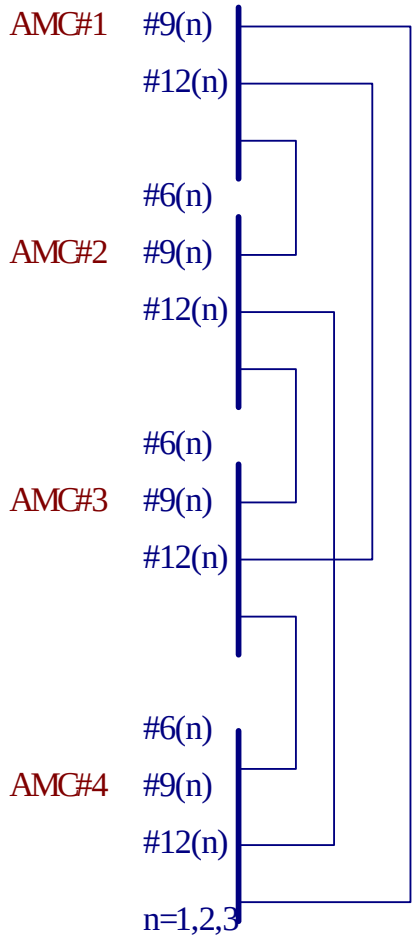
- JTAG chain downloading unsuccessful
  - Both in IHEP and Giessen
    - 1, ACAB(cb+ps) : failed FPGA + CPLD seen in the chain, DL failed
    - 2, ACAB(cb+ps)+ 1 amc (any slot): DL successful
  - IHEP with help of LUMI AMC
    - 3, ACAB(cb+ps)+ 2 amcs(12,23,34): DL successful,not 13,14,24
- Solution in short term
  - TDI,TDO,TMS: 10k pull up;
  - TCK: 68ohm +100pF pull down

Inter AMC data transmission

- Result at IHEP:
  - S1-S2(xFP <-> LUMI AMC）
    - Rx/Tx6-Rx/Tx12 4Gbps 2hours 0 err
  - S1(amc)->S4(connector) loopback
    - Rx/Tx12 – Rx/Tx6 2.5Gbps 2hours 0 err
    - Rx/Tx12 – Rx/Tx6 4Gbps 1/1000 err
  - AMC-AMC
- Solution
  - Rearrange recovered clock

AMC interconnections





- #9(n) =>#10(n)

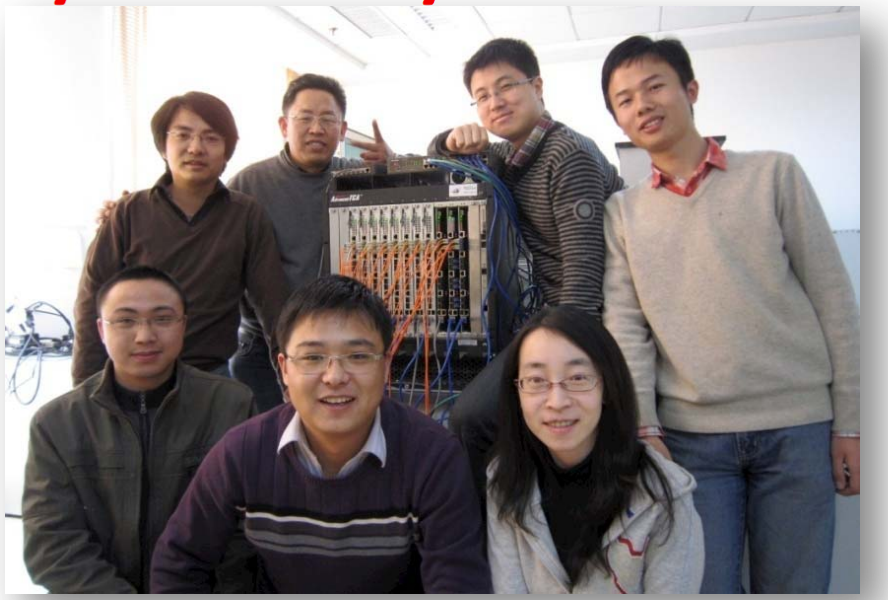
Future plan

- Production of more xFP's
- AMC Modification(short term)
  - Pin assignment correction
    - #9(n) => #10(n)
- ACAB modification(long term)
  - JTAG buffering and isolation

Summary

- CN ver. 2 works fine
  - ATCA compliant
  - No complains received
- CN Ver. 3 works basically fine
  - xTCA compliant
  - AMC card (xFP Ver.1-3) work fine.
  - ACAB basically works fine
    - Pin assignment in S2-3(to be changed in AMC)
  - Expecting feedbacks
- Implementation of timing
  - Some discussion in Barischzell and Bad Aibling, but
  - Need better understanding and further discussion

Thank you for your attention !



Backup Slides

Development of Carrier Board(ACAB)

- Aiming xTCA compliant
  - allowing backplane data transmission,
  - 4 AMC connectors,
  - FPGA0 for **switch**,
  - IPMC routing,
  - **Possiblly** Clock/trigger/ distributions,
  - Power conversions,
  - RTM **function** reservation