JÜLICH
FORSCHUNGSZENTRUM

panda

Ethernet Implementation into the Jülich Digital Readout System

2012-09-11 | André Goerres

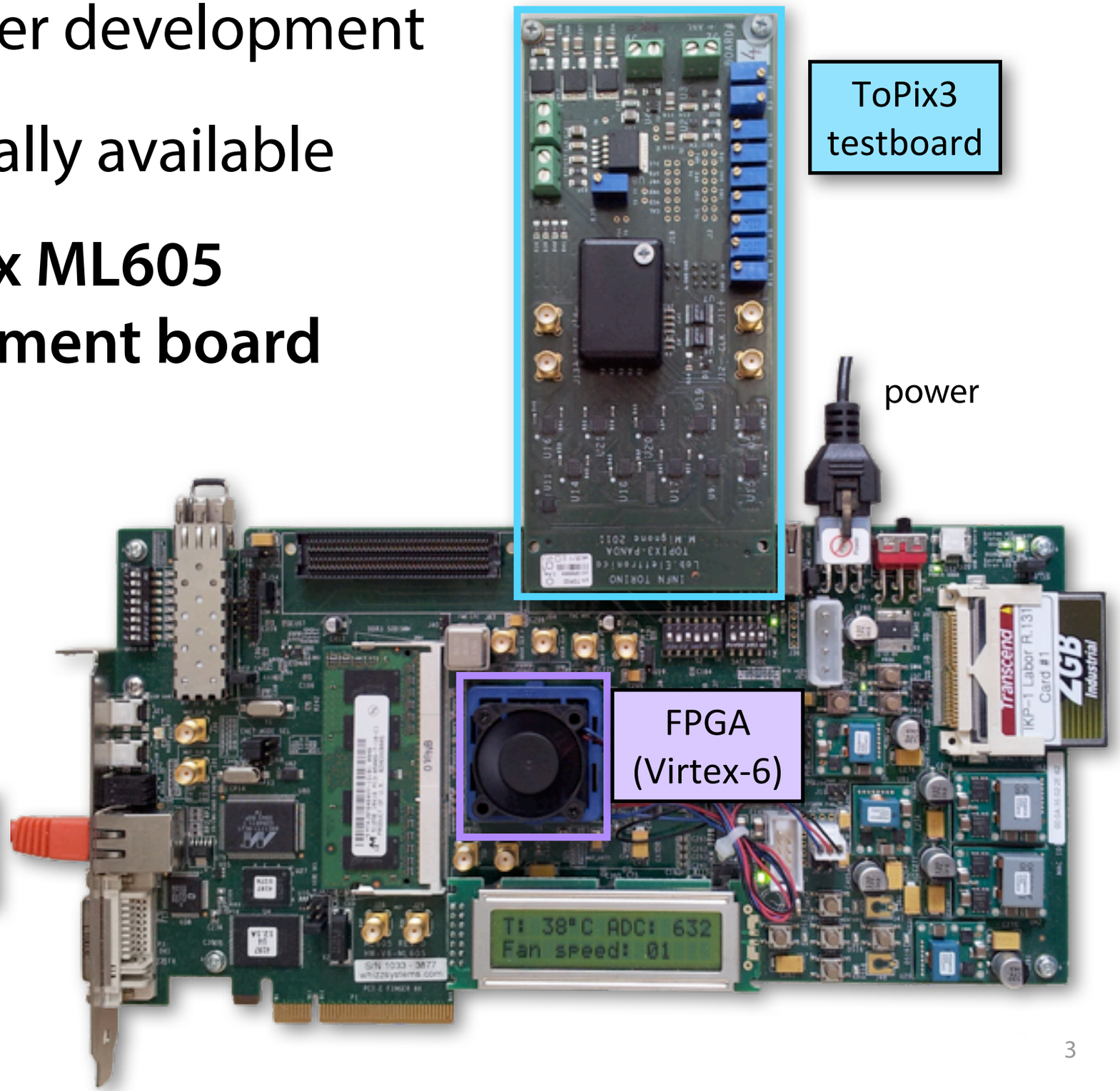
Outline

- Jülich Digital Readout System
  - Purpose & Structure
- Firmware Development
  - Ethernet Connection
  - LCD on the Board
- Conclusion

Overview

- **Purpose:** Flexible readout system for Frontend Chips under development
- Based on commercially available hardware:

Xilinx ML605 development board

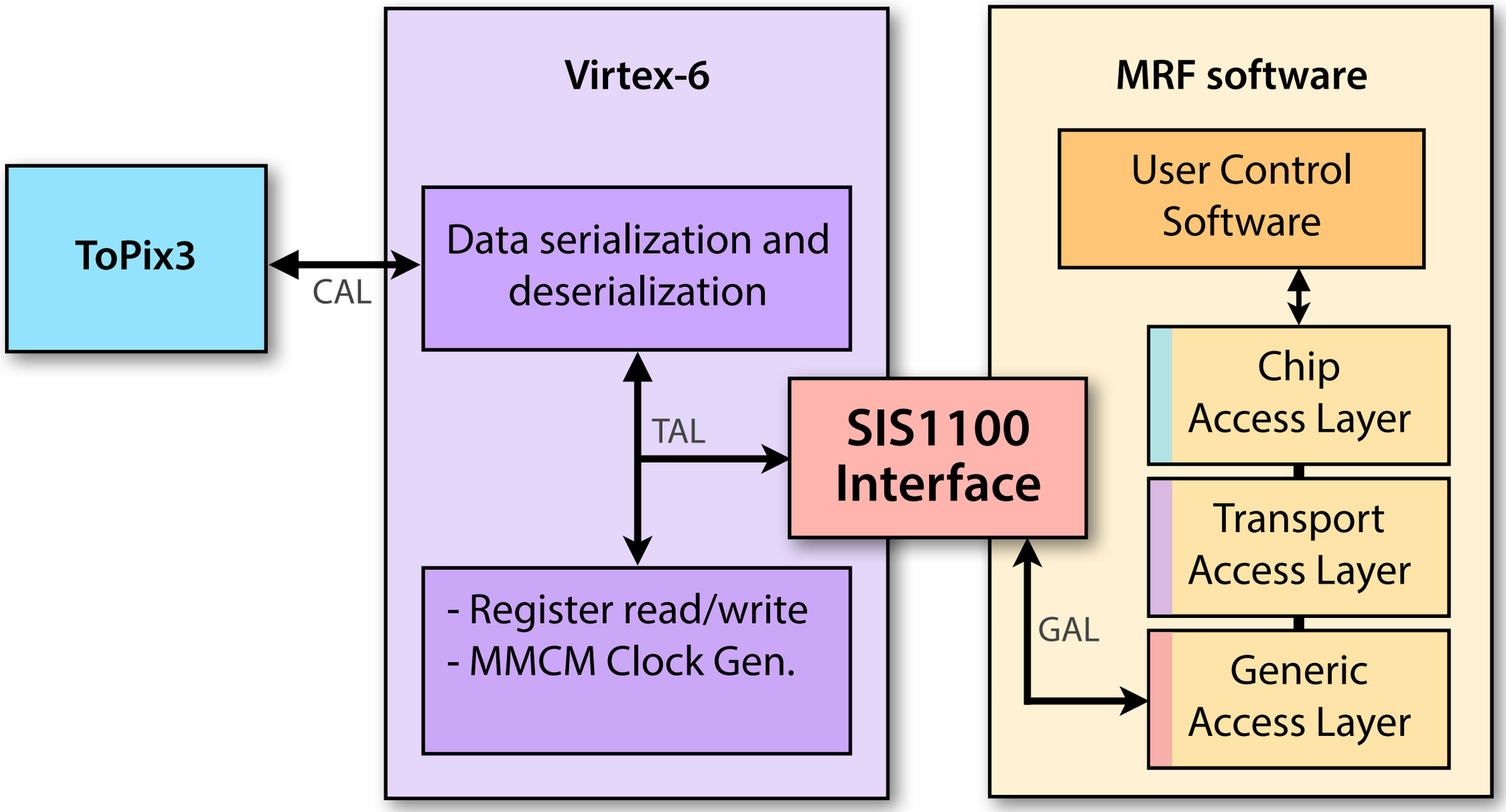


Specifications

- FPGA-based readout system (Virtex-6)
- Software framework (MRF) written in C++
  - Control FPGA & readout chip under test
  - Modular concept
    - ↪ Ability to adapt easily to new hardware
- Current communication to PC: **SIS1100**
  - Proprietary communication system via optical link
  - Dedicated PCI card & drivers needed

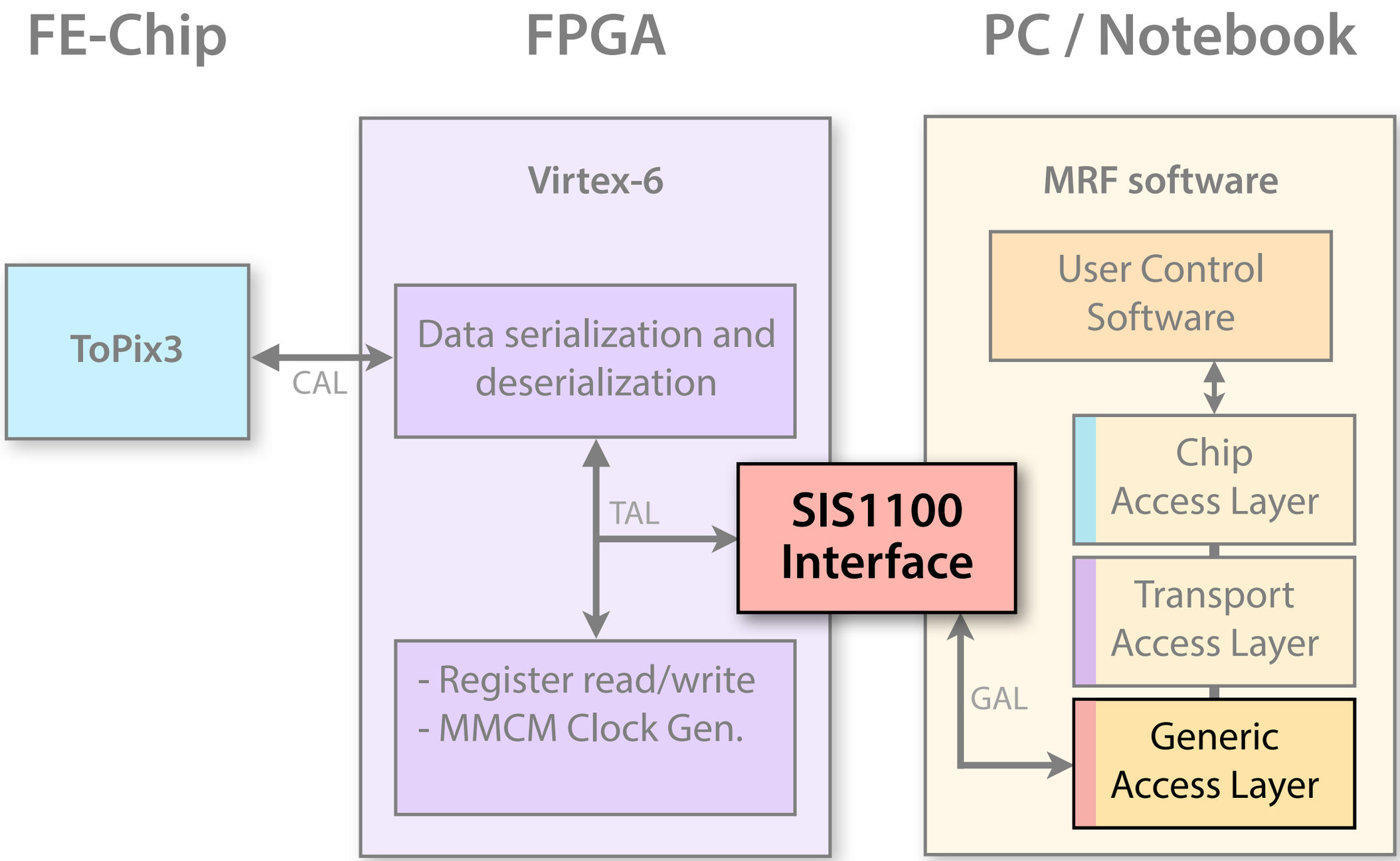
MRF: **M**VD **R**eadout **F**ramework

Data Flow



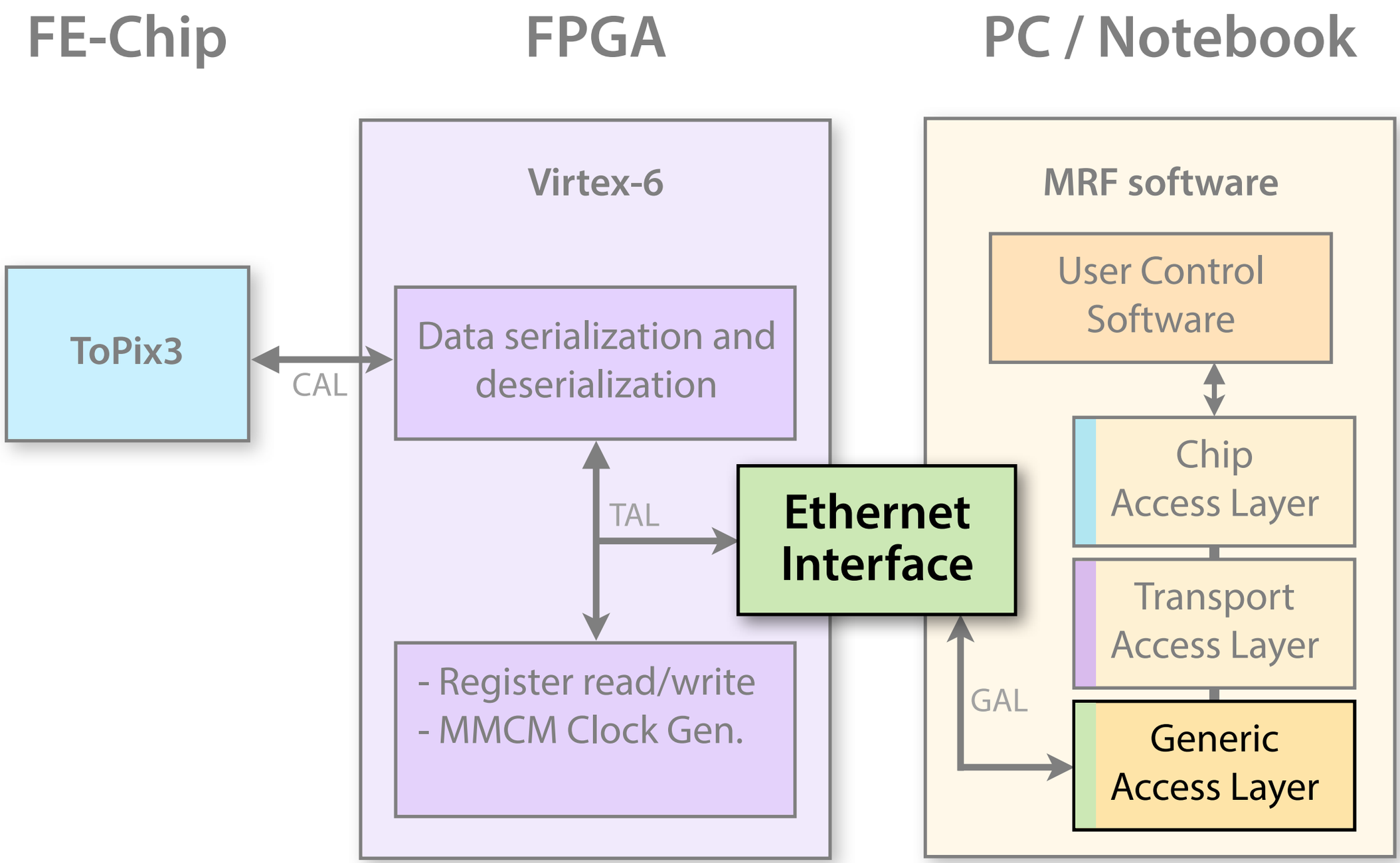
MRF: **M**VD **R**eadout **F**ramework

Data Flow



MRF: **M**VD **R**eadout **F**ramework

Data Flow



MRF: **M**VD **R**eadout **F**ramework

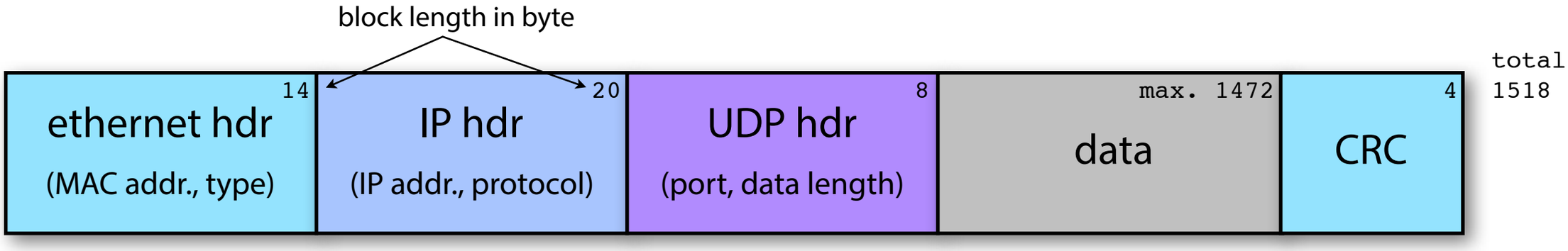
Why change to ethernet (UDP)?

- **Advantages**
  - + Almost no investment costs
    (Compared to ~1500 € for SIS1100)
  - + No additional drivers on PC side
  - + Useable with notebook
  - + UDP feasible for FPGA
  - + Additional communication link on ML605

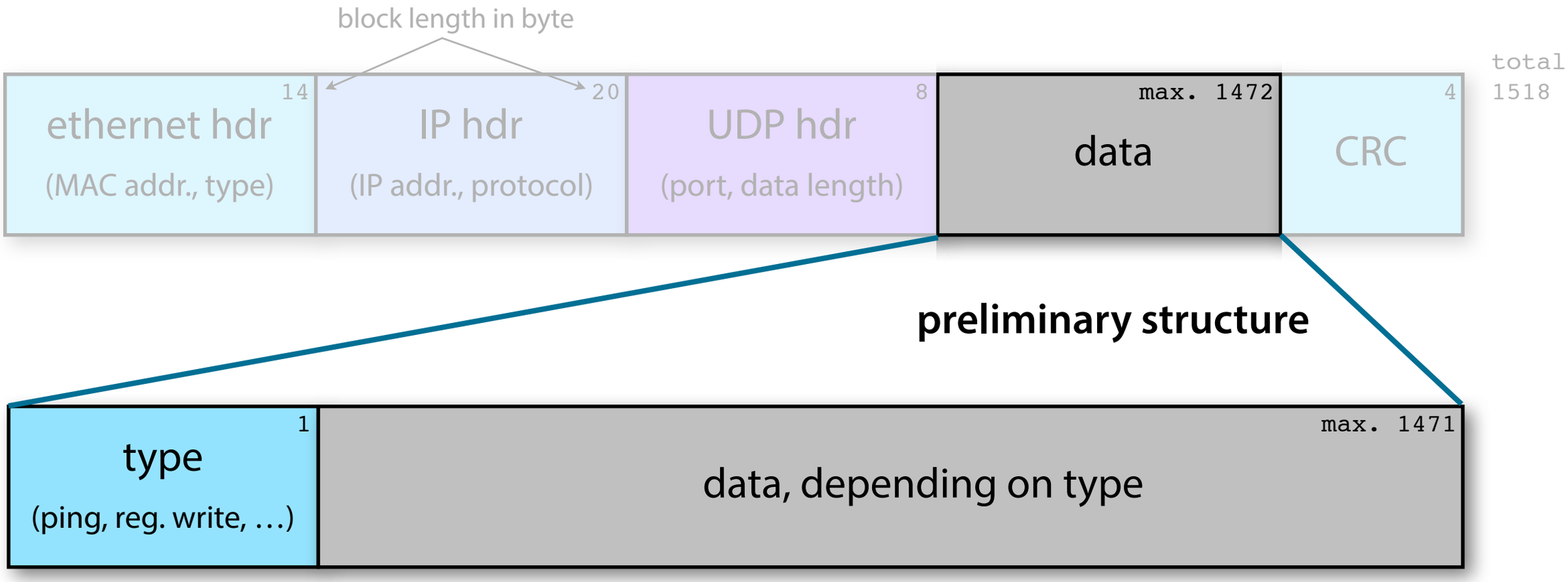
- **Disadvantages**
  - – Development needed
  - – No validation for receiving in UDP

UDP: **U**ser **D**atagram **P**rotocol

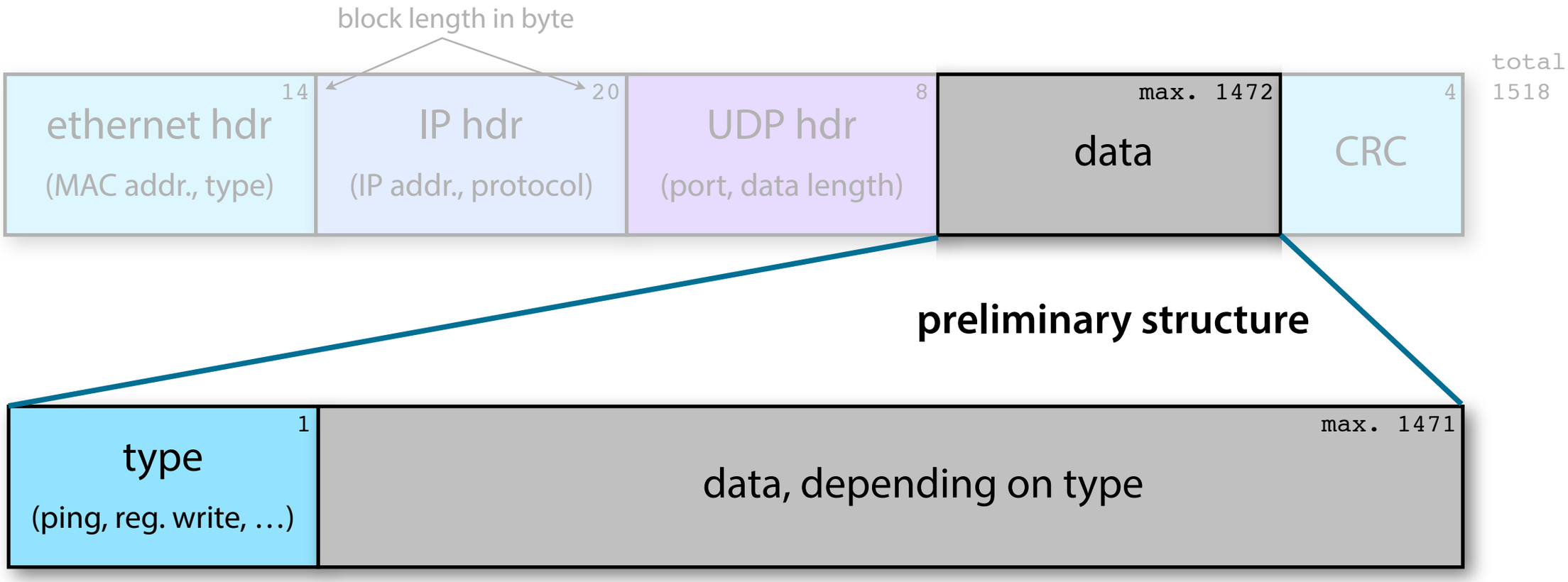
UDP Package Structure



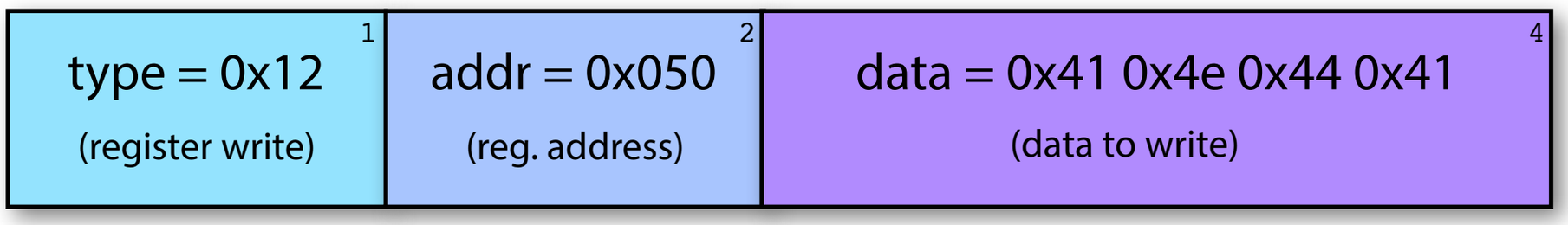
UDP Package Structure



UDP Package Structure



Example: writing a value to an FPGA internal register

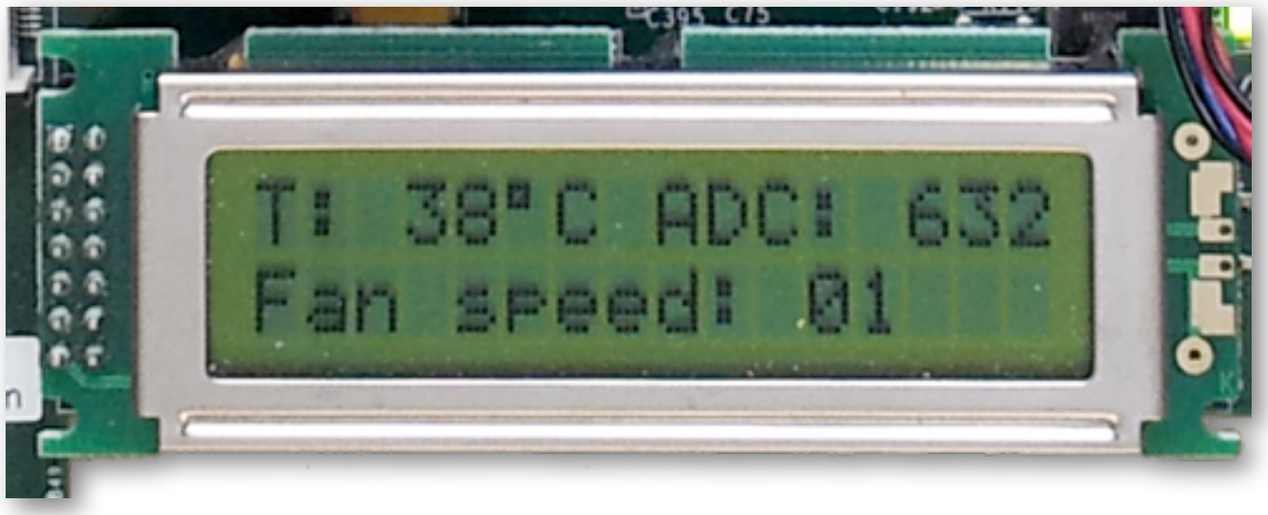


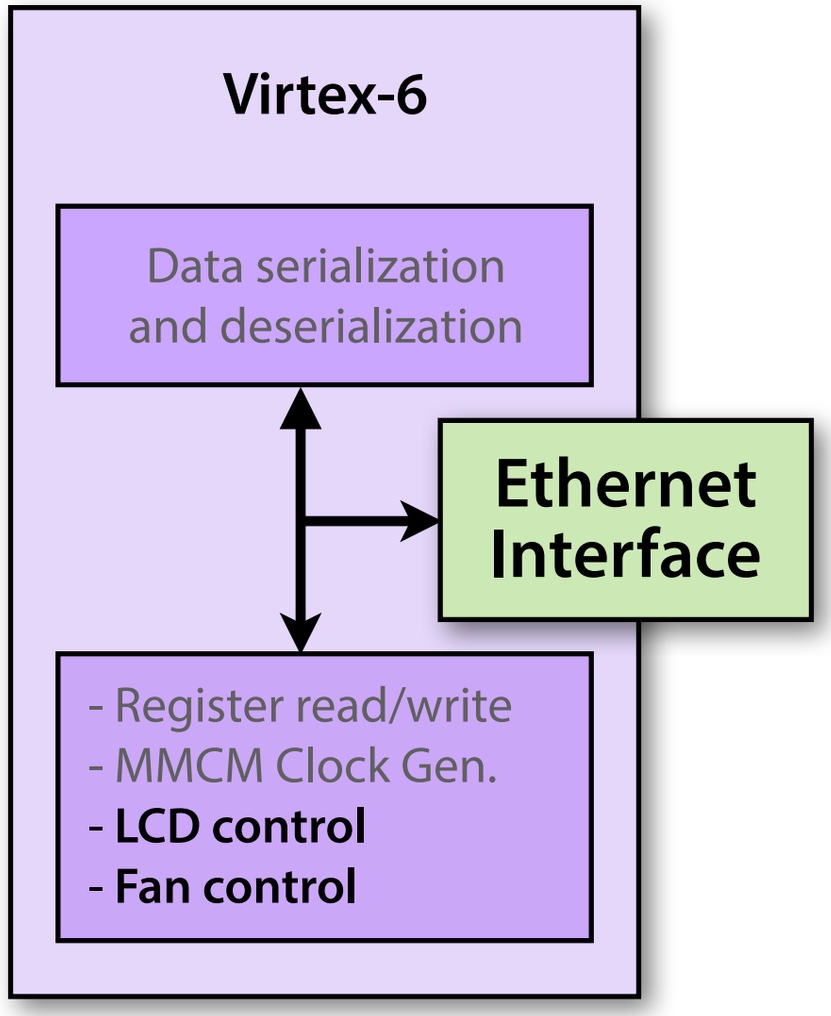
Current Implementation Status

- Working:
  - IP address resolution
  - Sending/receiving UDP packages on both sides
- In progress:
  - Adaption to current testing logic
  - Writing and reading FPGA internal values
- For the future:
  - Simple receiving check (e.g. package counter)
  - Continuous data flow

Simplification of Development

- Use built-in LCD
  - Easily adaptable to user's needs
  - Example:
    FPGA temperature and fan speed





Conclusion

- Jülich Digital Readout System
  - Modular structure
    - Easily adaptable to custom chip development
  - Now including LCD for direct debug output
- Communication
  - Change to UDP standard in progress
  - Usage of widely accessible hardware
    - Also usable with notebook

Conclusion

- Jülich Digital Readout System
  - Modular structure
    - Easily adaptable to custom chip development
  - Now including LCD for direct debug output
- Communication
  - Change to UDP standard in progress
  - Usage of widely accessible hardware
    - Also usable with notebook

Thank you!

a.goerres@fz-juelich.de