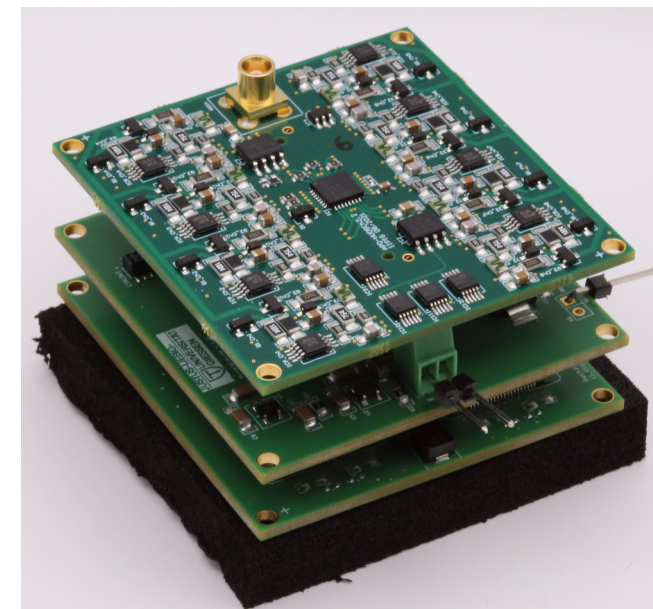
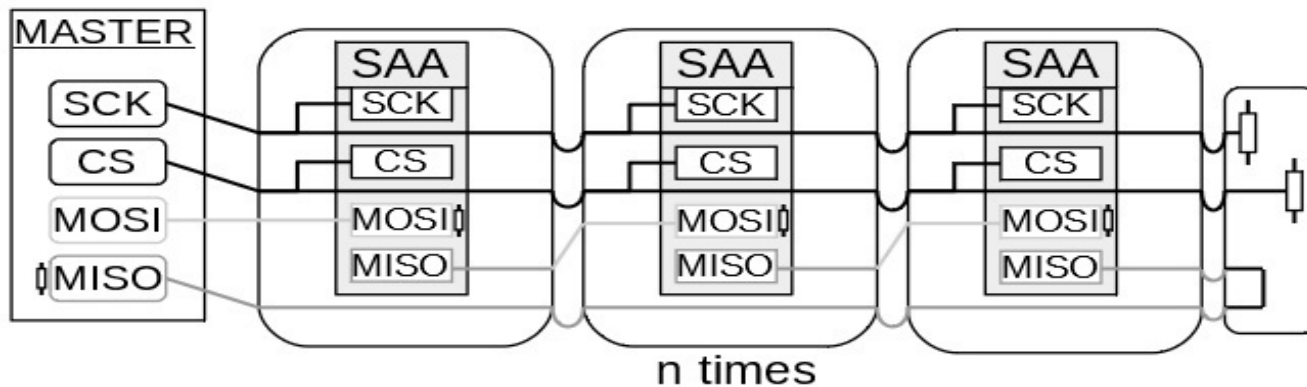
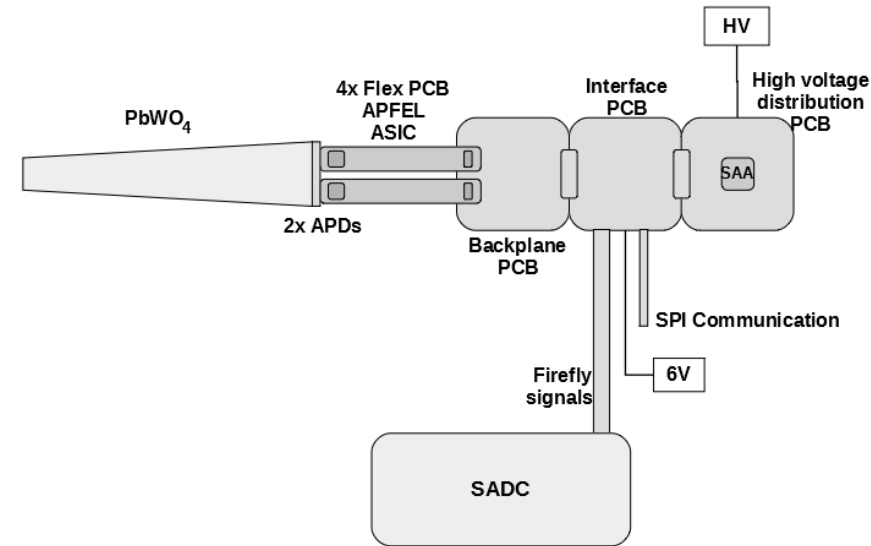
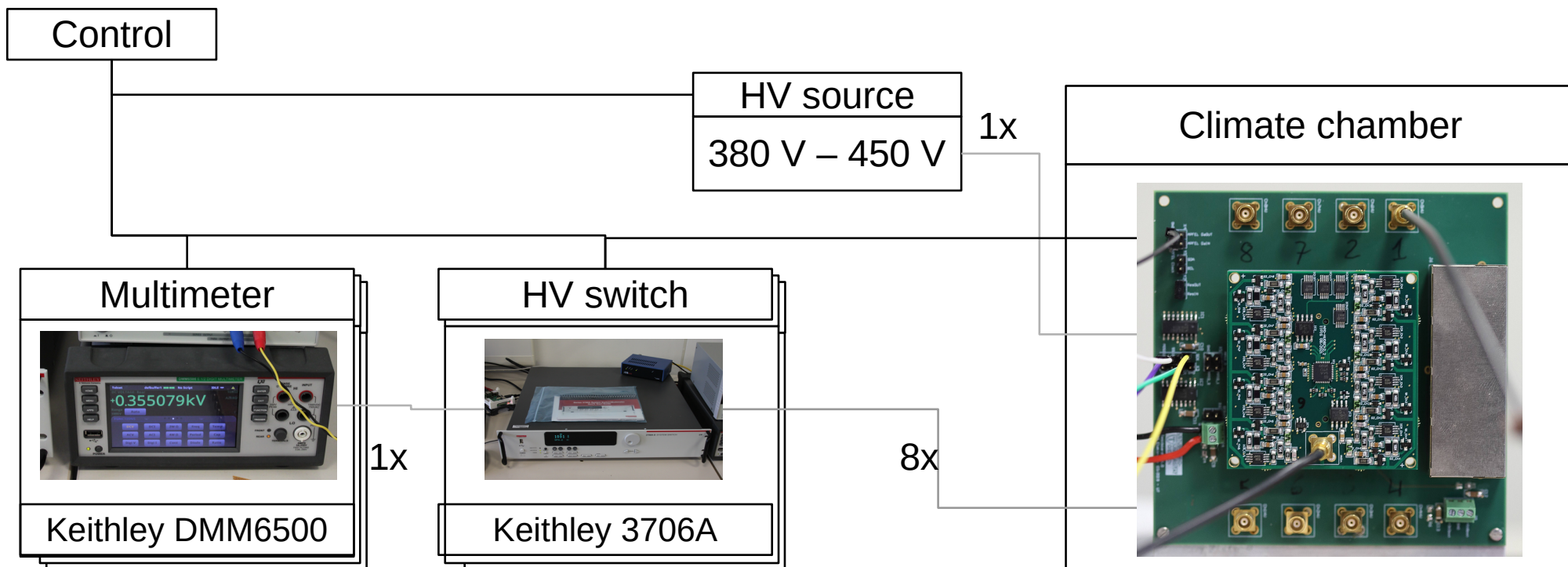


- One Frontend unit consists of 4 crystals, 8 LAAPDs, 4 APFEL ASICs and three specialized PCBs (Backplane-, Interface- and High voltage distribution PCB)
- 200 HVD PCBs ready for testing
- Backplane PCB ready for production
- Interface PCB (next to final version)
 - one more test run needed for finalization (5 PCBs for DaisyChain tests)
 - FPC connector, Power connector and disable need repositioning and/or reassignment

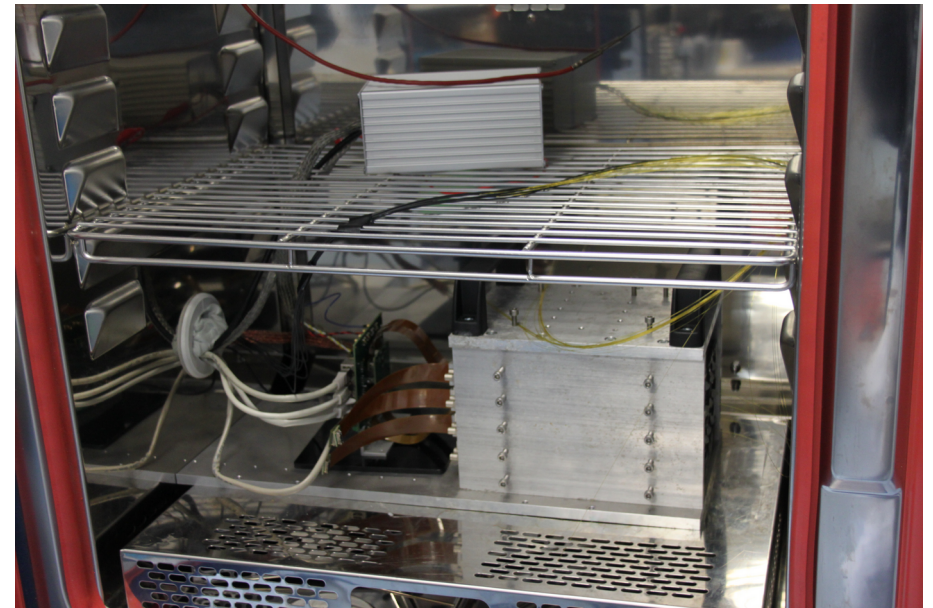
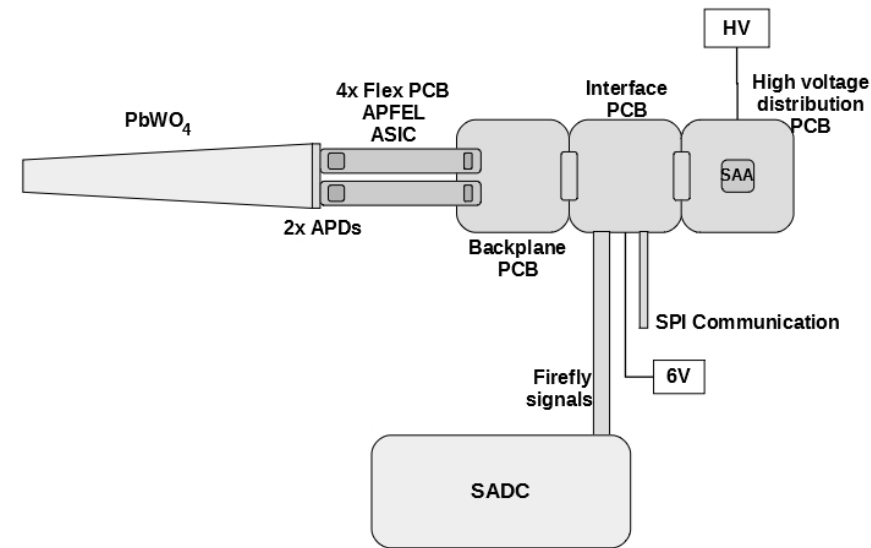


HV PCB calibration

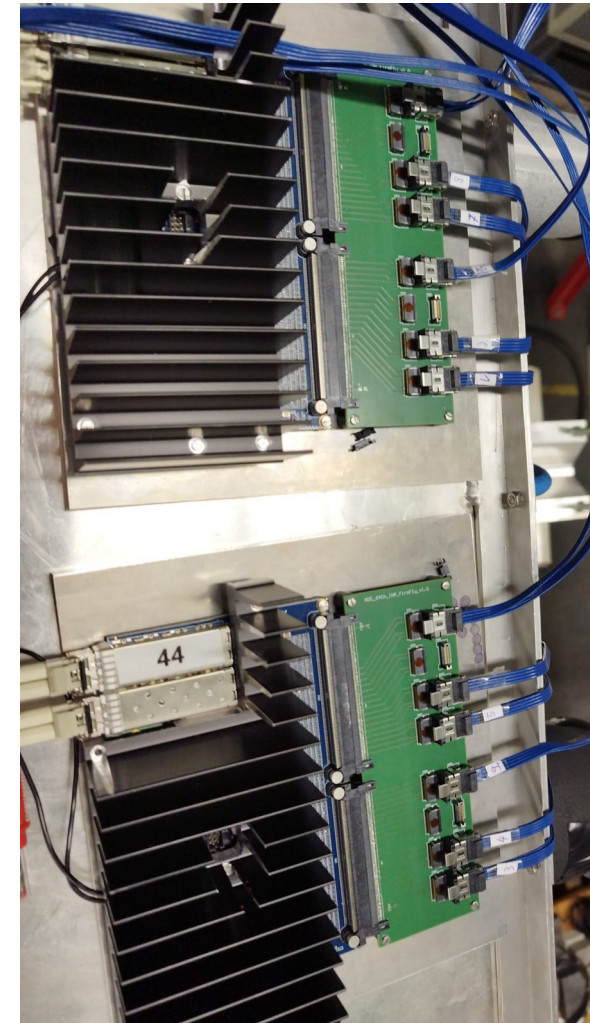
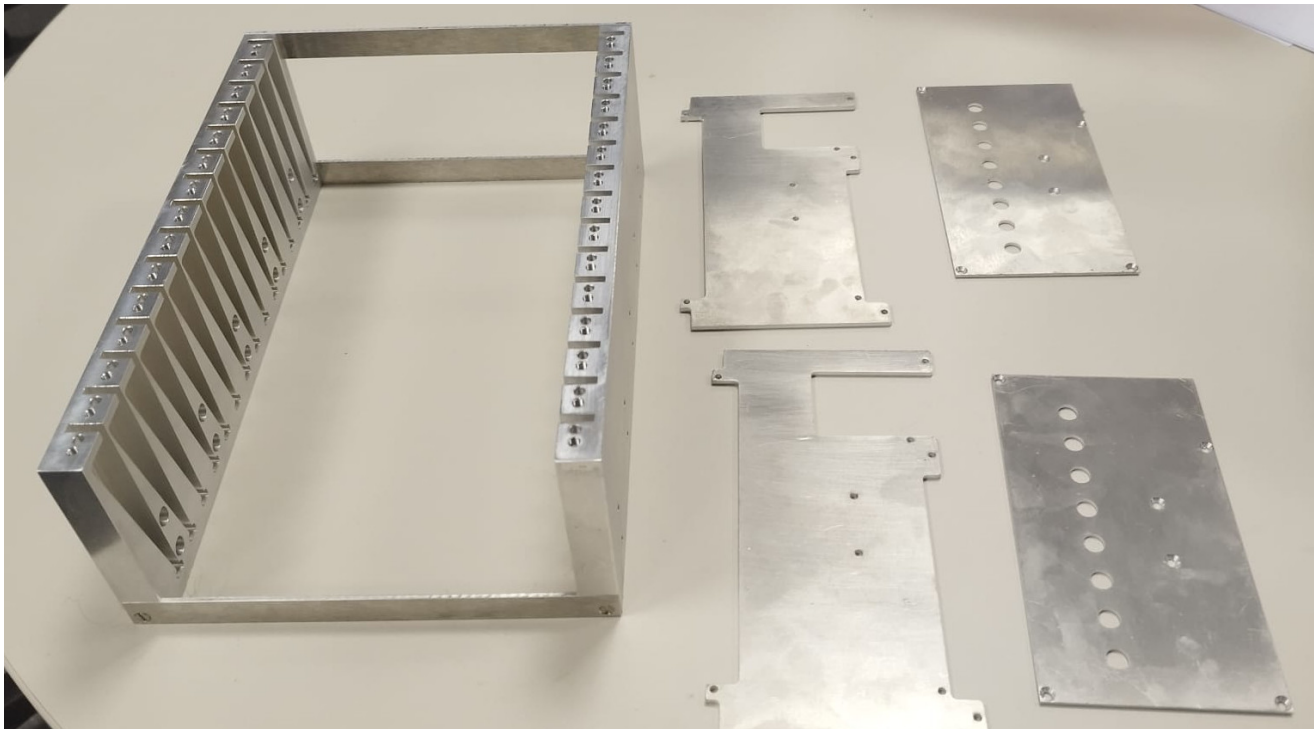
- First tests without HV (power consumption, slow-control, interfaces and so on)
→ Can be done in house
- HV test setup inside a climate chamber for temperature measurement and stabilization
- Switch, HV-source and measurement outside controlled volume
- Two systems available, approx. a whole day measurement time per unit
- Temperature calibration currently finalization process



- Backplane PCB & Interface PCB tests can be done at a small detector unit (4 Frontend units)
- Features and functionalities to be tested: Daisychaining, Lightpulsers signals, APFEL testpulse in lieu of real experimental signals
- Readout with SADCs and the setup should probably be in a climate chamber
- 1-2 days setup and measurement time

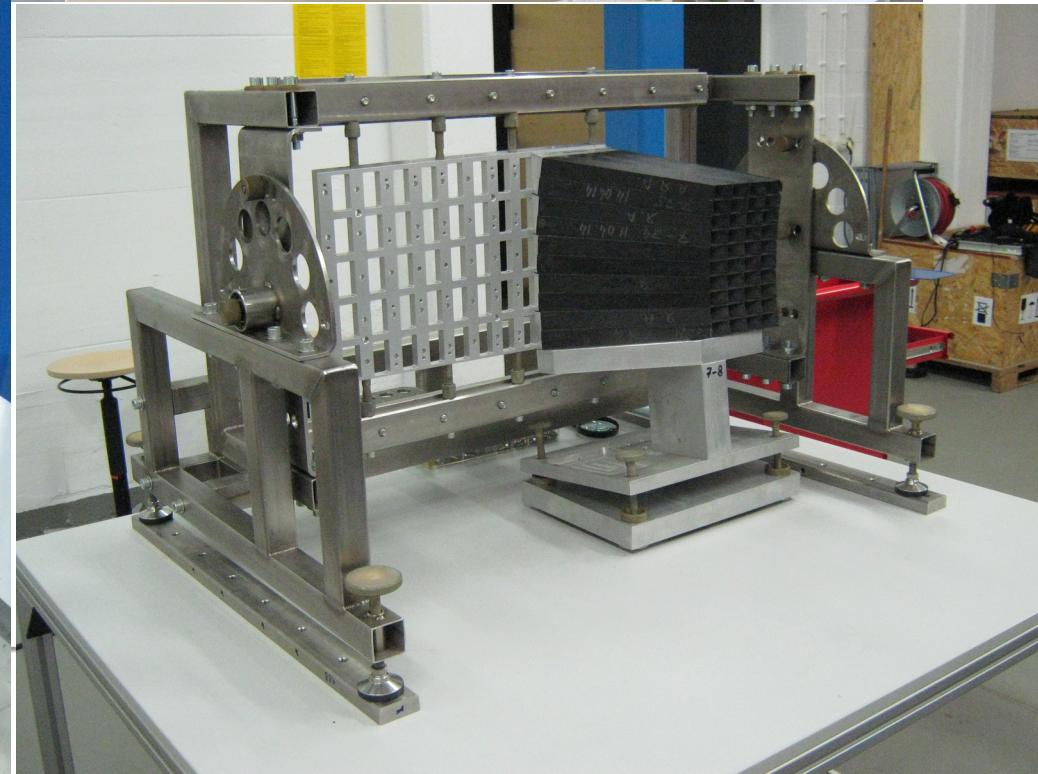
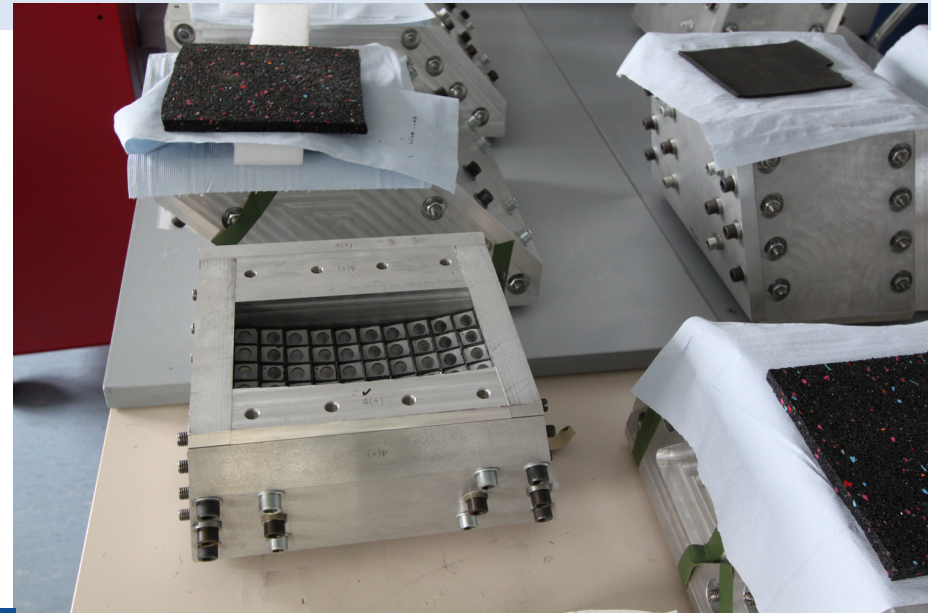


- Concepts (firmware/ measurement wise and mechanical/cooling wise) for whole slice tests/calibration needed
- Experience with VHDL necessary, if changes to the firmware are to be made
- Cooling/mechanical concept in progress by Pawel Marciniewski



Module Assembly

- Careful assembly and glueing of the parts into the carbon fibre alveoli
- Curing time of minimum 24 hours
- Careful assembly of the supermodule with specialized tools
- One complete set of tools is available in Giessen



Slice Assembly and Cabling

- Assembly of the super modules into the slice is fast, but the cabling and connecting of the FEE takes long
- Minimum 2 weeks for complete assembly of slice
- Cabling is an issue to be solved, when the first slice is assembled completely

