Update on hardware activities

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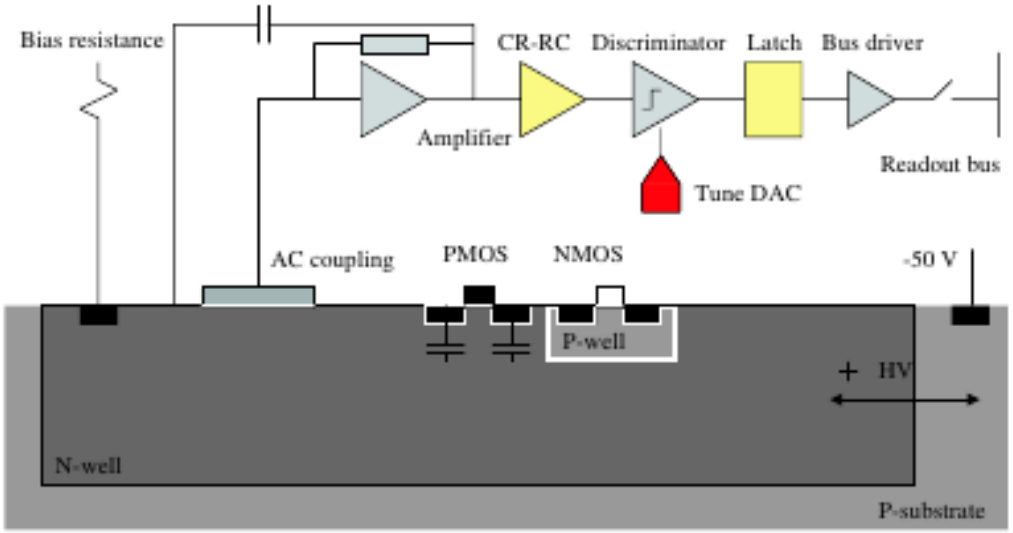
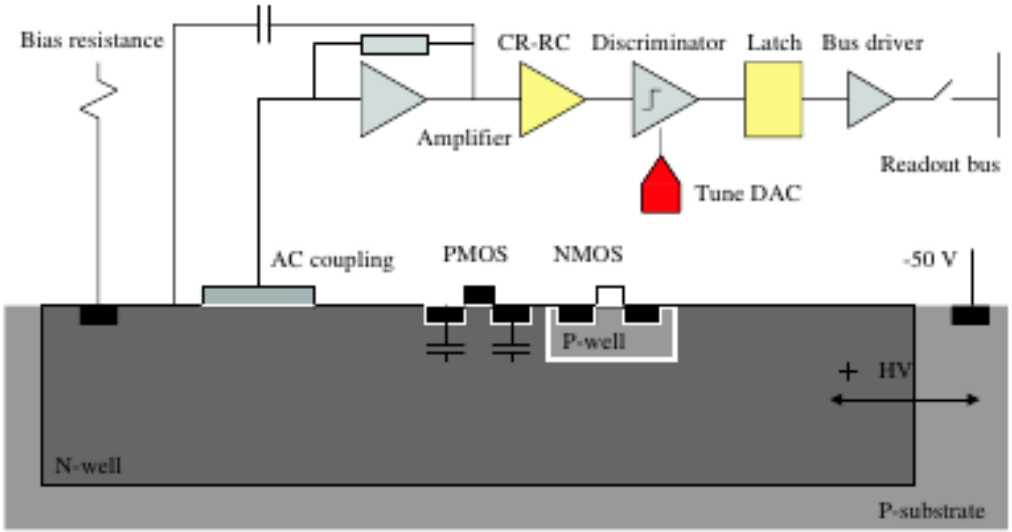
HV-MAP



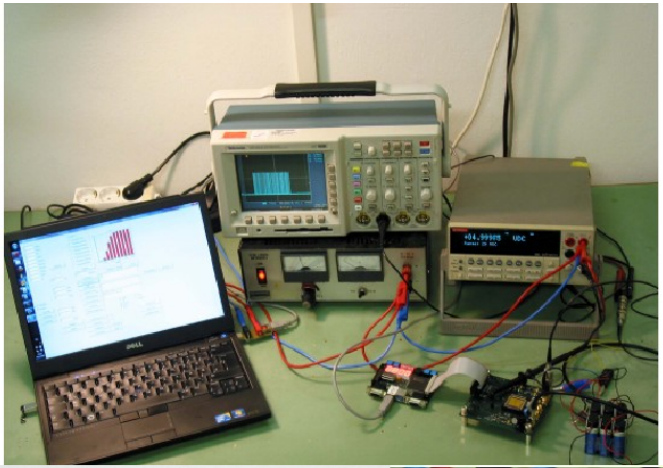
- high radiation tolerance
- fast charge collection
- thickness of 50 μm
- low power consumption

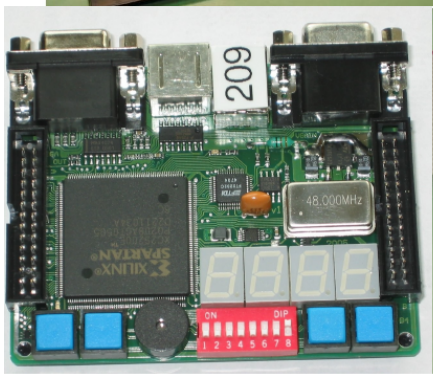
HV-MAP

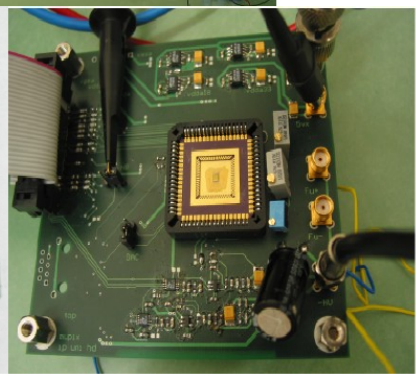


- ToT measurement
- self triggering (planned)
- readout frequency of 20-40 MHz (planned)

HV-MAPs test @ Heidelberg

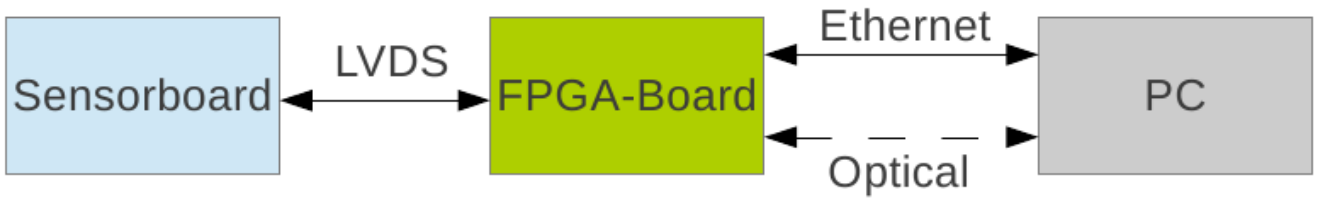




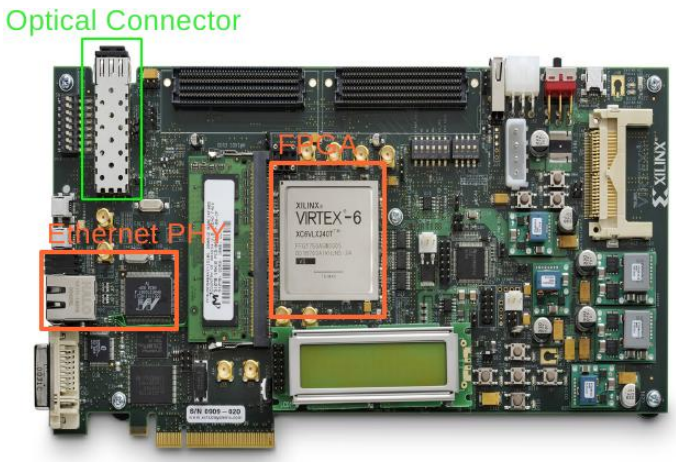


- data readout by FPGA-Board (Spartan 2)
- connection to PC via USB-Port

HV-MAPs test @ Mainz



- start with boards developed at Heidelberg/Mannheim
- replace FPGA with ML605:
  - slowcontrol via ethernet
  - data transfer using optical link (SIS1100-Protocol)



Status of Communication

Ethernet

- tri-speed ethernet interface (thanks to Simone Esch)
- UDP-Protocol implemented for sending data to PC
  - automatic calculation of IP-Header checksum
  - no checksum for UDP-data
- work on receiving of UDP-packets in progress

Optical link

- connection between FPGA-board and pc
- first tests successful