



# Status of ATR16 / CTR16 Development

Holger Flemming

07.02.2024

# Outline

- 1 Reminder ATR16 / CTR16
- 2 CTR16 Measurements
  - General Observations
  - Front End
  - Transient Recording and Digitisation
  - Data Transport
  - Conclusion
- 3 Outlook

# Outline

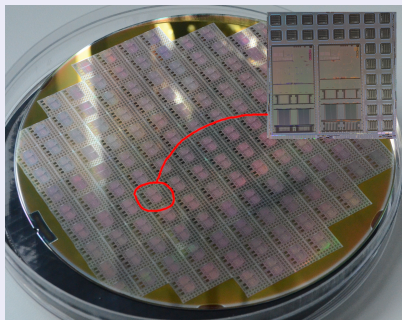
- 1 Reminder ATR16 / CTR16
- 2 CTR16 Measurements
- 3 Outlook

# Reminder ATR16 / CTR16

## 2 Variants of Transient Recorder

- ATR16
  - Transient recorder with input buffer for external preamps
  - PANDA EMC
- CTR16
  - Transient recorder with integrated charge sensitive amplifier
  - Originally PANDA GEM
  - SFRS GEM-TPC

## Engineering Run



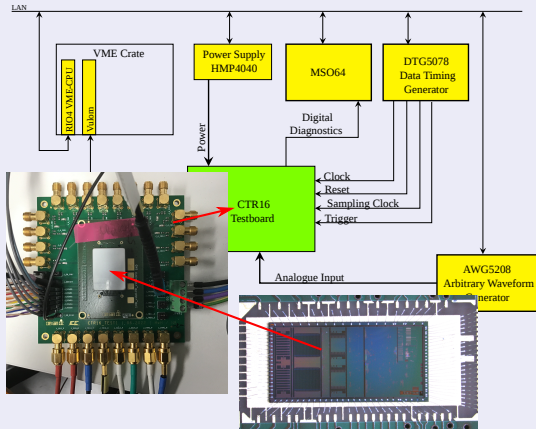
- GSI Engineering run end of 2021

# Outline

- 1 Reminder ATR16 / CTR16
- 2 CTR16 Measurements
  - General Observations
  - Front End
  - Transient Recording and Digitisation
  - Data Transport
  - Conclusion
- 3 Outlook

# CTR16 Test Setup

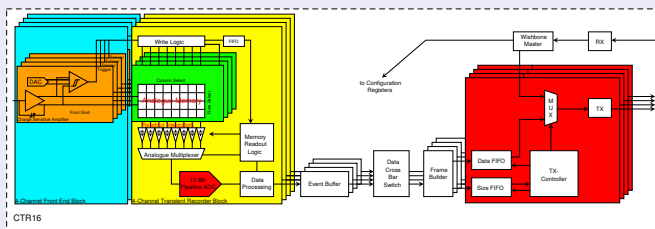
## CTR16 Testsetup in ASIC Lab



# CTR16 Measurements

## General Observations

### CTR16 Block diagram

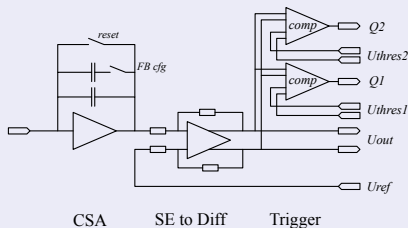


- Power consumption ✓
  - IO: 20 mW
  - Digital: 150 mW
  - Analogue: 740 mW
- Communication works ✓

# CTR16 Measurements

## Front End

### Front End Unit



- Threshold voltages generated by 12 bit differential DACs
- $U_{ref}$  generated by 12 bit single ended DAC

### Front End test and characterisation

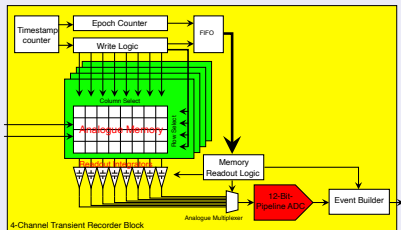
- Response to DAC settings as expected ✓
- Threshold scans ✓
- Automatic threshold setting works ✓
- Baseline tracking for drift compensation works ✓



# CTR16 Measurements

## Transient Recording and Digitisation

### Block Diagram of Transient Recorder



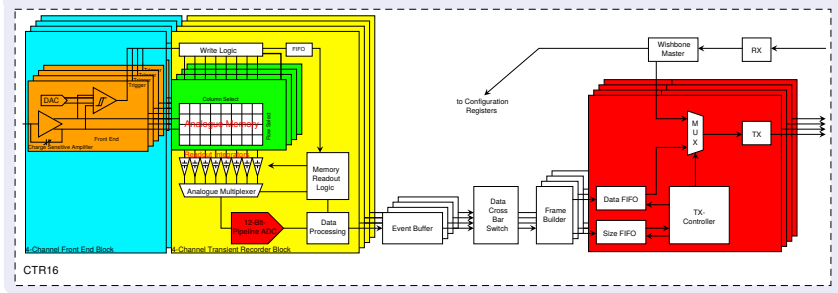
### Test of Recording Unit

- Finite state machines of all units checked on diagnostic outputs ✓
- ADC calibration stable over hours ✓
- Transient data seen ✓
- First look into analogue memory characteristics ✓

# CTR16 Measurements

## Data Transport

### Issues in Data Transport



# CTR16 Measurements

## Data Transport

### Issues in Data Transport

Several issues found in CTR16 data transport

- Large amount of error events  
**Understood:** Wrong handling of SRAM outputs in idle state causes error flag of hamming decoder
- First Event of an epoch is lost in each block  
**Understood:** Event builder → Block buffer communication; idle clock cycle has to be introduced between epoch and data event
- Data of a complete block are lost  
**Understood:** Non initialised flag for epoch prepending decision

# CTR16 Measurements

## Data Transport

### Issues in Data Transport

Several issues found in CTR16 data transport

- No data are seen when at least one block does not get any trigger  
**Understood:** Crossbar switch does block data time sorting.  
Frozen epoch number on one block inhibits data transport of other blocks
- Hang-up of crossbar switch  
**Not yet completely understood**

# CTR16 Measurements

## Data Transport

### Hang-up of crossbar switch

- Observation: Under unknown circumstances no further data from a complete block are send
  - Trigger selector state machine remains in *request back end* state
  - Request is not seen in crossbar switch diagnostics  
Probably masked by wrong epoch number
  - Frame builder is waiting
  - After very long time ( $O(\text{days})$ ) data are seen again
- Issue not yet completely understood
- Reasonable suspicion: Also connected to time sorting mechanism

# CTR16 Measurements

## Measurement Conclusion

- First iteration of CTR16 was extremely successful
- Except for issue in cross bar switch complete complex logic for control, readout and data transport is operational. Minor bugs are understood.
- Issue in cross bar switch makes precise analogue characterisation with high statistics and data taking difficult.

## Conclusion for ATR16

- ATR16 not yet tested
  - Analogue memory readout and data acquisition backend are identical on ATR16 and CTR16
- ⇒ It is expected that issues in data transport affect ATR16 as well

# Outline

- 1 Reminder ATR16 / CTR16
- 2 CTR16 Measurements
- 3 Outlook

# Outlook

## Next Prototype Iteration

- In May 2023 idea raised up to start a further GSI UMC180 engineering run.
- CTR16 foreseen to be placed on this run.
- New CTR16 with correction of all known Bugs.
- Extensive simulations done which in particular model the error conditions observed in the first prototype.
- Tape out originally foreseen for summer 2023. Current schedule: tape out end of this month.
- Last week I got the information that there would be space available for ATR16.
- Currently evaluating whether its feasible to produce new ATR16 design until end of this month.



# Thank you for your attention