Updates on the MVD front-end electronics
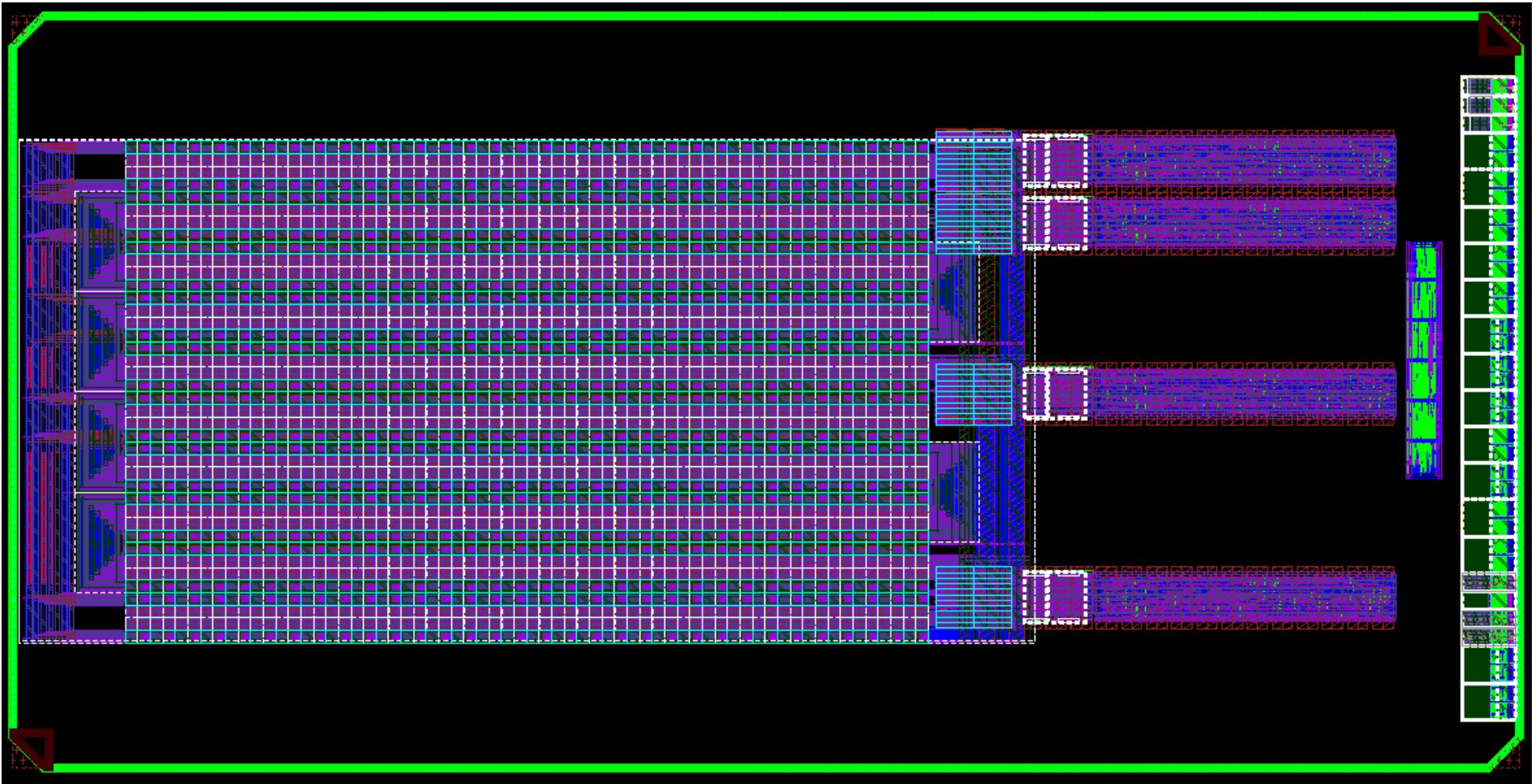
G. Mazza, A. Rivetti

INFN-Sezione di Torino, Italy
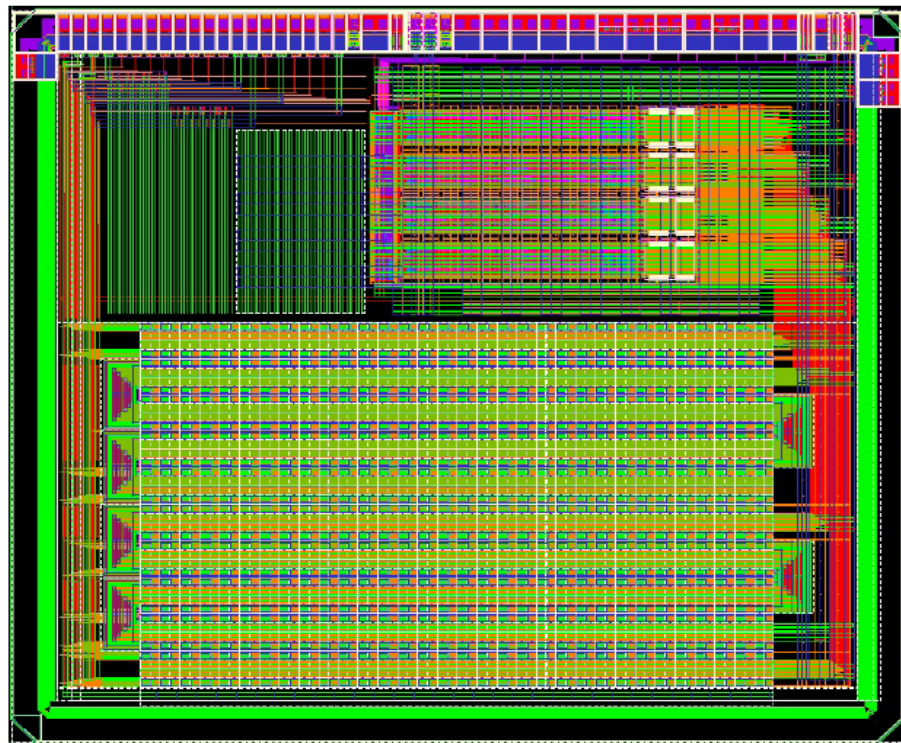
- Next submission scheduled for November 2012
- Matrix layout compatible with existing sensor geomerty.
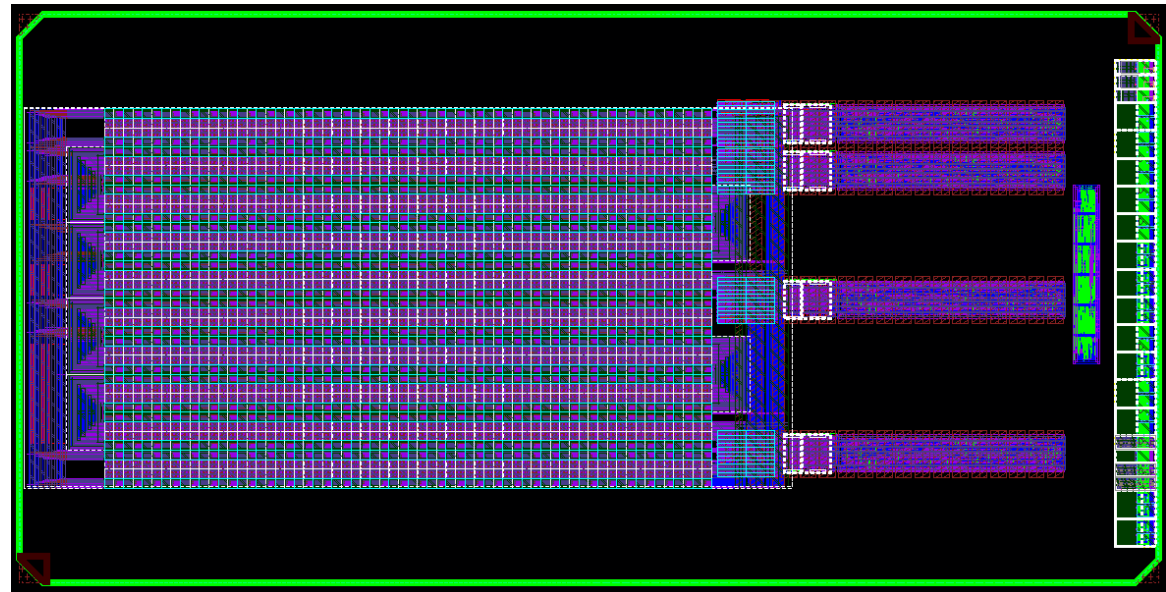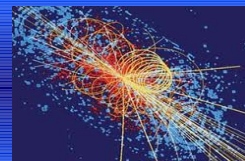- Modifications mainly in the digital part.

- New form factor: 6 mm x 3 mm
  - Motivation: Reduce the bus length between the end of column and the column readout logic, This arrangement is the same foreseen for the final layout.

Topiv_v3 layout

Topiv_v4 layout

- Reduce capacitive load on the time stamp bus.
  - Motivation: Reduce the power dissipation to drive the lines.
  - Increase the bus speed, targeting 160 MHz operation also for the long column.
  - Through layout optimization the capacitance on the lines has been almost halved (from 6.9 to 3.8 pF)

- New timestamp drivers and column receivers. Revise timing for column
  - Motivation: As above: increase speed, optimize the power

- E-link interface to the GBT
   - Motivation: have the final output structure

Topix_v4 status

| Activity	Status
End of column revision	done
New column RX/TX	done
Pixel logic redesign	done
New pre-charge circuit	ongoing
Matrix layout	ongoing
E-link	to be done

- A lot of work can still be done with Topix_v3.

  - Irradiation and beam tests.
  - Understanding performance with DC-DC converters. First test will be done soon (starting this week) on performance studies (mainly noise) of Topix_v3 chips powered by CERN DC-DC converter modules.
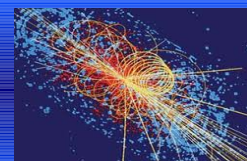 - Further details studies and performance cross-check.
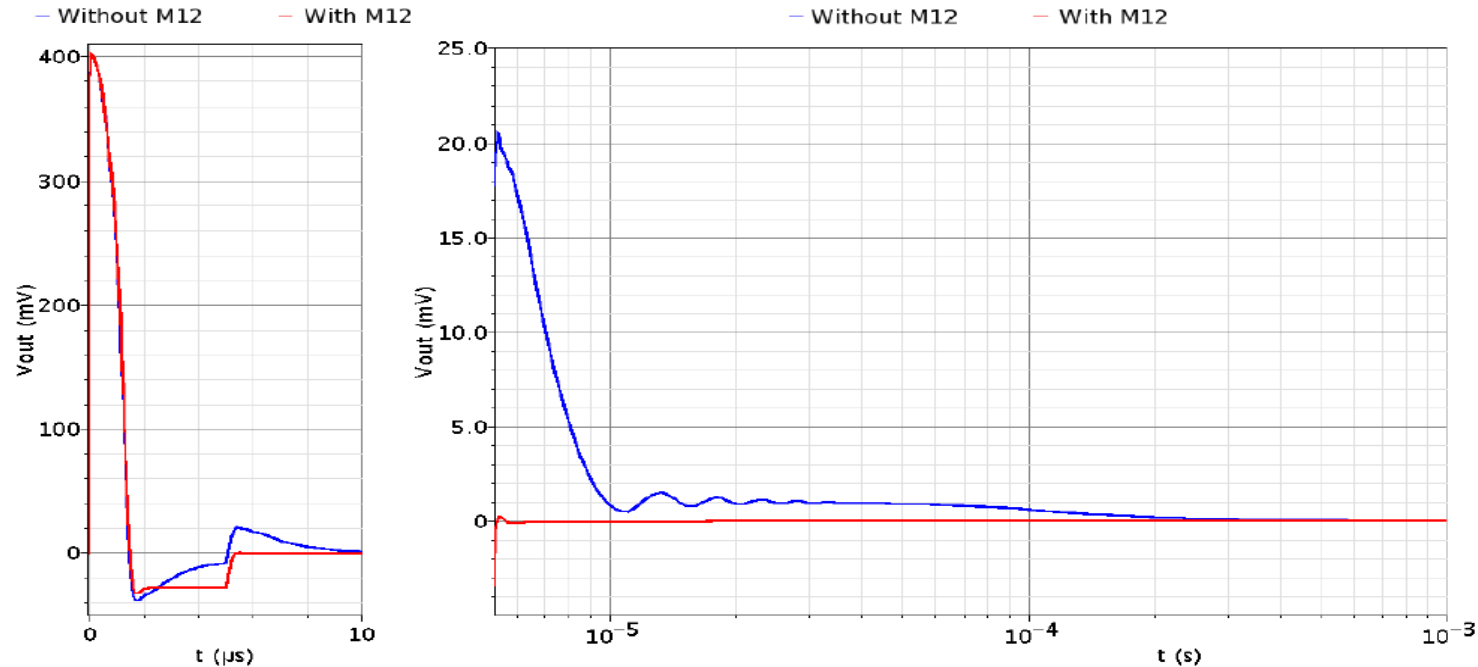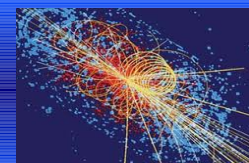
- An important issue to be understood is time walk.

- Time walk has to be expected, as getting in time values (especially for 160~MHz clock) would lead to prohibitive power consumption.

- Zero crossing techniques not effective as we have to work also with saturated pulses. So, some form of time-walk correction almost unavoidable. But where time walk can arise? Natural candidate: preamplifier, but...
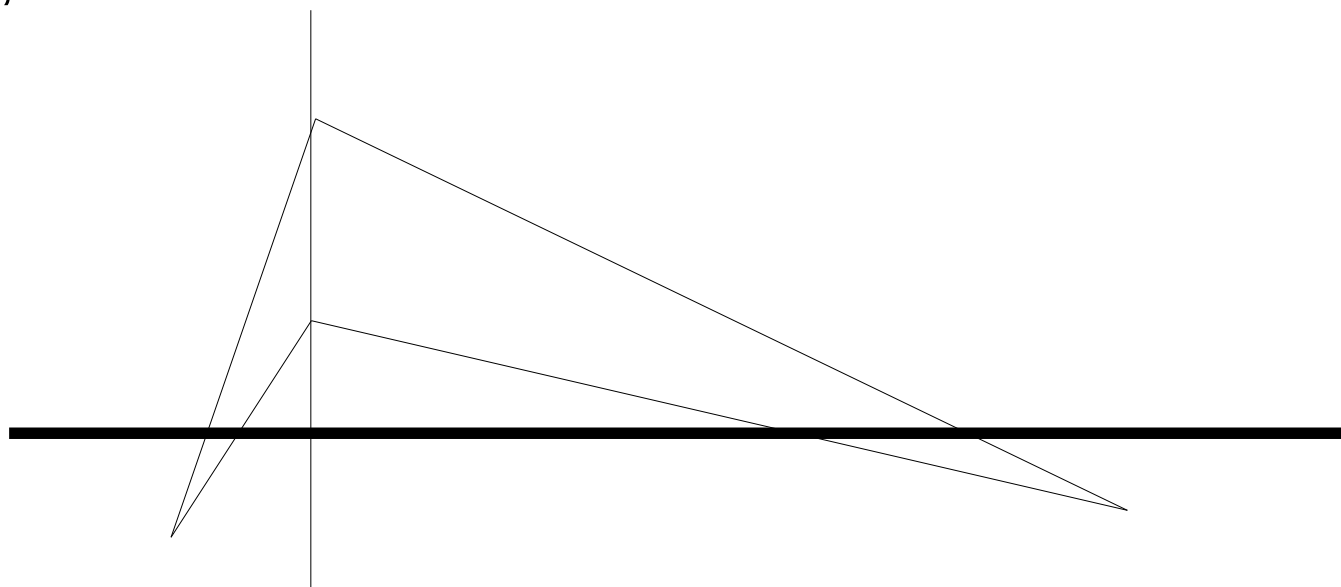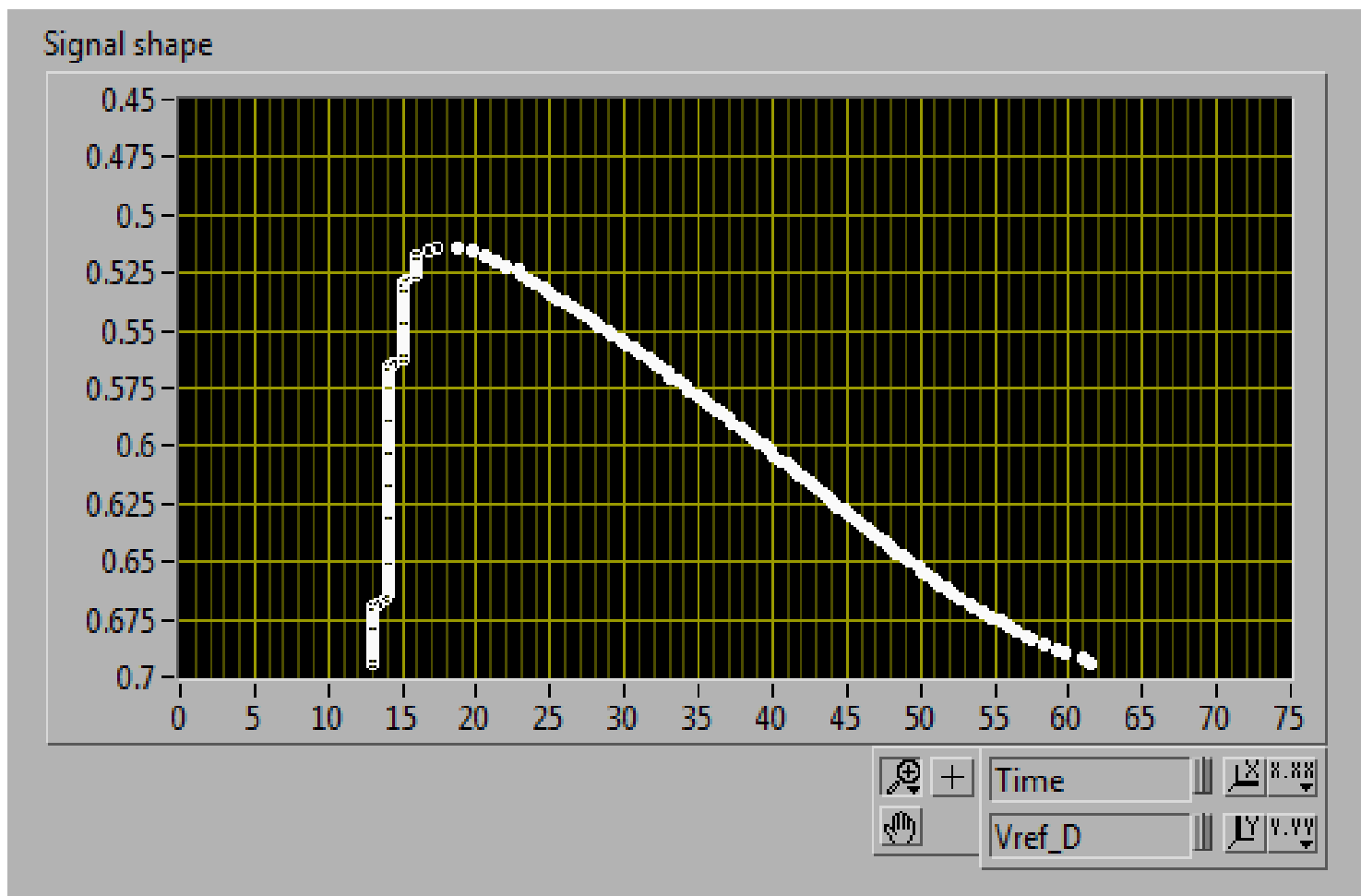
Threshold is put at 10~mV from the baseline (900 electrons)
Assuming 70 ns rise time a signal of 4500 electrons should cross the threshold in 14 ns...
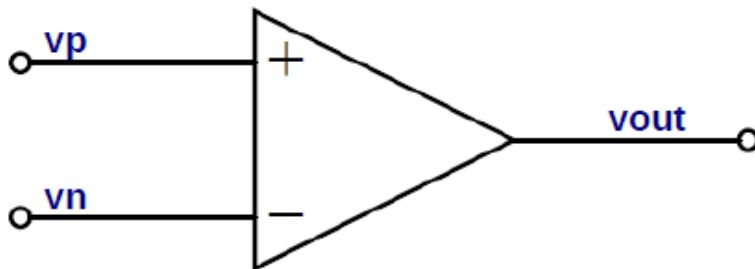
● This seems to be confirmed by the reconstructed pulse shape

But... what about the discriminator?

NSS 2011 Short Course on Integrated Circuits for Time and Energy Measurements

2011 IEEE Nuclear Science Symposium and Medical Imaging Conference

Discriminator propagation delay

$$A(s) = \frac{A_0}{(1 + s\tau_p)}$$

$$\frac{V_{OH} - V_{OL}}{2} = V_{in(min)} A_0 (1 - e^{-\frac{t_d}{\tau_p}})$$

$$V_{in(min)} = \frac{V_{OH} - V_{OL}}{A_0}$$

$$\frac{V_{OH} - V_{OL}}{2} = \frac{V_{OH} - V_{OL}}{A_0} A_0 (1 - e^{-\frac{t_d}{\tau_p}})$$

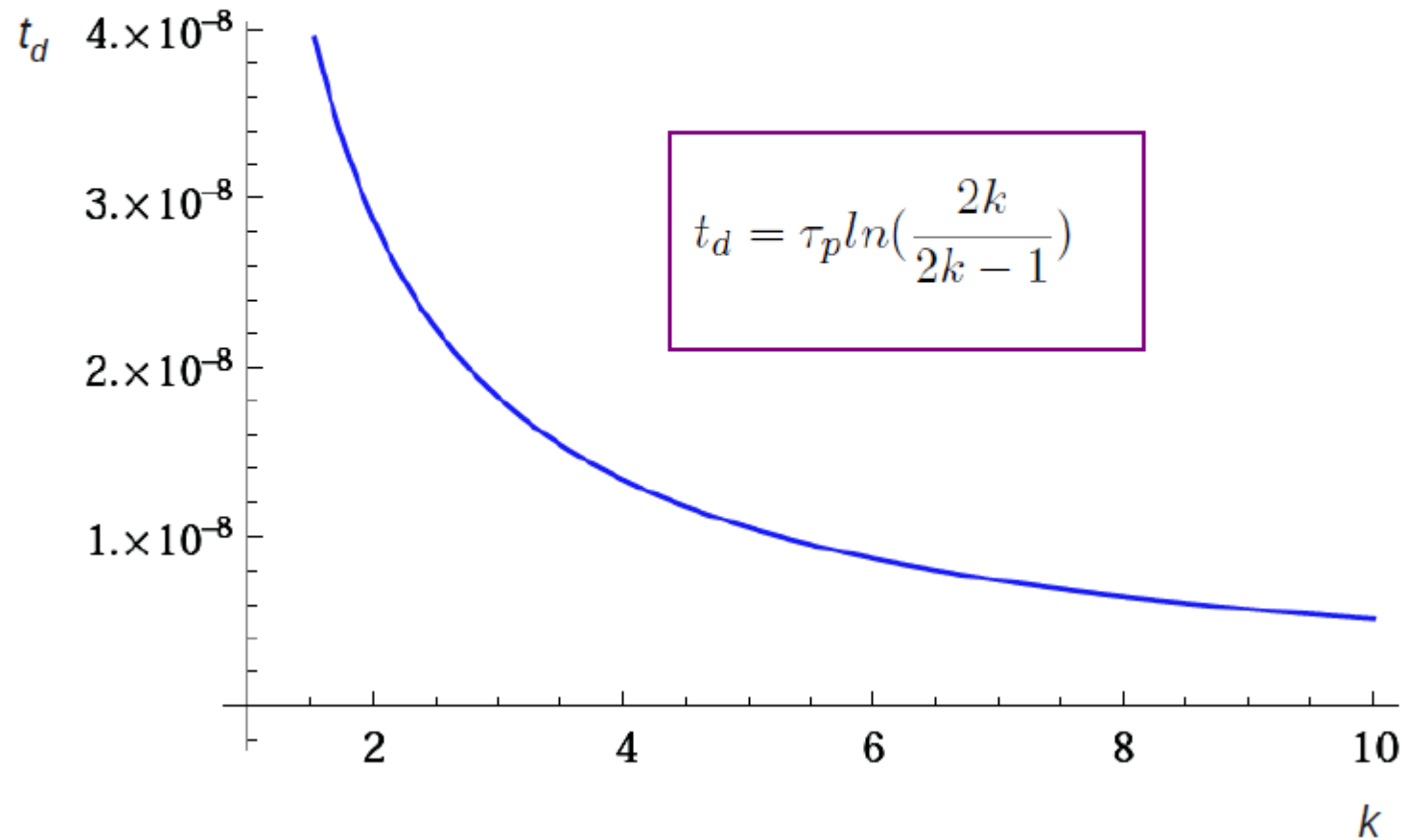$$\frac{V_{OH} - V_{OL}}{2} = k V_{in(min)} A_0 (1 - e^{-\frac{t_d}{\tau_P}})$$

$$t_d = 0.693 \tau_p$$

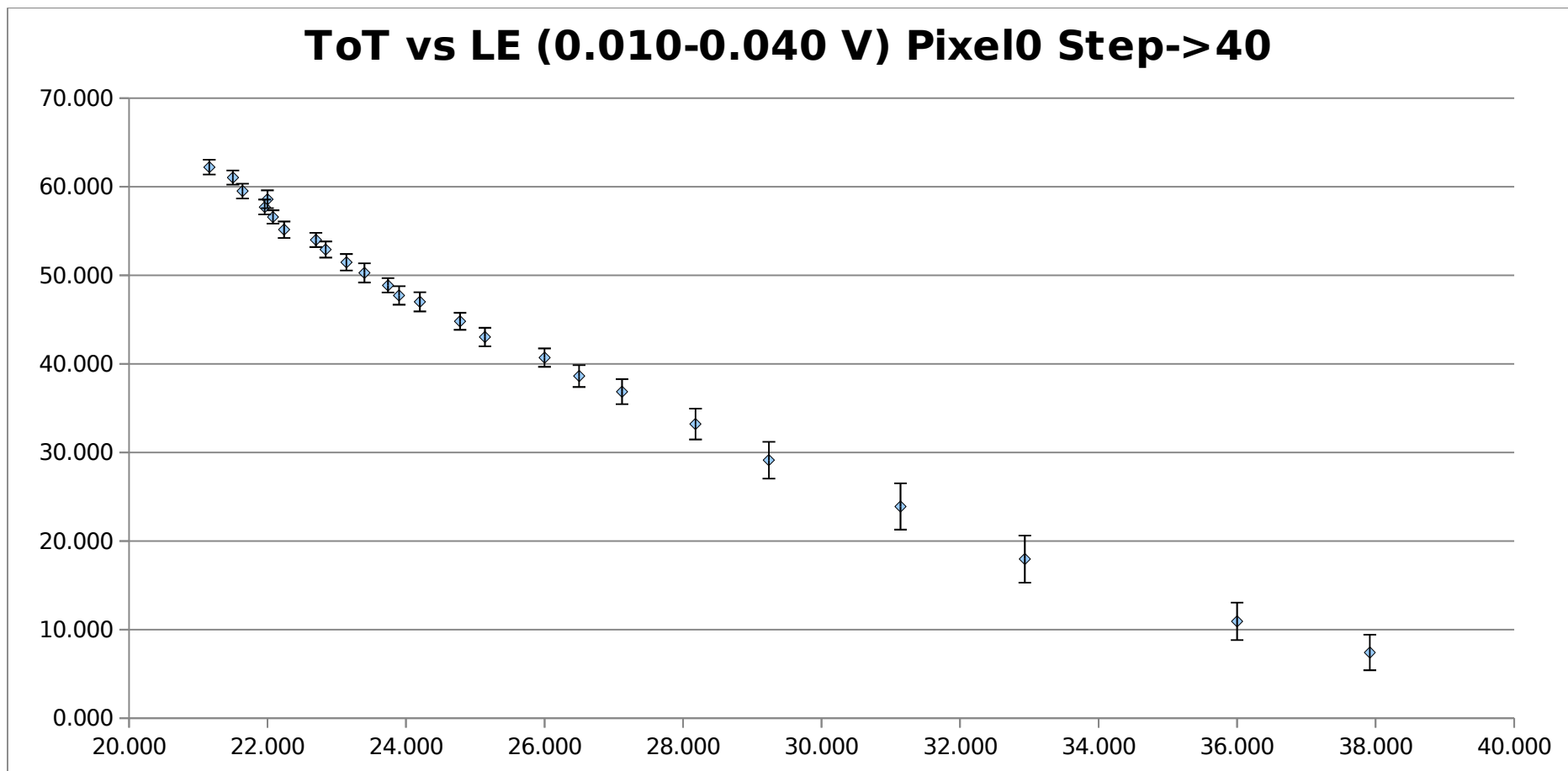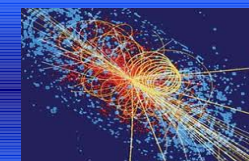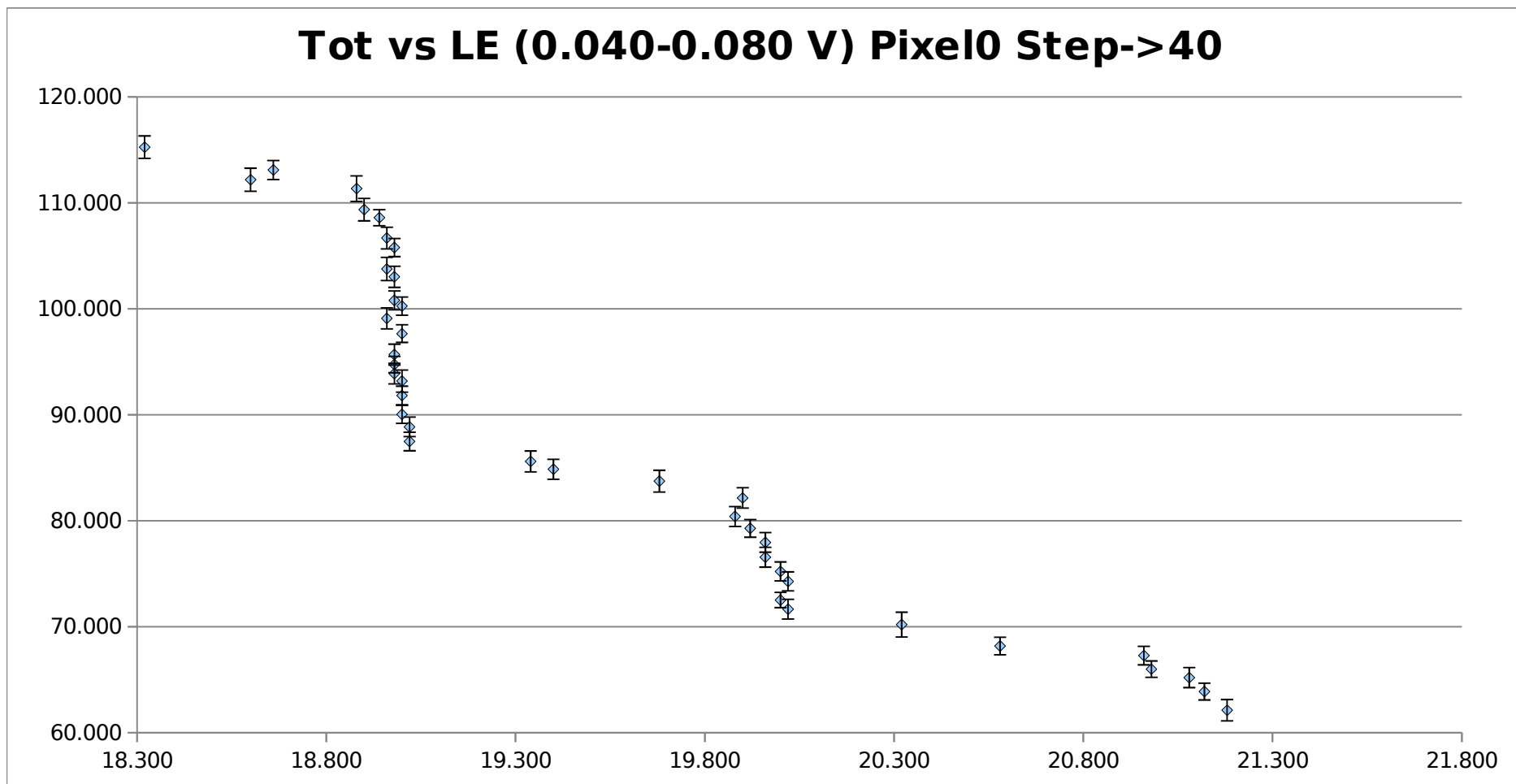$$t_d = \tau_p ln(\frac{2k}{2k - 1})$$
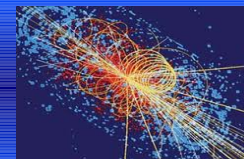
k=ratio between actual and minimum signal

- Propagation delay versus the ratio between the actual and the minimum detectable signal for $\tau_P = 100$ ns.
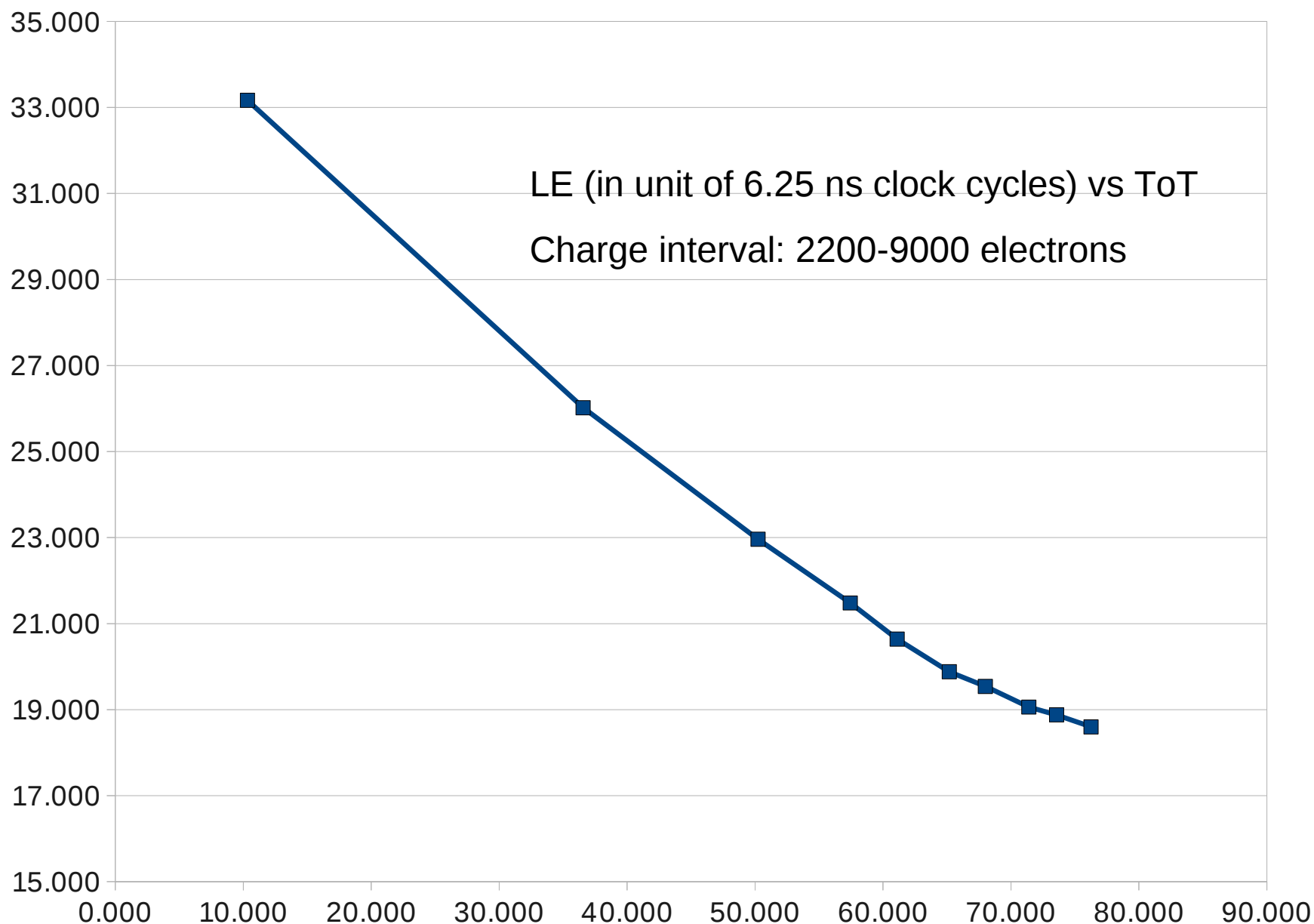
$$t_d = \tau_p ln(\frac{2k}{2k-1})$$

A first calibration exercise (1)

ToT vs LE (0.010-0.040 V) Pixel0 Step->40

Nominal input charge from 2200 to 9000 electrons

Tot vs LE (0.040-0.080 V) Pixel0 Step->40

Nominal input charge from 9000 to 18000 electrons

LE (in unit of 6.25 ns clock cycles) vs ToT

Charge interval: 2200-9000 electrons
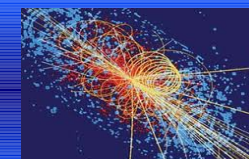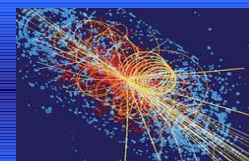
We manage to find two students who got started on the activity

Starting point:

1) The front-end of Topix provides charge digitization with low power (15 uW...)

2) It would be nice to have the readout of the two MVD subsystems as similar as possible to share as much as possiblle:

Back end electronics architecture, expertise, etc...

Unfortunately,the two readout cannot be exactly the same:

1) Detector input capacitance are very different (100 fF for pixels, 20 pF for strips)

- Need more powerful input stage
- Input stage should not saturate to avoid heavy cross-talk

2) Dead time for one single ToT element would be too long.

Assume 100 kHz per strip and 3.2 uS digitization time:

1) Inefficiency with only one ToT stage: 28%
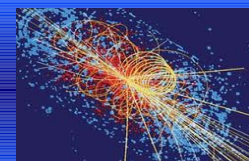
2) Inefficiency with fou ToT stages 3.6e-3

Note that 3.2 uS=9 bit with a clock of 6.25 ns
However, most of the hits will be smaller.
Need to evaluate properly this effect to avoid the risk of having inadequate
resolution on the smaller hits=>some basic physics simulations required
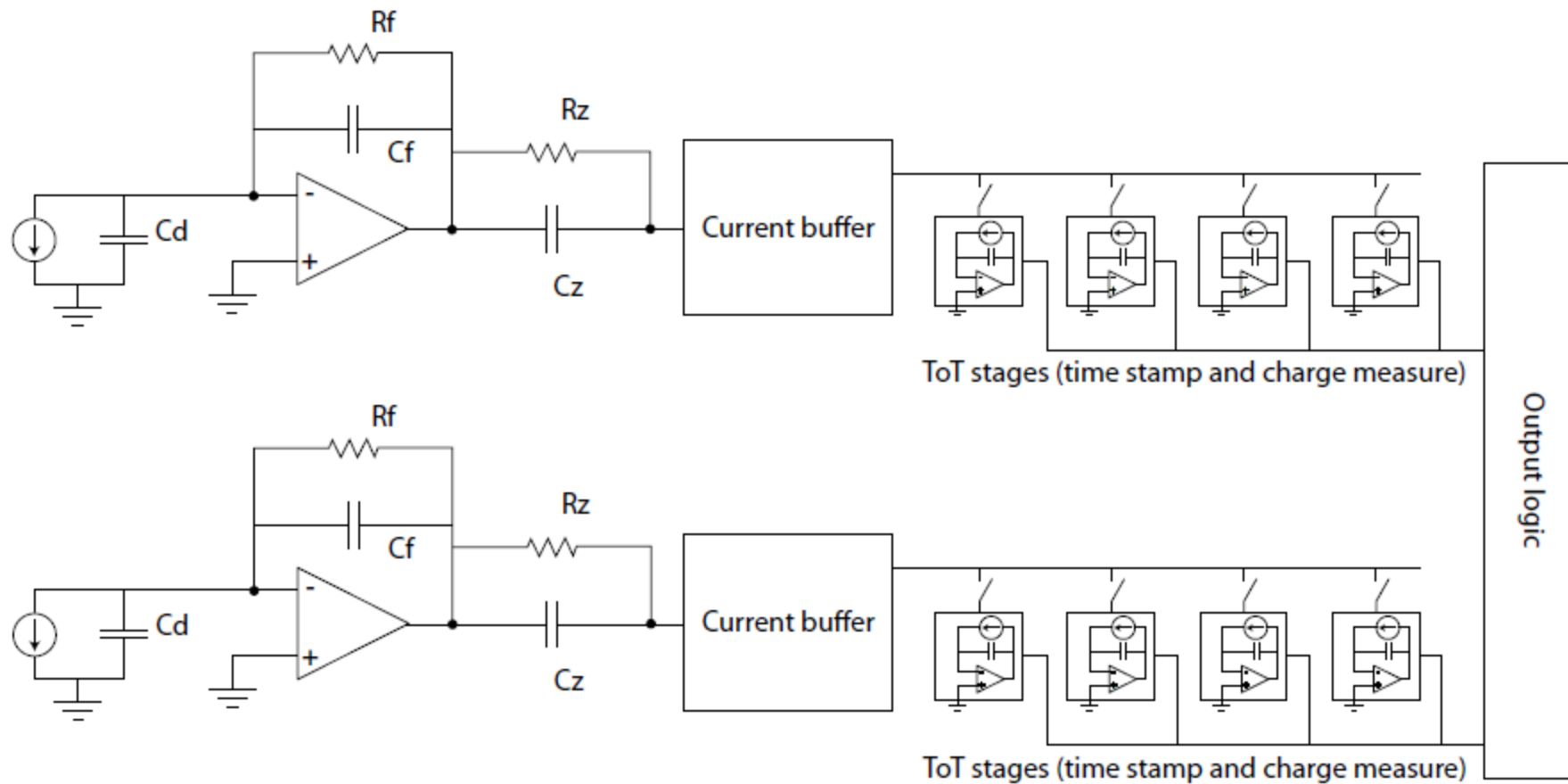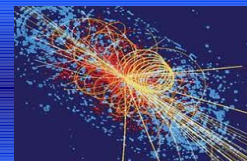
Need proper control logic for the ToT stages...

- Simulations should be run to understand the limits on dead time.

- Restart optimization of very front-end

- Students need also to be trained and write a diploma thesis!!!

- First report on first simulations expected for the GSI meeting in December...
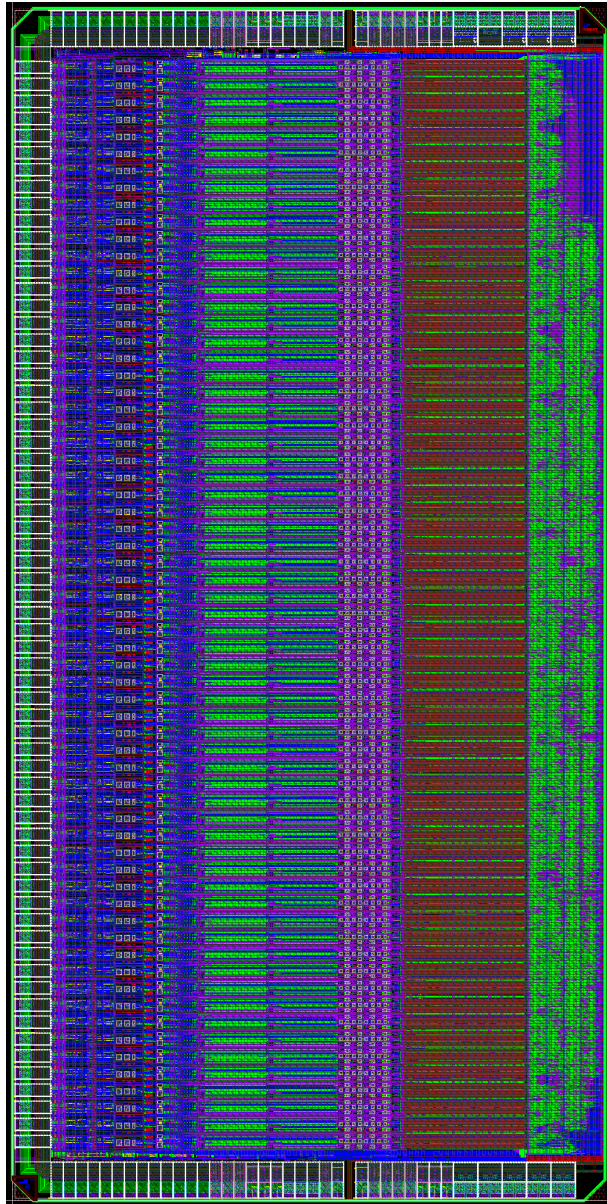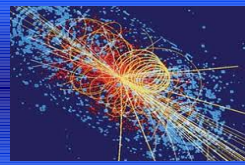
ASIC develop in Torino and LIP (Lisbon) by people
supported by a medical physics project (EndoTOF/US)

64 channels for time based readout of silicon PM
ToT done by measuring directly the duration
of the pulse shape of a fast amplifier with high resolution
TDC (50-100 ps binning)

Good point: The chip is using TDC with analog interpolators
Analog interpolator=Wilkinson ADC. Very similar
problem with efficiency=>Derandomization with 4 buffers

The logic controlling the buffer could be very similar, if not
Identical to the one that we need.

ASIC already produced in an engineering run, expected back
end of the year...