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SEIT 1386

SPADIC
2.2B: Test Results
3.0: ADC

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2023-11-08 CBM-TRD Retreat

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SPADIC 2.2B Testing

(2nd Round of Testing)

Test Procedure

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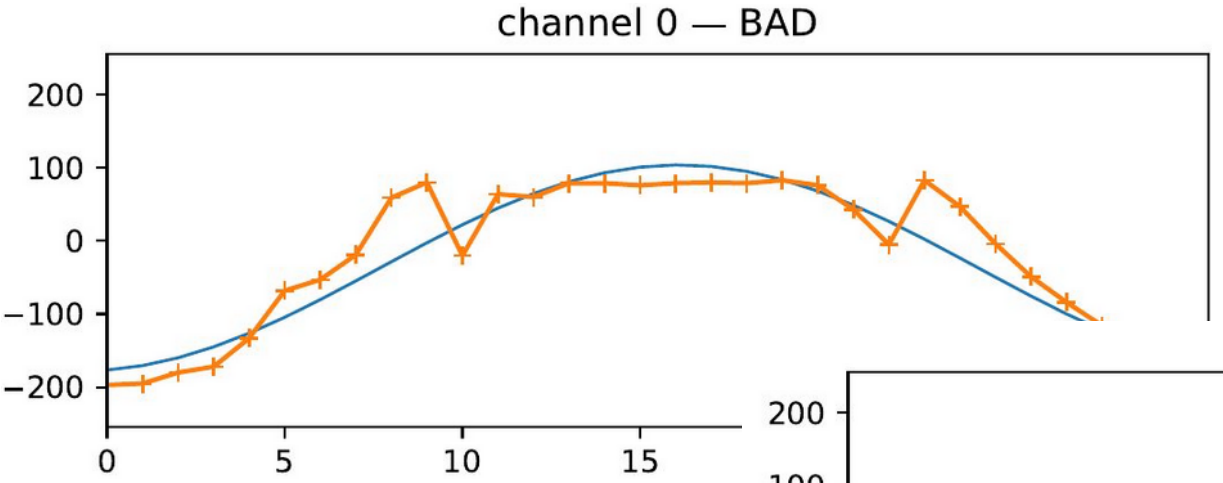
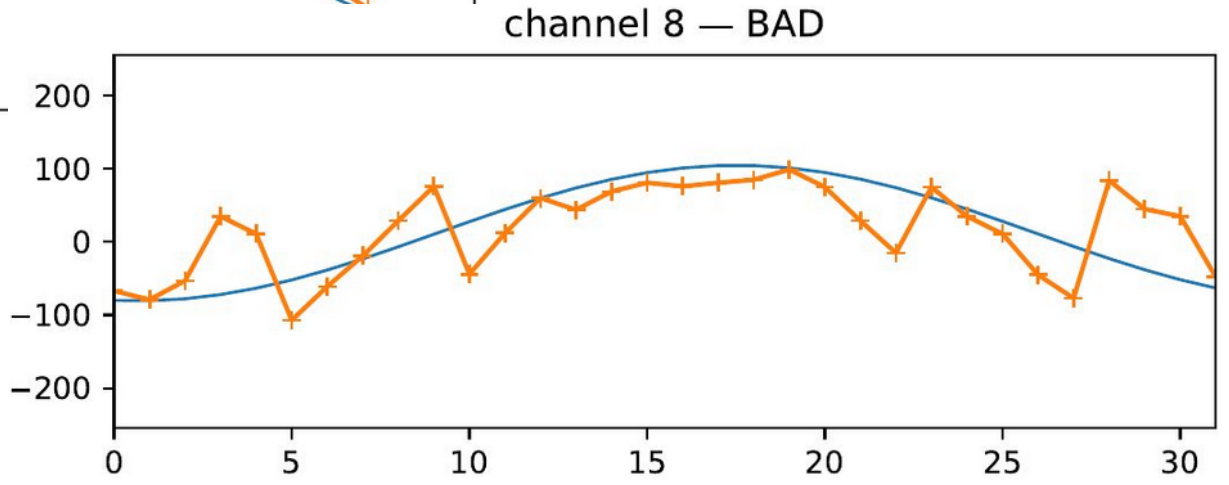
- Test procedure:
  1) Establish link to SPADIC.
  2) Inject a sine curve in all channels in parallel.
  3) Read out and analyze.

  ~ 45 seconds / chip

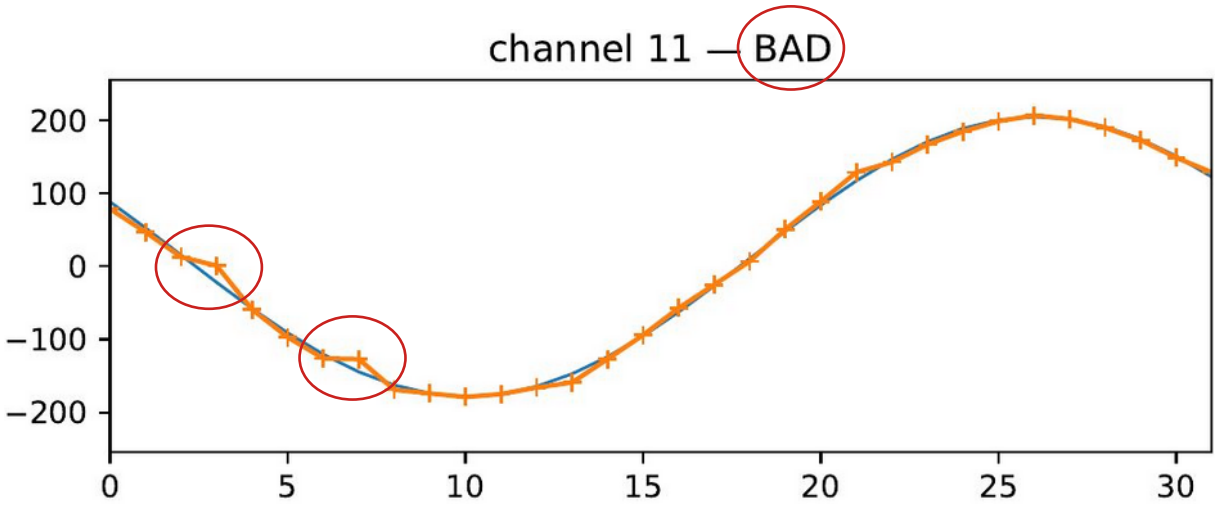
- Criteria for a „good“ channel:
  - Good fit to a sine curve
  - Good gain
- Criteria for a good chip: ≥ 30 good channels.

Very Bad Sine Curves

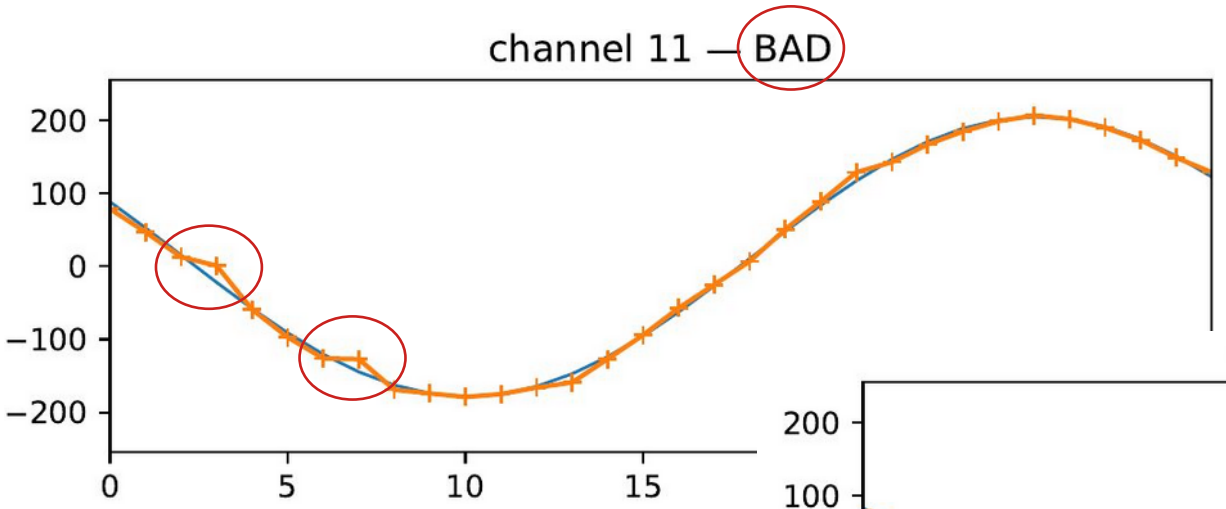


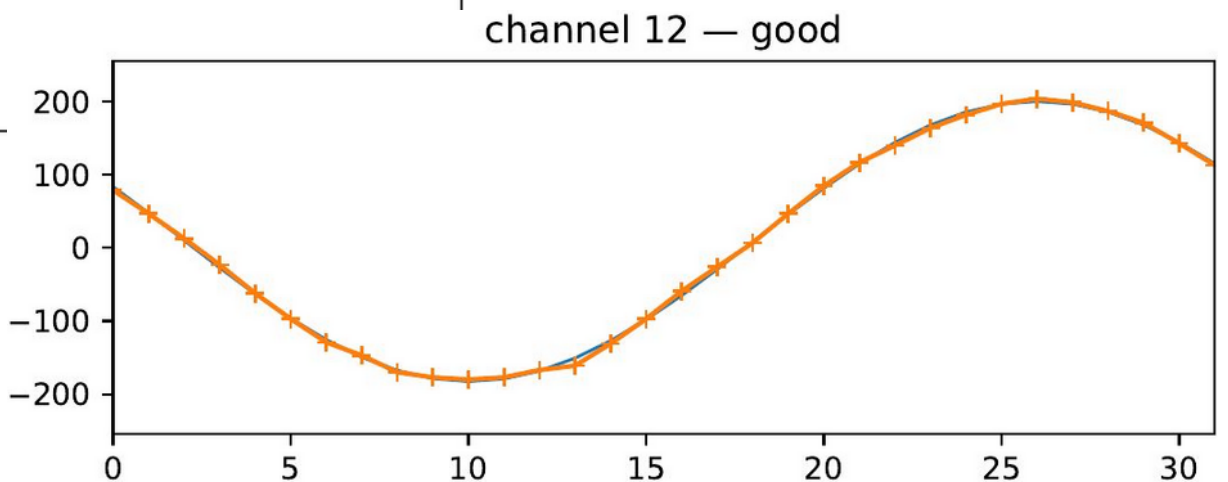


Good / Bad Sine Curve



Good / Bad Sine Curve

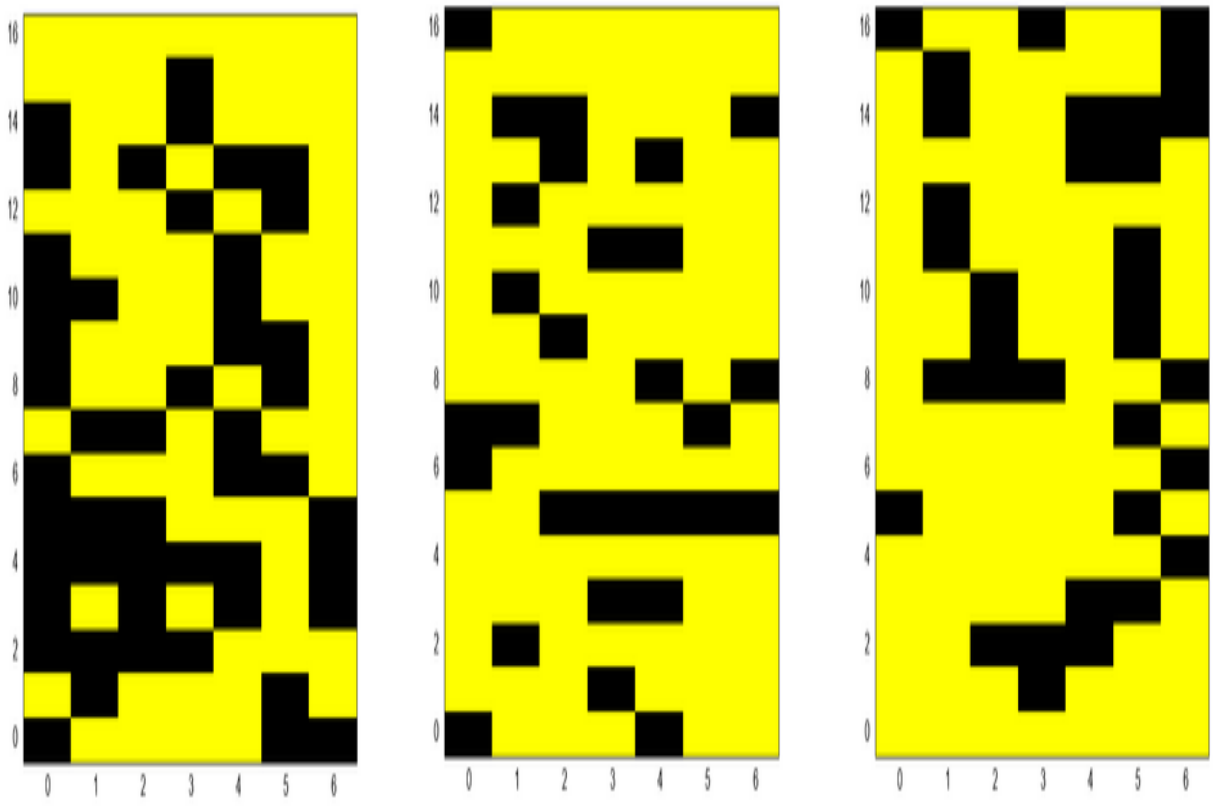




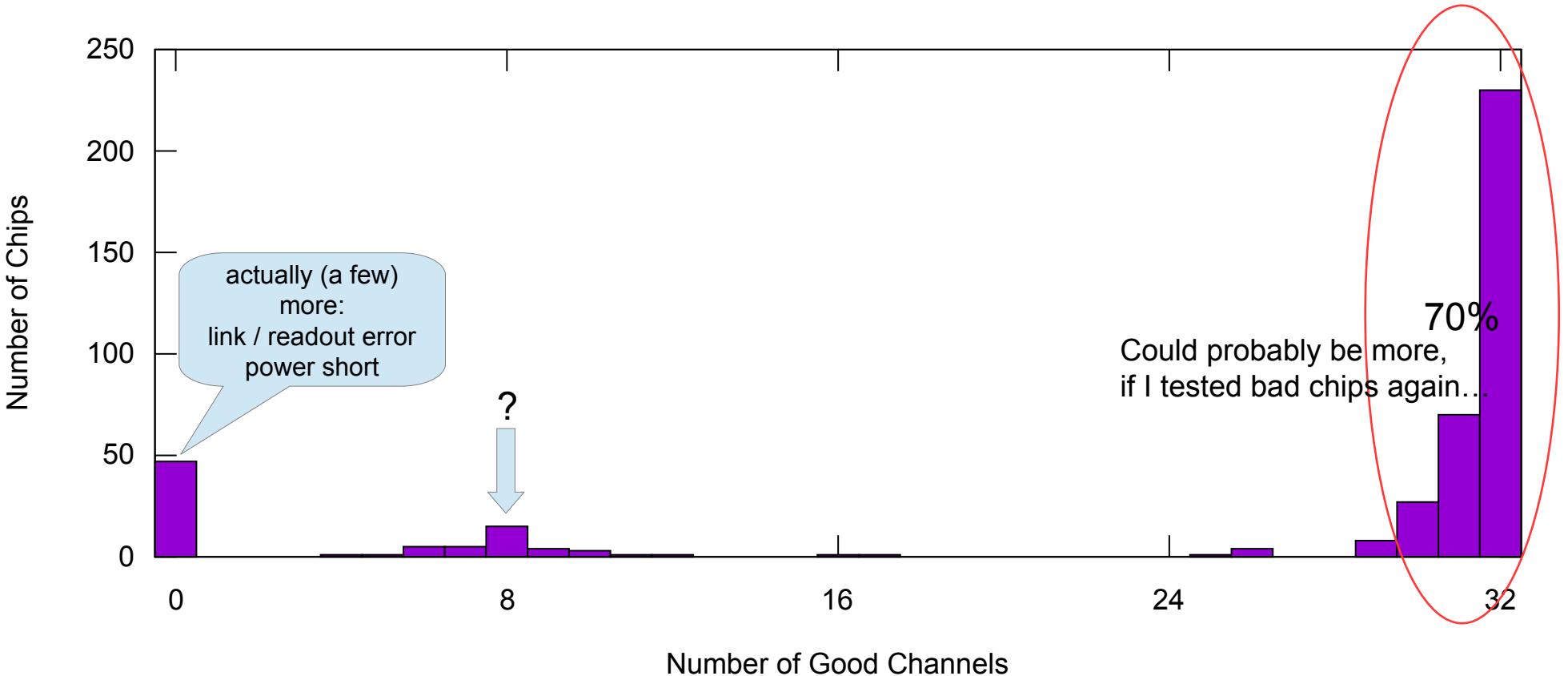
Results by Tray

- by position in tray.
  yellow: good
- 3 trays with 7×17 chips each
  = 357 chip tested.
- 2nd and 3rd tray: better yield.
  ⇒ I learned when it's worth
  to re-try a chip.
  Many „bad" chips are good
  on the second attempt.
- ⇒ The test setup is not
  super stable.

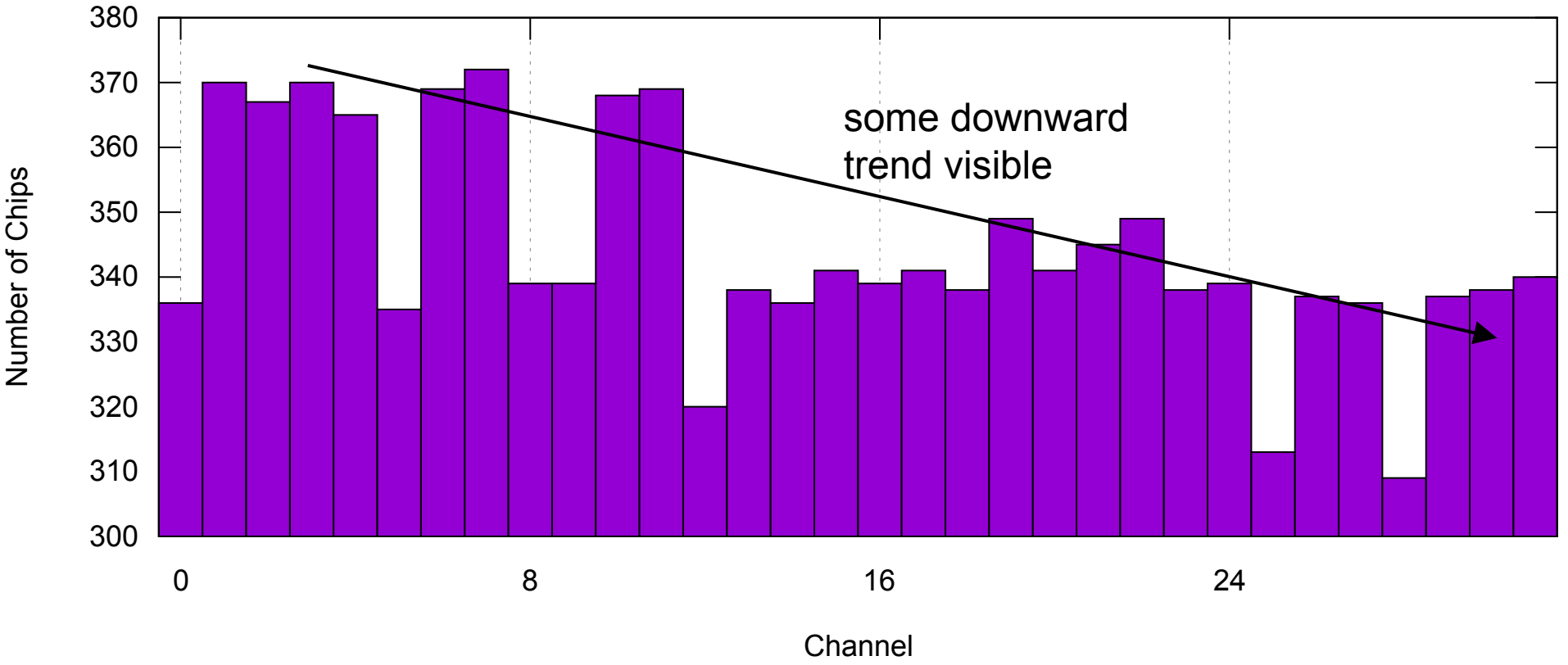
- Test results per chip
  available.



Number of Good Channels / Chip

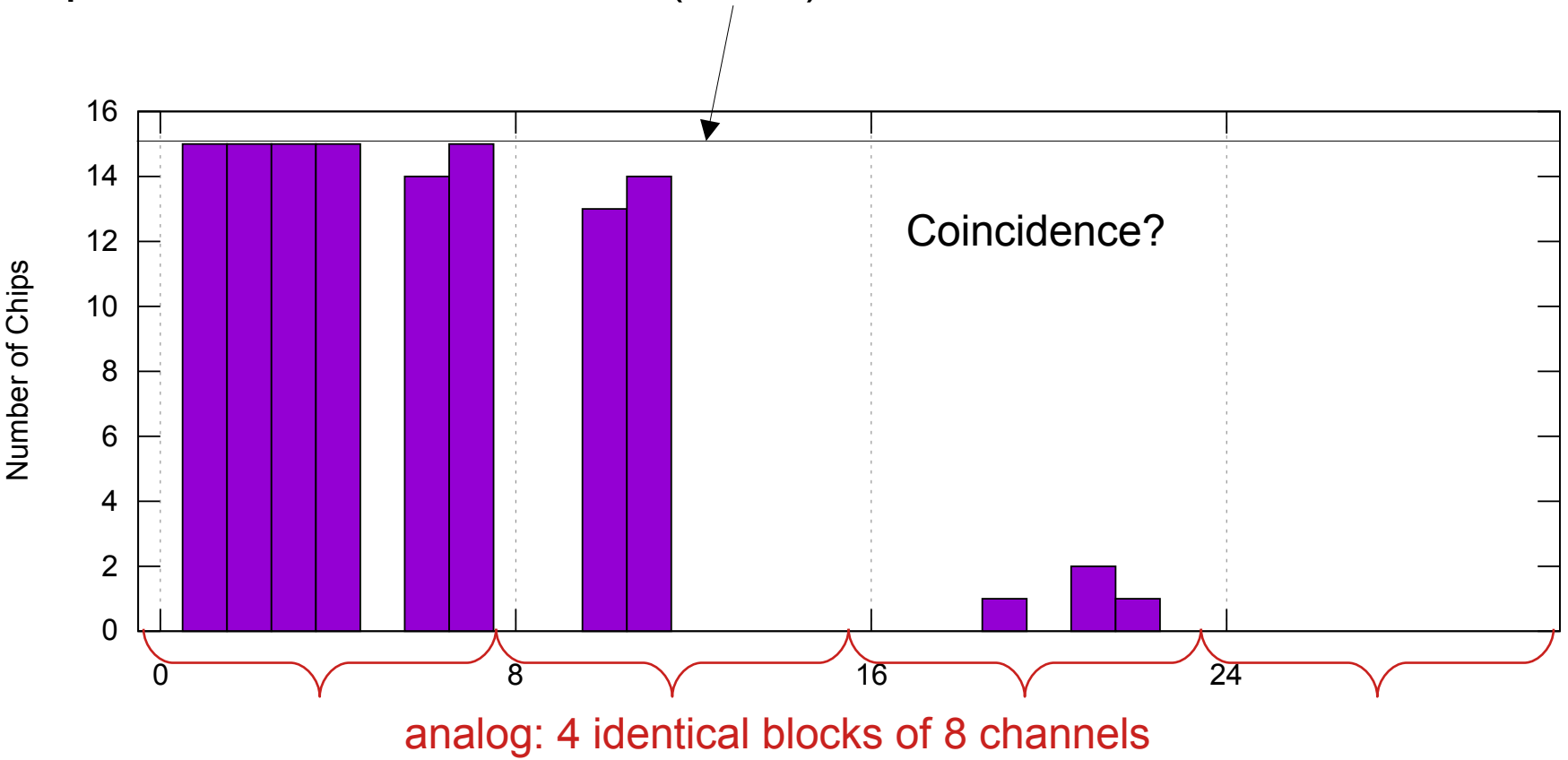


Statistics per Channel



Statistics per Channel

For Chips with 8 Good Channels (*n*=15)



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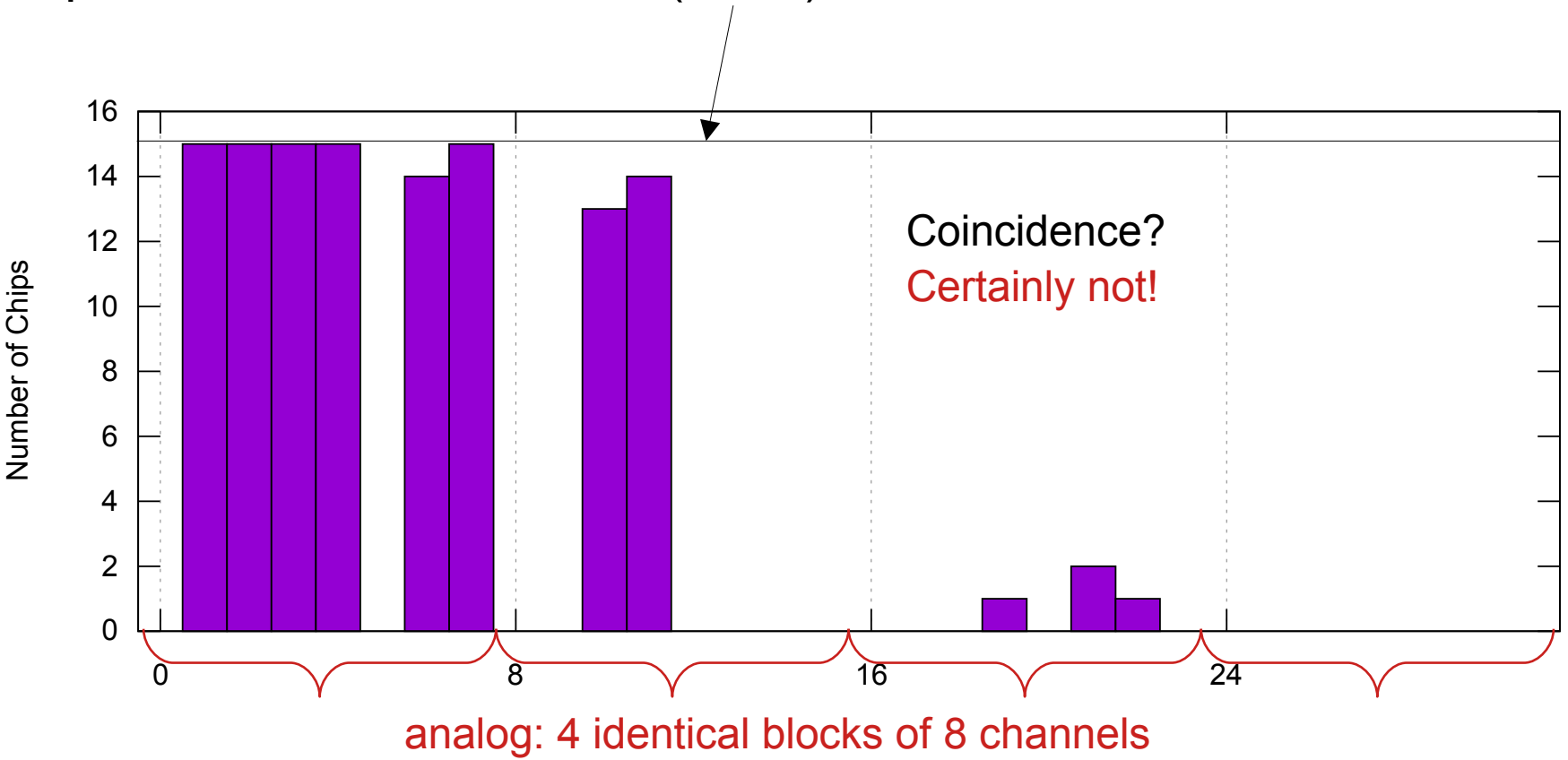

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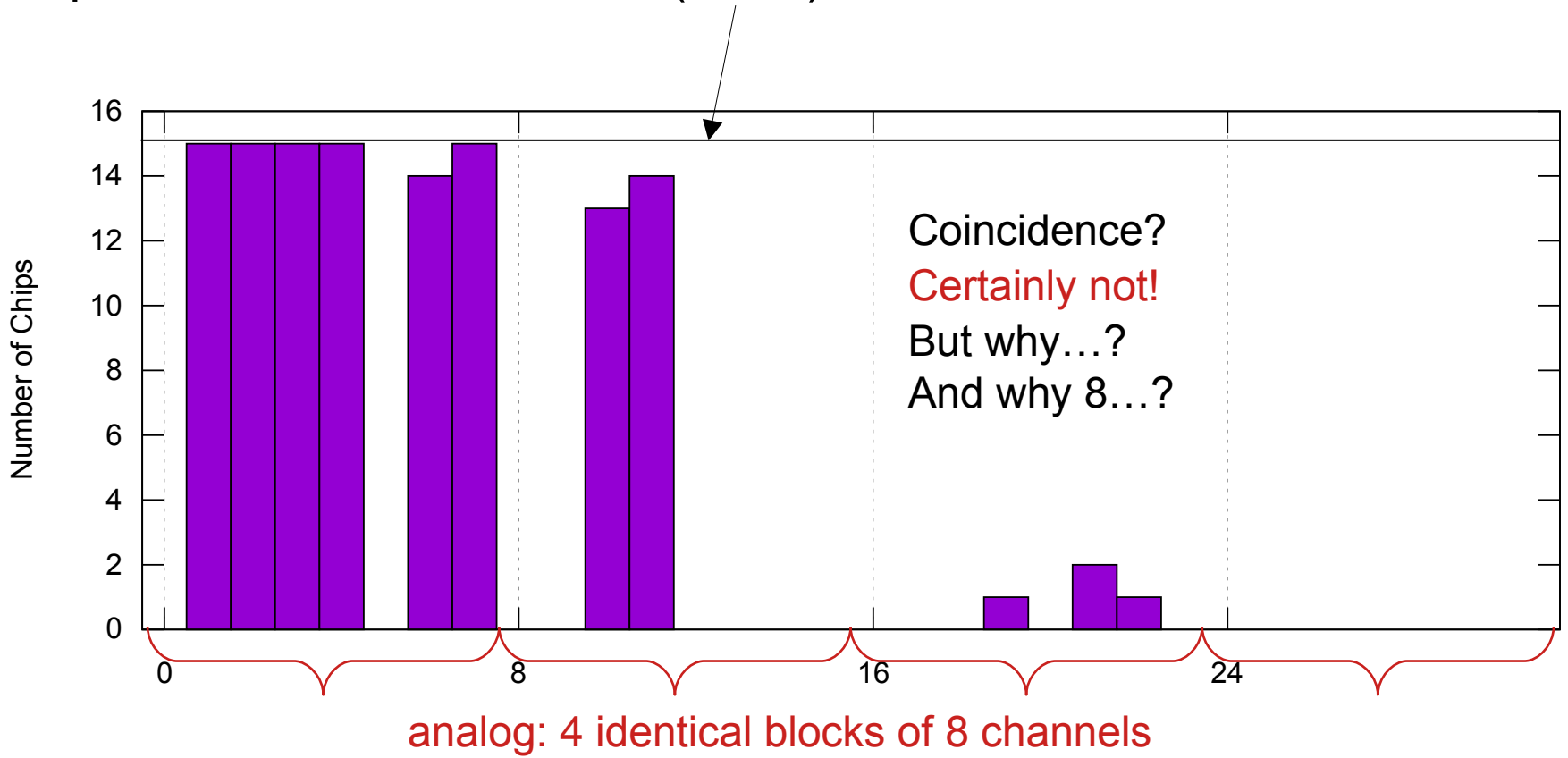

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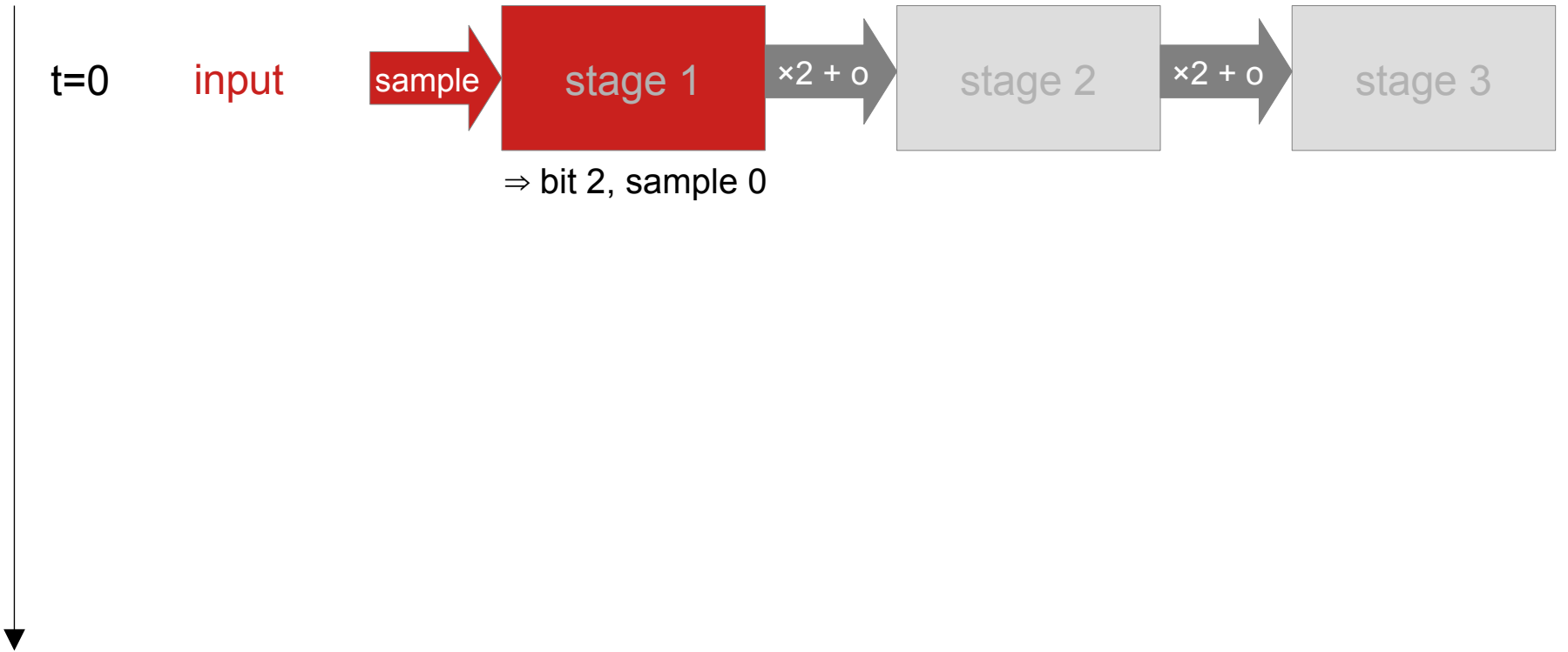
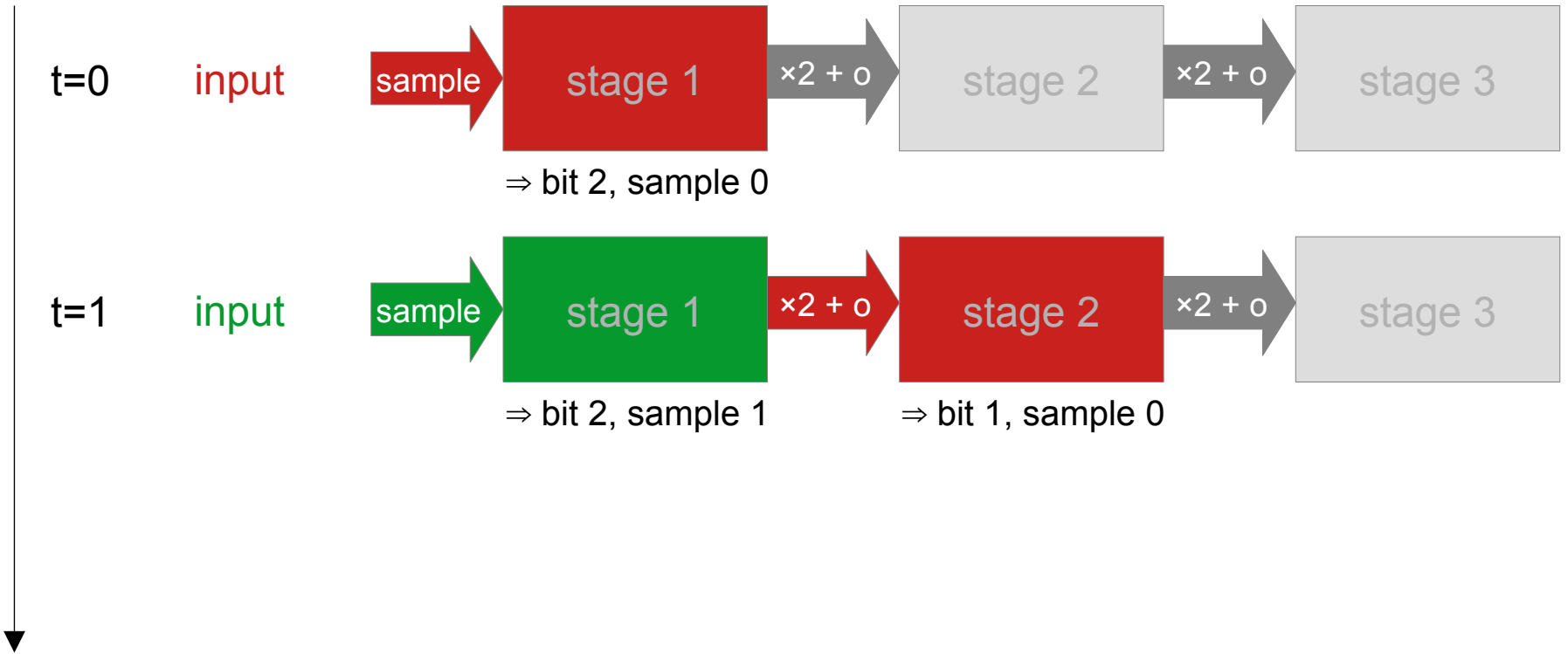
SPADIC 3 Design

Pipeline Principle

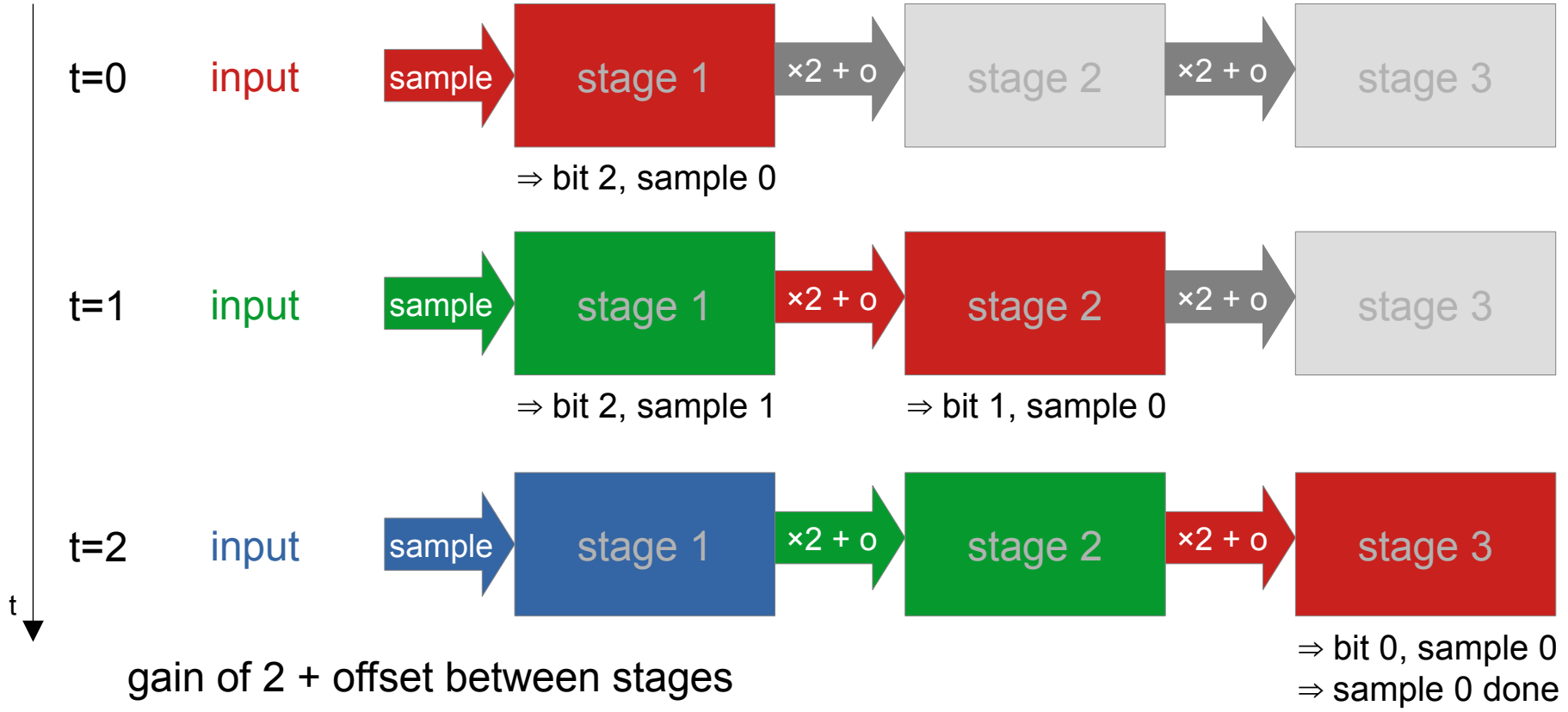


Pipeline Principle



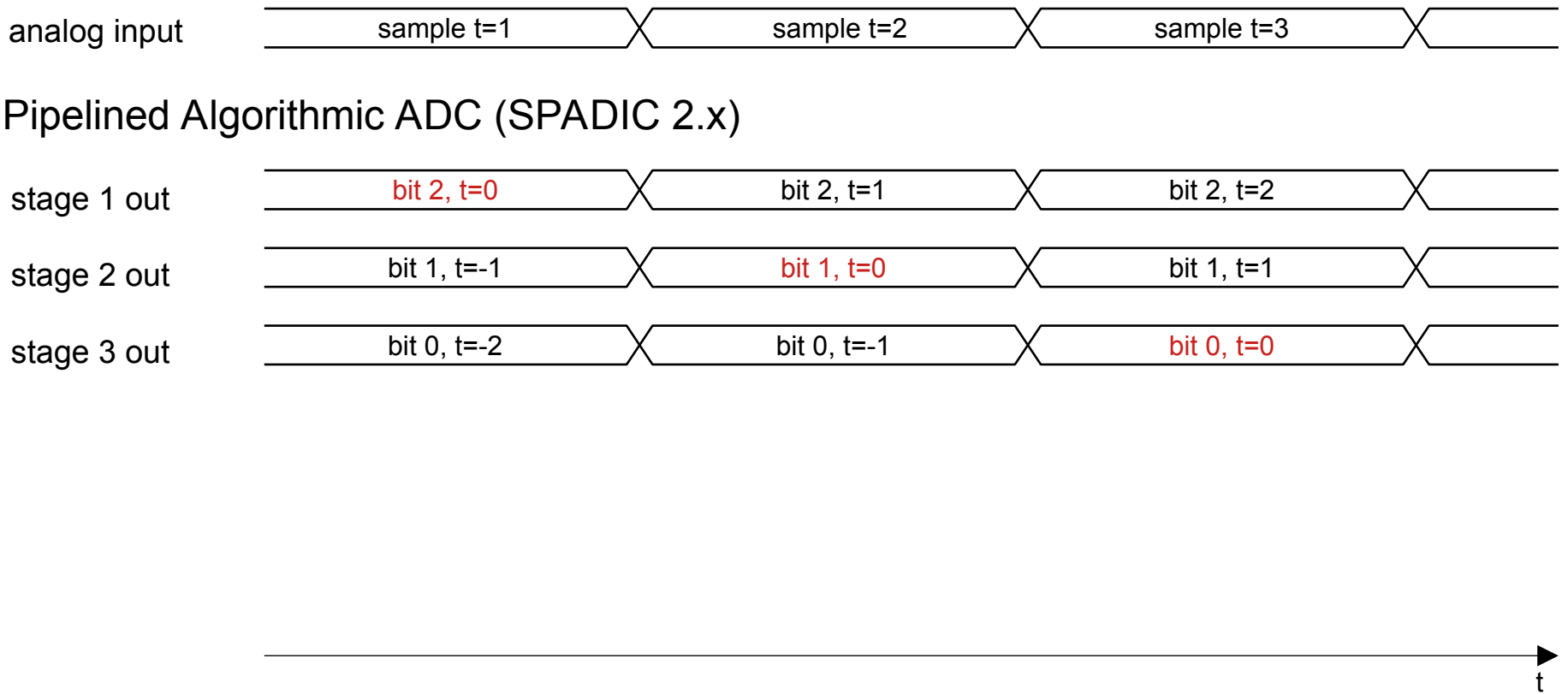
gain of 2 + offset between stages

Pipeline Principle



ADC Concepts

Pipelined vs. Single-Stage



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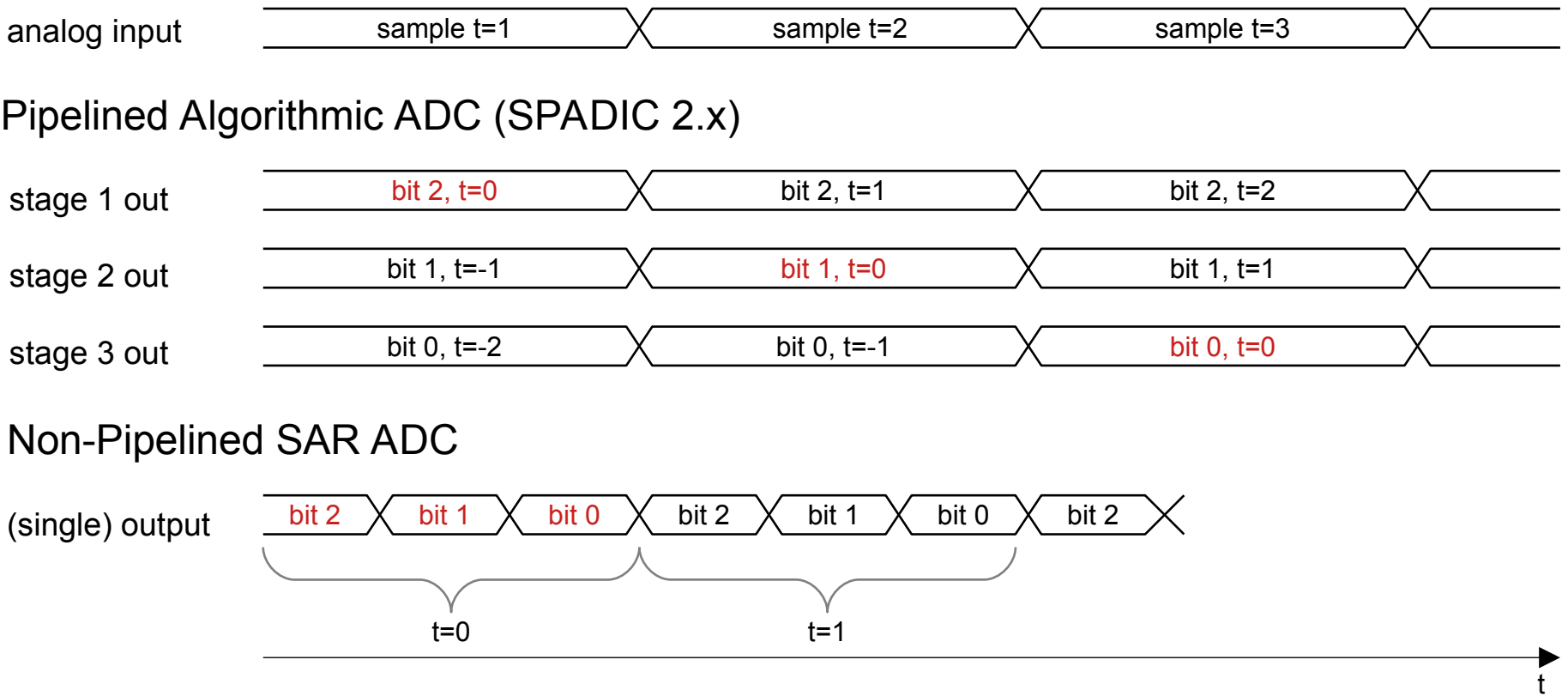

ADC Concepts
Pipelined vs. Single-Stage II

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- The pipelined version has a very relaxed timing (at least 9 times slower in SPADIC).
- But the input signal has to be transfered between the stages, mulitplied, shifted, …
  ⇒ sources of errors

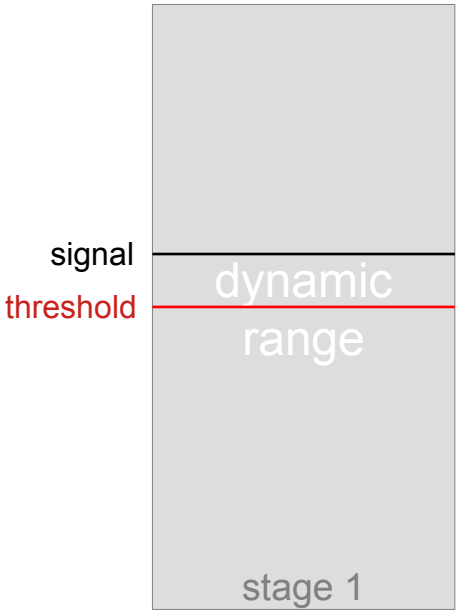
- For SPADIC, the sampling rate is 16 MHz ⇒ 62.5 ns per sample.

  - A pipelined ADC has the entire 62.5 ns for each bit: Comparison + transfer to the next stage.

  - A non-pipelined ADC has 6.25 ns per bit: Comparison + threshold adjustment.
    We think this is tight, but do-able.
    (Dynamic range ~ 750 mV ⇒ LSB = 1.47 mV)

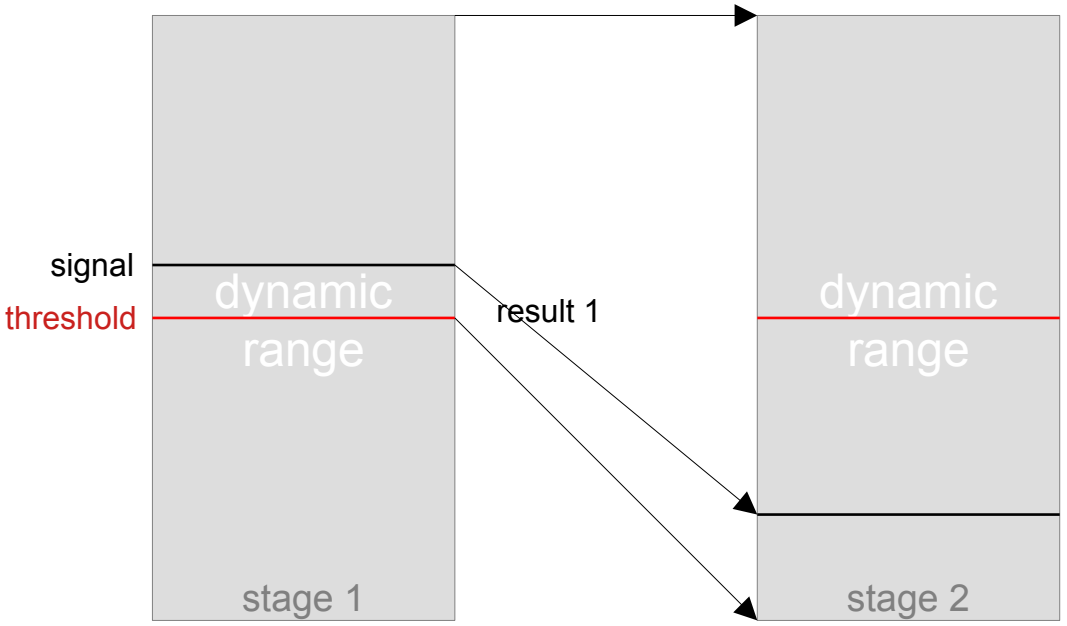
ADC Concepts

Pipelined Non-Redundant Algorithmic ADC



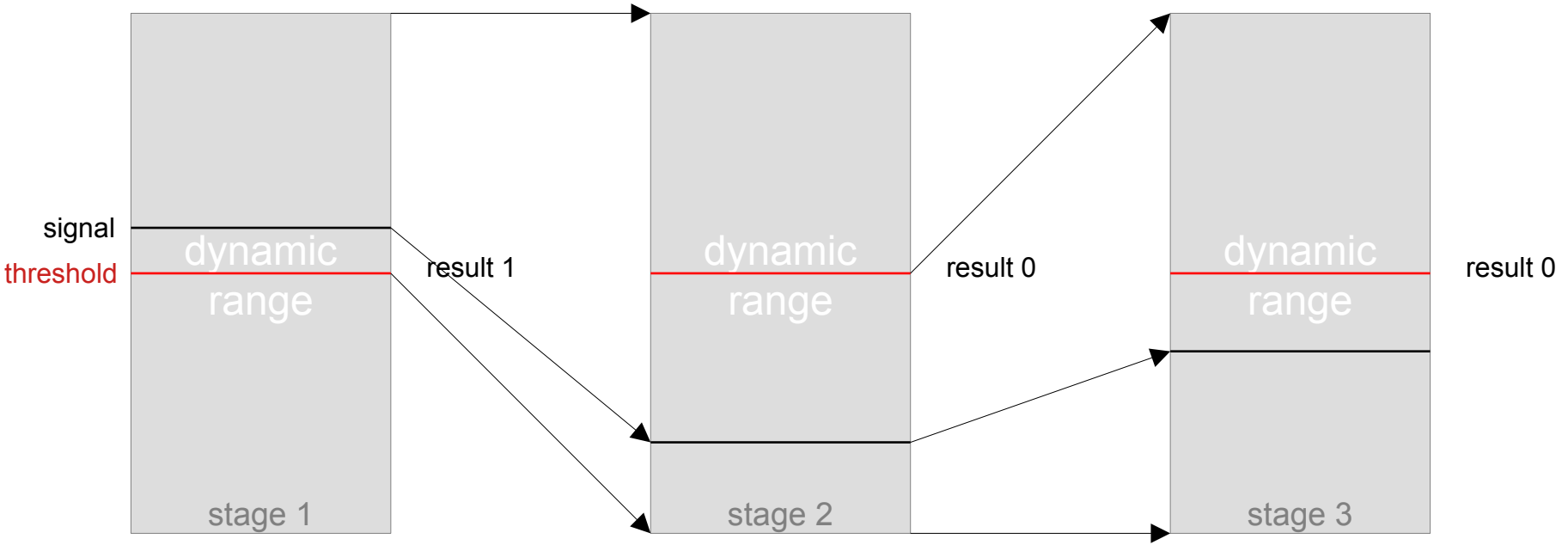
ADC Concepts

Pipelined Non-Redundant Algorithmic ADC



ADC Concepts

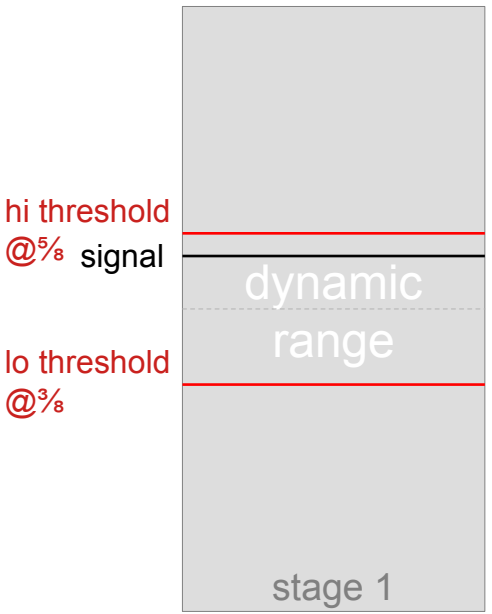
Pipelined Non-Redundant Algorithmic ADC



After three stages: The result is $100_b + 00_b + 0_b = 100_b$.
Very sensitive to comparator noise: Any error will never be recovered.

ADC Concepts

Pipelined Redundant Algorithmic ADC



ADC Concepts

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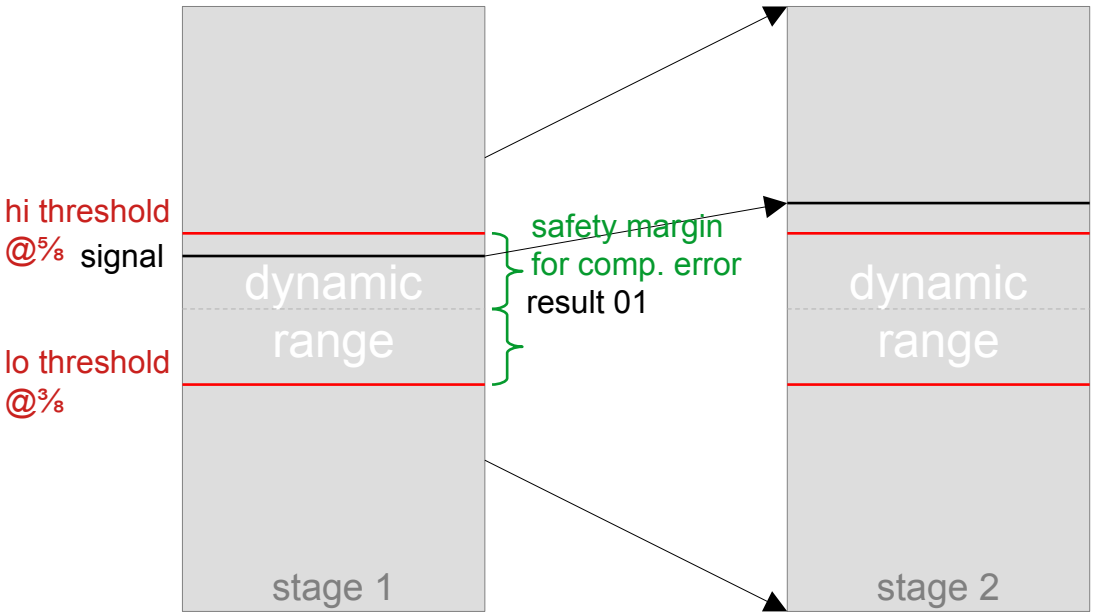

ADC Concepts

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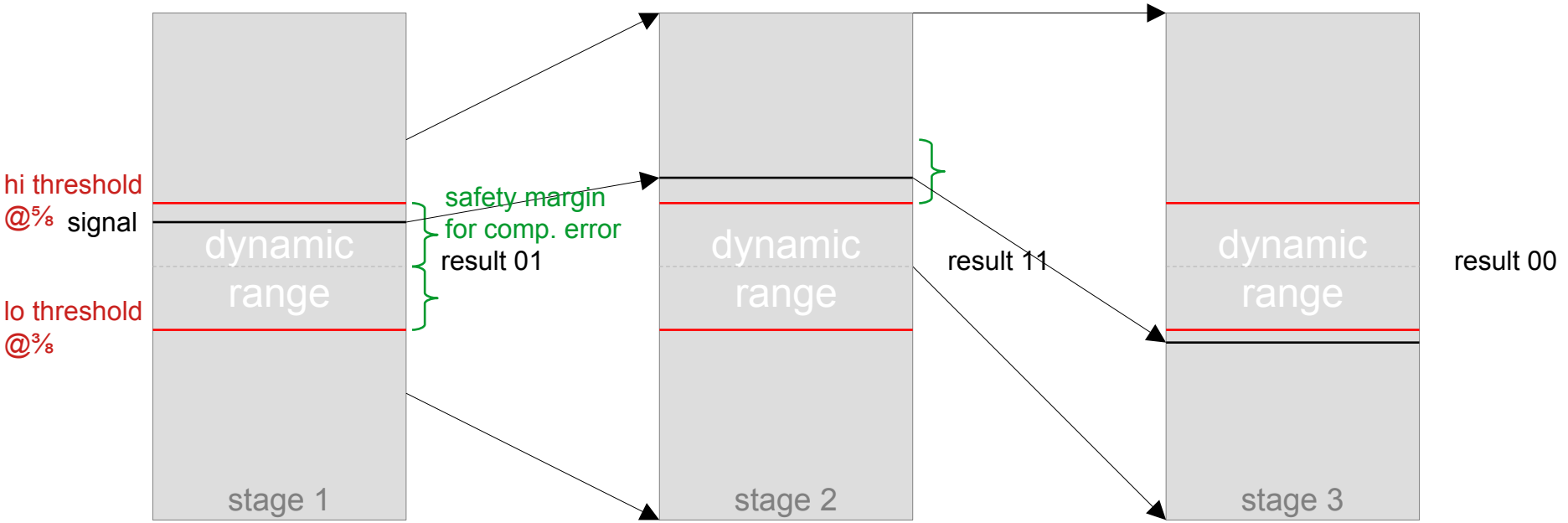
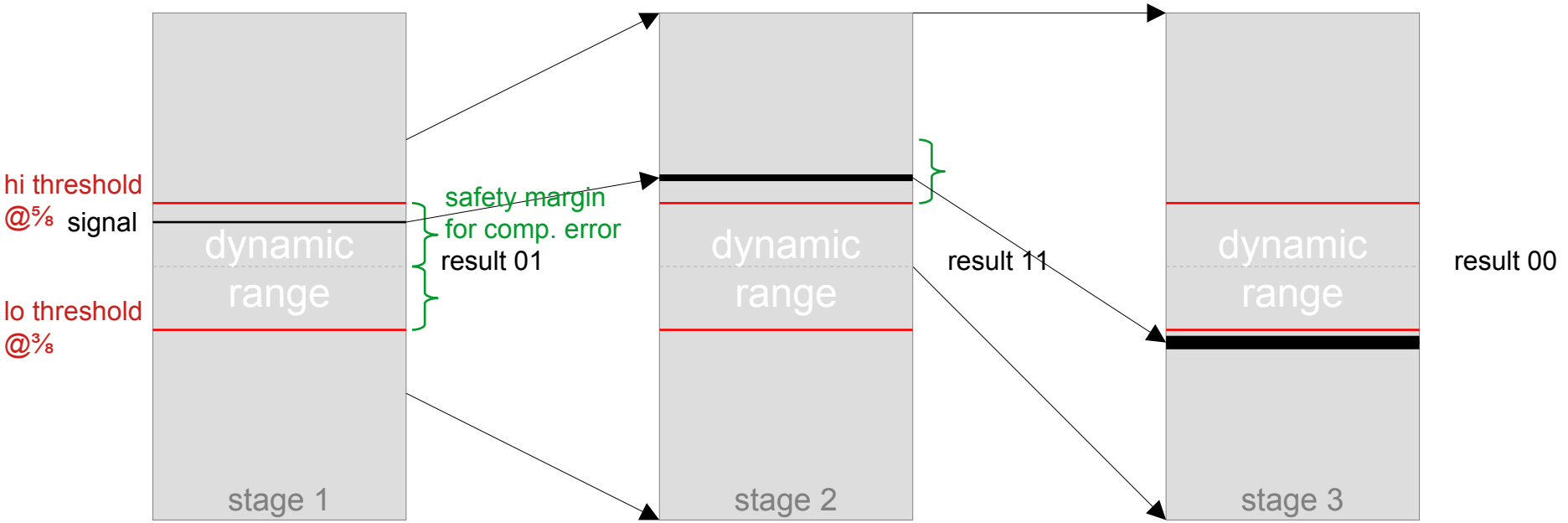


After three stages: The result is 000b + 100_b + 10b + 10_b + 0b + 0_b = 1000_b (the two comparator result have equal weights)

Note: One more bit than comparisons(!)

ADC Concepts

Pipelined Redundant Algorithmic ADC

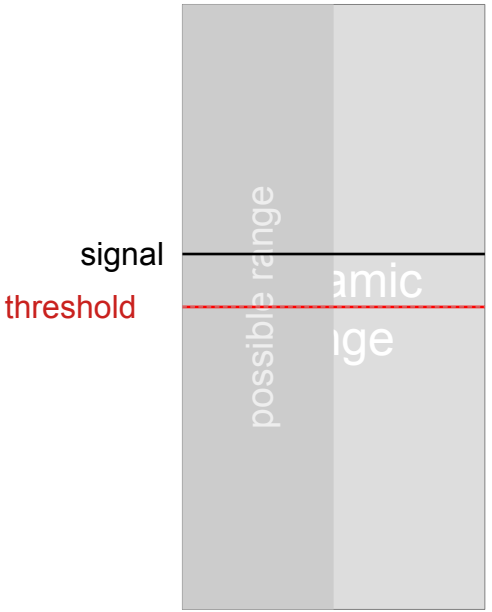


After three stages: The result is 000b + 100_b + 10b + 10_b + 0b + 0_b = 1000_b (the two comparator result have equal weights)
Note: One more bit than comparisons(!)

Used in all SPADICs so far. Implemented by multiplying + shifting the input signal between stages.

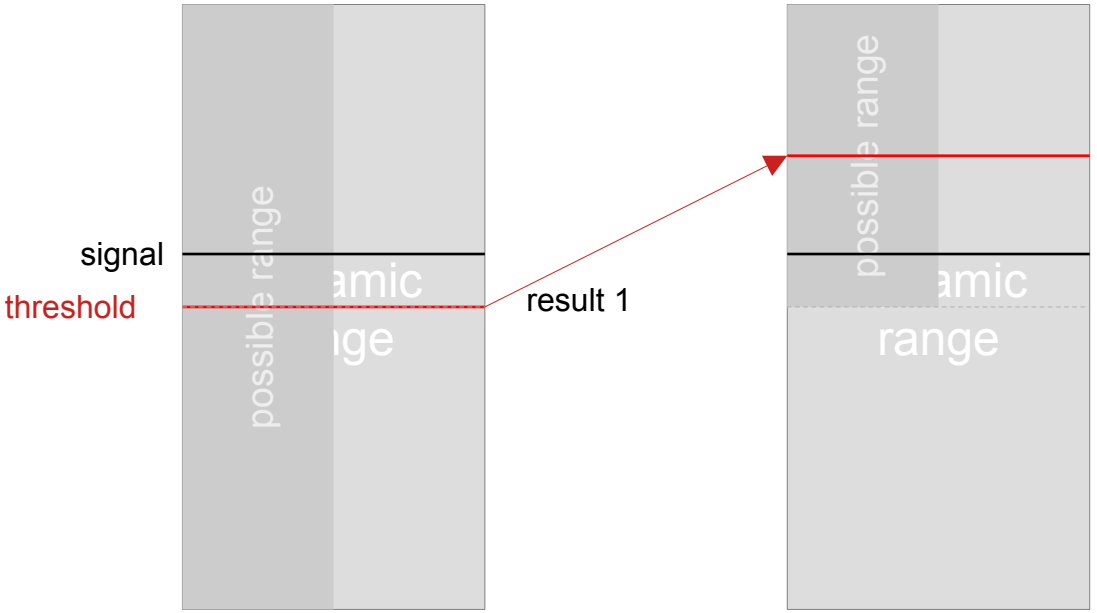
ADC Concepts

Non-Redundant SAR ADC



ADC Concepts

Non-Redundant SAR ADC



ADC Concepts

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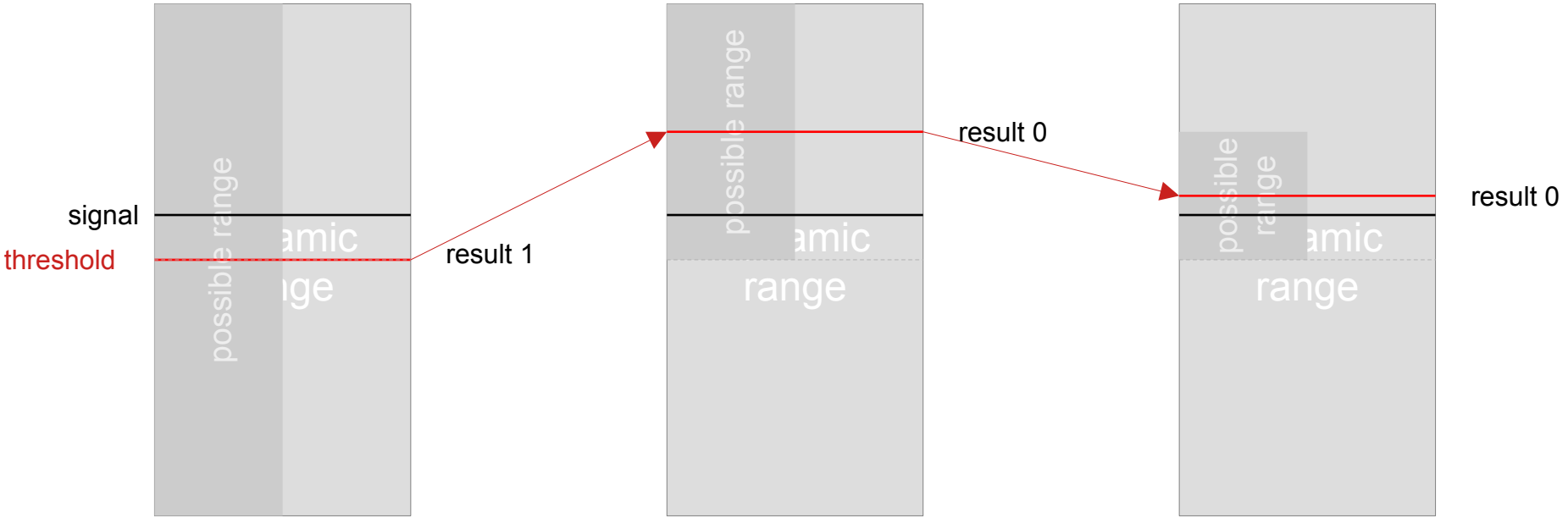
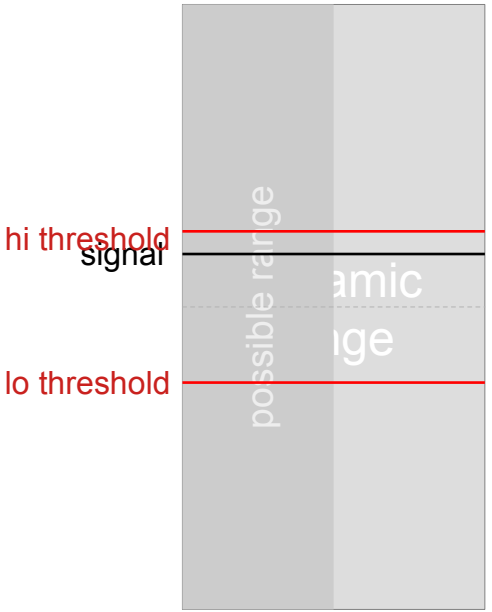


ADC Concepts

Redundant SAR ADC



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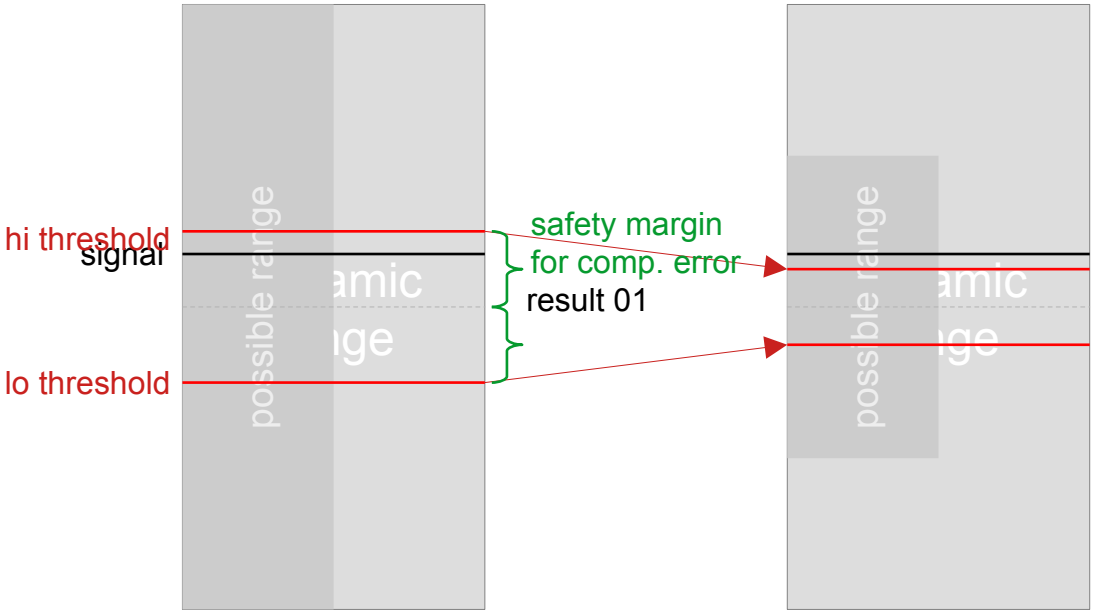

ADC Concepts

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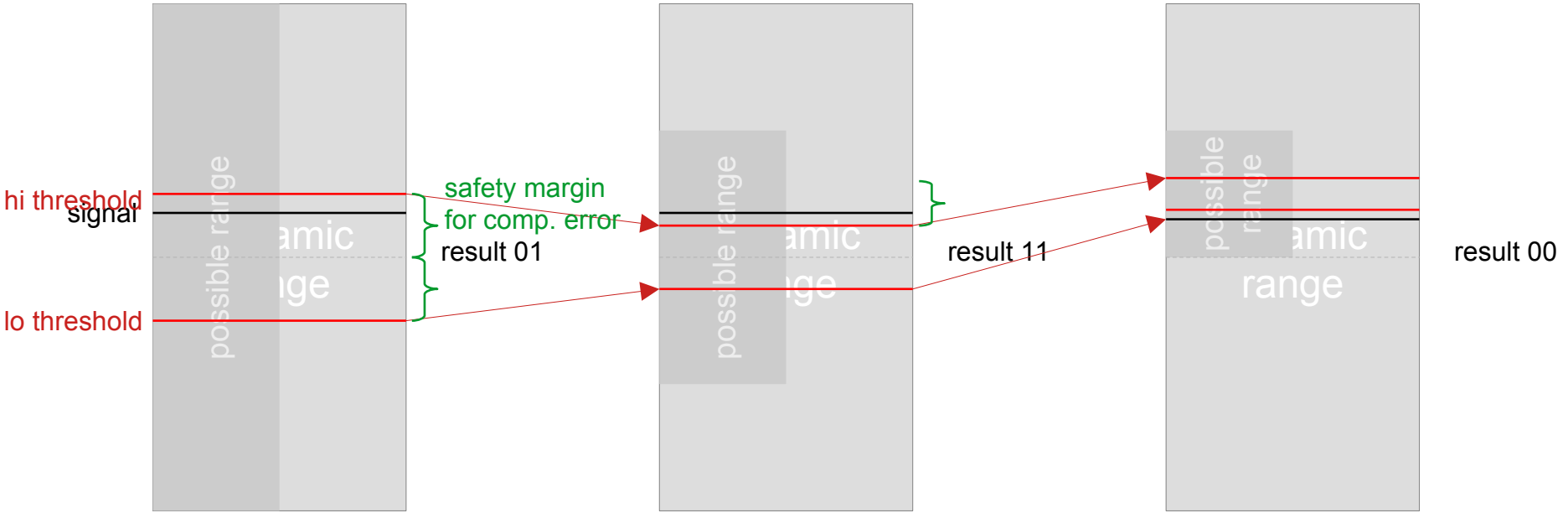

If we cannot adjust the input signal, we have to adjust the comparator threshold for the same effect.
The possible range is halved in each step. The thresholds are at ⅜ and ⅝ of this range.

Pipelined Redundant vs. Single-Stage Redundant

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Redundant Pipelined (SPADIC 2.x)

+ The comparator is never an issue;
  The safety margin is the same in each stage:
  ½ – ⅜ = ⅛ of the dynamic range
  ≙ ~100 mV
  (the SPADIC2 implementation compares currents, but „a lot“ remains „a lot“).

- The transfer of the signal between stages has to be precise.
  Errors propagate and multiply.

Redundant SAR (SPADIC 3.0)

- Comparator noise becomes a problem in later stages.
  Safety margin $1/(8\times2^{n-1})$ after n comparisons
  ⇒ 1/1024 ≙ 0.7 mV for the last comparison
  ⇒ precise DAC + comparator required

+ The signal is stable all the time.

Pipelined Redundant vs. Single-Stage Redundant

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  ⇒ 1/1024 ≙ 0.7 mV for the last comparison
  ⇒ precise DAC + comparator required

+ The signal is stable all the time.

⇒ lots of effects: mismatch, biasing, noise, …

Redundant SAR ADC
In the Case of SPADIC

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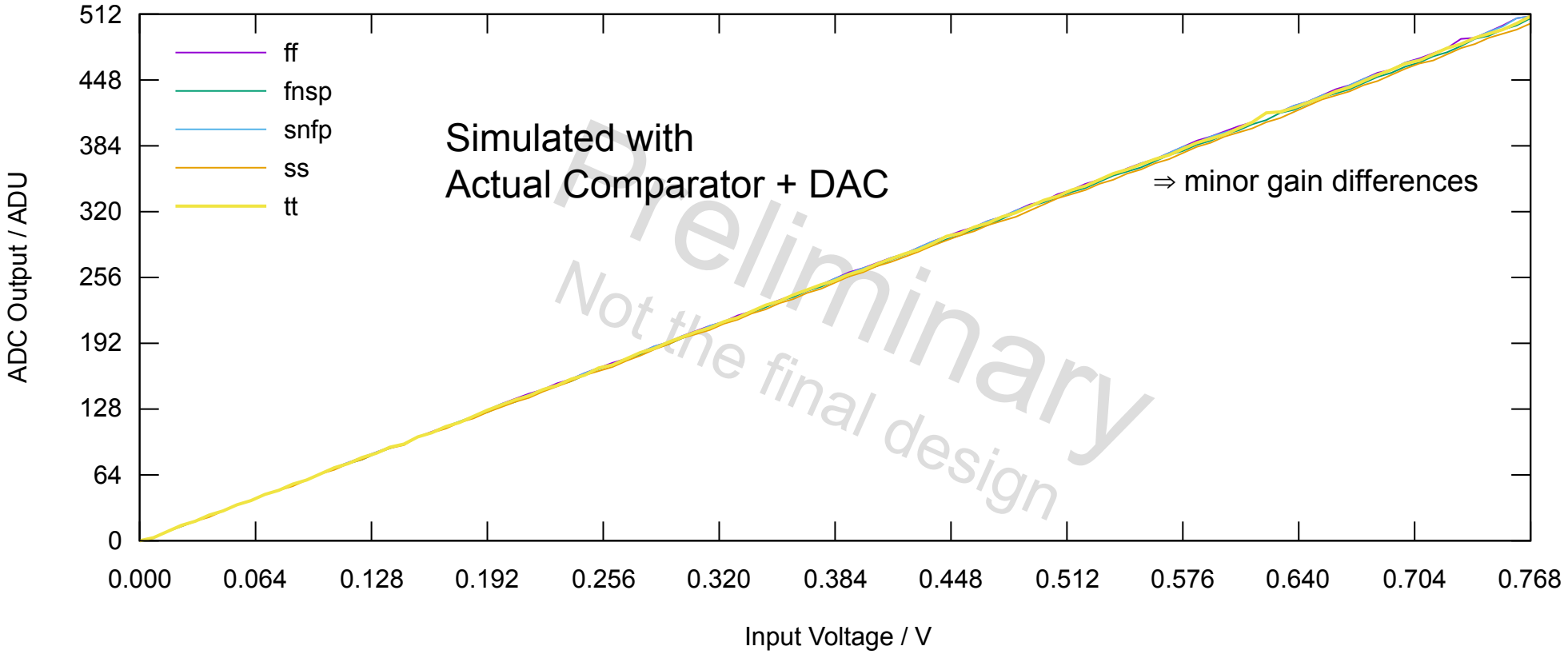
- Analysis of the algorithm:
  - The thresholds have to be provided by DACs (pipelined: static).
  - At the beginning, the DAC has to make larger steps.
    ⇒ Longer settling time. But also larger safety margins!

- We want a 9 bit result ⇒ 8 comparisons. Fits perfectly with the ×10 clock available:
  - 1 Clock Sample & Hold
  - 8 Clocks Comparisons
  - 1 Clock Reset

- This is a major change ⇒ working title **„SPADIC 3.0“**

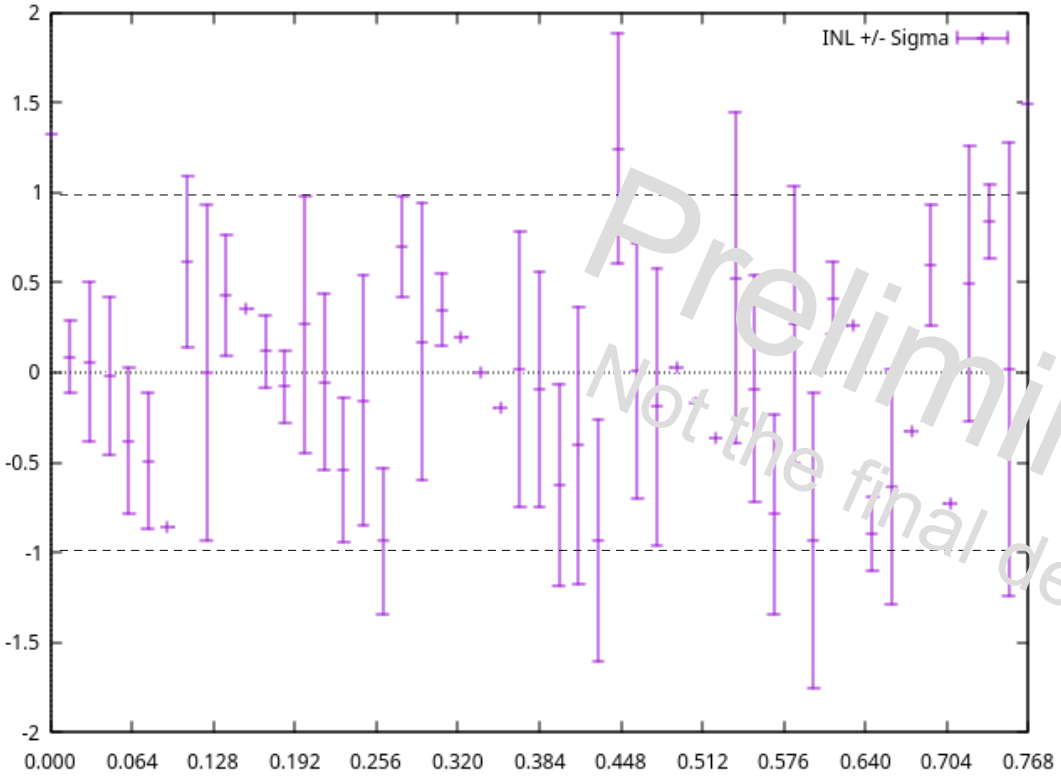
First Simulation Results

Linearity & Stability over Process Corners



First Simulation Results

Integrated Non-Linearity & Noise



50 Transient Simulations with Noise.

⇒ INL + Noise in the order of 1 LSB.

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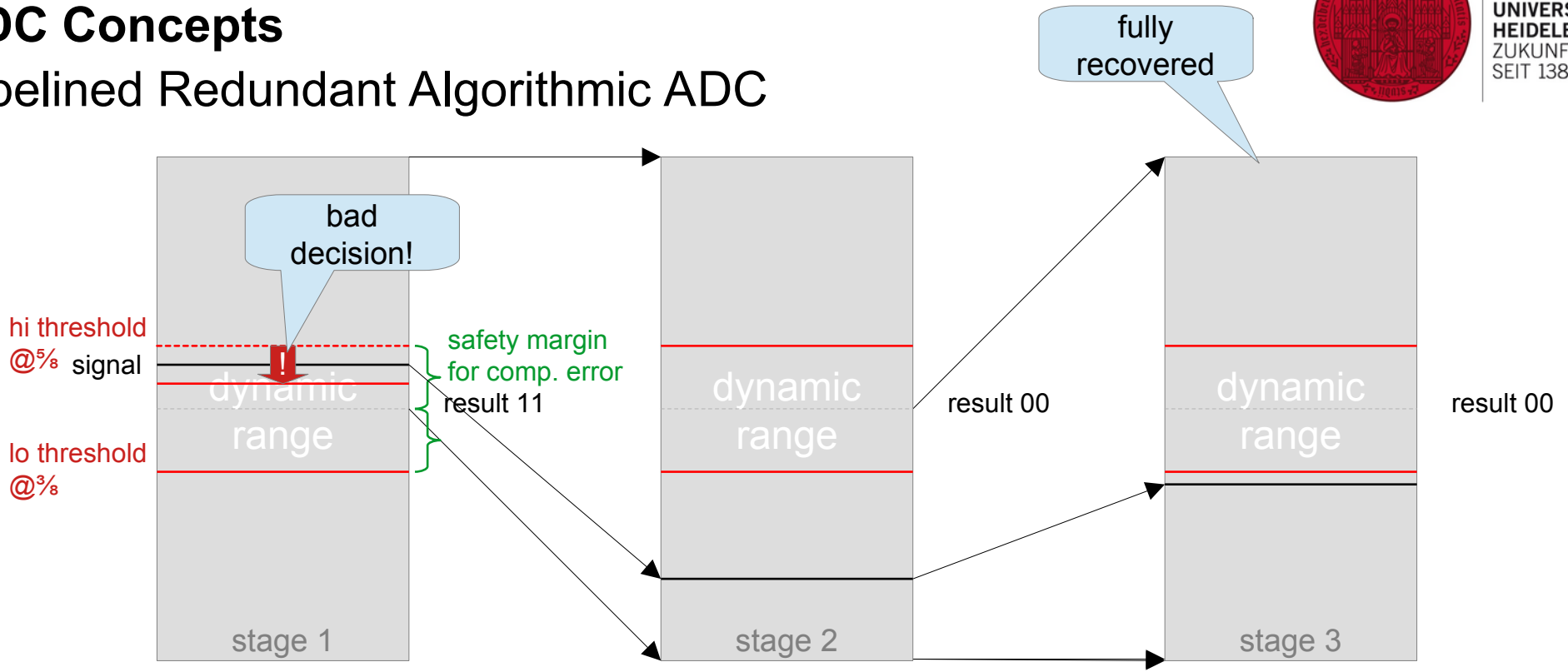
Thank you!

ADC Concepts

Pipelined Redundant Algorithmic ADC



After three stages: The result is $100_b + 100_b + 00_b + 00_b + 0_b + 0_b = 1000_b$
⇒ same conversion result, same state in stage 3 ✔.