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SPADIC

Topics

- Reminder of observations and issues in S2.3A
- Intermezzo: S2.2 Analogue Channel Layout
- SAR Design for S3.0

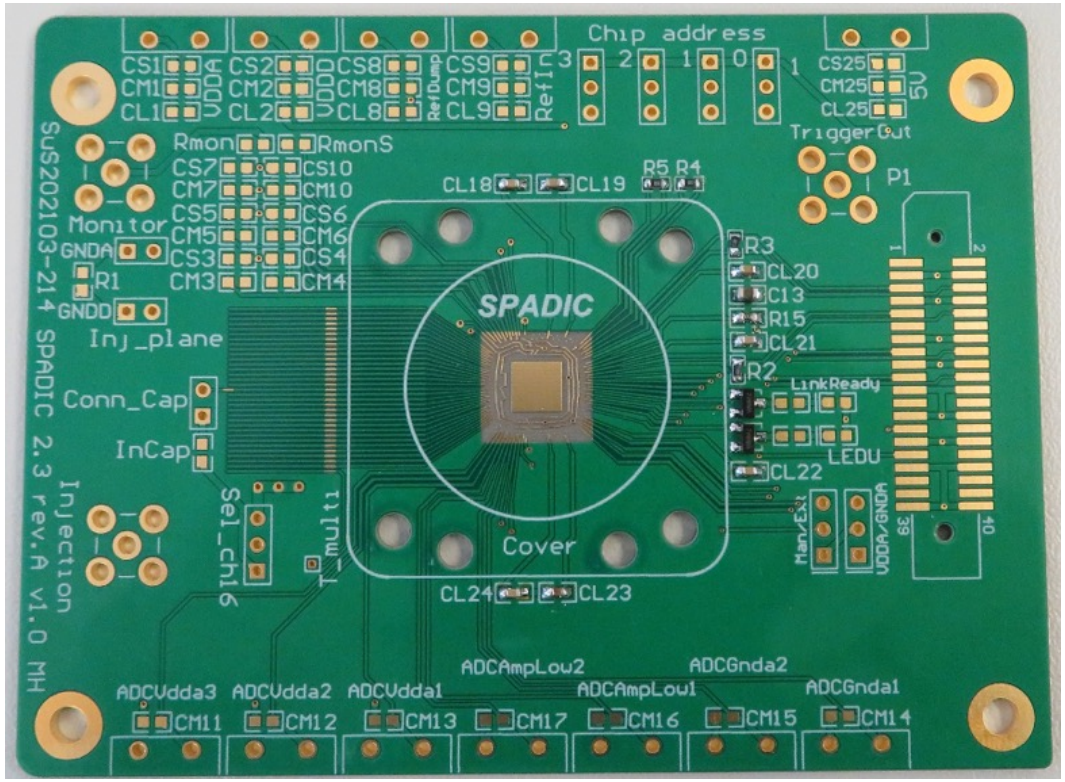
Reminder: S2.3A Design

- Goal of S2.3A was to improve S2.2 ADC linearity / yield
- S2.3A has only MINOR changes wrt. S2.2 in analogue part
  - 'Improved' matching in ADC (change in one place in schematic & Layout) with hope for better yield
  - Note that CSA is **unchanged**
  - Inputs:
    - Added fixed load caps (for noise measurement)
    - Added different sizes of protection diodes
  - Minor:
    - Range of Bias DACs doubled
    - Added injection per channel
- Several changes in digital part all seem to work

- S2.3B had major changes in ADC

Test Setup

- 2.3 is unpackaged -> New setup required for wire bonding
- New PCB designed
- Connects to Frankfurt Readout (thanks for the connectors!)



- Control software from S2.2 with minor modifications

S2.3A - Puzzle

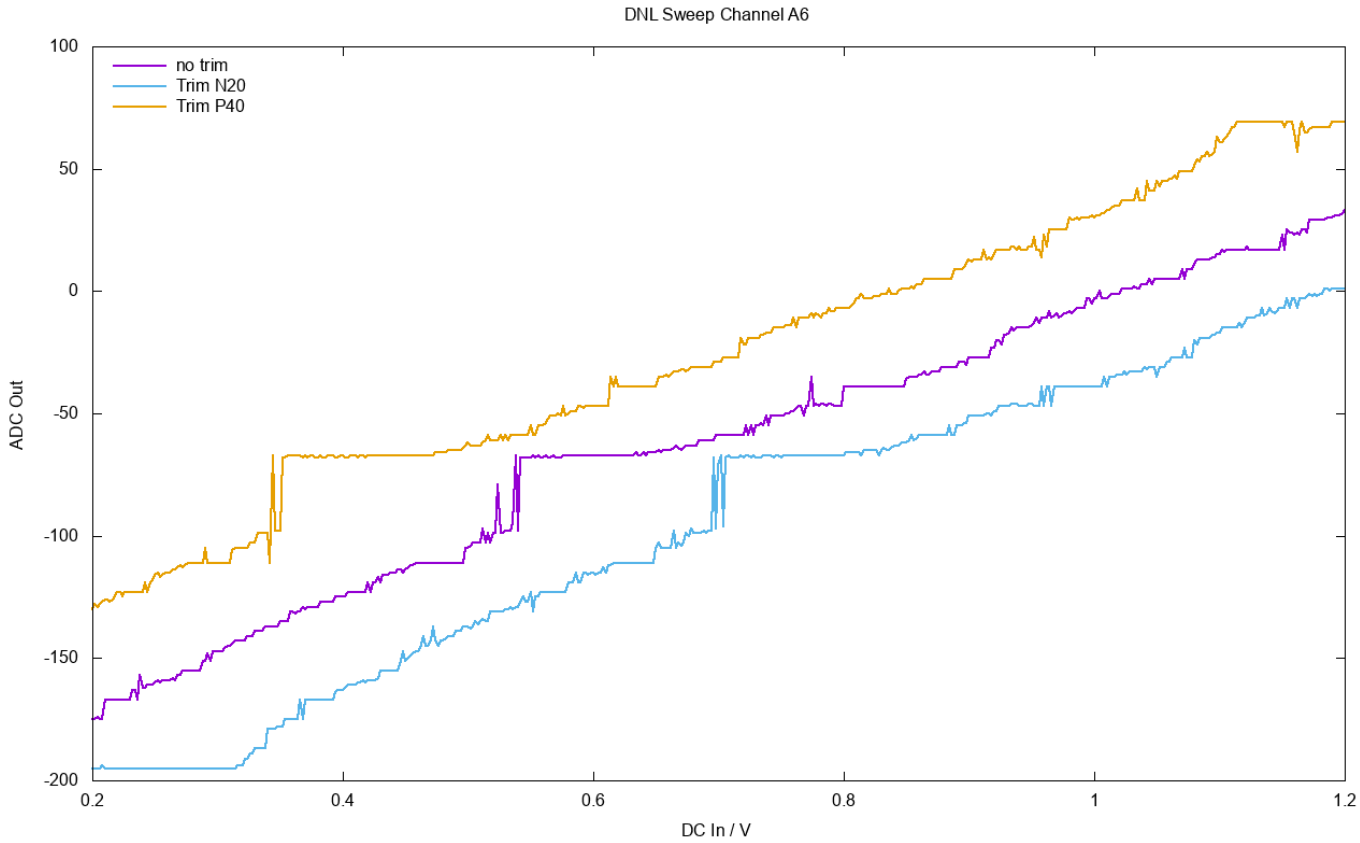
- Initial tests of S2.3A by a student looked very promising
  - (he sent me clearly nice looking plots)
- Later test by the same student were bad.
- Michael and myself did not manage to reproduce the nice results
- Fully unclear what happened. No more ideas.
  - Issue in setup or software? Not conformed by S2.2 re - measurement, see later.
- Assume for now that ‘good’ measurements were ‘fake’.

S2.3 Main Issues

- DNL of ADC **very** bad (worse than S2.2!)
- **Gain drop** in CSA output for increasing amplitudes

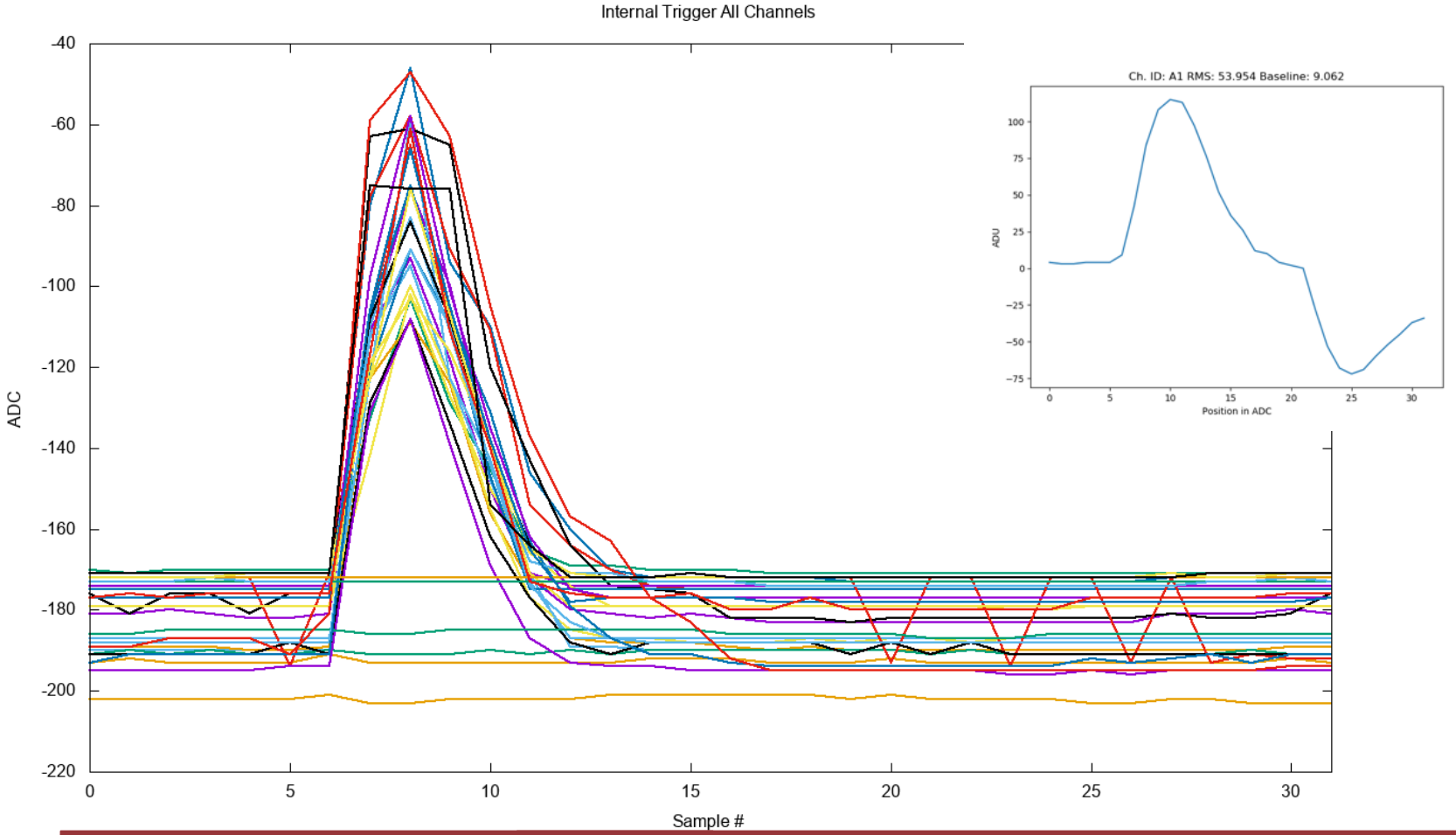
1. ADC Problem (DC input)

- ADU vs. DC input voltage. Very crappy curves
  - Shifting curve with offset trim works…



1. ADC signals (CSA pulses)

- Digitized CSA signals are also crappy
- Note that signals some channel seem to be dead.
  - These are always 9, 11, 17, 19, 25, 27 (with large input caps)



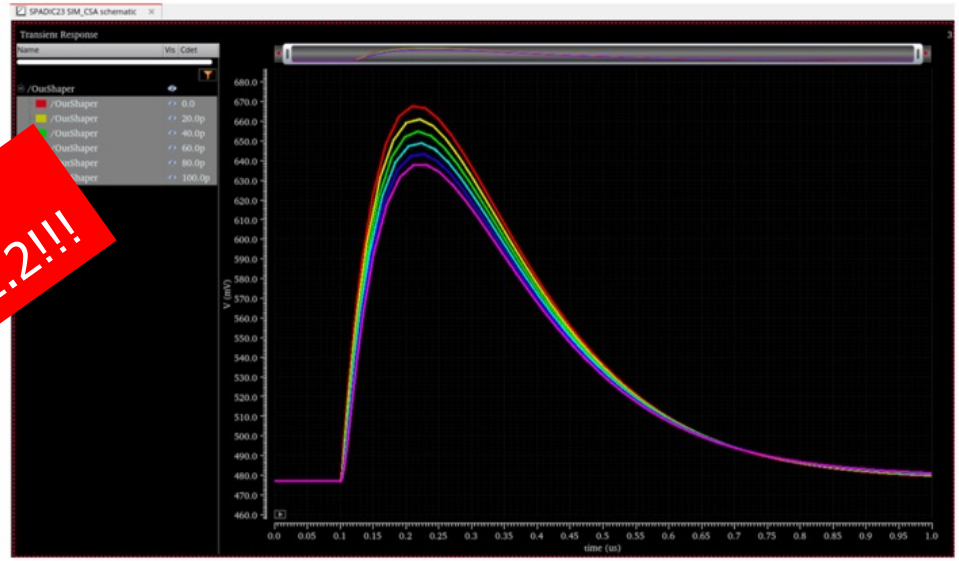
2. CSA Gain Drop

- Gain drops significantly when caps >20pF are connected to the CSA.

ADUs for internal injection (different channels):

- Cin=0pF
  - 166/166/170/169/170/170/160/120/168/165/100/168/175/80/165/166/130
- Cin=5pF
  - 150/163/165
- Cin=10pF
  - 172/173/169
- Cin=15pF
  - 182/163/167
- Cin=20pF
  - **90/80/70**
- Cin=30pF
  - **100/70/80**

A0 A8 B0 B8



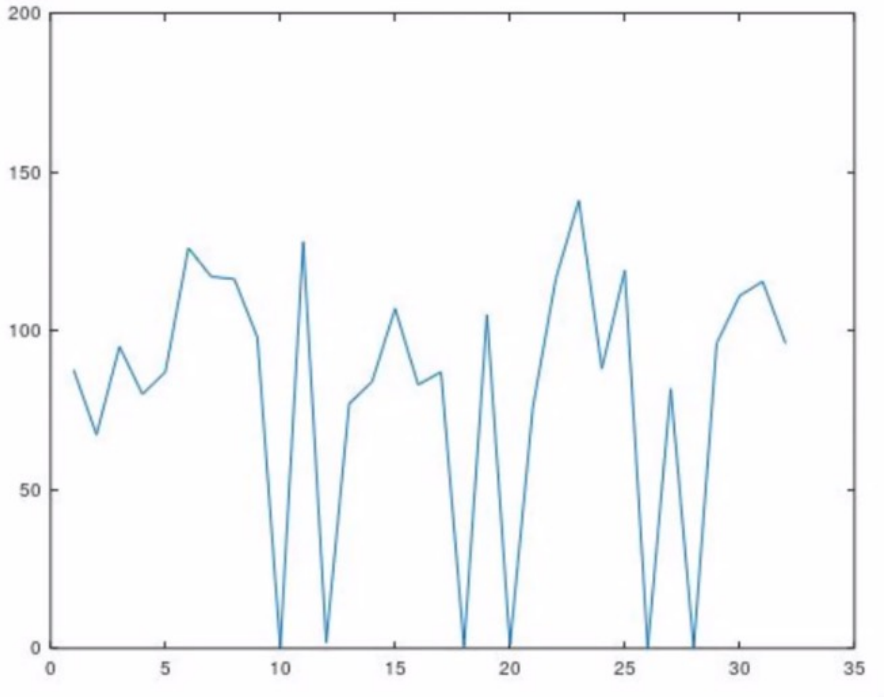
Simulation CSA output for Cin = 0pF…100(!)pF

- This is observed via ADC and via analogue monitoring pin.

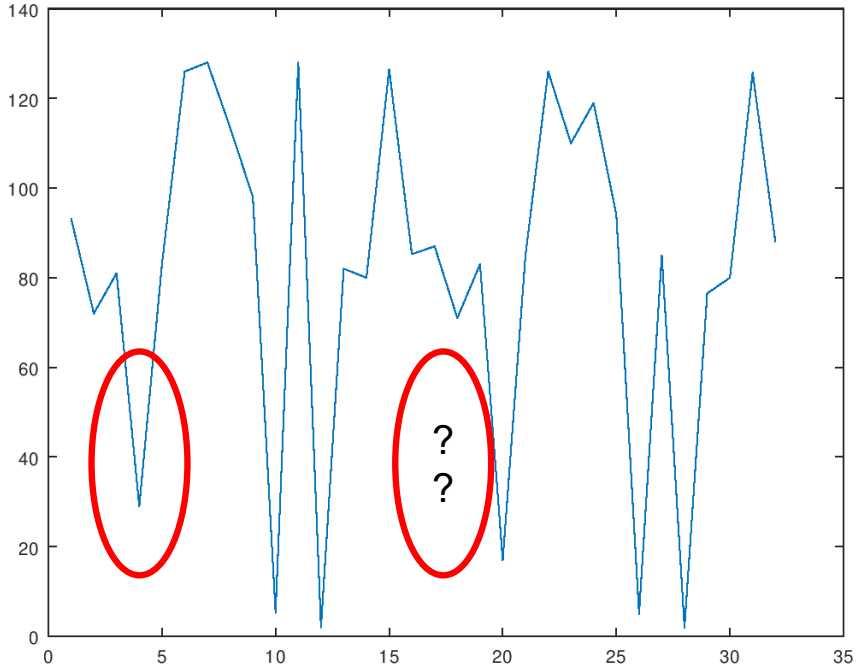
2. CSA Gain Drop

- This effect has been reproduced by Michael:
  - Plots show peak amplitude vs. channel ID, for single shots

Only internal load caps



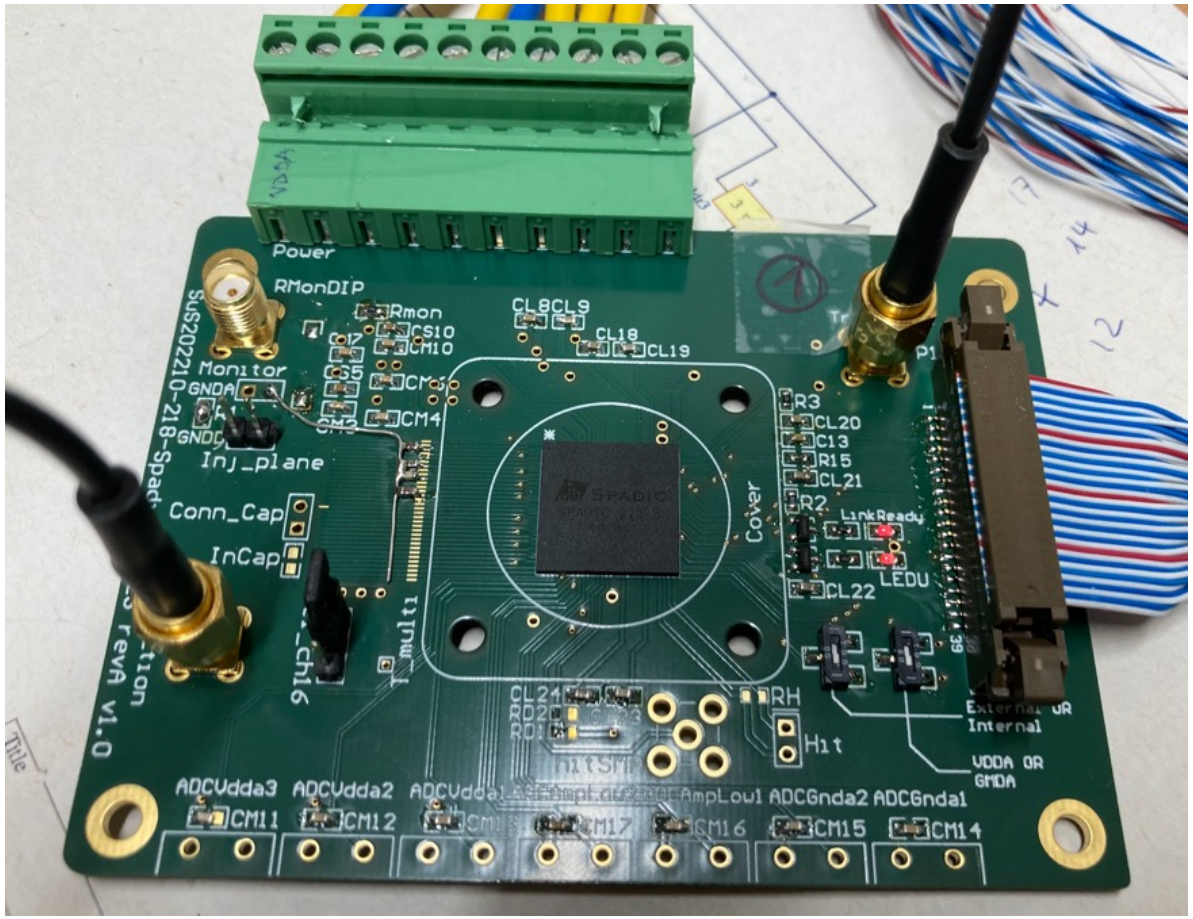
Additional EXTERNAL 33pF on Channel 3



(Channel IDs are offset by 1)

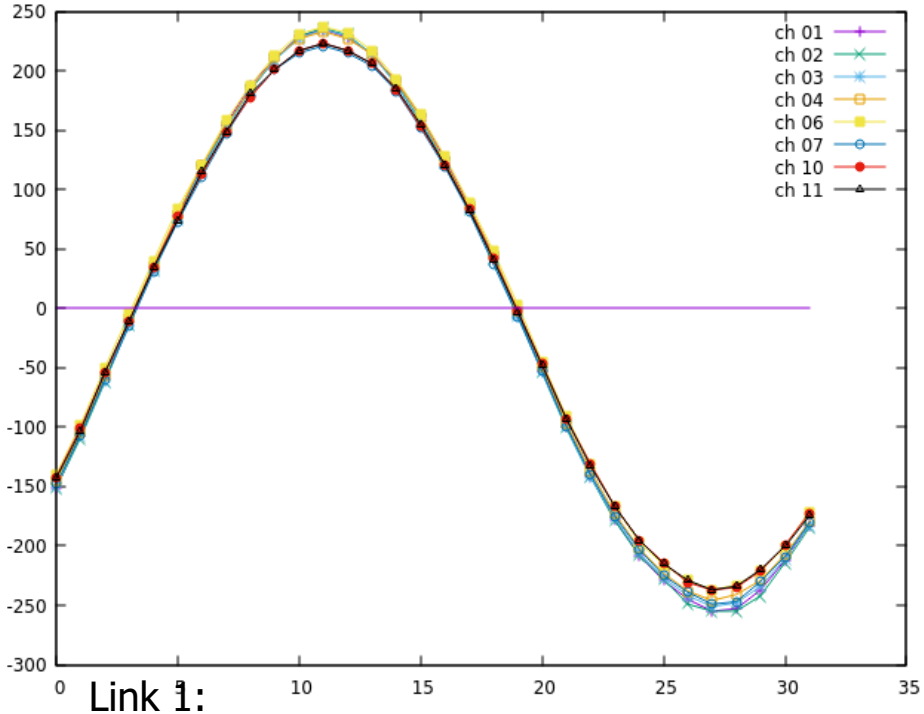
Check with SPADIC 2.2

- Want to bond a SPADIC2.2 to same setup
  - Problem: No naked S2.2 available
- -> Make another board for S2.2 in package

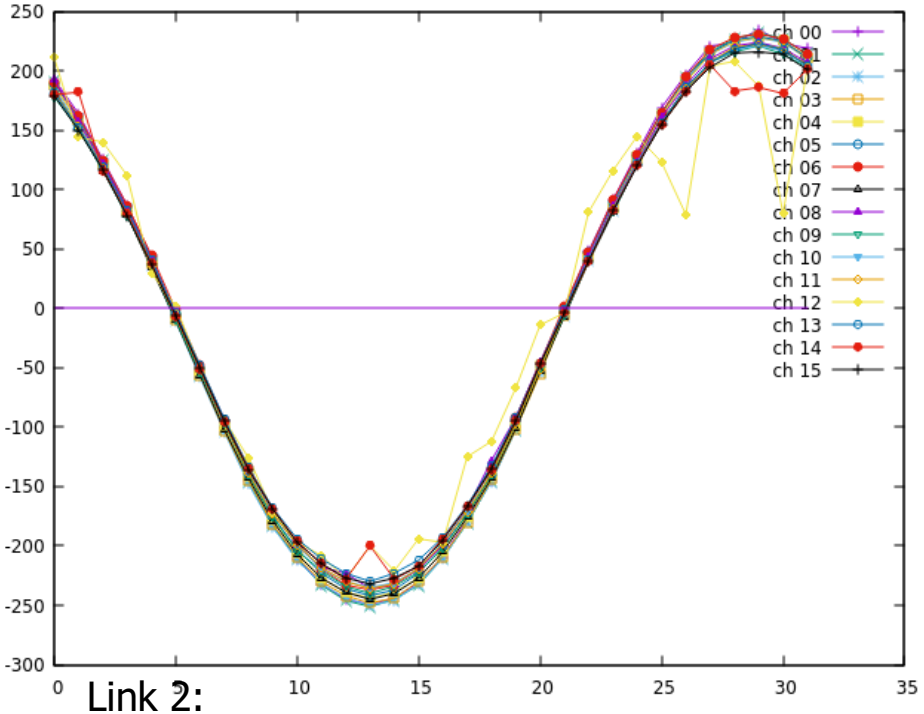


First result S2.2 on Setup for S2.3

- Board has nearly same schematic, just chip in package
- Same software as 2.3 with few register address changes
- Sine waves TO ADC for both links (1st chip tried):



Link 1:
Only very nice channels shown

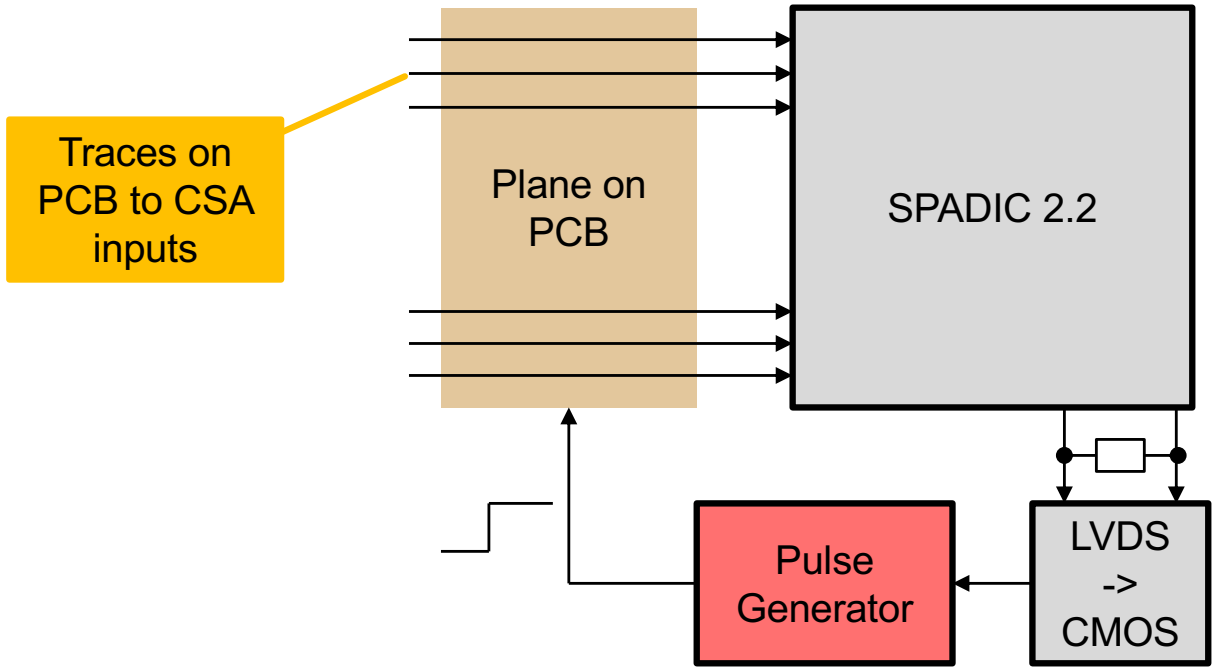


Link 2:
All channels

- 80% good channels or so, as before
- Setup/software ‘probably not’ cause for bad S2.3 behavior

Injection into all CSA cannels

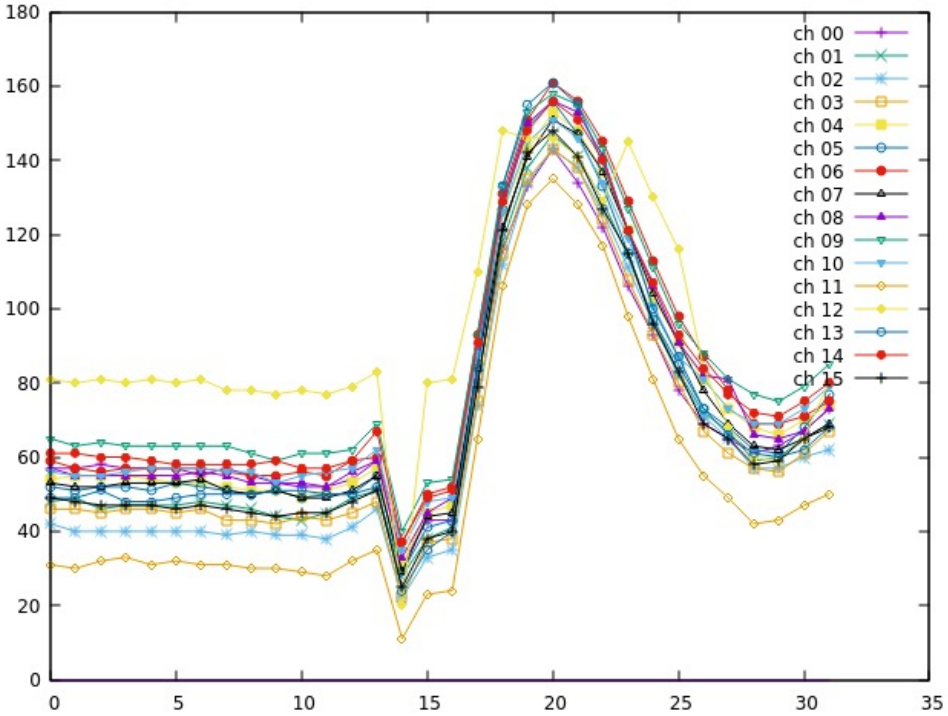
- S2.2 has only internal injection to one channel
- To inject all, use test plane under input traces on PCB

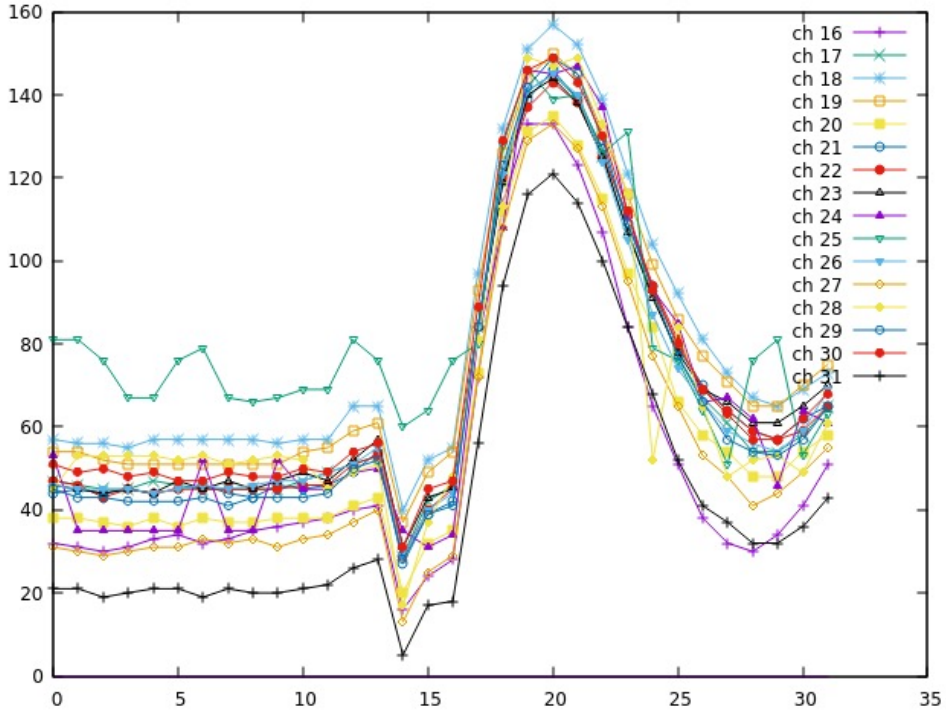


- Pulser triggered synchronously to readout by SPADIC trigger output

CSA outputs (S2.2)

- All 32 channels:

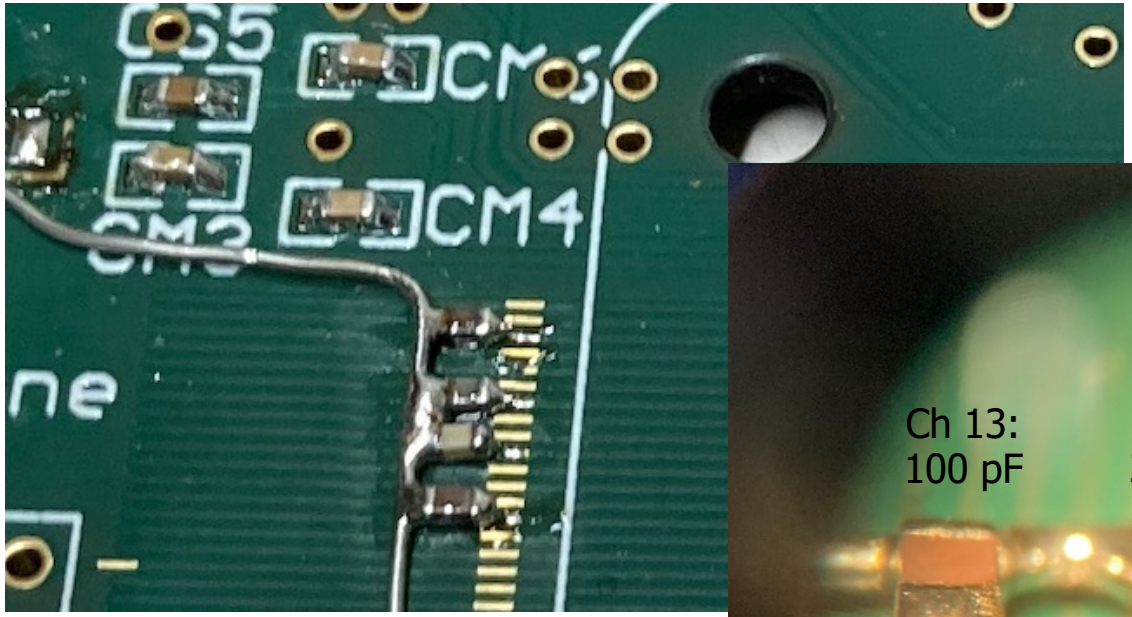


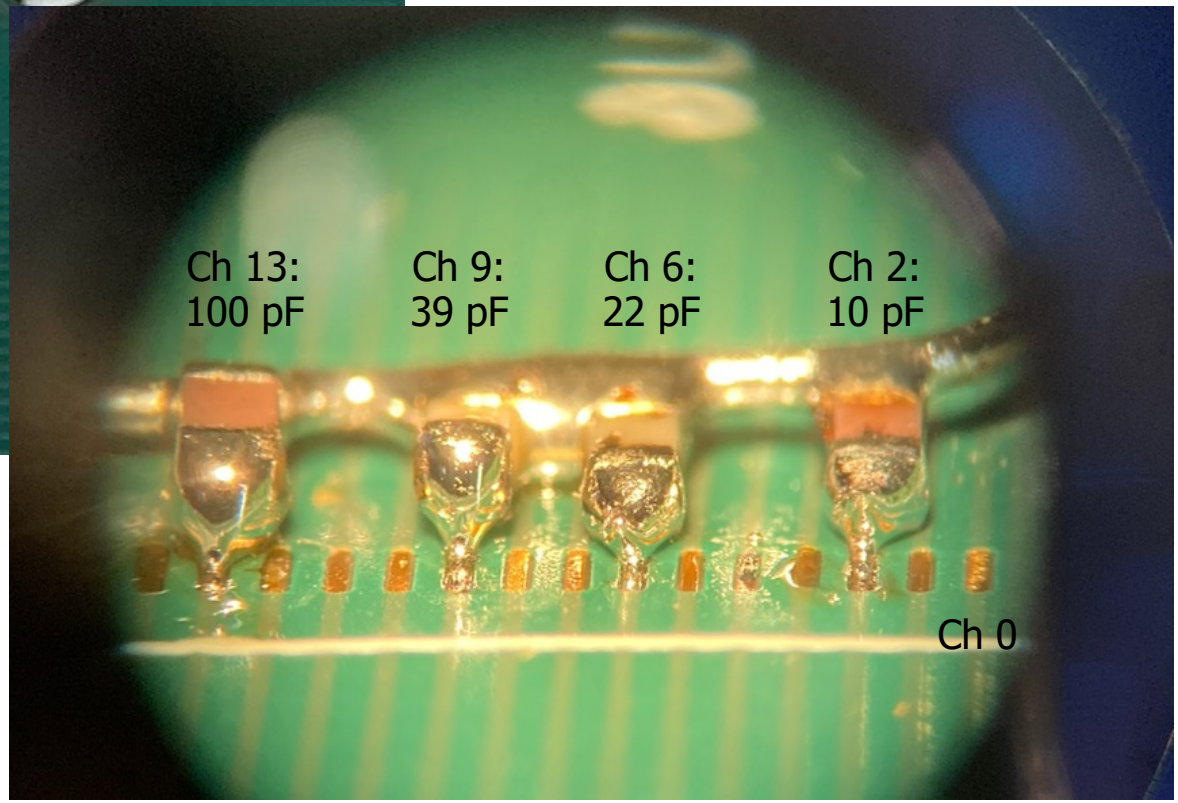


- Initial kink due to crosstalk of trigger signal
  - Is visible also if pulser signal in turned off
- (Signal ‘late’ due to delays in setup, better in S2.3…)
- Some bad ADCs (as before)

Adding Capacitors

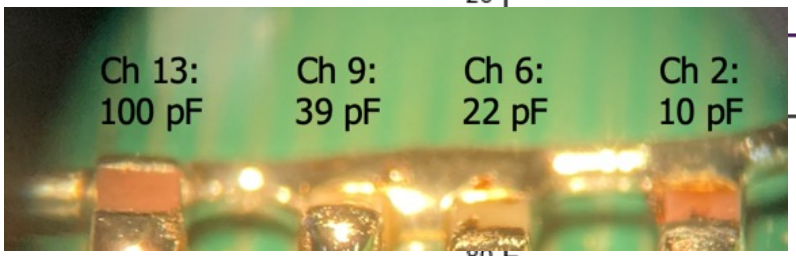
- Soldered (small … very large) caps of **10,22,39,100 pF** to some input traces on PCB:

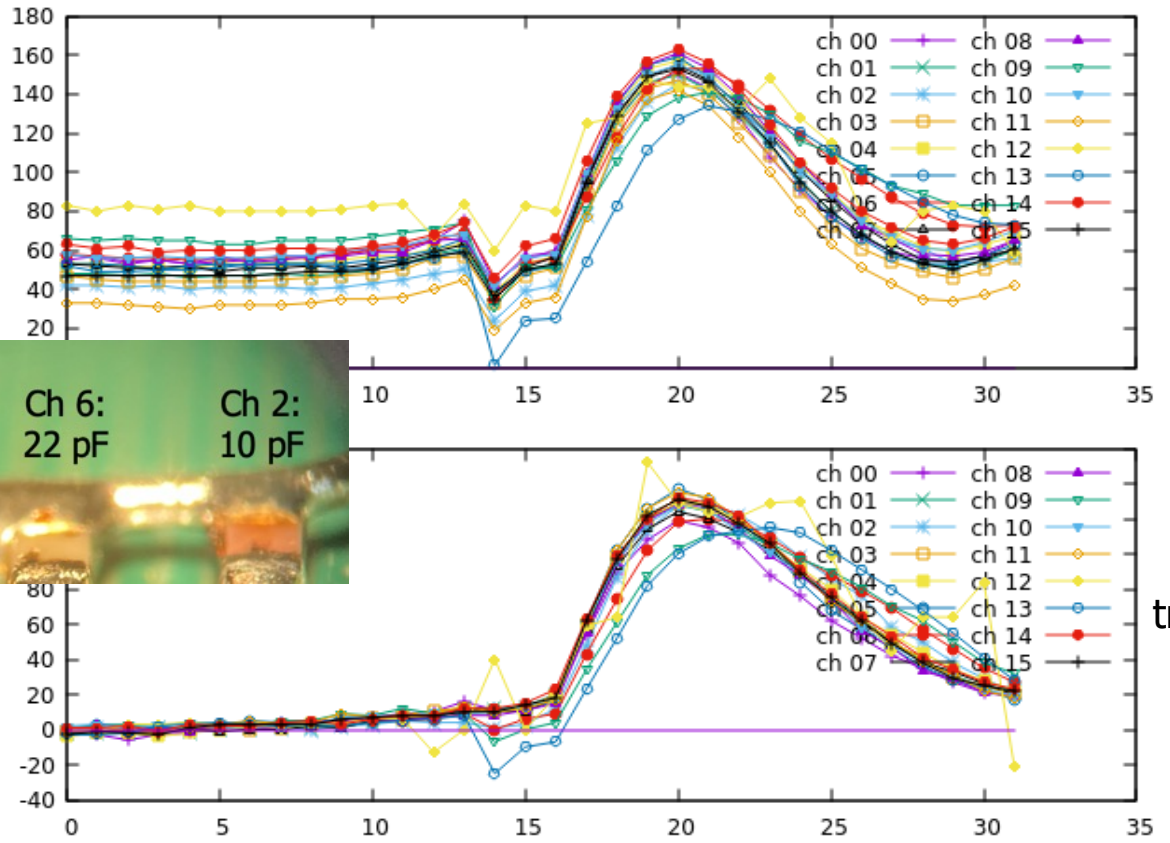




Capacitance Dependence

- Same injection measurement





Ch 13:
100 pF

Ch 9:
39 pF

Ch 6:
22 pF

Ch 2:
10 pF

in lower plot, trace of 'empty' event is subtracted

- Signal gets slower for channels 13 and 9
- amplitude drops only little (note caps are very high!)
- -> CSA in S2.2 behaves as expected.

Discussion / Frustration

- Changing all possible settings in S2.3 does not help
  - Automatic Over-the-weekend sweep by Michael
- Switching chip boards does not help
- Using newly bonded chips does not help

- After many ‘measurement sessions’, we ran out of ideas.

Conclusion

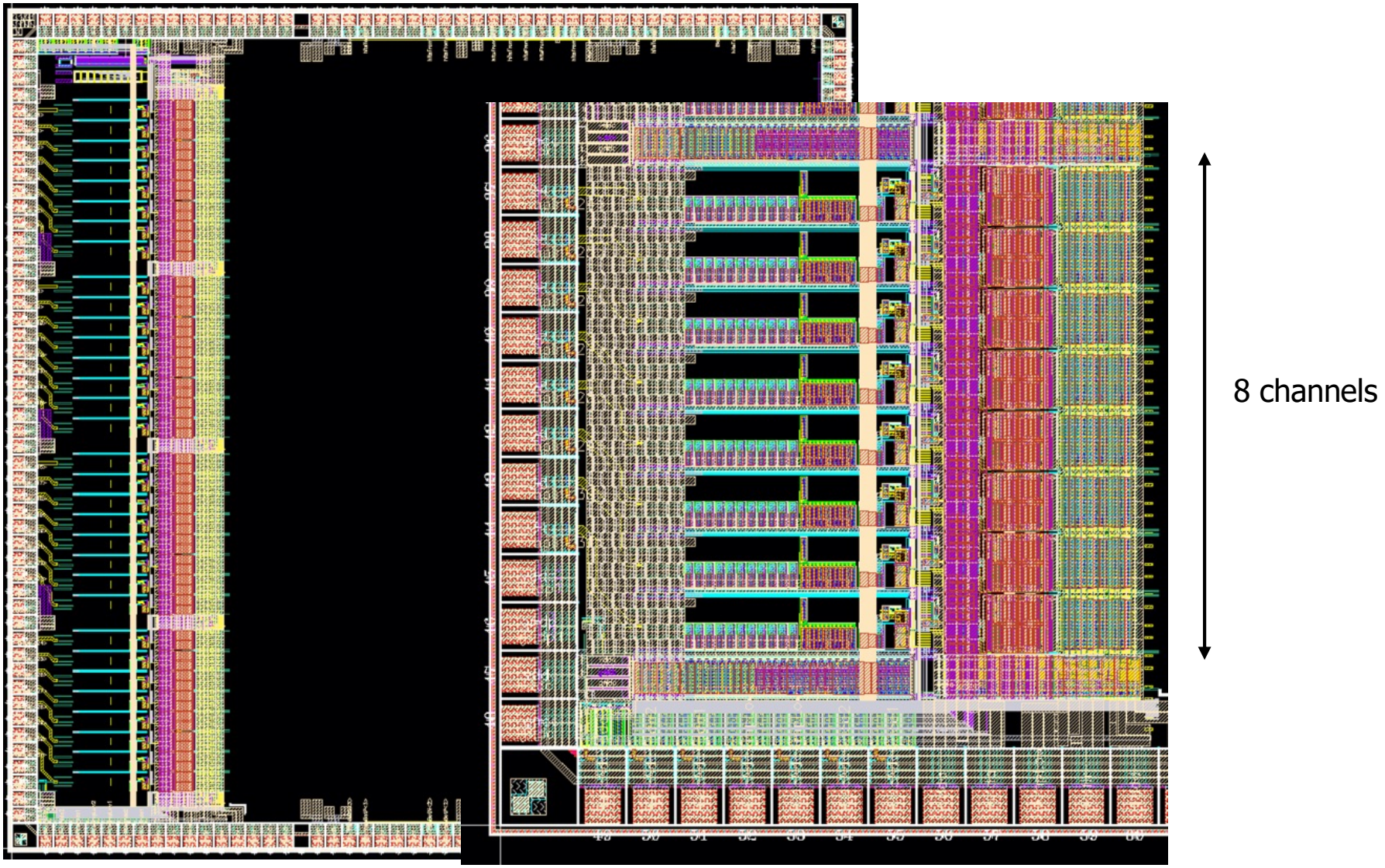
- Setup and Software are fine
- S2.2 behaves as before
- Gain drop of S2.3 CANNOT BE SEEN in S2.2

- Gain drop must be property of S2.3 DESIGN or RUN
  - Chances that we operate chip wrongly are small
- Again: CSA SHOULD be identical
  - Unintentional change (but: checked several times in cadence)
  - Side effect of other measure (Caps, injection). How?
  - Bad production run? Unlikely

- Still unclear.
  - Therefore we also DO NOT KNOW if the very bad ADC performance in S2.3 is from design, or a similar ‘strange effect’ as CSA gain drop.

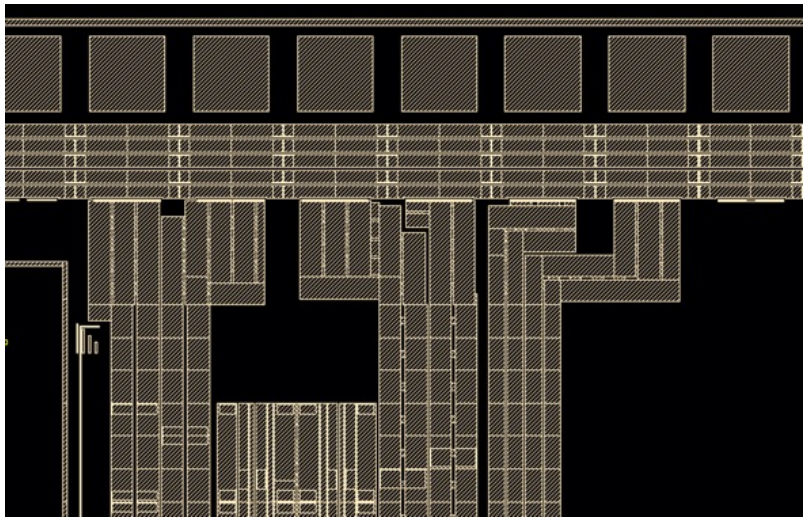
INTERMEZZO:
S2.2 CHANNEL LAYOUT

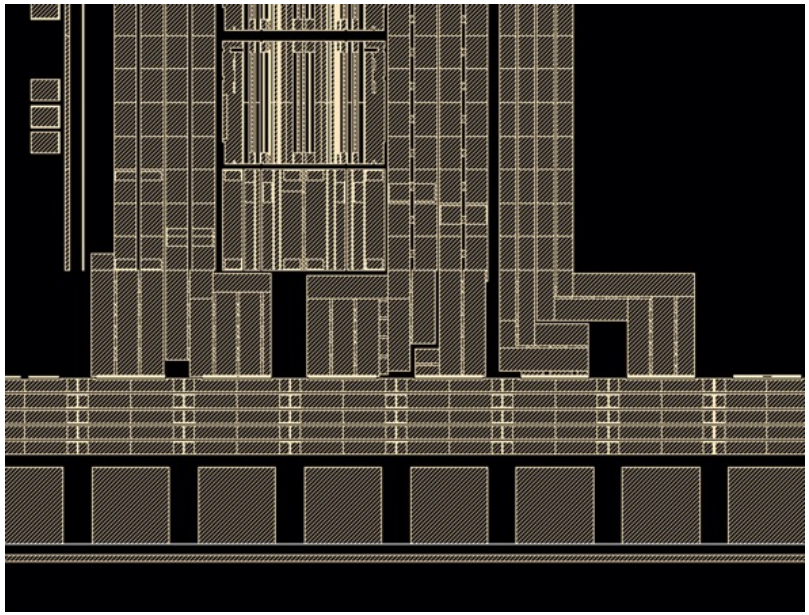
- 32 input channels are arranged in 4 groups of 8 channels



Power Distribution

- Power is equally connected to/bottom
  - Different behavior of low channel numbers unclear





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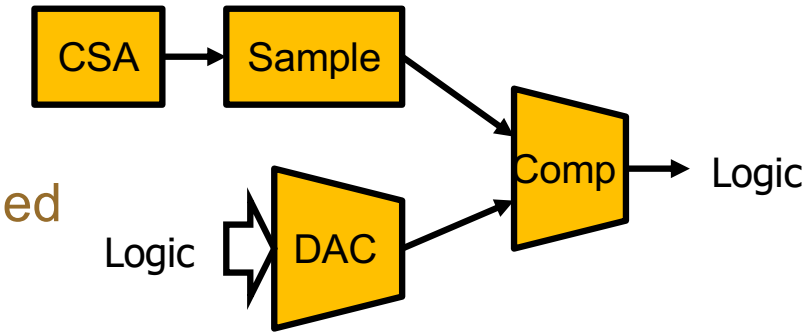
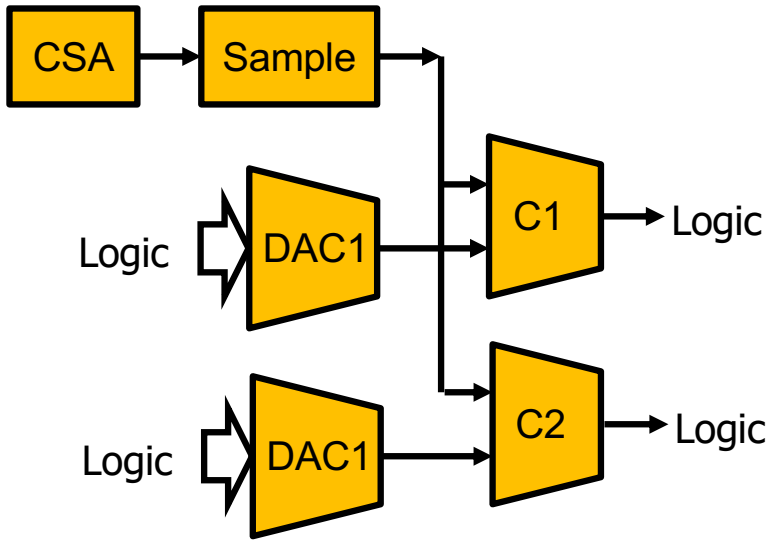
NEW ADC

New ADC

- Go for successive approximation ('SAR')
  - Sample CSA output
  - Compare sampled value to varying reference values, provided by a DAC and controlled by logic.



- Michael has 'invented' a more robust version using two DACs & Comparators.
- It is less sensitive to wrong comparator decisions in the coarse steps
- See Michael's talk

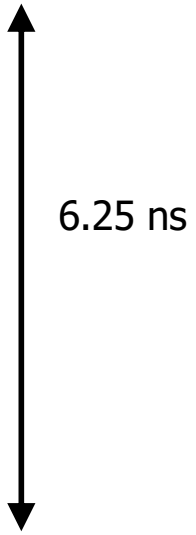


DAC Speed

- System Clock is 16 MHz
- We have 10x clock available = 160 MHz

- -> 6.25 ns are available per conversion step:

  CLK ->
  - Logic sends new DAC values
  - DACs logics decode values
  - DACs generates output voltages
  - Comparators compare
  - Results are sent to logic
  - Logic calculates next DAC values -> CLK



- Not easy !

DAC Speed Optimization

Idea:

- In each step there are at most 4 possible outcomes of the Comparator decision
- Logic can pre-calculate the new DAC values and send them to the DACs, which can prepare the new analogue value
- Some task operate in parallel

CLK ->

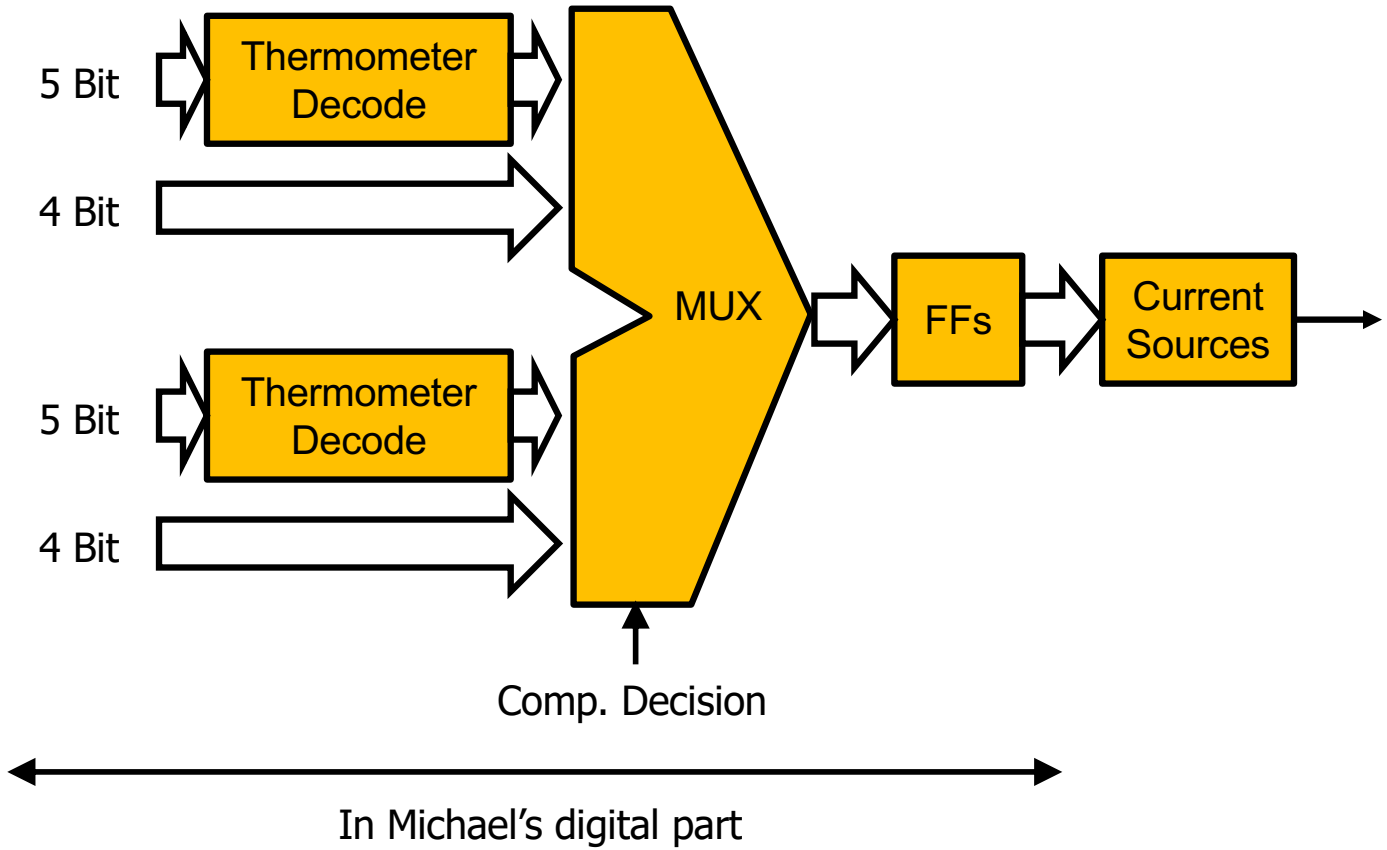
- Logic tells DACs which value to use
- DACs generates output voltages
- Comparators compare
- Results are sent to logic
- Logic calculates next DAC values -> CLK

Decoding is saved

- Logic calculates potential new values
- Values are sent to DACs
- DAC logic decodes values

ADC Components: 9 Bit DAC

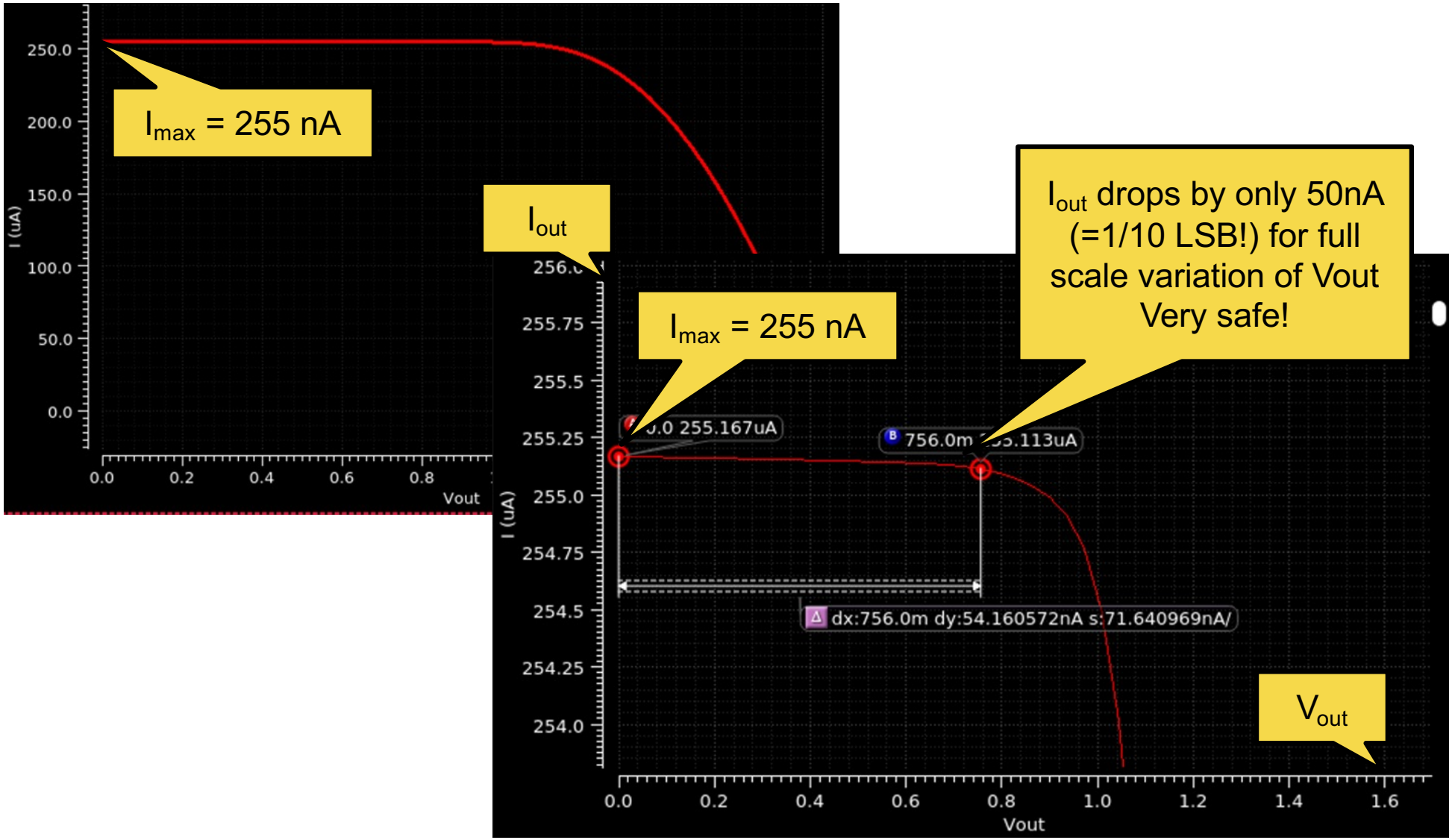
- Based on proven, good 11 Bit DAC!



- I_{LSB} = 500 nA
- Drive into 3k -> V_{LSB} = 1.5mV, FSR = 750 mV

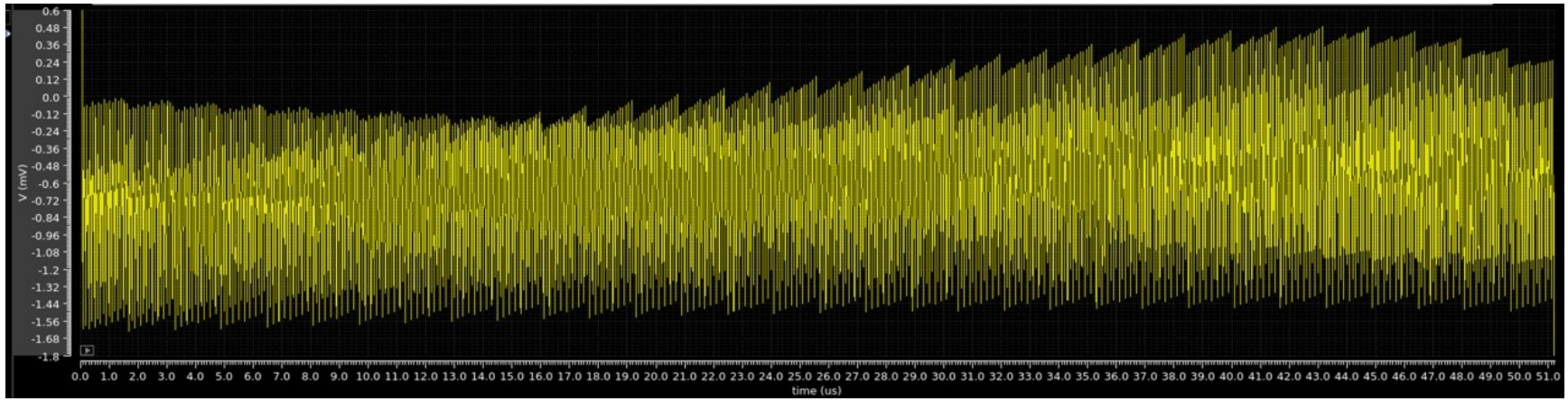
DAC Output Compliance

- Iout (Vout) – Required for linearity

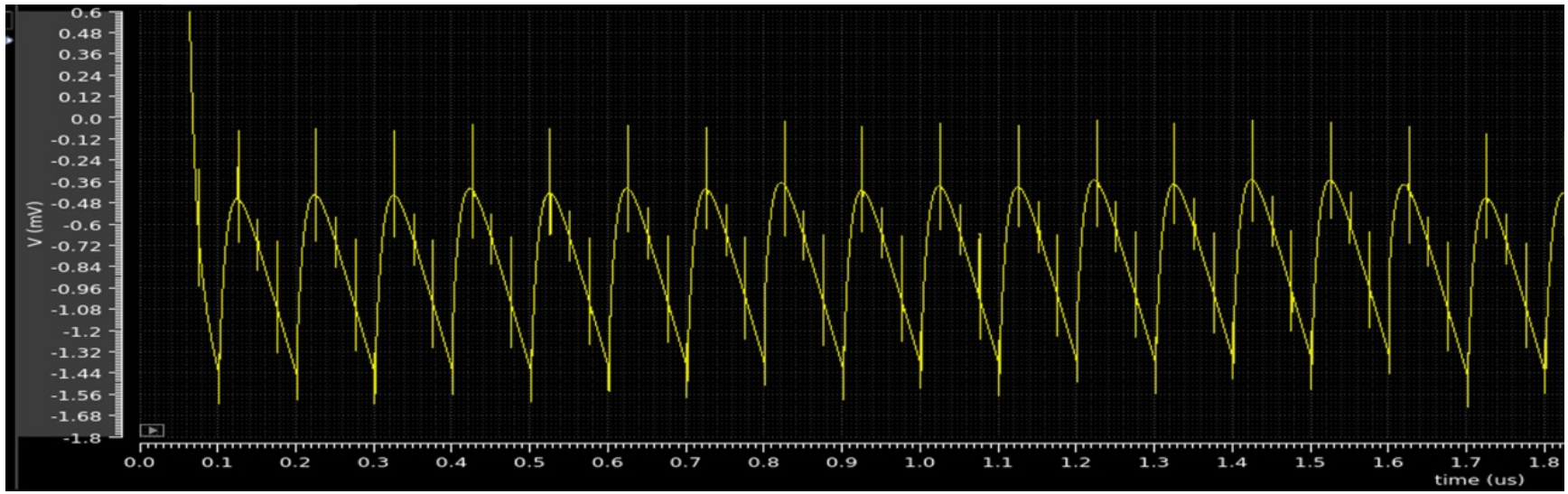


DAC Linearity

- Sim all 512 steps. Subtract ideal line. Expect sawtooth.



1.5mV

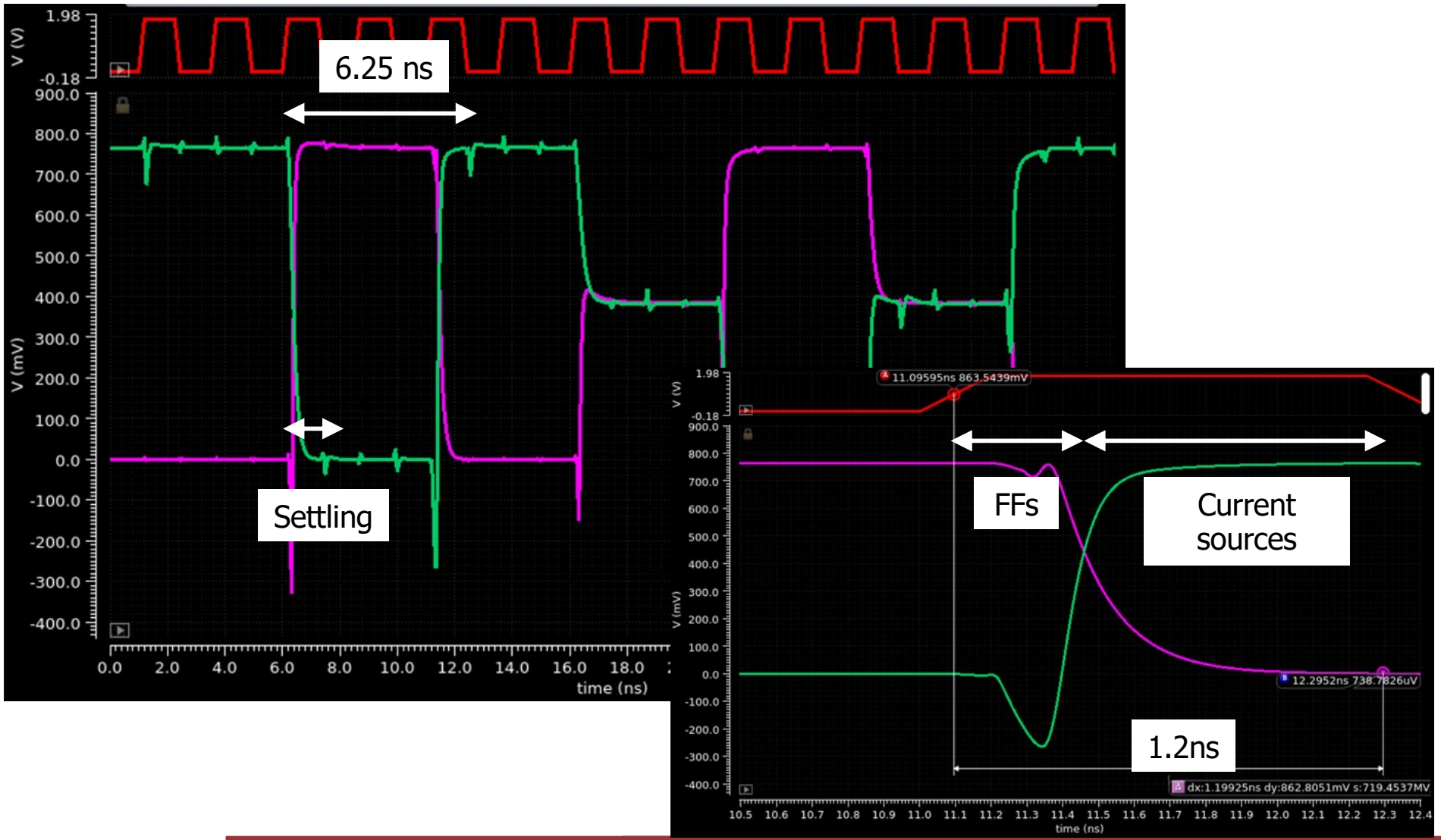


1.5mV

- Very good INL (much < LSB)

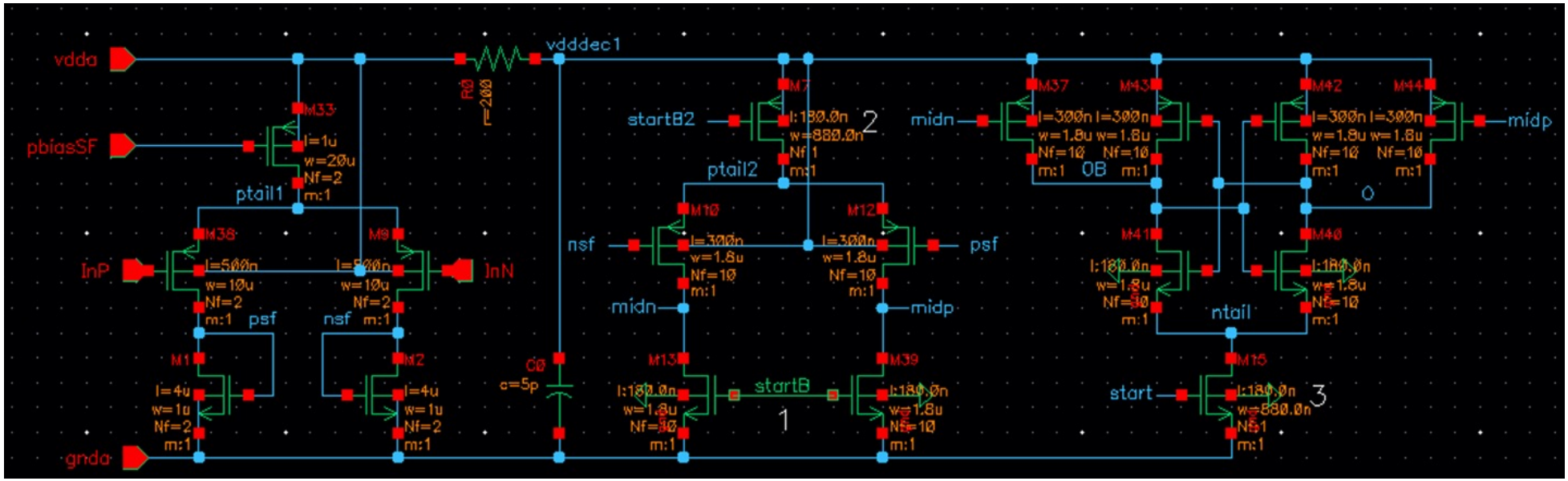
Settling Time

- Simulation shows full scale steps (= worst case)



Comparator

- Improved design has



Differential input stage for some gain and level shifting

Filter to reduce kickback

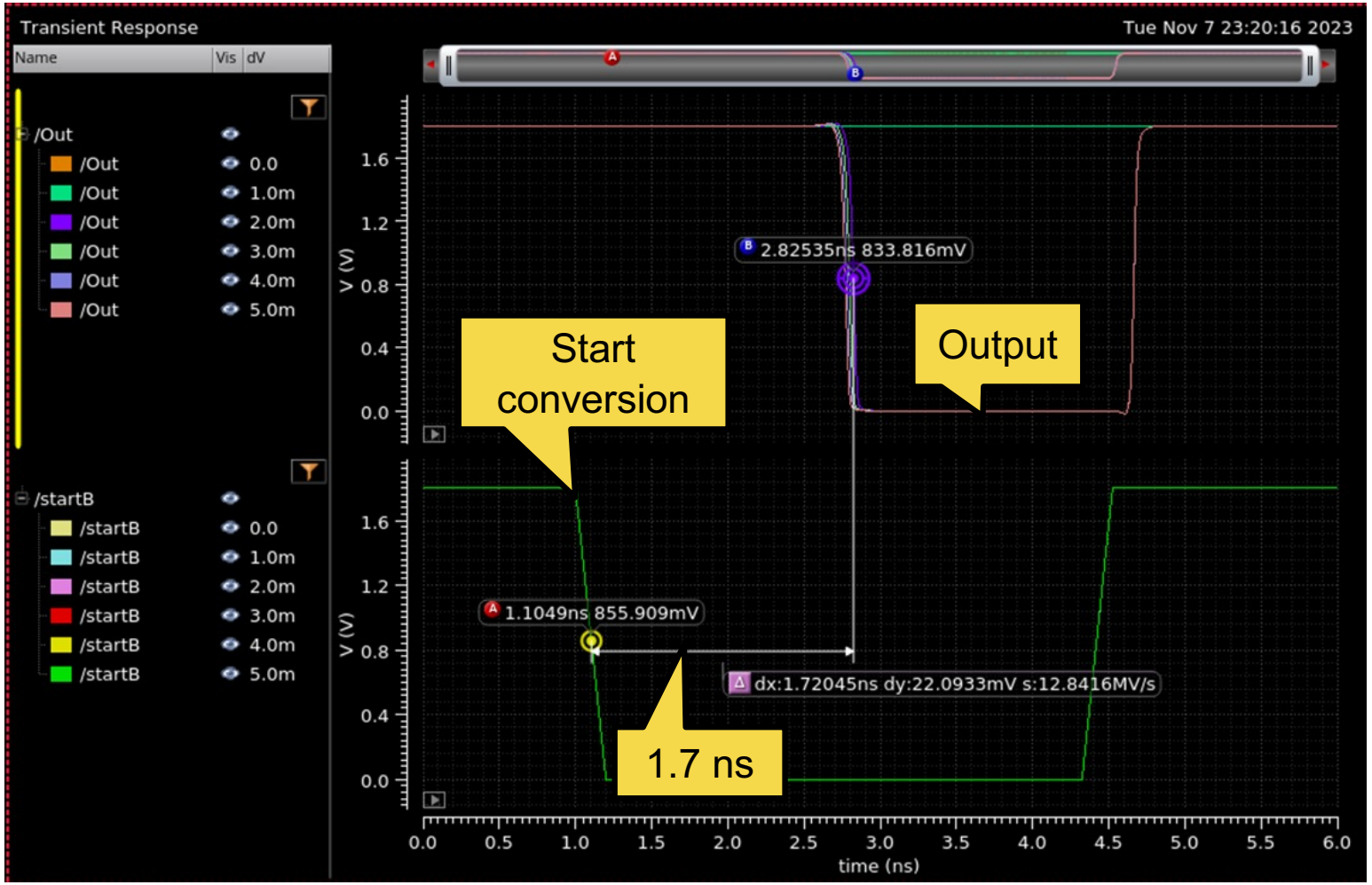
1st stage latched comparator

2nd stage latched comparator

Buffer (not shown)

Comparator speed

- Sim input offsets of 0…5 mV
- Slowest signal switches after 1.7 ns

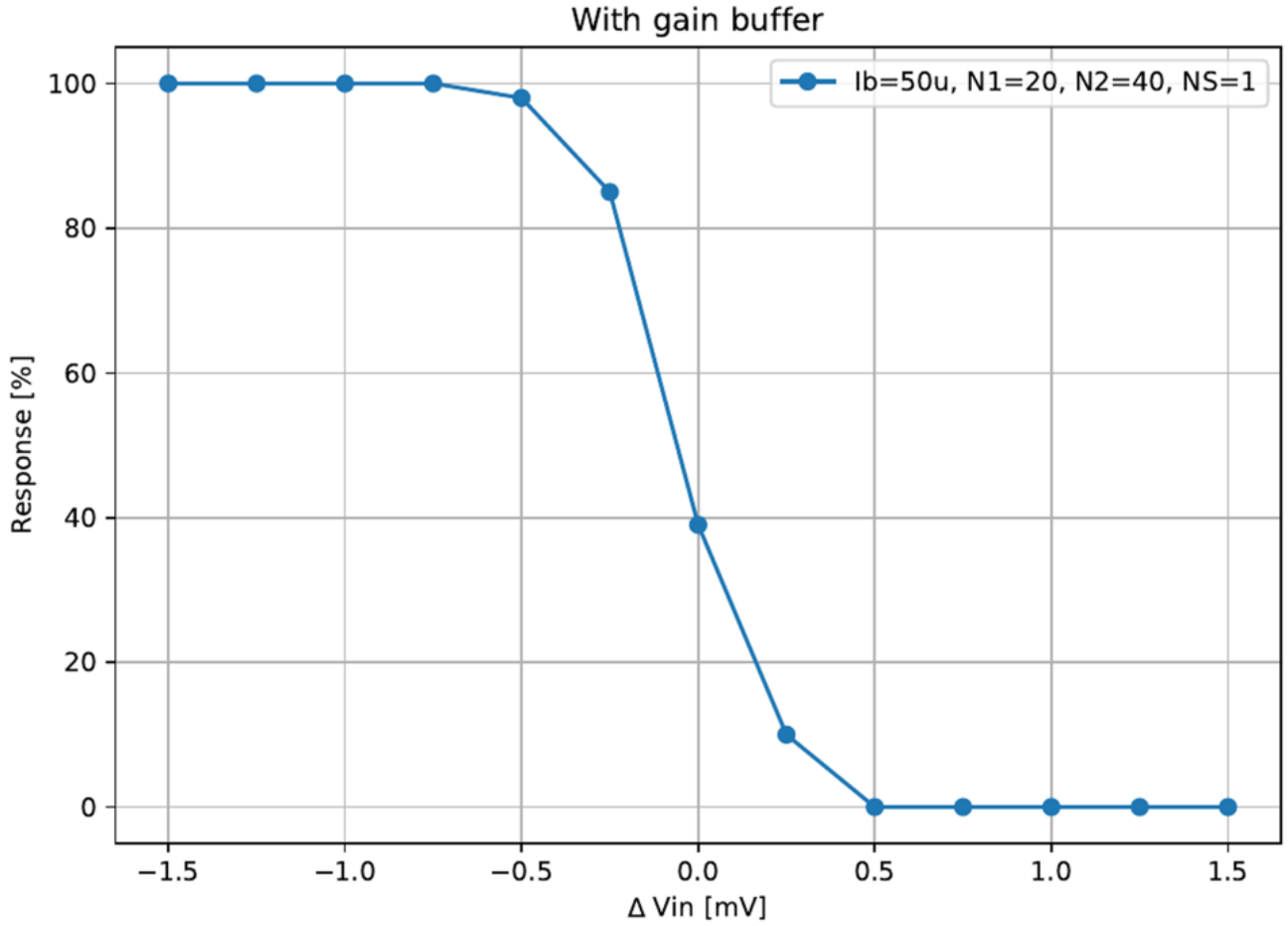


Comparator Noise

- Repeat simulation above several times for one input voltage
- Vary input voltages
- Design parameters (transistor sizes, currents) have effect:

Comparator: Best noise so far

- ‘Full scale’ noise ~1 mV < 1 LSB. Looks promising…



Submission Plan

- Submit new S3.0 with redundant SAR ADC
  - No input caps so that it could be used with chambers
  - Start from S2.2 CSA to avoid any unintentional bug possibly introduced in S2.3
- Unchanged S2.3 to find out if gain drop persists.
  - Check technology
- Submit chip on common engineering run organized by GSI (Ch. Schmitt), together with PADI & Co.
- Presently collecting money and preparing paperwork.

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Wish List

Wish List

- Charge Range:
  - Signals up to 140fC should not start ‘overload’ circuit, so that no charge is lost and (falling) edge is still proportional to primary charge (Cf ~ 0.5pF)
- Low Gain Mode has priority
  - This will make it more difficult to operate at low noise (ADC noise has more effect)
- Drop CRRC2
  - Short shaping time is used and works better.
- Question: Aim at which FSR for ADC?
  - 9 Bit ADC
  - Assume LSB ~1000 Electrons
    - Max FSR is 512000 e = 82 fC -> 70 fC with ‘border regions’
    - ADC DNL of 0.8 ADU -> 800e Noise.

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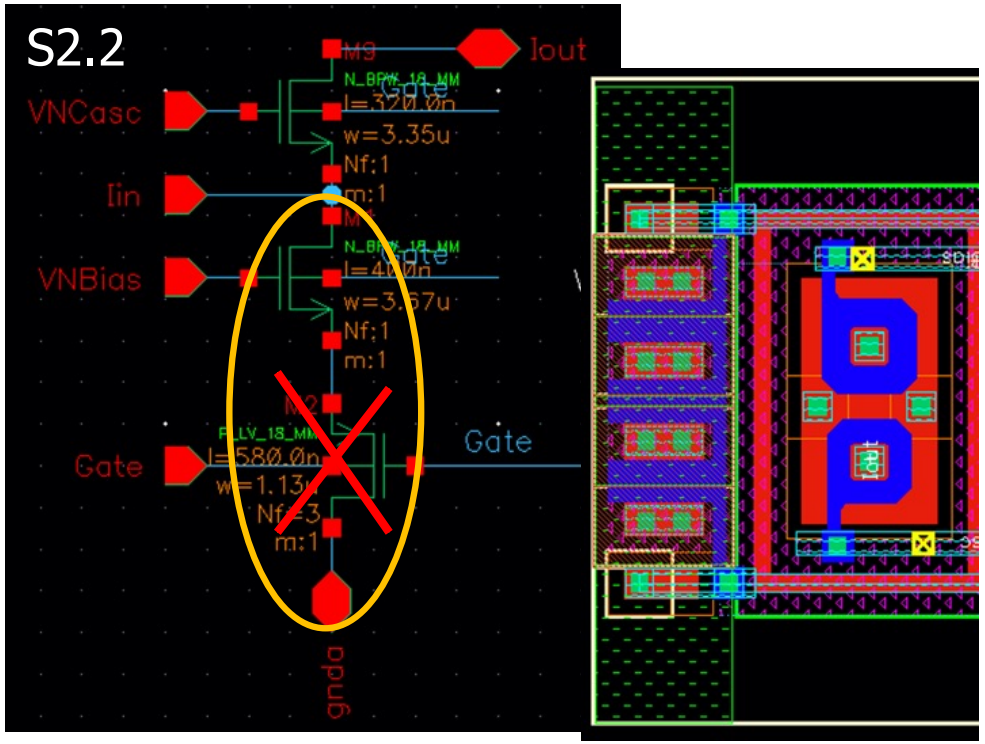
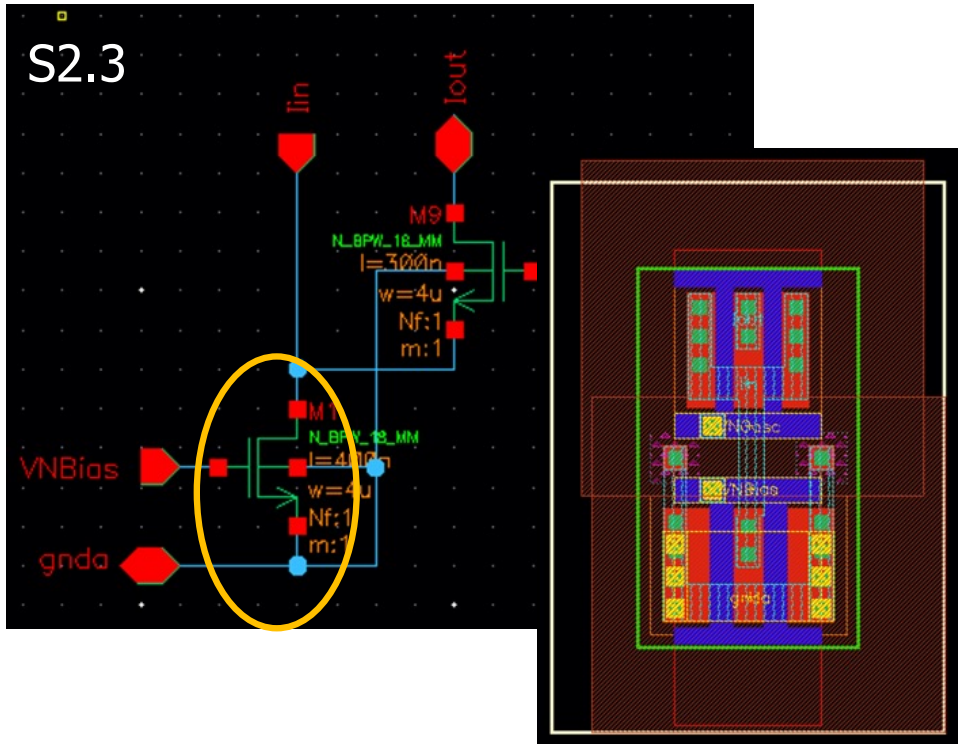
BACKUP

SPADIC2.3A: Comparator Changes

- Original design used ‘trick’ for voltage drop compensation (chip had 256 ADCs!)
  - The extra MOS add mismatch.
  - Also, NMOS are annular for radiation hardness





- Eliminated extra MOS and made NMOS linear and larger
  - Functionality is unchanged

SPADIC2.3A: Analogue Changes

	0 pF	5 pF	10 pF	15 pF	20 pF	30 pF
small input protection	24,26,31	30	29	28	27	25
medium input protection	16,18,23	22	21	20	19	17
normal input protection	0 ... 8, 10, 15	14	13	12	11	9

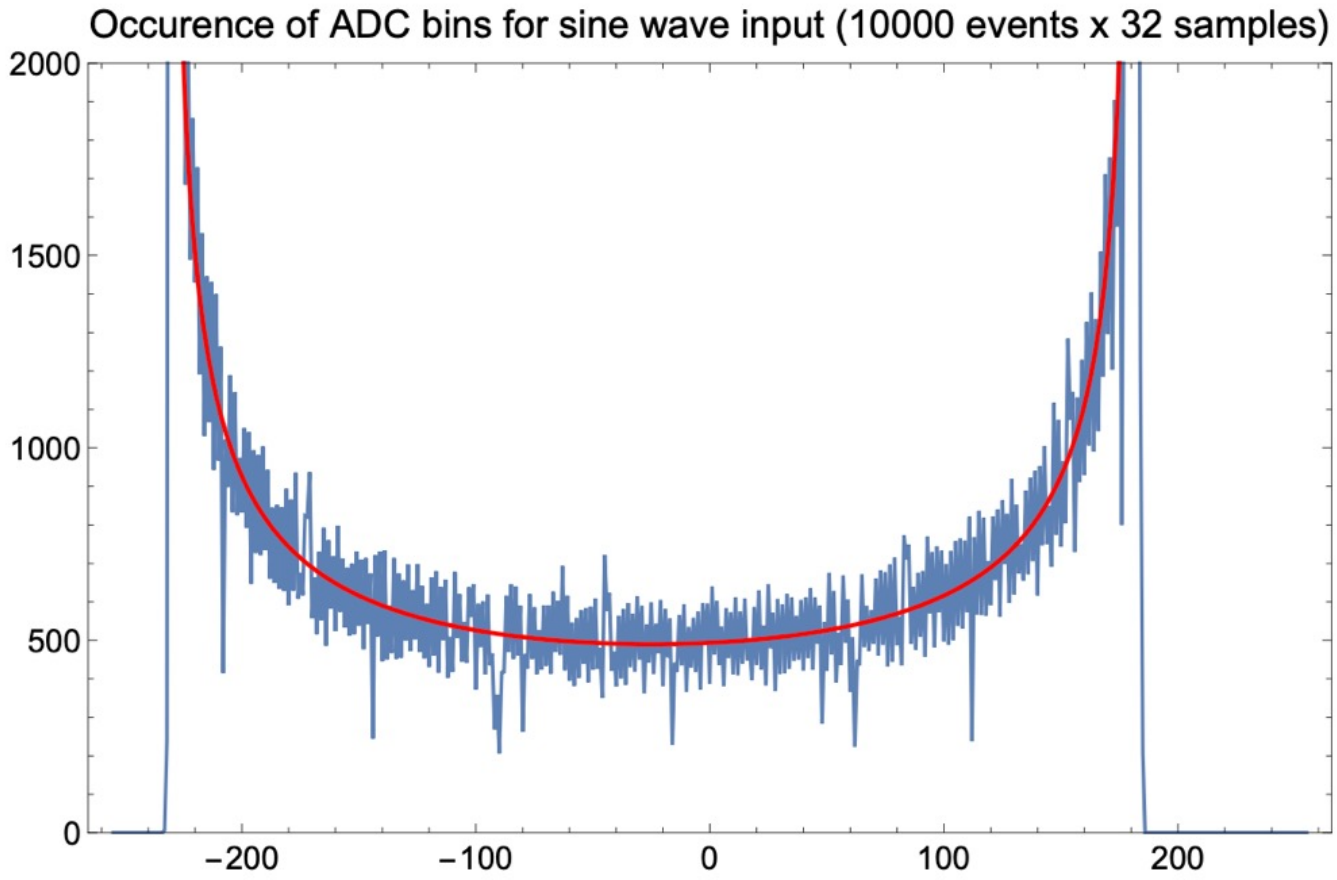
- In N-load of U2I converter, gate voltage is eliminated and layout uses normal MOS. Transistor dimensions are slightly changed. Bias circuit is adapted.
- Fixed capacitors of varying size are connected to some inputs.
- The size of the ESD input protections is varied in different channels.
  - The supply connections of the protection diodes now use the analogue supply.
- All channels now have an internal injection (works)
- The range of the internal Bias DACs has been doubled (by using the unused LSB Bit)
- Wrong Bias Diode in VNDel has been exchanged (was PMOS, must be NMOS) (very uncritical circuit part)

SPADIC2.3A: Digital Changes

- Timestamp is reset to a programmable register value when sync command is executed
- A configurable number of pre-samples is possible
- The bug in the baseline averaging circuit is fixed (wrong bits were read)
- The read back issue of analogue shift register has been fixed
- Injection and digital trigger are in same register and thus more flexible. In particular, the analogue trigger and the readout are started simultaneously so that the (time) position of the injection in the sample is stable. The polarity, the width and the timing of the analogue pulse can be adjusted.
- The LVDS output drivers have been improved to better reach a swing of 800 ± 200 mV

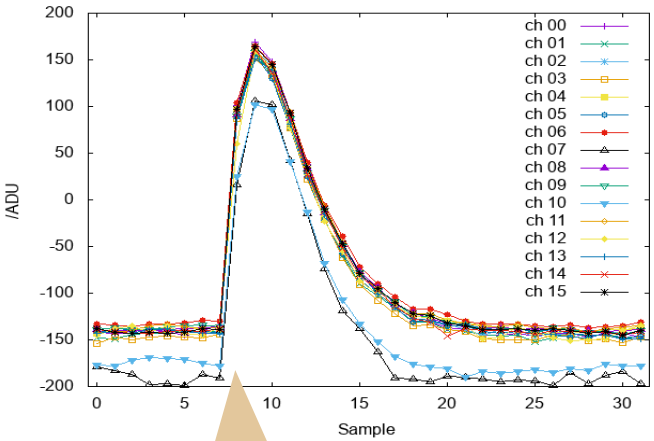
SPADIC2.2 Bathtub

- Input Signal (directly to ADC) is sine wave
- Histogram of ADUs should follow red function – nice match
  - Overall operation as expected, some outliers.



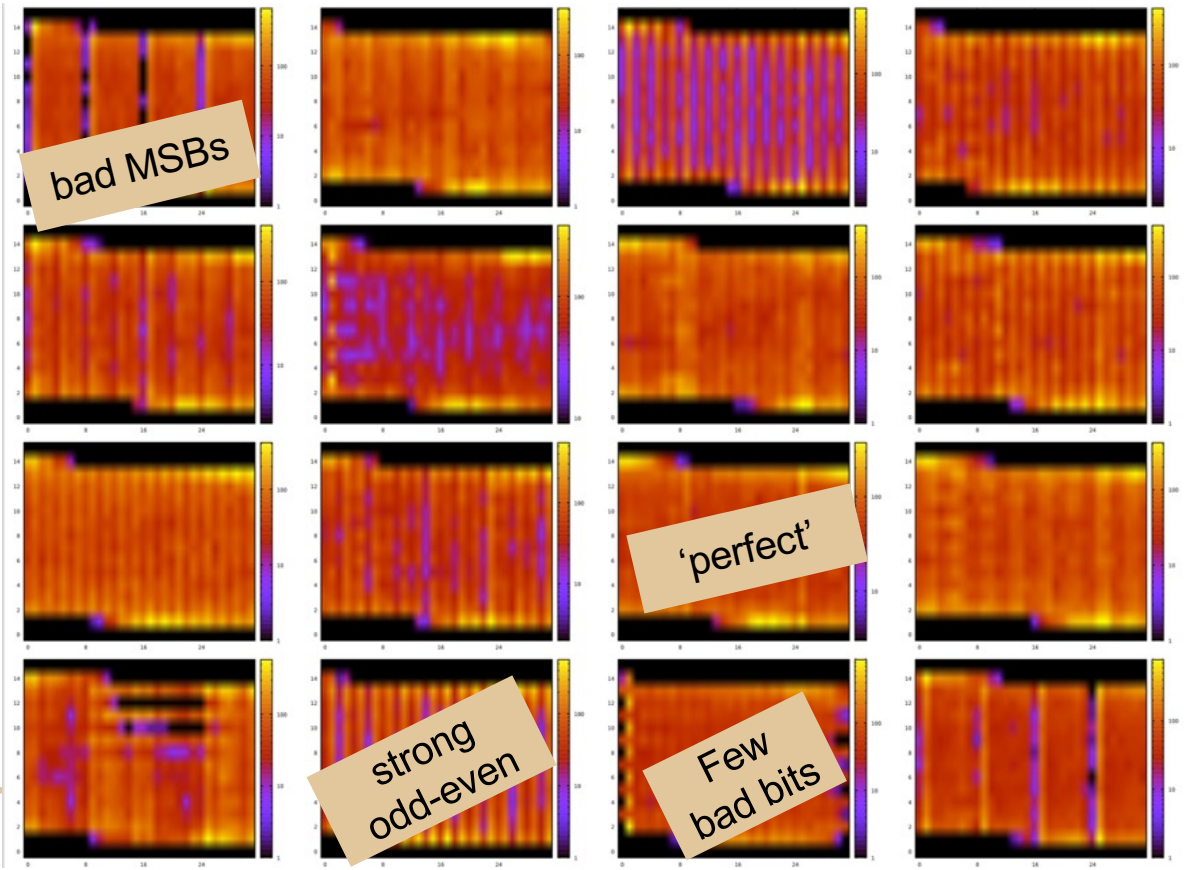
SPADIC2.2 Main Issues

- **Pulses** look ‘relatively nice’, but **density maps** (occurance of values) of most ADCs look bad



Sampled Pulses

2D map of occurrence of ADU values



- Noise ‘a bit high’ (1200 @ 0pF, 2500@50pF)