



LMD in FPGA to Time Sorter via Fakernet

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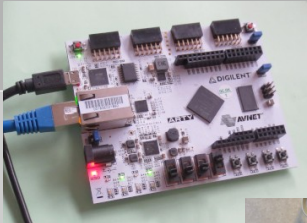
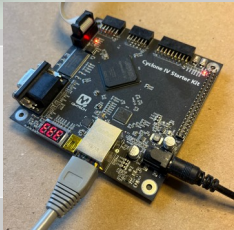
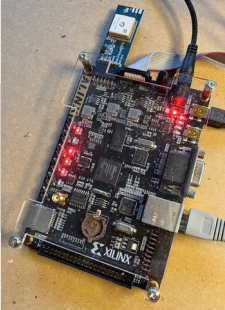
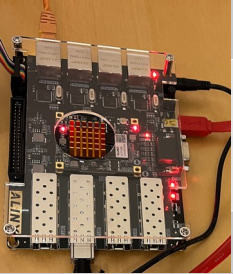
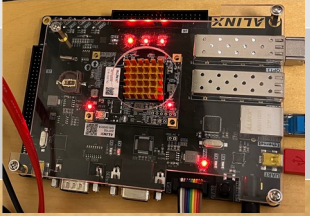
Bad news first

What will be presented is **not** ready for *large-scale* use.

Requires excessive monitoring...

Can be used small-scale / testing.

Fakernet: FPGA-independent TCP + UDP

Manufact.	Board	FPGA	Ethernet	
Digilent	Arty A7	Artix 7-35/100	100 Mbps	
QMTECH	Cyclone IV Starter Kit	Cyclone IV	1 Gbps	
ALINX	AX516	Spartan 6	1 Gbps	
ALINX	AX7101	Artix 7-100	1 Gbps	
ALINX	AX7201	Artix 7-100	1 Gbps	

Xilinx
Altera

Fakernet LMD...

- Produce LMD events in FPGA

~ 1000 lines of VHDL.
~ 1000 LUTs.

```
...

when WAIT_EVENT =>
  -- We cannot process data until there is at least one word
  -- in the event buffer (the internal header).
  if (has_in_word = '1') then
    state <= READ_EVENT_HEADER;
  elsif (i_flush = '1') then
    state <= PREPARE_PAD;
  end if;

when READ_EVENT_HEADER =>
  -- Latch the internal header data. One cycle later to allow the
  -- write to the RAM block to have completed.
  cur_ev_words <= inevh_payload_words;
  cur_ev_trig <= inevh_trig;
  cur_ev_cnt <= inevh_cnt;
  ts_has <= inevh_ts_has;
  ts_err <= inevh_ts_err;
  state <= PREPARE_EVENT;

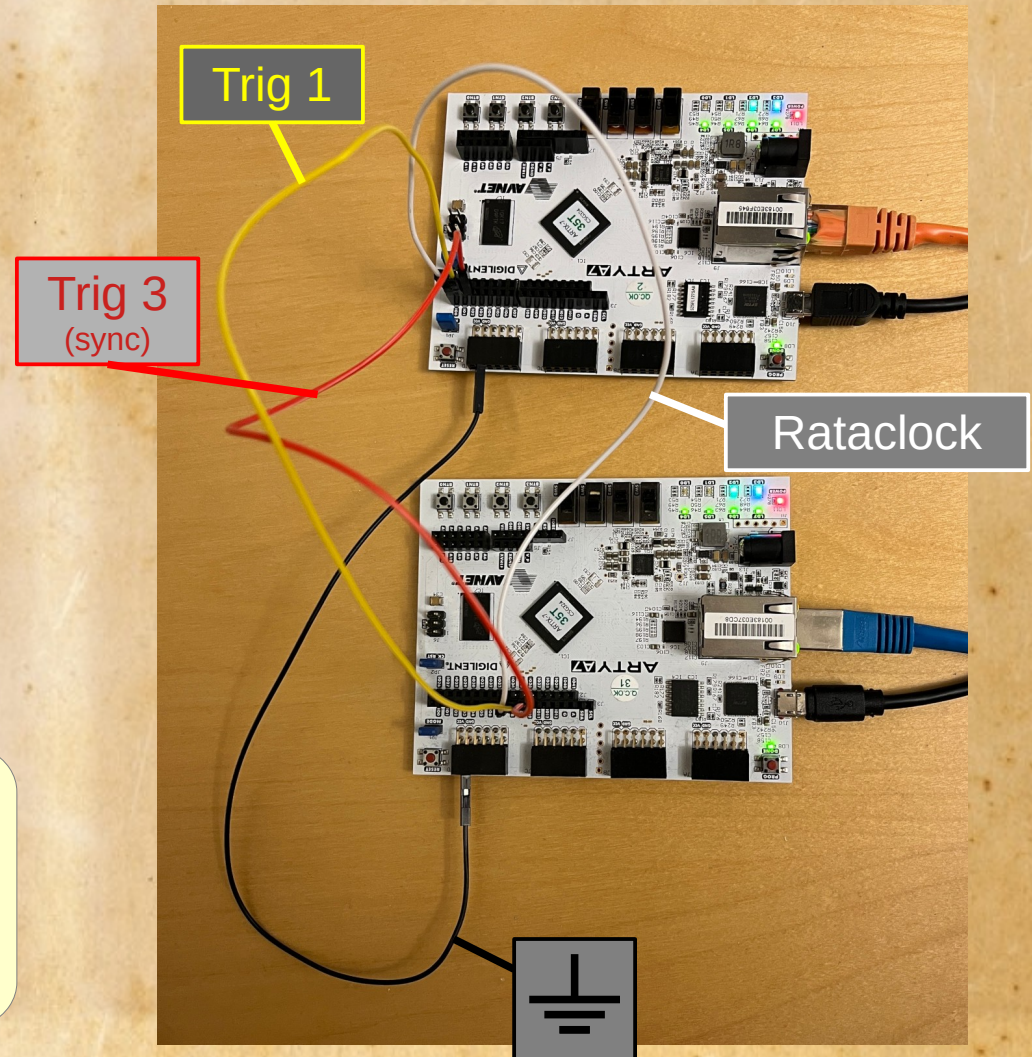
when PREPARE_EVENT =>
...

```


Fakernet LMD => Timesorter

- Produce LMD events in FPGA
- Two boards, sync'ed with rataklock timestamps
→ Combined in drasi TS (timesorter)
- Sync triggers...
- Sync check values...

One small addition before TCP open().

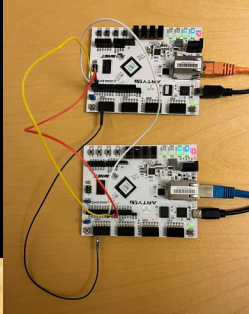


Fakernet LMD => Timesorter

- Produce LMD events in FPGA
- Two boards, sync'ed with rataklock timestamps
→ Combined in drasi TS (timesorter)
- Sync triggers: < 5 ns
- Sync check values: ok

”Go To Jail”
Go directly to Time Sorter.
Do not pass Readout,
do not collect deadtime

The image shows three terminal windows from an xterm application. The top two windows display network statistics for two boards, both identified as 'Digilent Arty A7-35T'. Each window shows buffer and event counts, a timestamp (TS), and sync values. The bottom window shows a detailed network statistics table with columns for 'ts-chk', 'ts-t-i', 'bu', and '500:1'. It lists data for two IP addresses: 192.168.1.193:1 and 192.168.1.194:1, along with a 'localhost' entry. A summary row at the bottom shows 'ncv nrf good amb bad mis spu rel #o sync-trig >20o' with values like '-171.2k', '14', and '0 ± 4'. A red ribbon is visible in the top right corner of the slide.



Fakernet LMD => Timesorter

- Produce LMD events in FPGA
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The terminal window displays the following text:

```
[ 0] buffer_no      2322693 ;      4766
[ 1] event_no      86172065 ;     171275
-----
Descr: Diligent Arty A7-35T
UDP: connected 00, active 00
TCP: connected
Compiled: 2023-10-15 18:26:52 UTC
TS: 000
```

TODO:

”Get Out of Jail Free”

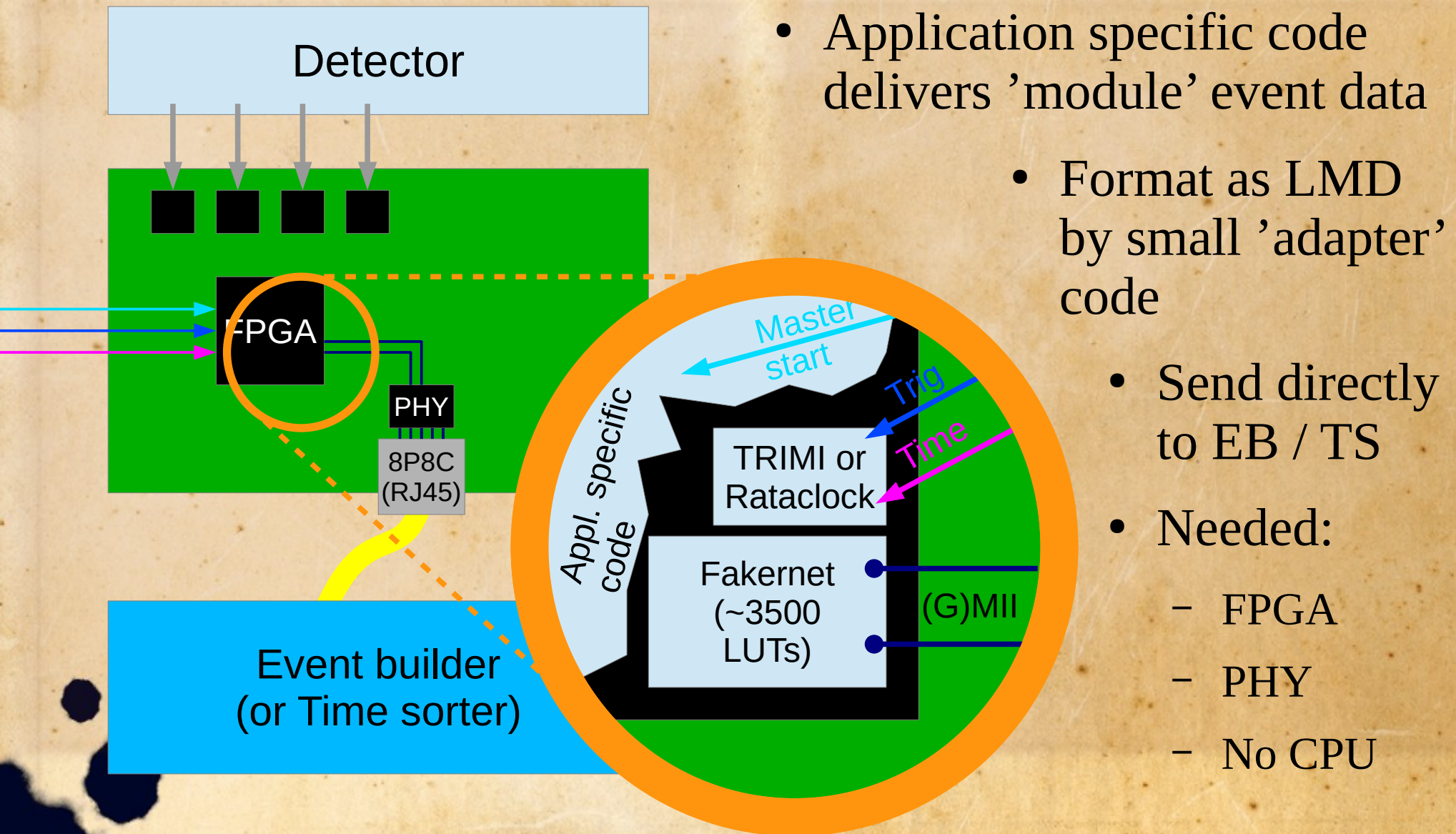
Go to Event Builder.

Event sync in hardware
by
Triva mimic (TRIMI) ”bus”

TimeSorter sources
require (much)
more monitoring

EB could strip
event+subevent headers

Direct LMD from FPGA



- Application specific code delivers 'module' event data
- Format as LMD by small 'adapter' code
- Send directly to EB / TS
- Needed:
 - FPGA
 - PHY
 - No CPU

Fin!



Fakernet thanks:

- Philipp Klenze
The Idea!
- Anders Furufors
Initial impl. help
- Gorka Landaburu
External use
- Bastian Löher
Rataclock popularisation

• Wonderful community tools:

- openFPGALoader
- GHDL (simulator)
- GTKWave
- Wireshark

Fin!



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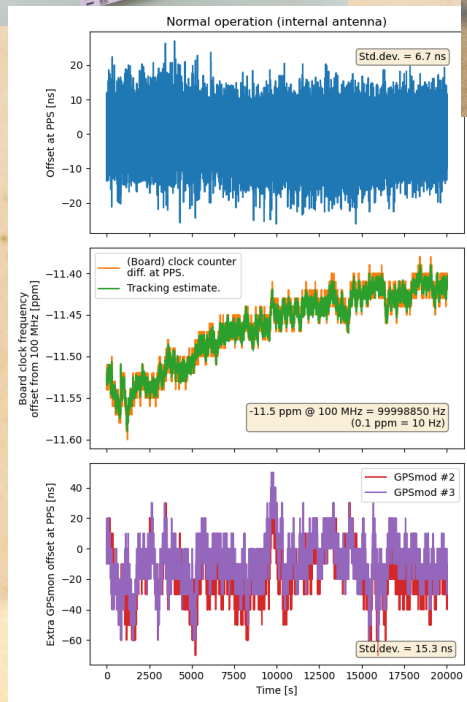
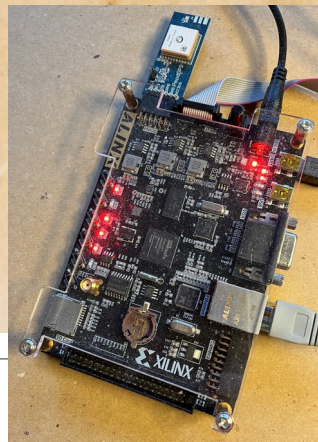
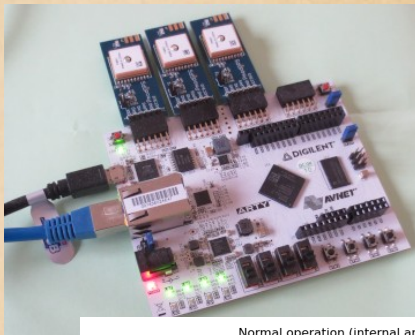
Thank you!

Backup

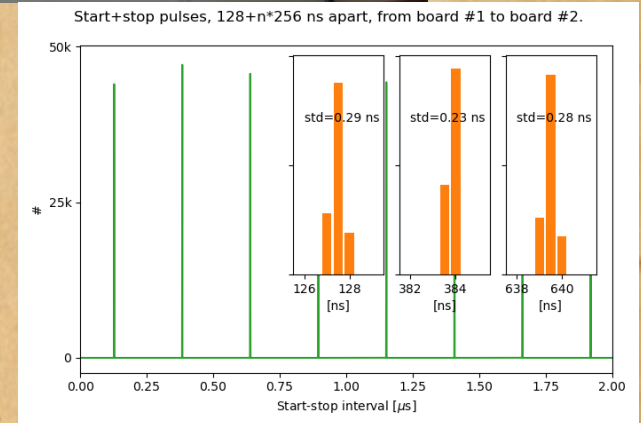
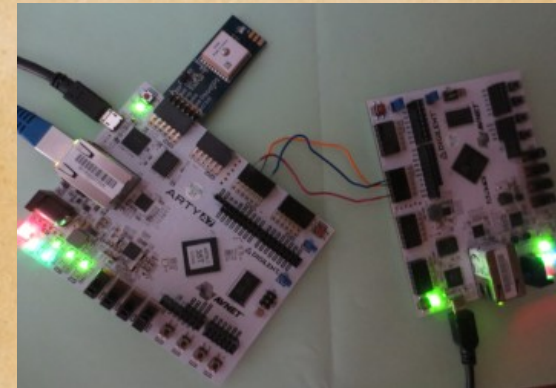


Fakernet in other use

FPGA NTP server



0.5 ns sampler



`ntpdig`
`fnet-ntp1.fy.chalmers.se`