The FOOT detector electronics

The good, the bad, the ugly

What are we talking about

1. **A set of 3 electronic boards connected to a FOOT detector**
   Called Front-end, ADC and FPGA boards
2. **Provide peak sensing ADC infofmation to the outter world (DAQ) for every channel**
3. **Bias the back side of the FOOT detector (HV)**
4. **Center part is the Front end ASIC IDE1140 from IDEAS (commercial product)**
5. **All needed interfaces/parts to generate and transfer digital information to the DAQ**

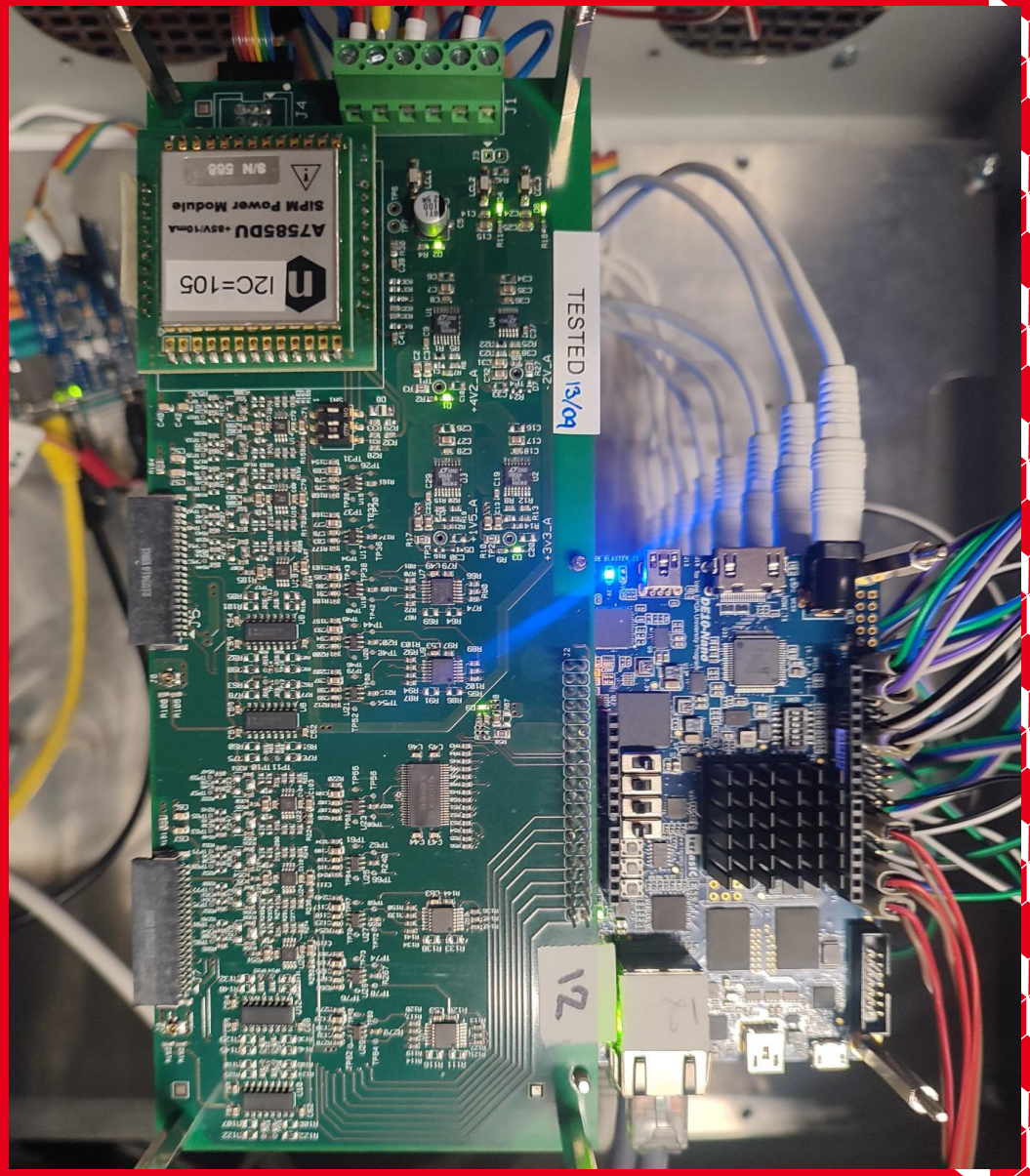
1. How does it look like

Pics courtesy Andrea Jedele

Overview

Detector + FE board

ADC + FPGA boards

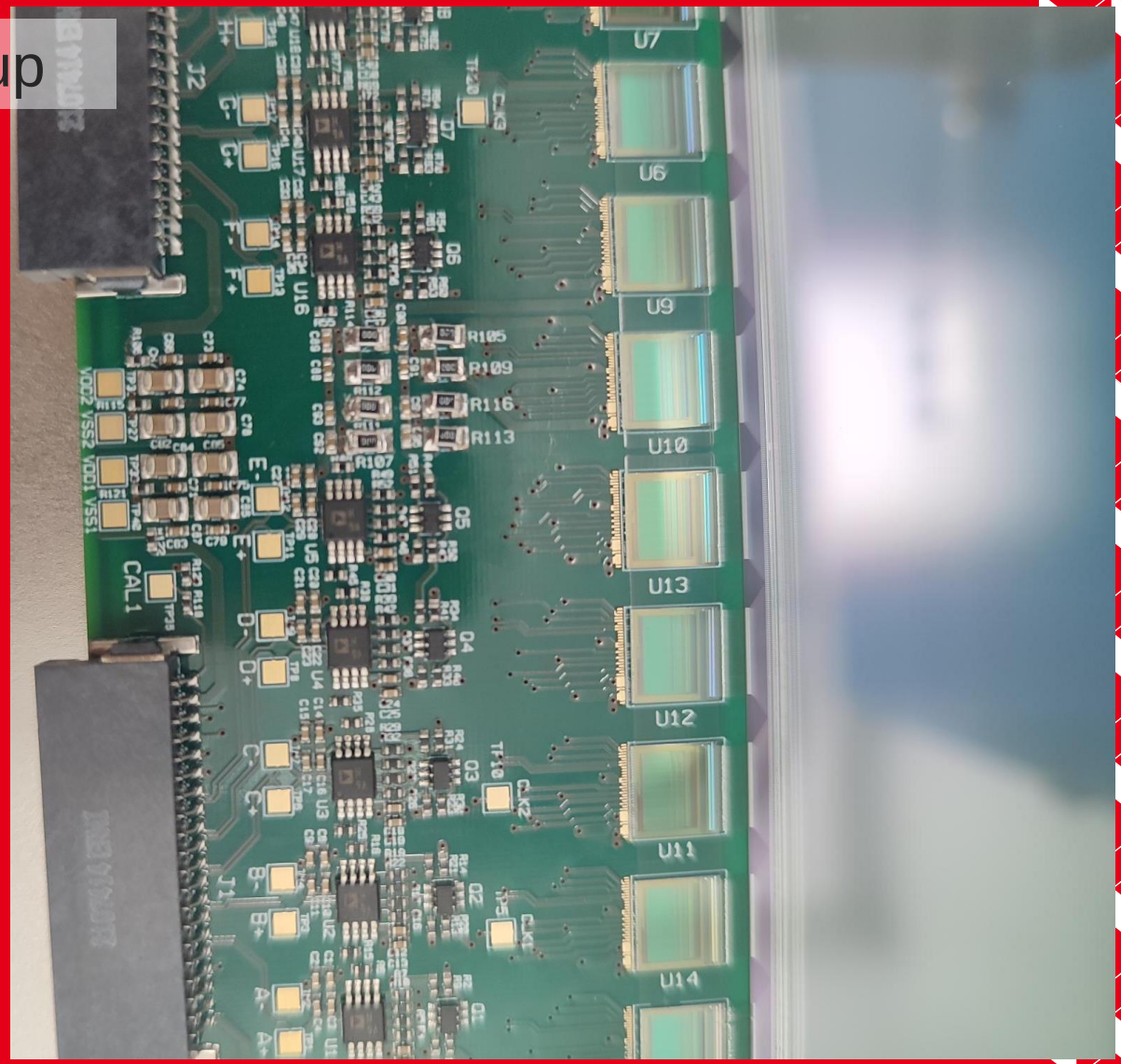


The Front-end board (in vacuum)

IDE1140 64 ch
ASIC X10

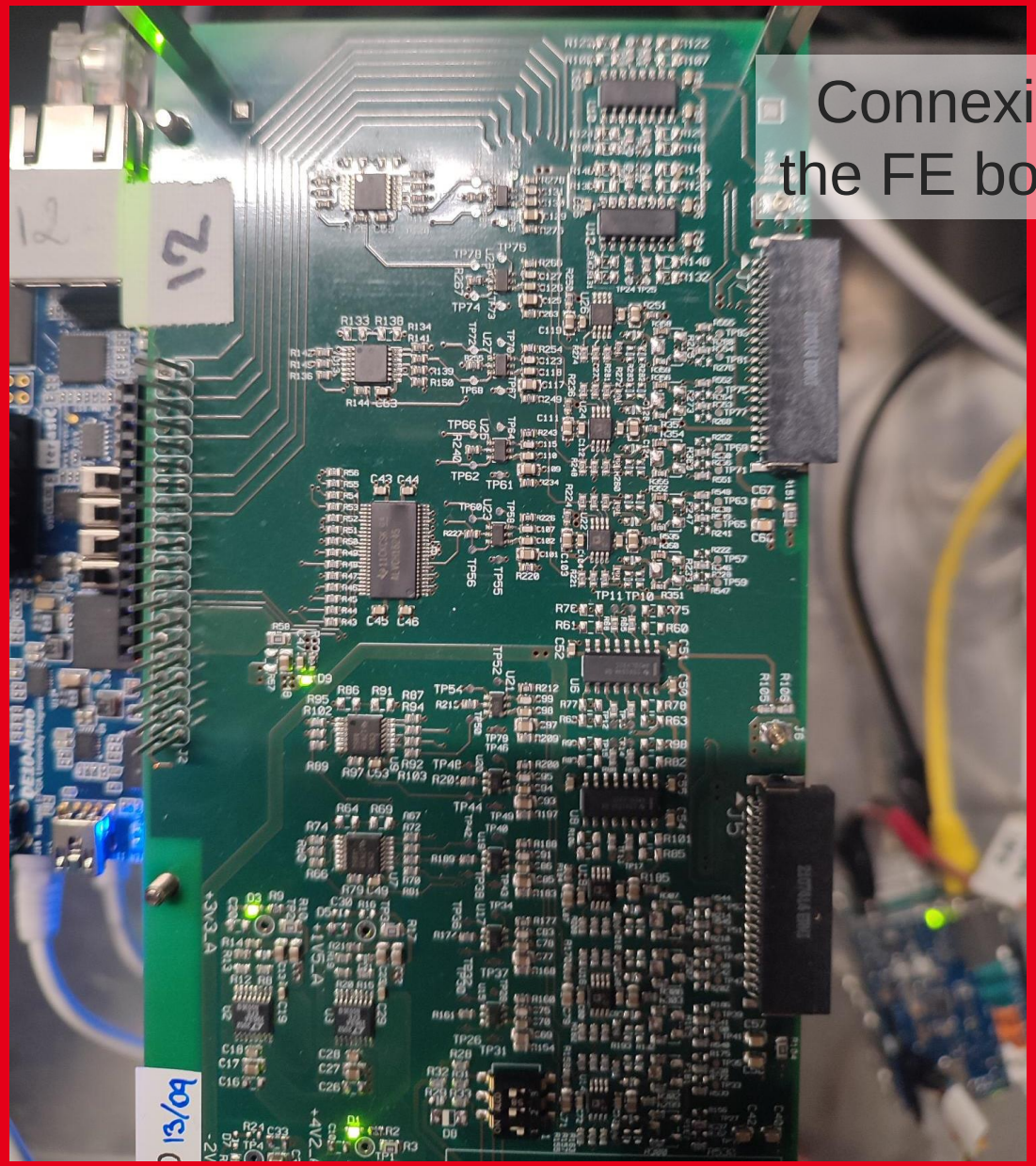
FOOT Detector
640 channels

Close-up



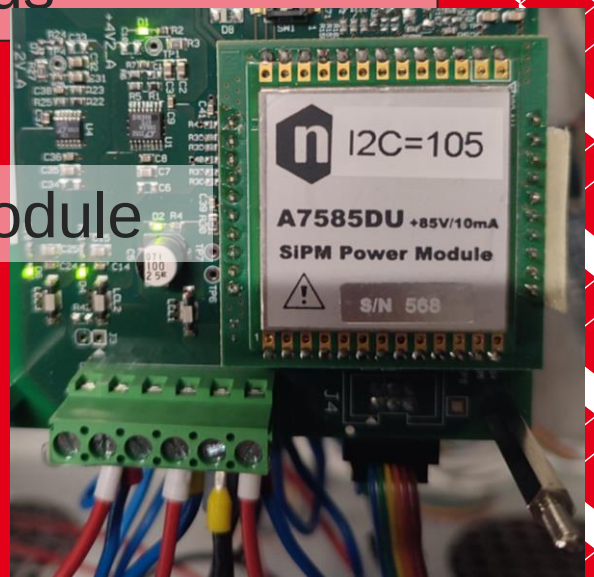
Very limited action in the FE board (low part count

The ADC board (outta vacuum)



Connexion to the FE board x2

Wider board, higher part count :
-exchange in both directions with FE Board
-Generate Digital dataflow
-handle logic signals (trigger, clock)
-Generate Low voltage rails for all components
- Connect to FE and FPGA boards



HV module

2. The FE board

Details, details

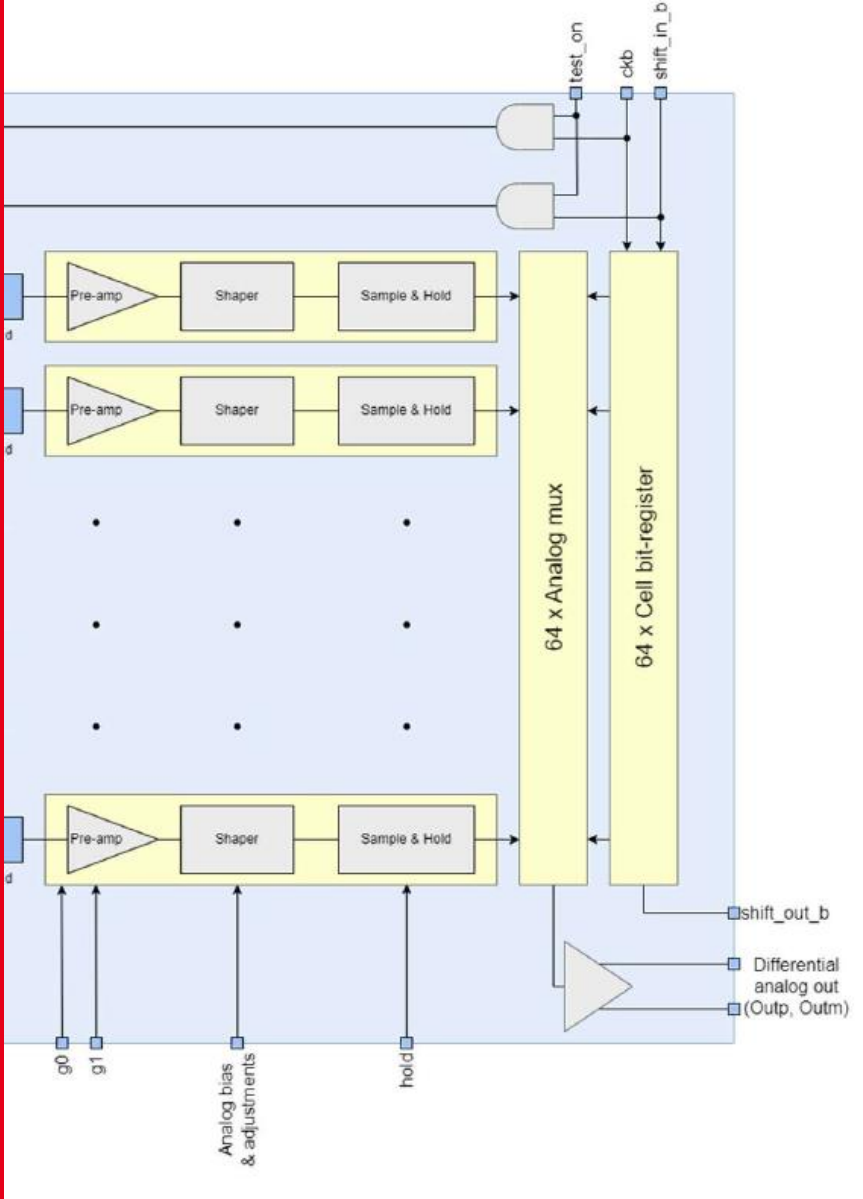
Functionalities

1. Base board for the FOOT detector and IDE1140 ASICs
2. Pipe in some basic functionalities/interfaces from the ADC board : Low Voltages, trigger , delay, clock, reset, HV
3. Pipe out the minimally processed analog dataflow from the VA1140 ASIC to the ADC board
4. Overall very good intention : attach the FE ASIC very close to the detector, no alteration of the ASIC output signal… but .. The devil is in the details .. as often

The IDE1140 ASIC

1. This is a simple but good ASIC
2. Provide the energy information for 64 input channels in a multiplexed way
3. Very decent noise level (6-8 keV threshold in principle)
4. Low power: suitable for vacuum operation
5. No time branch (no time information at all) : a pitty would help a lot to correlate various detector layers
6. Slow energy shaper (8 us peaking time), pile up issues at 10+ kHz rate (would be partially mitigated with a time branch)
7. No zero suppression, the whole 64 channels sequence is read out (not a major issue)

The IDE1140 ASIC



1. Looks like a modernized GASSIPLEX ASIC
2. DC-coupled Charge sentive preamp,
3. Slow shaper (8us peaking time)
4. Track and hold (store peak amplitude)
5. Analog multiplexer
6. All needed interfaces (trigger, delay, readout sequence timing, reset, LVs)
7. 4.5 MeV total dynamic range, 1.5 MeV usable range, non adjustable…

The IDE1140 time sequence

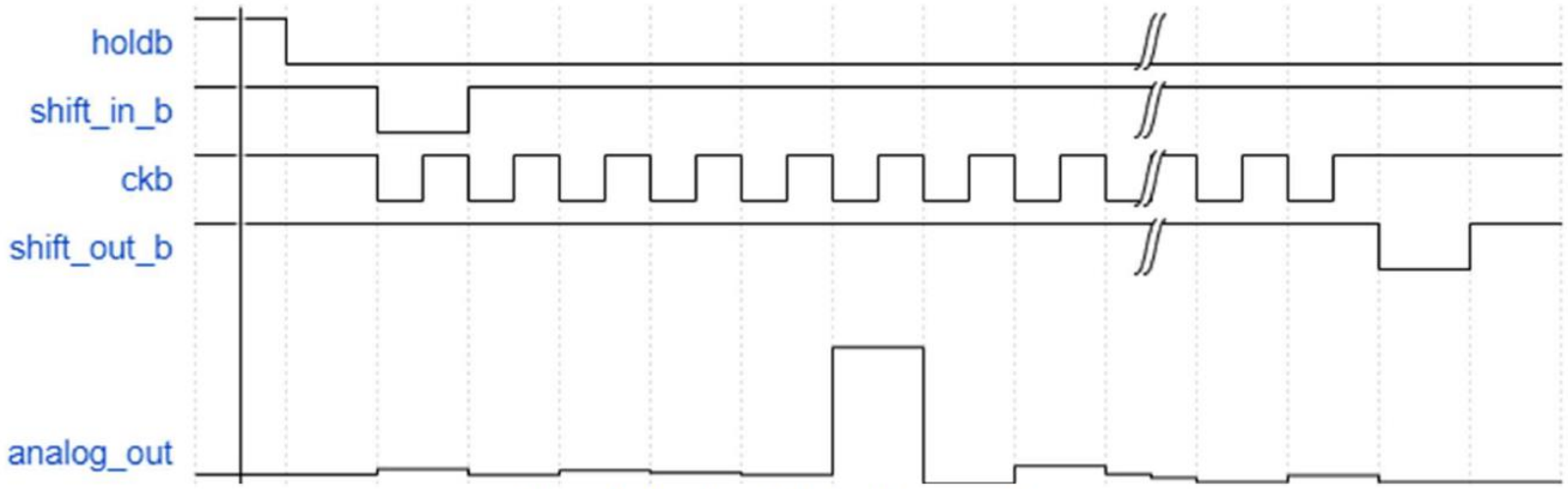


Figure 4: Read-out timing for one chip.

1. **The Hold signal freezes the energy signal**
2. **The readout sequence is started by « shift_in »**
3. **And clocked by the … clock signal (few MHz)**
4. **Each plateau correspond to one detector channel**
5. **The whole 64 channel readout sequence starts**
6. **ASIC reset**

The IDE1140 operation

1. The 10 ASICs should be read in parallele
2. The duration of the readout sequence should be of 15 to 20 us
3. 8 us « waiting » (peaking time) to be added
4. Charge injection capability (testing, calibration purposes)
5. The ASIC pipe out a differential current signal
6. The multiplexed output signal needs to be converted to a voltage signal to be transported and converted into digital information
7. The IDE1140 manual requests the implementation of a current to voltage converter (transimpedance amplifier) at the ASIC output

The IDE1140 integration into the FE board

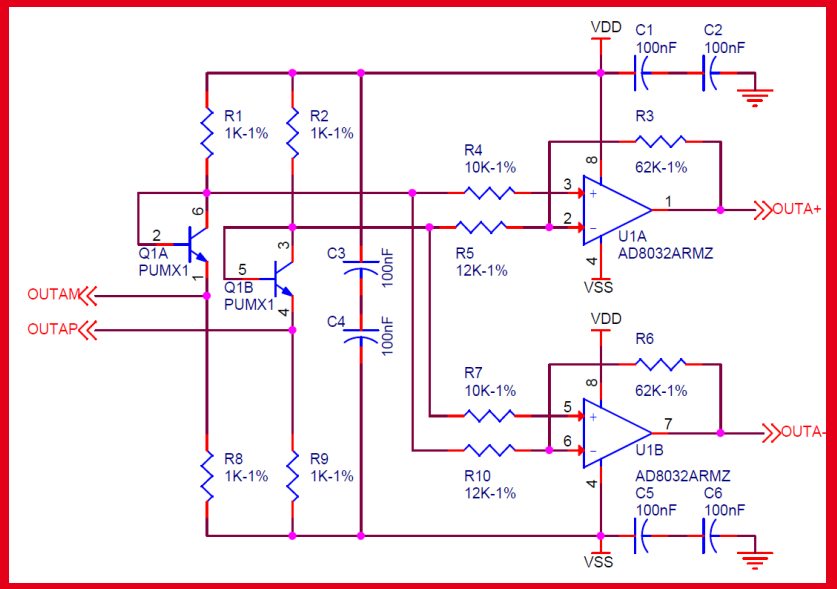
1. **The IDE1140 is a mixed analog/ digital ASIC**
2. **Always complicated to handle**
3. **The digital signal commutation lead to a strong current request**
4. **This should not affect te analog circuitry**
5. **We should make sure that we have separated low voltage rails**
6. **The IDE1140 pinout request the LV separation**

dvdd	p	digital VDD	+1.5 V
dvss	p	digital VSS	-2 V
avss	p	Analog VSS (+ chip backplane). 2 pads.	-2 V
avdd	p	Anaolg vdd	+1.5 V

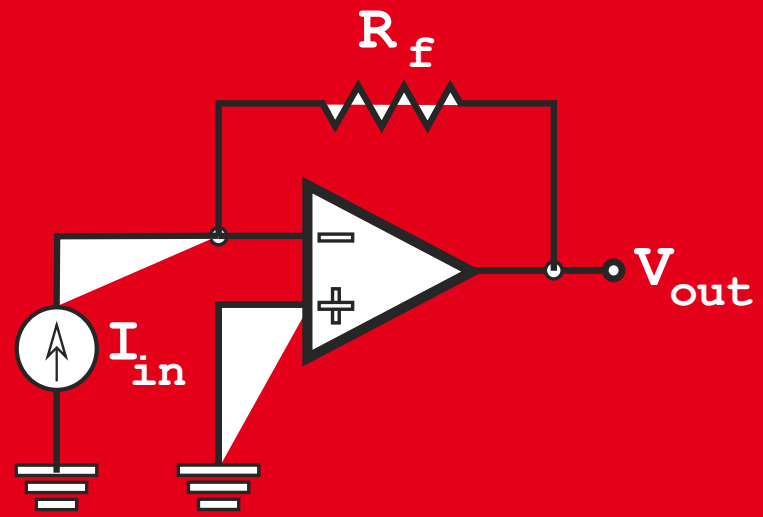
7. **The attempt to separate the LV in our FE board leads to LV shifts with rate**

The IDE1140 integration into the FE board

1. **The current to voltage conversion is the only real functionnality of the board**



1. **Does not follow the requested circuit topology**
2. **Put some burden on the ASIC output circuitry**
3. **Affect the noise level**
4. **Very minimal Low Voltage stabilization : 50 nF on 1 rail, affects operation at increased rate. These caps are stored energy used when the amp operates ... Crucial**



3. The ADC board

less details

The ADC board

1. **The logic signal distribution for all 10 ASICS is made there : shift, clock, reset,**
2. **Some level shifting, connection to the FPGA**
3. **The ADCs are there**
4. **The low voltage rails are generated (+2V -1V5) for the FE card thanks to linear regulators**

   Again, one unique positive and negative rail for digital and analog purposes
5. **Similar issues with very limited LV decoupling and filtering on active components. Too few and too small cpacitors**

The HV supply in the ADC board

1. The FOOT HV is not provided to the board, it’s generated there
2. A 12V input is used to generate the HV (<85V) using a CAEN 7585DU
3. This is a switching power supply that we introduce into a sensitive ADC board
4. Leakage current monitoring of limited accuracy
5. Max voltage limits the use to 100um thick silicon detectors
6. Strange choice ? Why not go for an additional LEMO/BNC input

3. Proposal for an upgrade

2 phase approach

Phase 1 : minimum change

1. **Keep the changes as limited as possible**
   Reduce the risk of mishaps
2. **Redesign the FE Board**
   Full redesign (not much there)
   LV stabilisation,
   IDE1140 output amplifier
3. **Marginal modification of the ADC board**
   New low voltage distribution strategy (separate analog from digital rails)
   Improve LV stabilisation
   Remove the HV module
4. **Open question**
   Keep the local ADC or go for an external ADC solution (FEBEX for instance)
   I tend to favor minimum change option (keep the current ADC), but debatable
   K. Koch suggest to go for FEBEX

Phase 1 : expected improvements

1. **Better baseline stabilisation**
   Stable operation at higher rate, 10 kHz
2. **Lower noise level**
   Better energy resolution
3. **Higher efficiency for the detection of high energy protons**
   90+% efficiency at 4 sigmas should be feasible
   50+% detection efficiency for the detection of 2 protons is reasonnable
4. **Still limitation**
   No timing information : we grab everything that comes within 8 us : no selectivity
   Pile up possible at high rate
   Long readout time .. Rate limitation still present
5. **Time line**
   Depends on the ADC option (internal vs external)
   Fast route : 6 months to 1 year to get both boards
   Might require a second iteration (shit happens)

Phase 2 : full refurbishement

1. **More drastic changes**

   No more IDE1140 ASIC

2. **A commercial VMM3 based ASICs**

   Simplified version suitable for Silicon strip detector

3. **Lots of expected improvements**

   Shorter shaping time, zero suppression, more suitable gain, timing

4. **High resolution timing**

   A dedicated timing branch should provide a sub 1ns hit time resolution. Removal of many delta electrons and allows for the hit correlation between various layers

5. **2 year horizon**

   Higher failure risk, no pain no gain. Support needed on the DAQ side for the integration into the R3B ecosystem

6. **Should be discussed in the light of the progress of the ALPIDE tracker**

   Will not replace a pixel based tracker but should provide a very strong improvement w/r to the current and short-term options