Characterisation of ToASt ASIC

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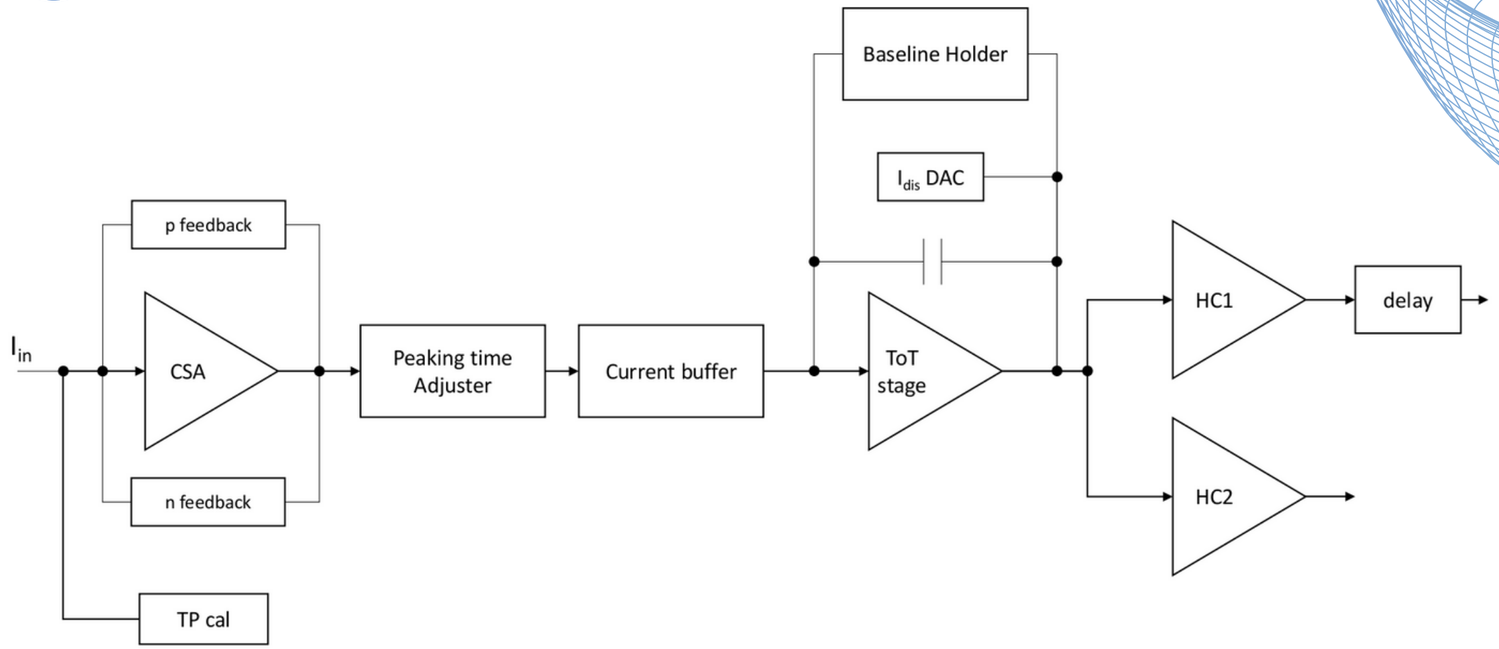
ToASt main characteristics

- 64 input channels
- Time of Arrival (ToA) and Time over Threshold (ToT) measurements
- Master clock frequency: 160 MHz
- Region: groups of 8 channels with local FIFO
- Second level FIFO buffering for the 8 regions
- Two output serial links at 160 Mb/s
- Serial configuration protocol at 80 Mb/s
- Full SEU protection via Triple Modular Redundancy
- CMOS 0.11 μm technology

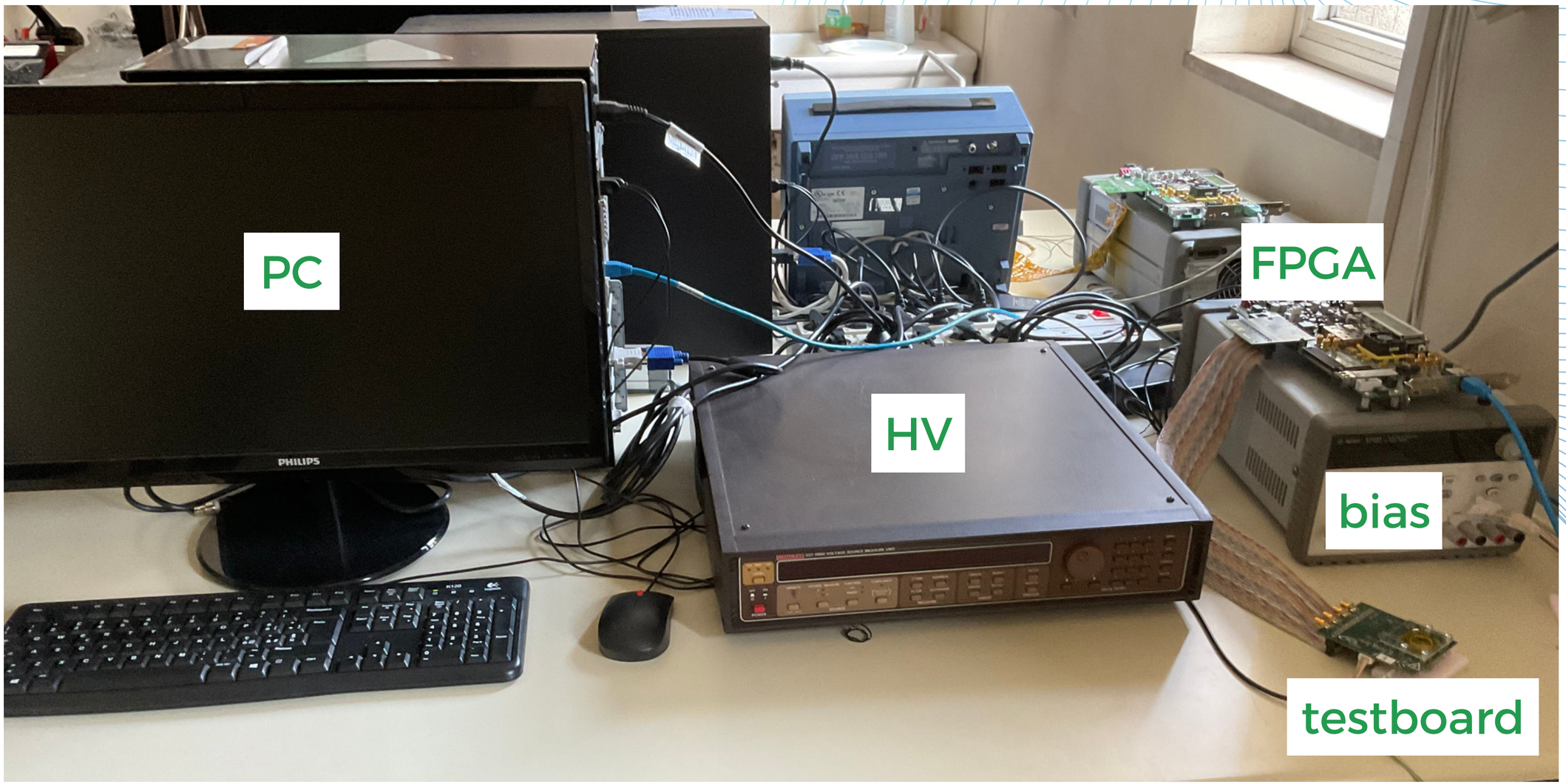
Analog channel



- CSA with selectable input signal polarity, gain ≈ 5 mV/fC
- Shaper with adjustable peaking time
- Current buffer
- Test pulse injection via integrated capacitor

- ToT stage with programmable discharge current
- Two comparators with independent thresholds
- Local DACs for threshold and discharge current fine tuning

Setup



Boards

6 BOARDS IN TOTAL

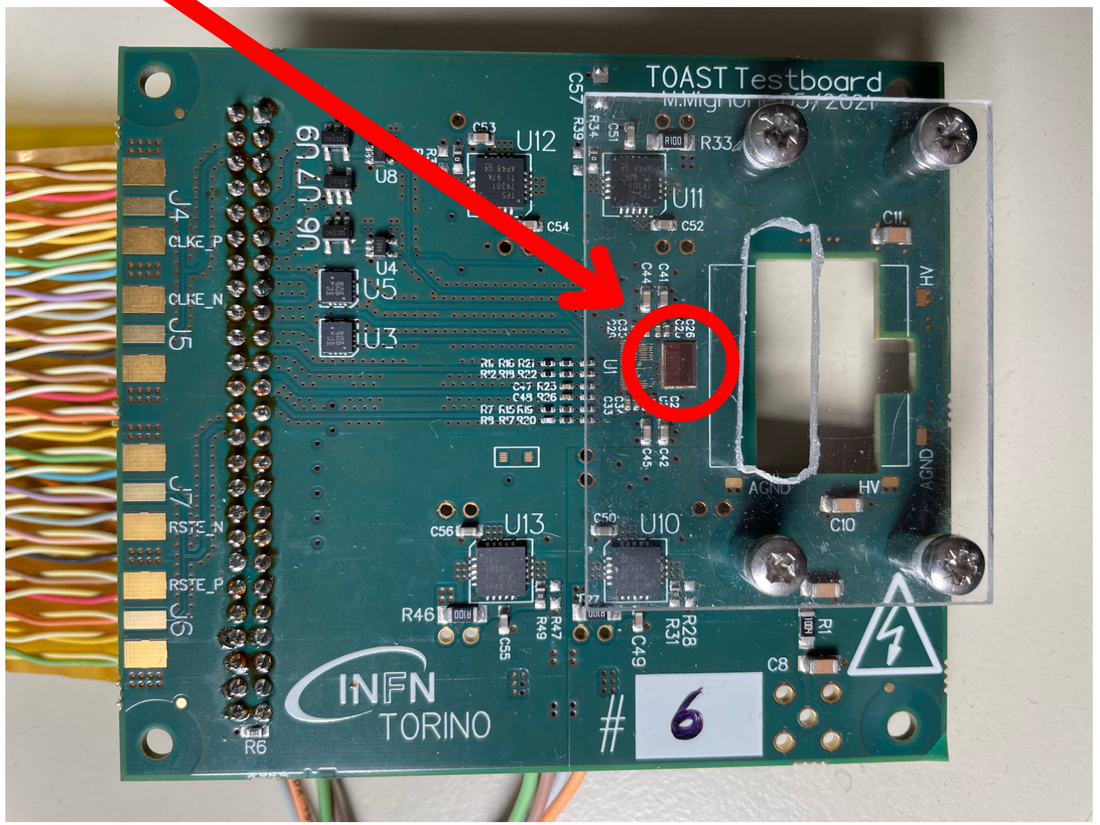
TURIN

- board 1 ⟶ S3 sensor
- board 4 ⟶ FBK sensor
- board 6 ⟶ without sensor

GERMANY

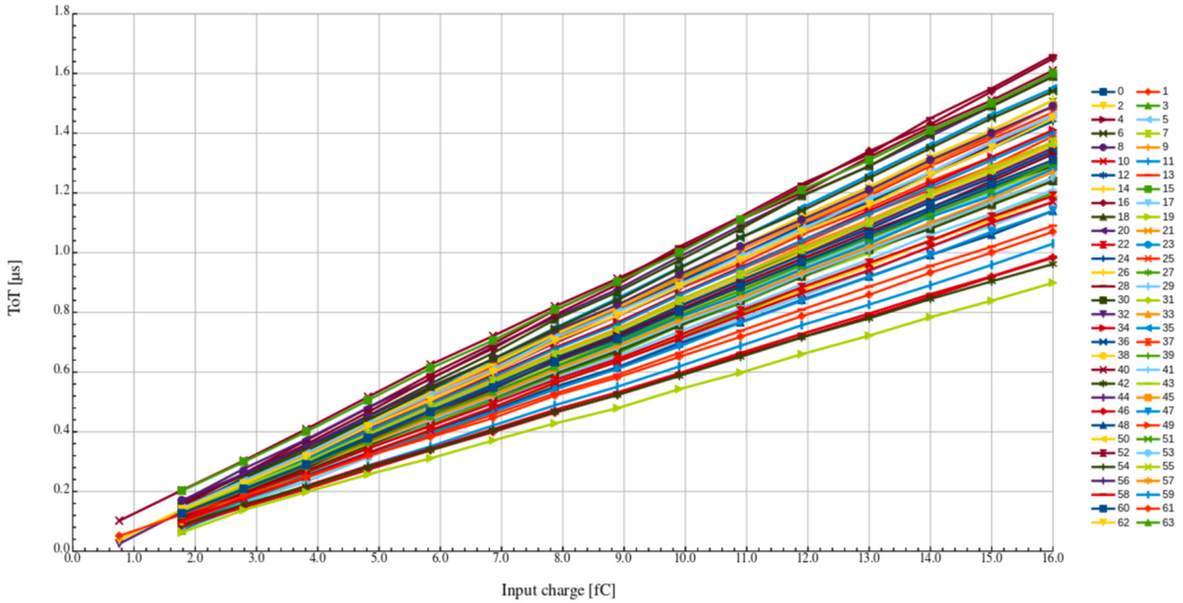
- board 2 ⟶ S4 sensor
- board 3 ⟶ without sensor
- board 5 ⟶ S4 sensor

ToASt



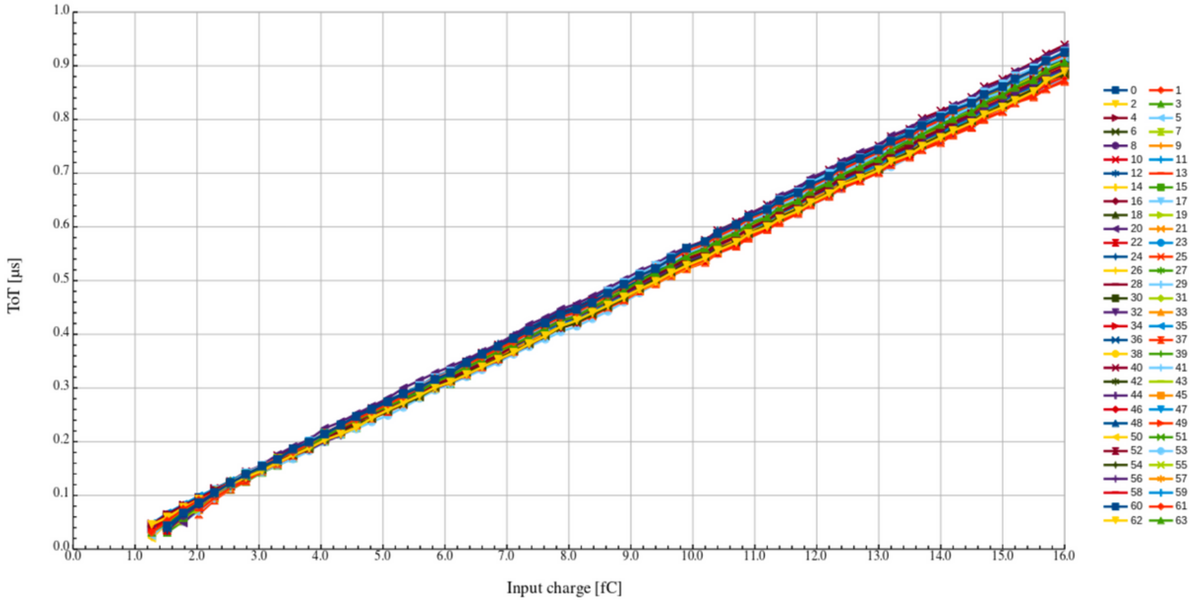
Measurement - transfer function

BEFORE CALIBRATION



- Fairly large gain spread
- Channel level gain calibration implemented - gain spread reduce from 12% to 1.7%
- ToT REFERENCE GAIN
  - **p-type: 55 ns/fC**
  - **n-type: 60 ns/fC**

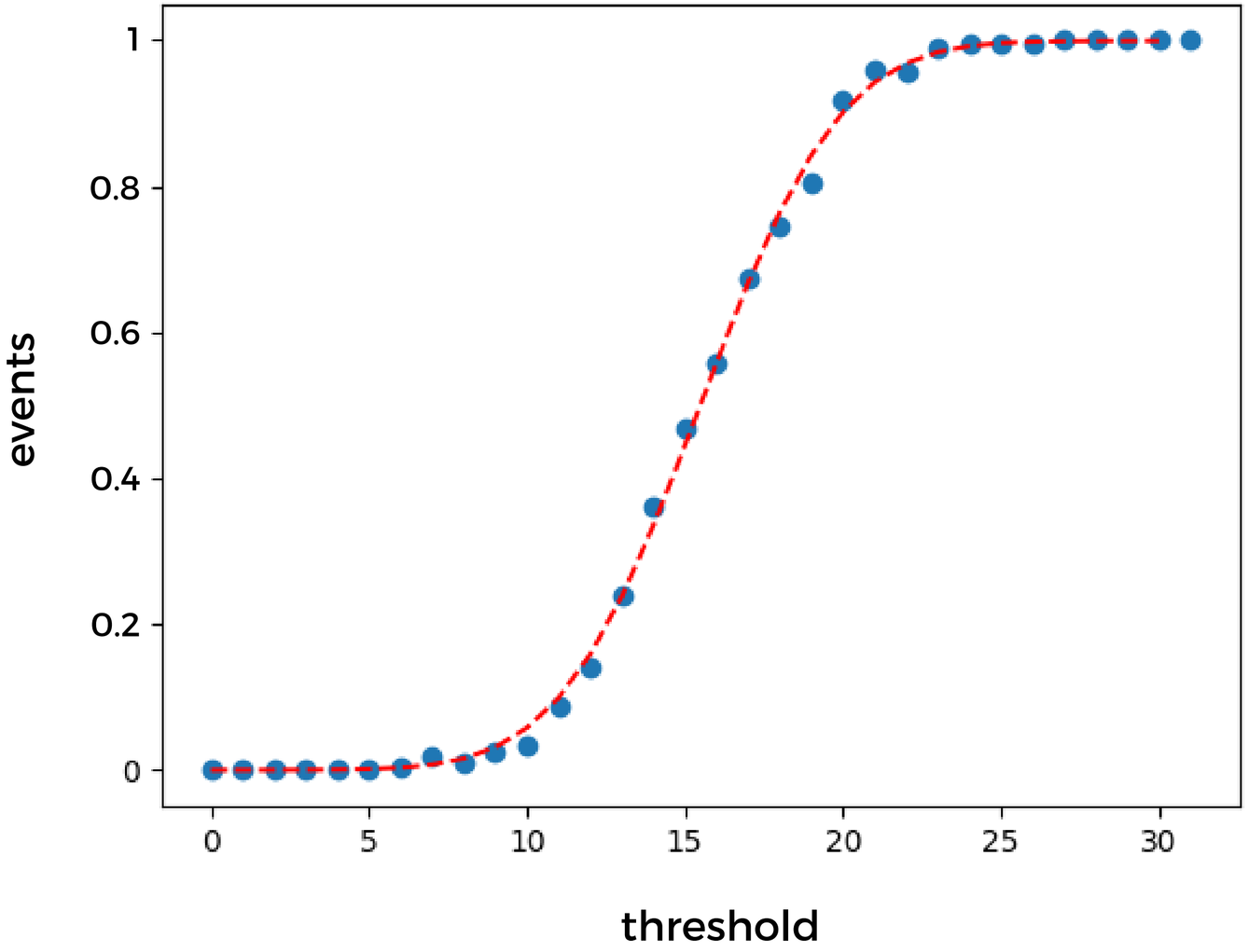
AFTER CALIBRATION



Calibration procedure :

- For each channel, measure the transfer curve for each channel ToT Ibias DAC value
- Select a reference gain
- For each channel, select the DAC value providing the gain closest to the reference

Measurement - noise



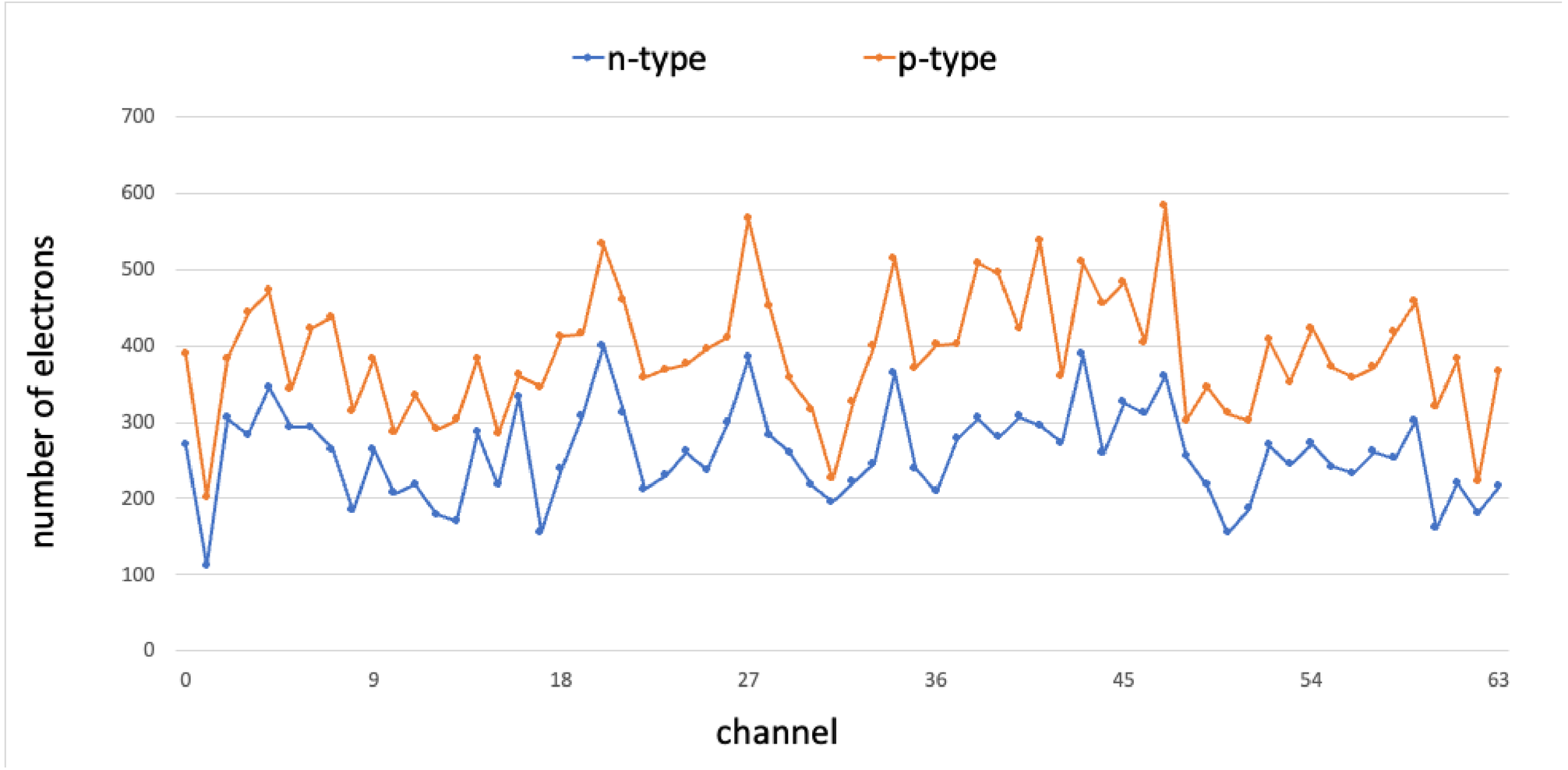
Scan performed with a fixed number of pulses (500) and changing the threshold.

$$f(x') = \frac{N}{2}\left(1 + \frac{2}{\sigma\sqrt{\pi}}\int_0^{x'} exp(-s^2)\, dx\right)$$

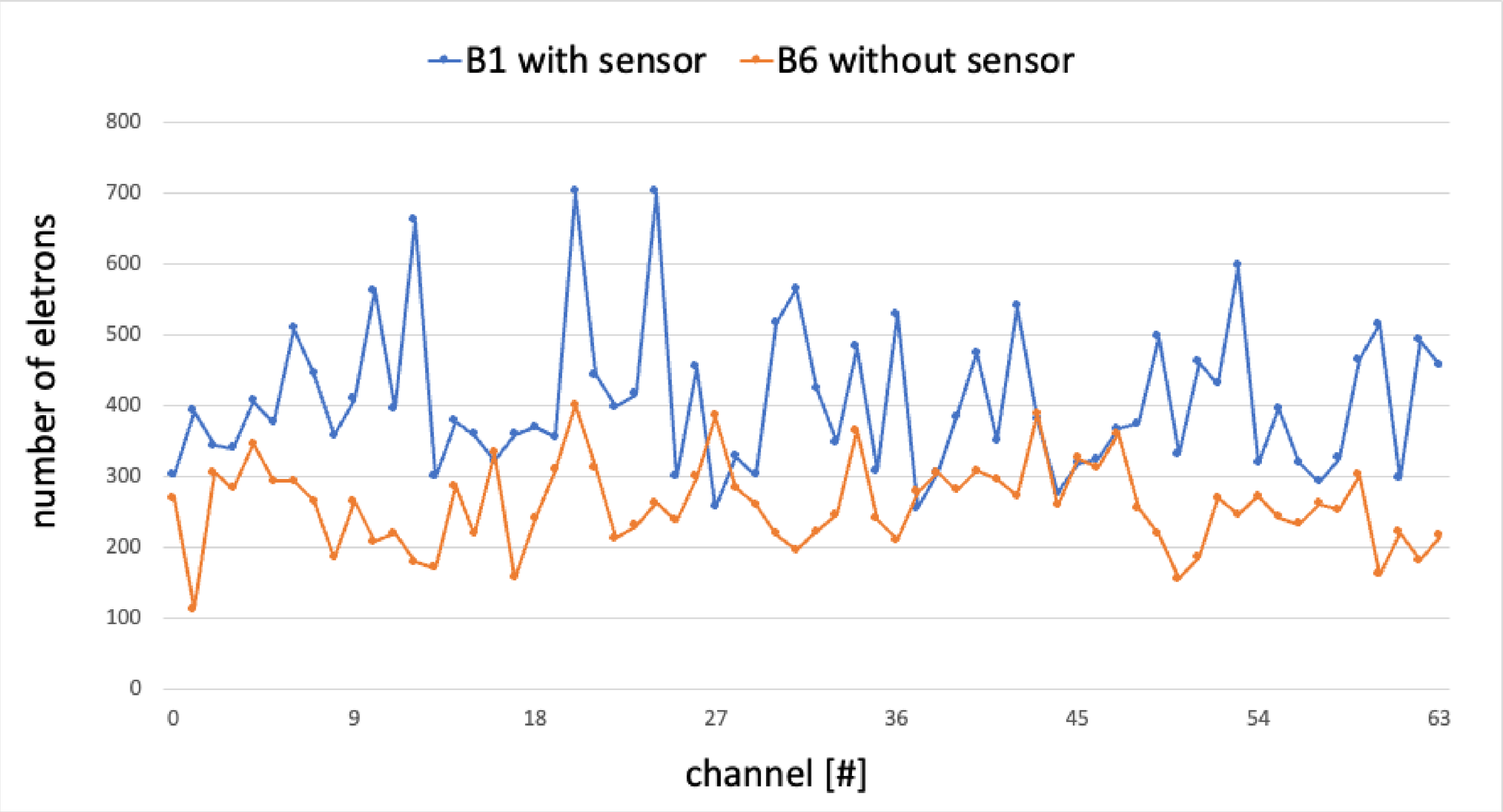
$$s = \frac{x - \mu}{\sigma}$$

Measurement - noise

COMPARED POLARITIES OF BOARD 6 (without sensor)

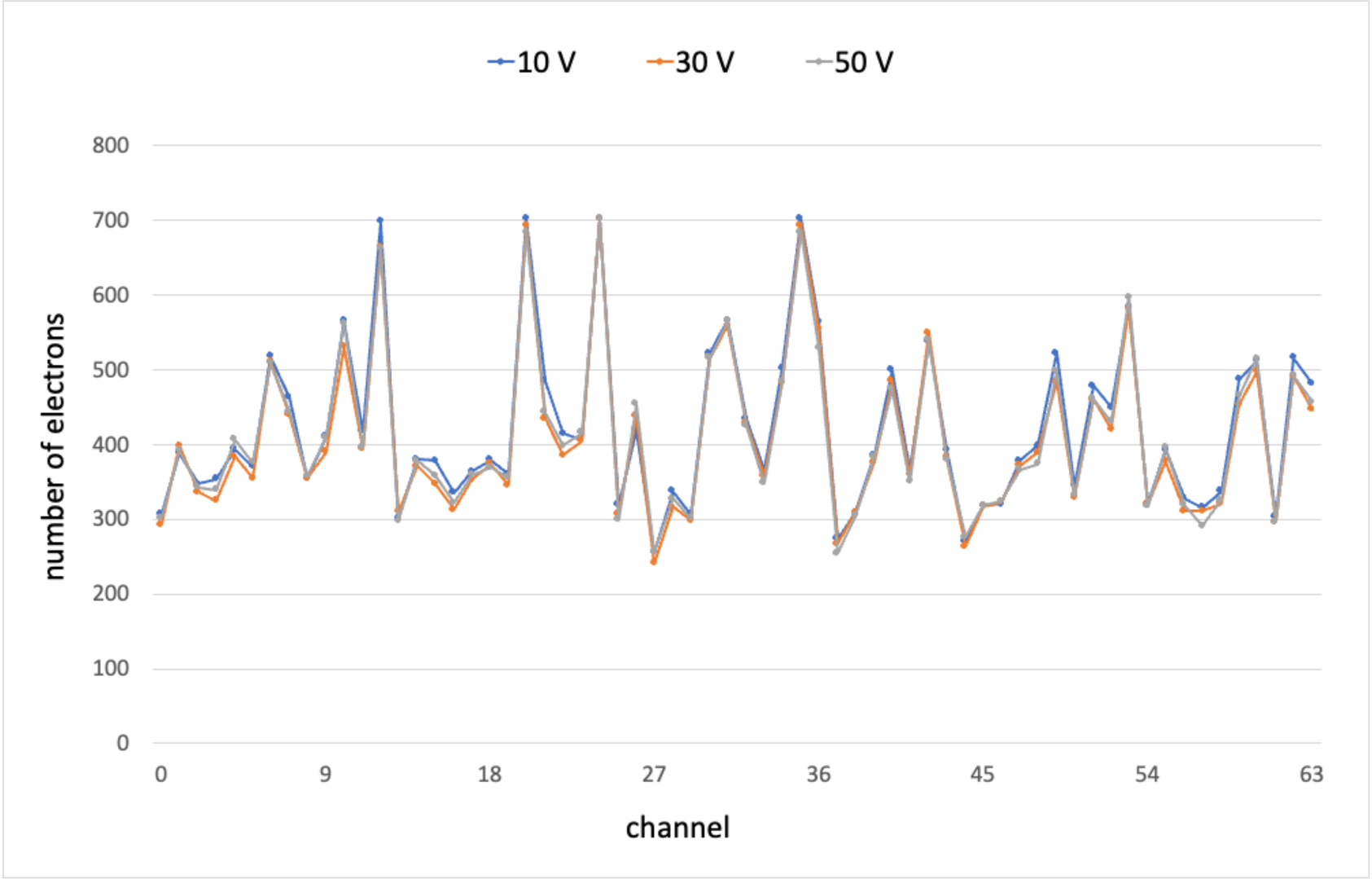


Measurement - noise



strip lenght ≈ 20 mm

Measurement - noise with different Vbias



Conclusions

ToASt:

- A 64 channel ASIC, designed for the readout of the solicon strip detectors of the PANDA MicroVertex Detector
- Each channel provides particle Time of Arrival (ToA) and energy deposited informations (via ToT)
- Is designed in a commercial CMOS 0.11 μm technology

6 BOARDS AVAILABLE:

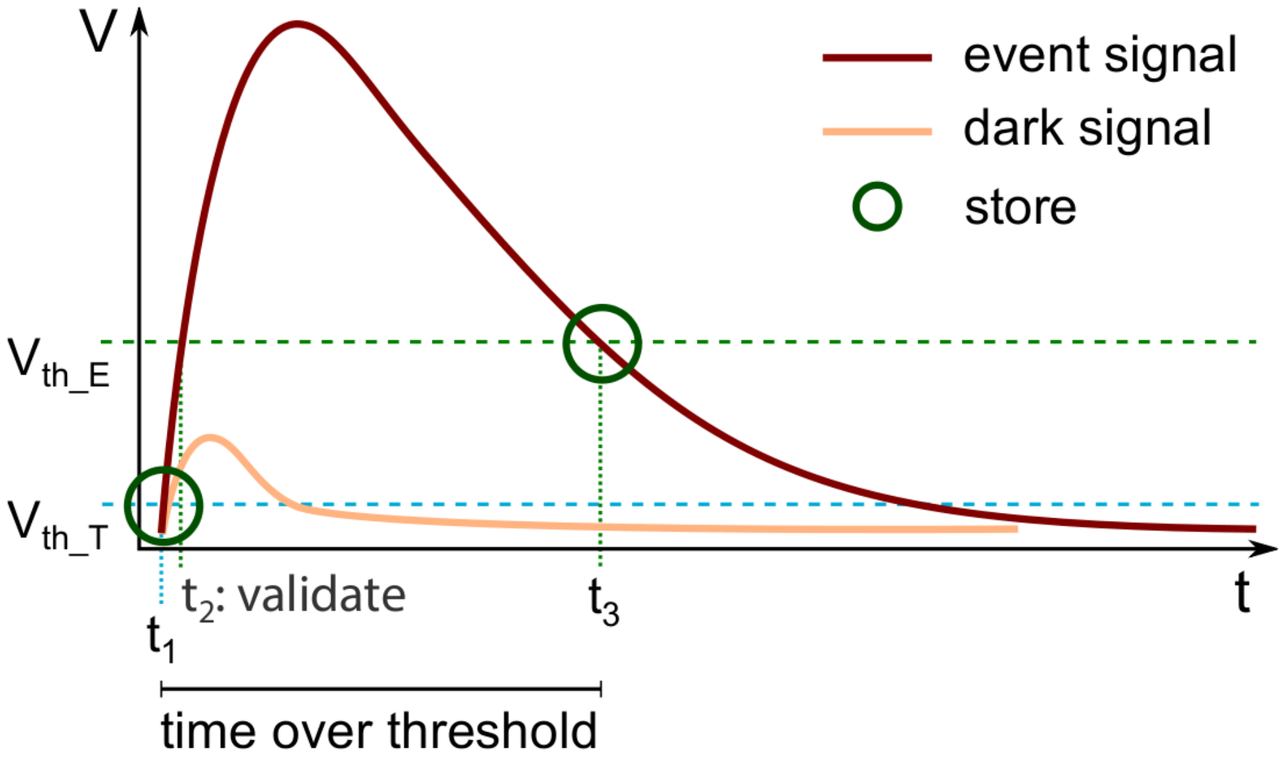
- 3 in Turin
- 3 in Germany

TEST made on ToASt:

- electrically performances
- calibration procedure
- noise performances
- in future will be characterised for radiation tolerance

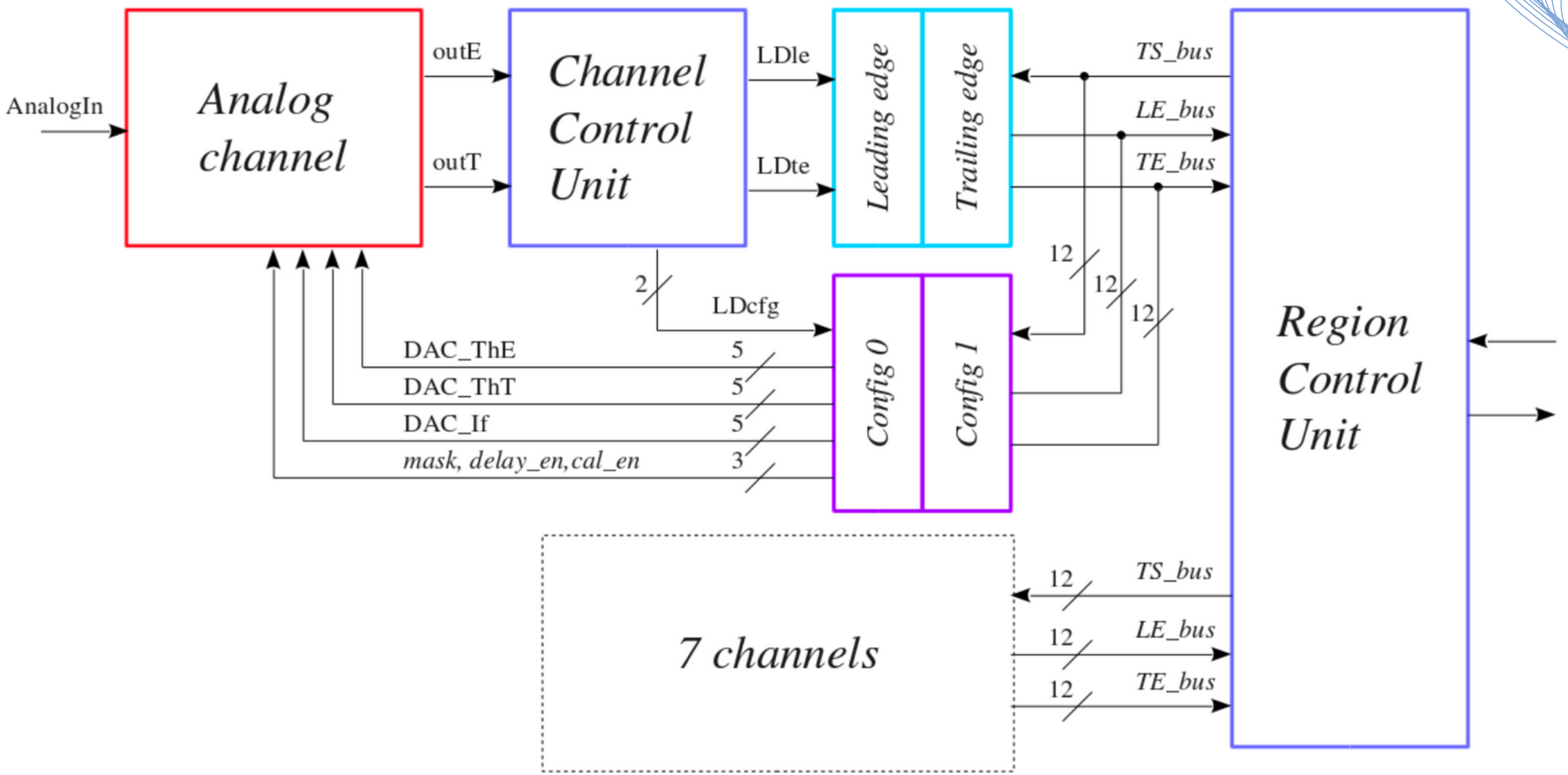
BACKUP SLIDES

Time measurements



- Two thresholds : V_thT and V_thE
- Time measurement on V_thT to minimize jitter
- Data validated on V_thE to minimize noise hits
- ToT = t_3 -t_1
- Double threshold validation can be disabled

ToASt channel schematic



- Common time reference : 12 bits time stamp distributed to all channels
- Time stamp are Gray-encoded
- LE and TE registers latch time stamp at comparator rising/falling edges

ToASt architecture