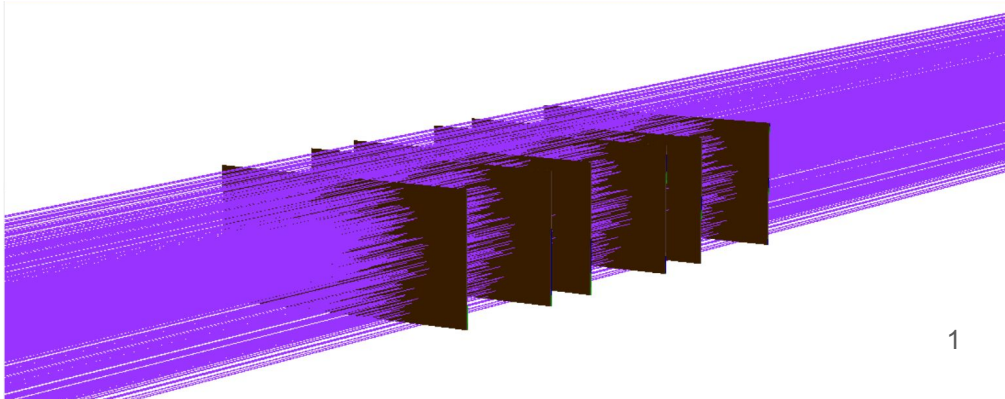
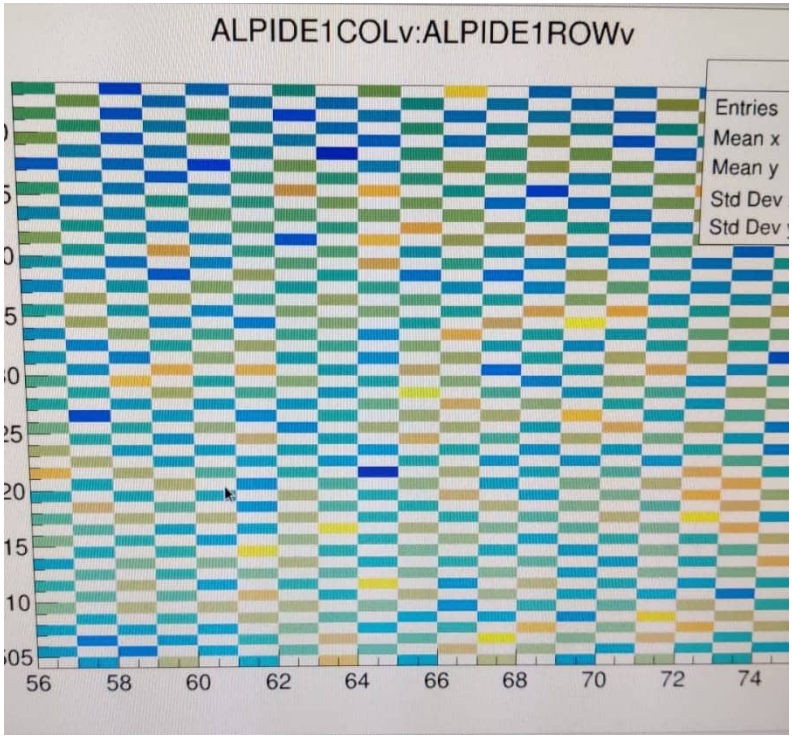
ALPIDE DAQ development and the analysis of the 2022 CERN data

By Luke Rose
Date: 24/05/2023



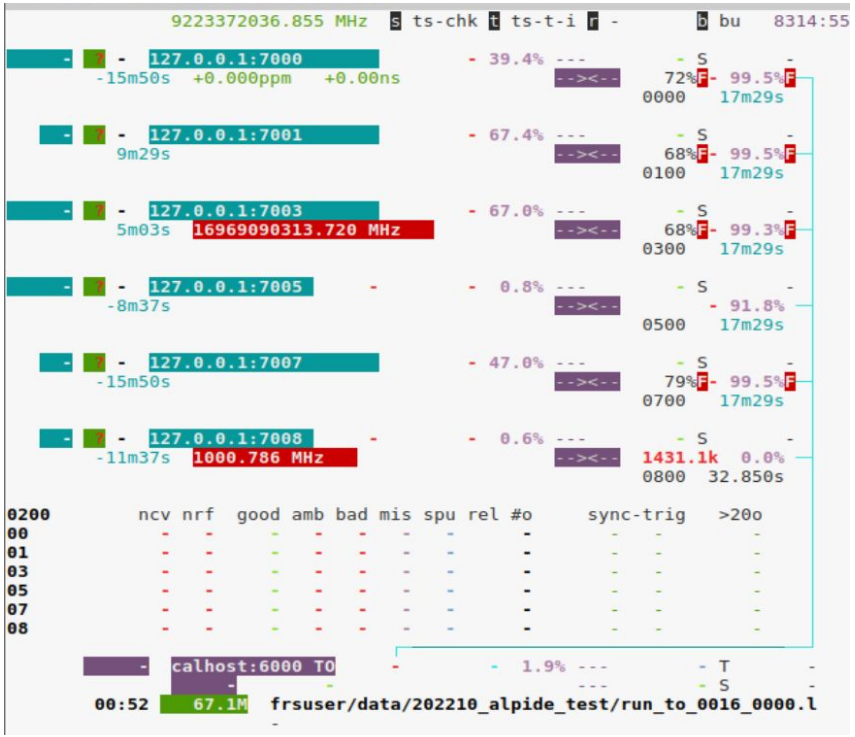
Status 2022

1st hurdle



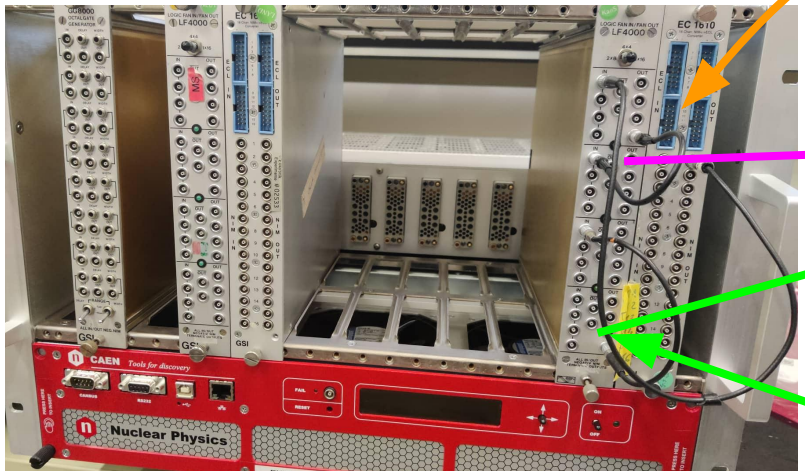
Mapping borked

2nd hurdle



Time sync borked (frequency ratio of the CPU clock vs the received timestamps = 18Phz at max)

Initial Daq Setup



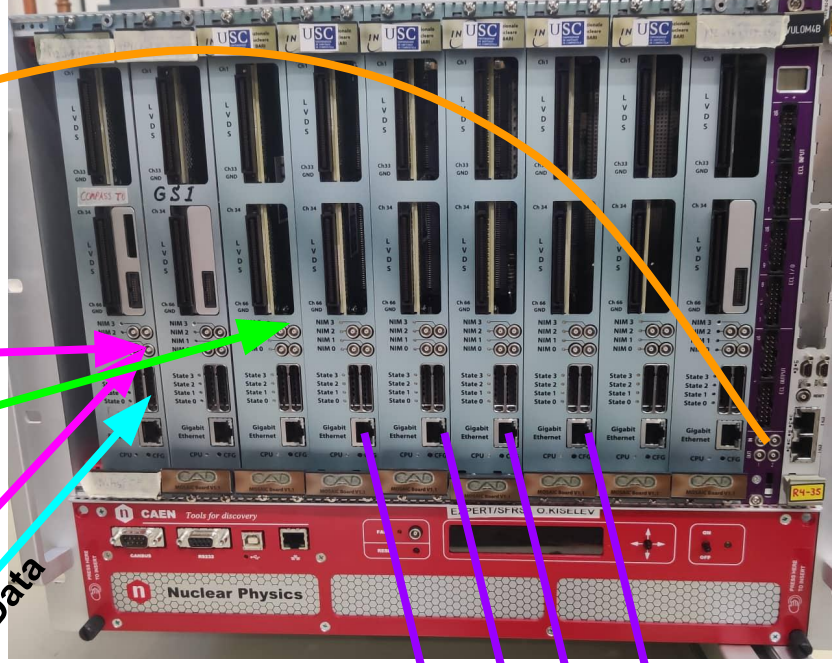
Pulsar

Trg

Trg

Data

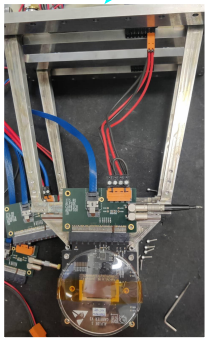
Clock



Data

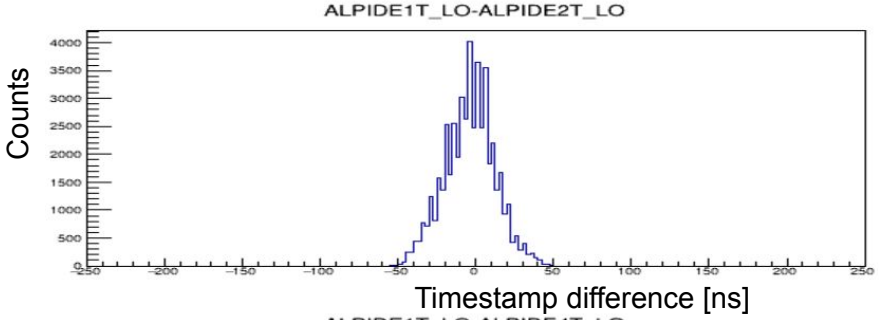
Data

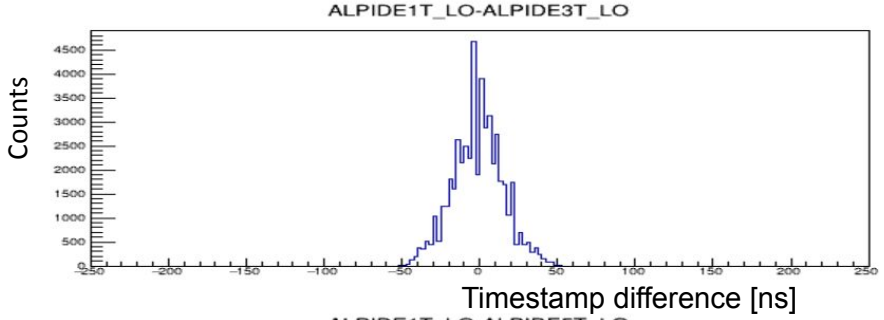
Data

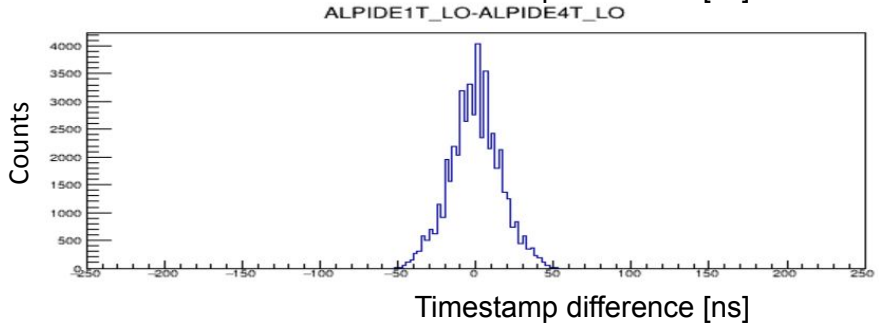


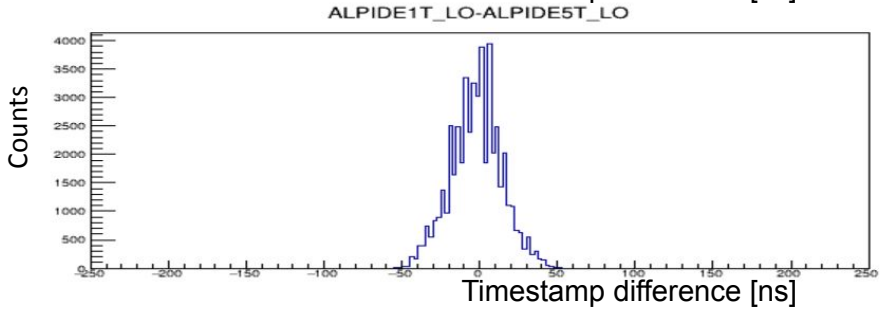
- Rio4 ->VME controller configers pulser.
- VULOMB 4B->Generate Pulse trigger signal.
- EXPLODER->Timestamping WR.
- ECL to NIM convertor
- FiFo->Distributes trigger and TS to mosaics.

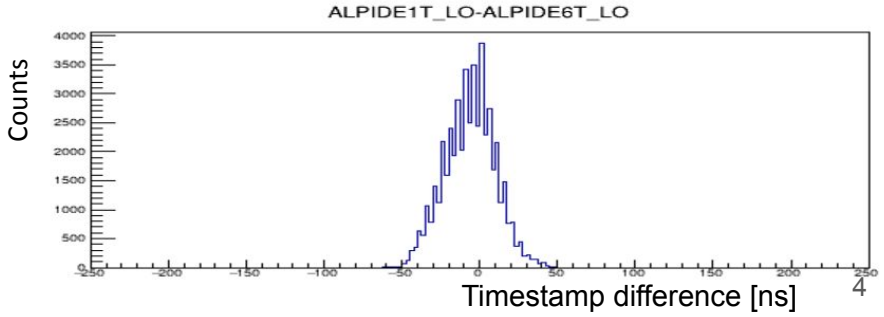
Analysis 2022 -Timestamp diff between FPGA





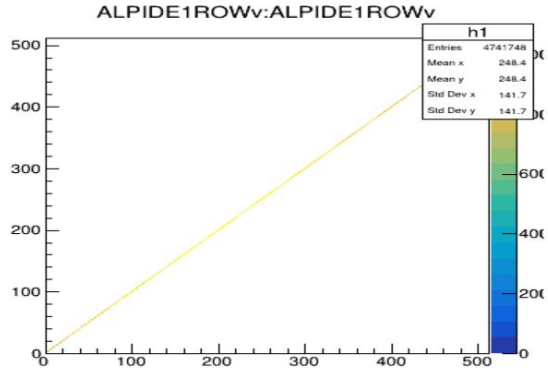


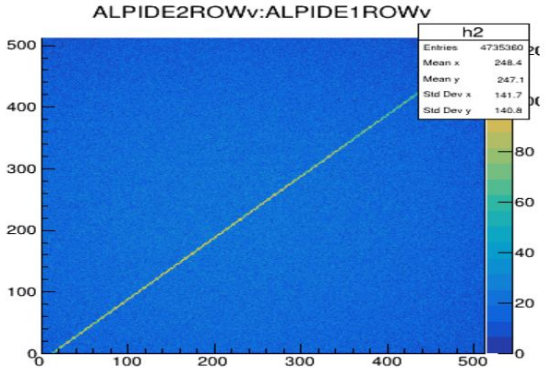


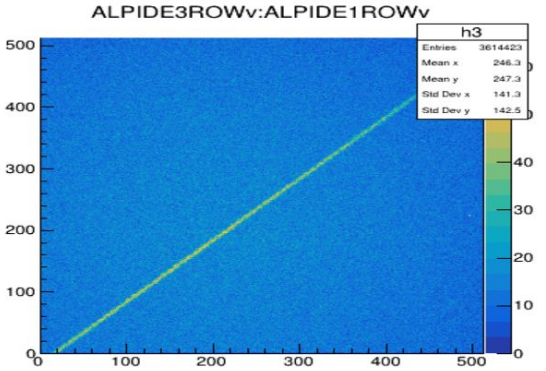


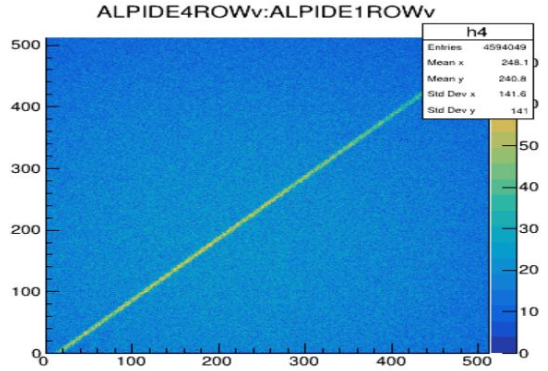
sigma=5.6893ns.
mean=-3.08081 ns

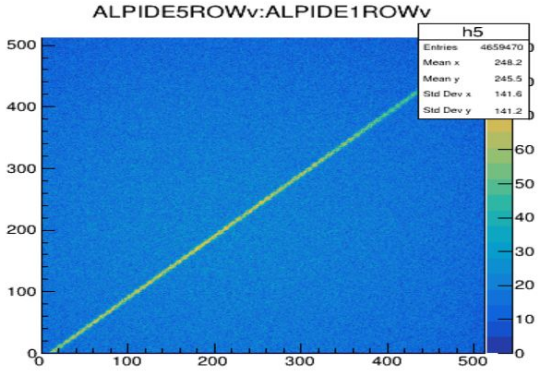
Analysis 2022 - Mapped level hits Row v Row

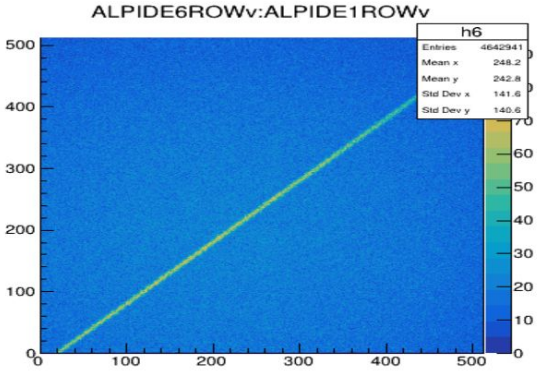




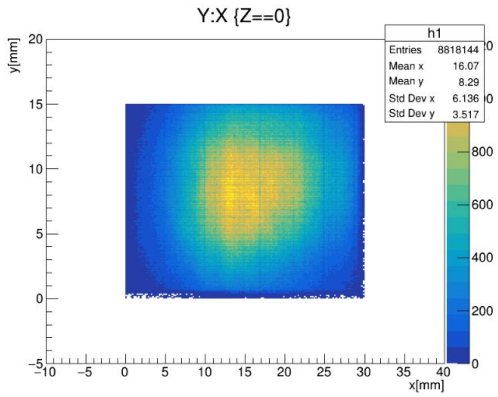


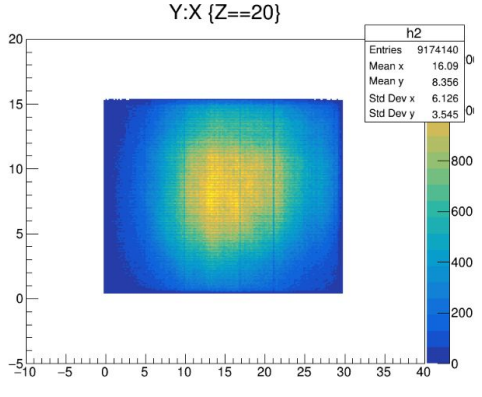


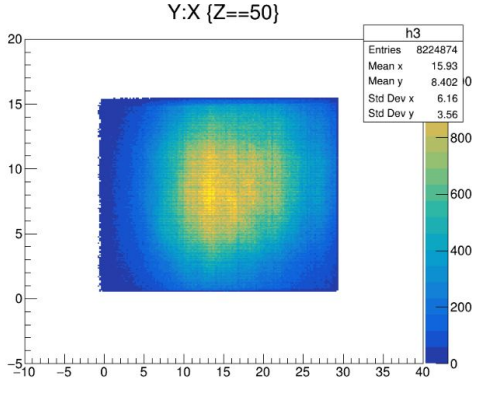


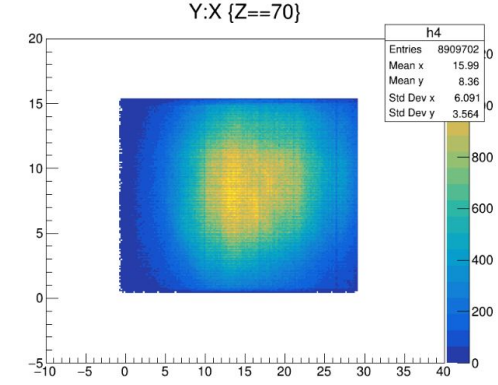


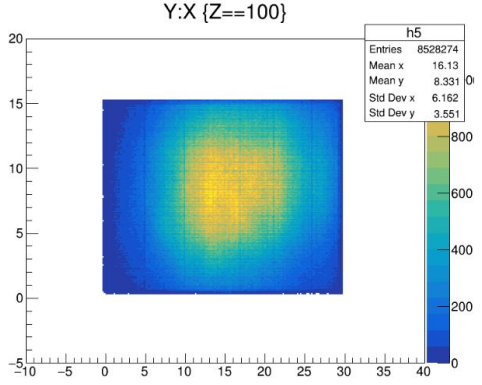
Analysis 2022 - Row v Col

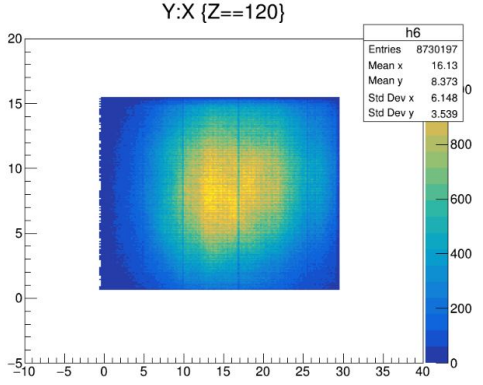




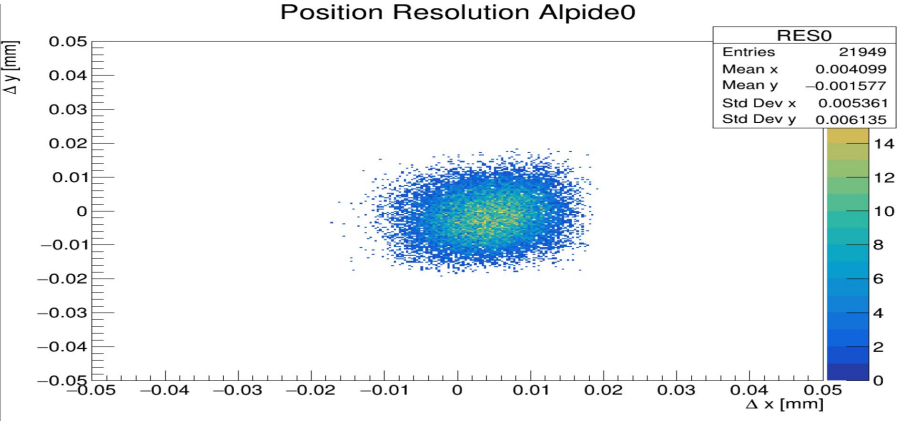


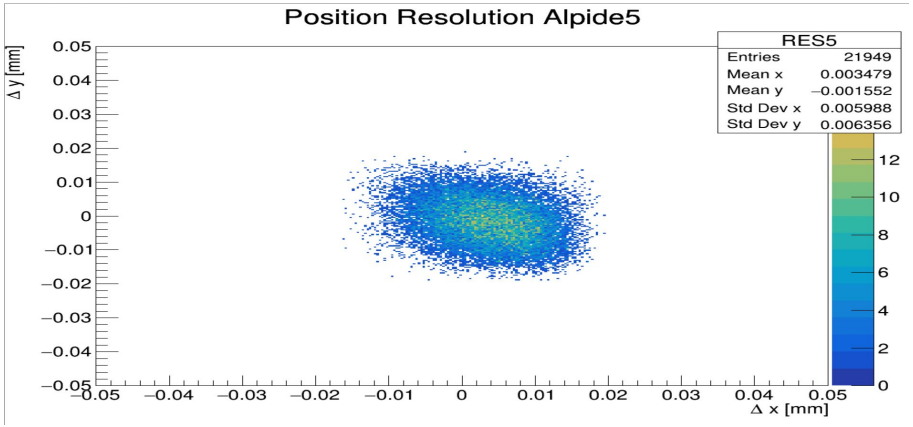


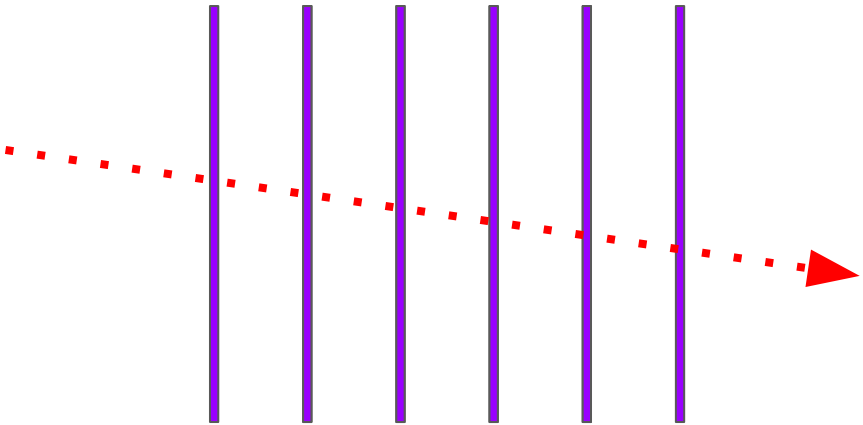


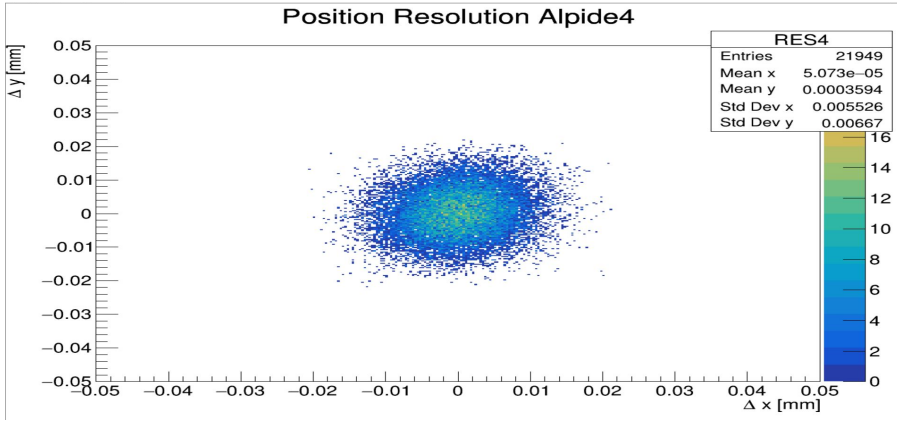


Analysis 2022 -Tracking resolution









Timestamping Issues (CERN 2022)

- Problem of time synchronisation with a foreign DAQ that doesn't run a WR protocol
- Rataclock - source of Heimtime pulses => foreign DAQ needs to stamp the ticks, decoding done offline
- If rataclock doesn't serve WR but it's own internal clock counter, then local DAQ **also** must stamp the ticks
- Correlation hence done "crudely" on trigger pattern matching
    - https://github.com/kLayz3/AMBER-ALPIDE-2022-Correlator

Timestamping Issues (II)

- Events sometimes get trivially fragmented:
  - Red color -> one event
  - Blue color -> another event

```
Event      9527074 Type/Subtype  10    1 Size     1208 Trigger  1
 00000800 03e1a2be 04e16a59 05e13554 06e10005
 00000500 03e1a2bf 04e16a59 05e13554 06e10005
 00000700 03e1a2c2 04e16a59 05e13554 06e10005
 00000100 03e1a2c9 04e16a59 05e13554 06e10005
 00000000 03e1a2d2 04e16a59 05e13554 06e10005
 00000300 03e1a2d3 04e16a59 05e13554 06e10005
Event      9527080 Type/Subtype  10    1 Size      208 Trigger  1
 00010300 03e10d33 04e16c5c 05e13554 06e10005
Event      9527081 Type/Subtype  10    1 Size     1008 Trigger  1
 00000000 03e10d23 04e16c5c 05e13554 06e10005
 00000800 03e10d2b 04e16c5c 05e13554 06e10005
 00000500 03e10d2e 04e16c5c 05e13554 06e10005
 00000100 03e10d3b 04e16c5c 05e13554 06e10005
 00000700 03e10d3f 04e16c5c 05e13554 06e1000
```

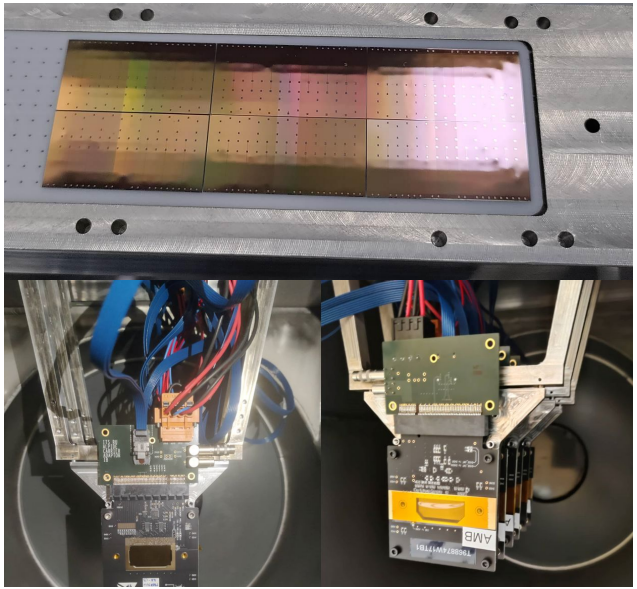
- … and sometimes it is completely scrambled:

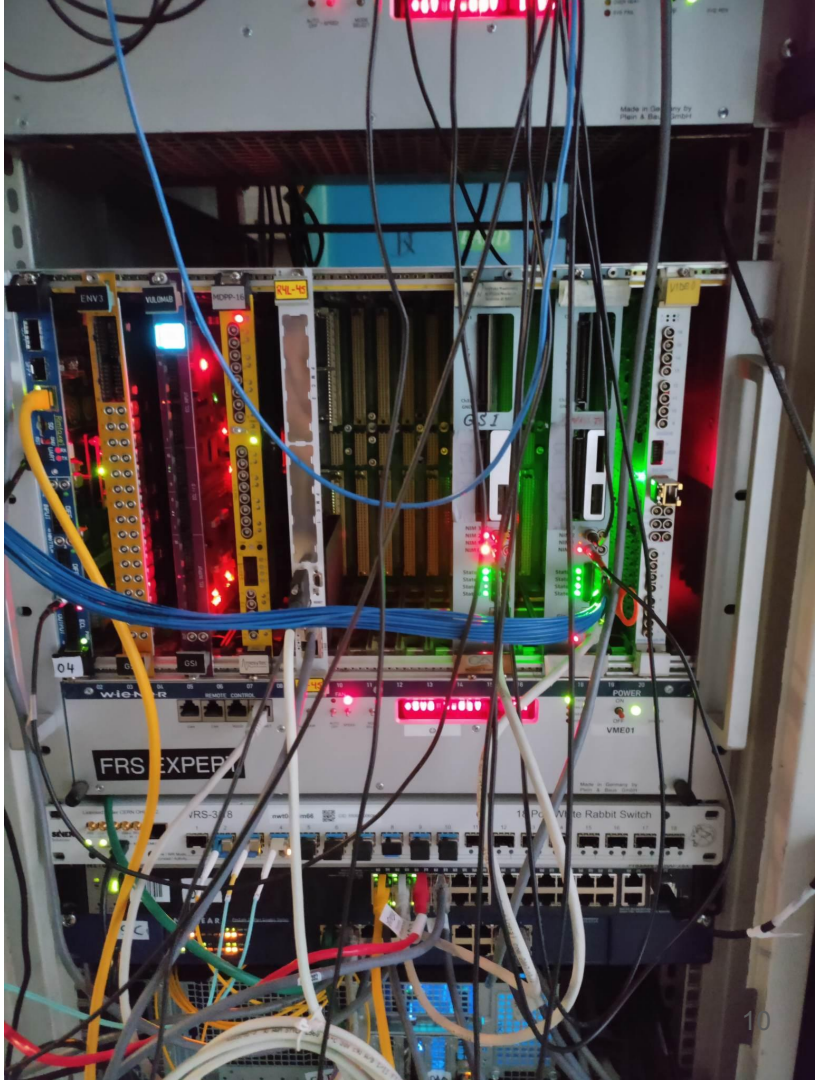
```
Event      9525754 Type/Subtype  10    1 Size      408 Trigger  1
 00000300 03e14195 04e1b045 05e13552 06e10005
 00000500 03e14195 04e1b045 05e13552 06e10005
Event      9525756 Type/Subtype  10    1 Size      208 Trigger  1
 00010500 03e1abf5 04e1b247 05e13552 06e10005
Event      9525757 Type/Subtype  10    1 Size      408 Trigger  1
 00000700 03e1419b 04e1b045 05e13552 06e10005
 00000000 03e141b1 04e1b045 05e13552 06e10005
Event      9525759 Type/Subtype  10    1 Size      208 Trigger  1
 00010000 03e1abf9 04e1b247 05e13552 06e10005
Event      9525760 Type/Subtype  10    1 Size      408 Trigger  1
 00000800 03e141b2 04e1b045 05e13552 06e10005
 00000100 03e141b9 04e1b045 05e13552 06e10005
Event      9525762 Type/Subtype  10    1 Size      208 Trigger  1
 00010100 03e1ac00 04e1b247 05e13552 06e10005
Event      9525763 Type/Subtype  10    1 Size      608 Trigger  1
 00000800 03e1abf4 04e1b247 05e13552 06e10005
 00000700 03e1abf5 04e1b247 05e13552 06e10005
 00000300 03e1abfa 04e1b247 05e13552 06e10005
```

- This happens roughly 0.1% of the time! Investigations ongoing

Juelich Daq Setup

- Rimfaxe ->VME controller + TRLO
  - Backup RIO4 + VULOM
- WR switch->Timestamping WR.
- ECL to NIM convertor
- FiFo->Distributes trigger and TS to mosaics.



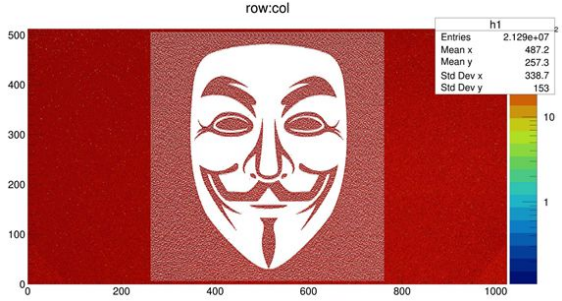


Juelich software

Making macro to auto generate structure containing information of FPGA mapping

This will then go straight into drasi_reader

Masking function exists, param currently in text →
Also need to make sure can feed into R3BRoot




```
//trg params
MOSAIC_GLOBAL.device_name = "IBHIC"; //Inner Barrel Hybrid interface card
MOSAIC_GLOBAL.strobe_delay_board = 50 ;
MOSAIC_GLOBAL.pulse_delay  = 500 ;

MOSAIC_GLOBAL.pulse_delay_board  = 50 ;
MOSAIC_GLOBAL.strobe_duration = 200;
MOSAIC_GLOBAL.strobe_delay_chip = 20;


MOSAIC_GLOBAL.trig_delay          = 50 ;
//default form alice
MOSAIC_GLOBAL.ctrl_latancy_mode  = 0;
MOSAIC_GLOBAL.polling_data_time_out = 500;
MOSAIC_GLOBAL.data_link_polarity     = 0;
MOSAIC_GLOBAL.data_link_speed        = 2 ;
MOSAIC_GLOBAL.trg_record_enable      = 1;
MOSAIC_GLOBAL.readout_mode = 0 ;
MOSAIC_GLOBAL.link_speed = 1 ;
MOSAIC_GLOBAL.enable_skewing_global = 1 ;
MOSAIC_GLOBAL.enable_skewing_start_ro = 1 ;
MOSAIC_GLOBAL.enable_busy_monitoring = 1 ;
MOSAIC_GLOBAL.test_pulse_mode = 1;
MOSAIC_GLOBAL.enable_internal_strobe = 0 ;
MOSAIC_GLOBAL.enable_test_strobe = 0;


MOSAIC[0].host_id = "200";
MOSAIC[0].pulse_duration = 500;
MOSAIC[0].chipName = {"R3BSCC001","det3"};
MOSAIC[0].chipId ={4,1};
MOSAIC[0].recId ={3,1};
MOSAIC[0].chipITHR = {15,15};
MOSAIC[0].chipVCASN = {50,51};
MOSAIC[0].chipVCASN2 = {62,62};
```

Summary

- Modifications to the ALPIDE+MOSAIC software made to handle FPC
- FPC fit through test will start after Budapest with LTU flex
- FPC needs building
- Timestamp debugging started.