Characterization and commissioning of the front-end electronics for the Silicon Tracking System of the CBM experiment

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"The best that most of us can hope to achieve in physics is simply to misunderstand at a deeper level"

Wolfgang Pauli

To my family

Contents

Abstract

The Compressed Baryonic Matter (CBM) experiment is a fixed-target heavy-ion physics experiment at the Facility for Antiproton and Ion Research (FAIR) in Darmstadt, Germany. The CBM physics program aims at exploring the QCD phase diagram at very high net-baryon densities, where a first-order phase transition from hadronic to partonic matter and a chiral phase transition is expected to occur. For high-statistics measurements of rare probes, CBM is designed to cope with very high interaction rates up to 10 MHz. Therefore, the experiment will be equipped with fast and radiation hard detectors employing free-streaming readout electronics.

The central detector for determining the momentum of charged particle in the CBM experiment is the Silicon Tracking System (STS). It is designed to measure up to 1000 charged particles per event in nucleus-nucleus collisions at interaction rates between 0.1 and 10 MHz. The detector system consists of 876 double-sided silicon micro-strip sensors arranged in 8 tracking stations covering a physics aperture of $2.5° \leqslant \Theta \leqslant 25°$. It is placed between 30 cm and 100 cm downstream the target, inside 1 Tm dipole magnetic field. The experimental conditions pose demanding requirements in terms of channel density and readout bandwidth to be met by the front-end electronics.

The detector's functional building block is the module, consisting of a double-sided, double-metal silicon microstrip sensor, microcables and two front-end electronics boards. An essential component is the STS-XYTER, a dedicated ASIC for the readout of the double-sided silicon micro-strip sensors. It is a low power, self-triggering ASIC with 128 channels, 5-bit ADC charge and 14-bit timing information.

The STS-XYTER v2.2 is the latest and final revision of the chip, therefore, its characterization is one of the major steps before its operation in the full readout chain. During this work, the STS-XYTER v2.2 have been extensively characterized and a set of procedures and software tools, used in the ASIC characterization, have been implemented and optimized.

The collection and analysis of the analog waveforms, where gain values were extracted for the slow and fast shaper, represent one of the first tested functionalities. The slow shaper peaking time was estimated for all possible values. The discharge time constant was calculated, obtaining larger values for holes polarity compared to electrons polarity. The ADC global threshold response was measured and its linearity evaluated for all possible ranges.

In the last version of the ASIC (v2.2) it was found out that, since the inclusion of the diode-based ESD protection circuit, the CSA fast reset is not working as expected. However, it is possible to operate the chip at high rate without the fast reset feature, by reducing the discharge time constant of the CSA. It has been demonstrated that the ASIC can be operated without the fast reset feature, non compromising the performance in terms of ballistic deficit or noise levels.

Among the multiple operation requirements of the STS-XYTER v2.2 ASIC, the noise performance is one of the most important. The noise performance of the ASIC has been evaluated as a function of different parameters such as: input capacitance, CSA bias current, IFED resistor, shaping time, shaping current and stability tests. These results have demonstrated a stable and reliable performance with no significant deterioration of the noise levels for a large range of studied settings.

A prerequisite for the assembly of functional detector modules, in any experiment, is a rigorous Quality Assurance (QA) of the components. A dedicated setup has been used, based on a custom designed pogo-pin station where a big sample of ASICs and chipcables were tested. QA protocols have been designed and optimized in order to improve the testing procedures. A quality grade for every ASIC and chipcable, based on the gained experience from testing previous versions of the chip, have been proposed. A GUI has been developed in PyQt version 4.0 for making the testing process as user friendly as possible. The implemented software for testing the chips and chipcables has been used since 2021, improving significantly the detector modules assembly aiming to the STS production.

The test and characterization of fully assembled modules is fundamental for proving assembly concepts for the final STS detector. Across the last years, the CBM-STS project has achieved important milestones related to the assembly and successful operation of the first modules. The systematic testing of fully assembled STS modules allowed to verify the performance of the latest version of the front-end ASIC functionalities and the electrical properties of the modules. Several parameters such as ASIC communication and control functionalities have been monitored across all checks. The results of the charge calibration have shown a good and homogeneous response for all produced modules. These results are independent of the overall dimensions of the modules or the version of the front-end electronics in use.

The noise measurements demonstrated that an overall level of approximately 1000 e- ENC is an achievable goal for most of the largest produced modules. The scans of the CSA bias current have exposed a large and stable plateau, at which the modules can be operated without deteriorating the system noise. The noise levels for different shaping times showed the dominance of the voltage noise component at smaller shaping time (90 ns).

For a selected module, signal readouts have been studied using an ^{241}Am gamma source. This allowed to verify the calibration procedure and assess the transfer function of the ADC threshold register in the chip. The measured charge collection efficiency was estimated to approximately 96% for the selected module. An average signal to noise ratio (SNR) above 13 was calculated for both polarities.

The iterative testing of STS modules is, in general, an essential step for developing a reliable quality control procedure and establishing classification criteria towards series production. These studies brought important insights regarding the fraction of broken and non-operational channels in the modules, and consequently assembly yield.

A small scale prototype of the full detector, named mini-STS (mSTS), has been built as part of the CBM Phase 0 activities. The setup was operated during July 2021 campaign with O + Ni at 2 AGeV at the Heavy Ion Synchrotron SIS18 in GSI, Darmstadt. For the first time, a setup comprising of two tracking stations and a total of 11 modules have been built and operated in a realistic environment.

Periodic structures were observed in the time distribution of all modules. These replica hits are generated due to significant noise in the MHz range in the fast discriminator. This behavior is well understood and consistent with the ASIC design. The replica effect can be significantly reduced by setting the fast discriminator threshold as low as possible without affecting the time resolution of the system and by reducing the noise in the relevant frequency range to the largest possible extent.

A successful time calibration have been implemented. The system time resolution was estimated to be 5.9 ns, which indicates a good time resolution achieved by the detectors. The noise contribution from the fast shaper (σ_n) was calculated. The charge distributions of reconstructed hits have been presented for different strip clusters and showed a clear separation between noise and MIP position. The average SNR was evaluated for 1 strip-cluster signals for some modules, resulting in a value of approximately 21. This result is an important milestone for the STS detector since the mSTS modules are some of the largest, and therefore, higher capacitance objects in our

detector system. The operation of mSTS in a common, high-speed, free-streaming readout chain at intensities up to 10^9 ions/s, helps to prove the STS concept in conditions close to the final operation.

Kurzfassung

Das Compressed Baryonic Matter (CBM) Experiment ist ein Experiment der Schwerionenphysik mit festem Target an der "Facility for Antiproton and Ion Research" (FAIR) in Darmstadt, Deutschland. Das CBM-Physikprogramm zielt auf die Erforschung des QCD-Phasendiagramms bei sehr hohen Netto-Baryonendichten, wo ein Phasenübergang erster Ordnung von hadronischer zu partonischer Materie und ein chiraler Phasenübergang erwartet werden. Zur Messung seltener Sonden mit hoher Statistik ist CBM für hohe Wechselwirkungsraten von bis zu 10 MHz ausgelegt. Daher wird das Experiment mit schnellen und strahlungsharten Detektoren und einer Free-Streaming-Ausleseelektronik ausgestattet sein.

Der zentrale Detektor zur Bestimmung der Impulse geladener Teilchen im CBM-Experiment ist das Silicon Tracking System (STS). Es ist ausgelegt, die Spuren von bis zu 1000 geladenen Teilchen pro Ereignis in Kern-Kern-Kollisionen bei Wechselwirkungsraten zwischen 0.1 und 10 MHz zu messen. Das Detektorsystem besteht aus 876 doppelseitigen Silizium-Mikrostreifensensoren, die in 8 Tracking-Stationen angeordnet sind und eine physikalische Apertur von $2.5^\circ \leqslant \Theta \leqslant 25^\circ$ abdecken. Das STS ist zwischen 30 cm und 100 cm hinter dem Target innerhalb eines Dipolmagnetfeldes von 1 Tm installiert. Die experimentellen Bedingungen stellen hohe Anforderungen an die Kanaldichte und die Auslesebandbreite, die von der Front-End-Elektronik erfüllt werden müssen.

Das wichtigste Element des Detektors ist das sogenannte "Modul", das aus einem doppelseitigen, Doppel-Metall-Silizium-Mikrostreifensensor, 32 Mikrokabeln und zwei Front-End-Elektronikplatinen besteht. Eine wesentliche Komponente ist der STS-XYTER, ein spezieller ASIC für die Auslese der doppelseitigen Silizium-Mikrostreifensensoren. Es handelt sich um einen stromsparenden, selbsttriggernden ASIC mit 128 Kanälen, der pro Treffer 5-Bit-ADC-Ladungs- und 14-Bit Timing-Information zur Verfügung stellt.

Der STS-XYTER v2.2 ist die neueste und letzte Version des Chips, daher ist seine Charakterisierung ein wesentlicher Schritt vor seinem Einsatz in der finalen Auslesekette. Im Rahmen der vorliegenden Arbeit wurde der STS-XYTER v2.2 ausgiebig getestet sowie eine Reihe von Verfahren und Software-Tools, die bei der ASIC-Charakterisierung verwendet werden, entwickelt, implementiert und optimiert.

Die Messung und Analyse der analogen Signalformen, aus denen die Verstärkungsfaktoren für den langsamen und schnellen Shaper extrahiert wurden, war einer der ersten Charakterisierungsschritte. Die Peaking-Zeit des langsamen Shapers wurde für alle möglichen Konfigurationen bestimmt. Die Entladungszeitkonstanten wurden berechnet, wobei größere Werte für die Polarität der Löcher im Vergleich zur Polarität der Elektronen ermittelt wurden. Das Verhalten der globalen ADC-Schwellenwertsetzung wurde gemessen und ihre Linearität für alle möglichen Messbereiche verifiziert.

In der neuesten Version des ASIC (v2.2) wurde festgestellt, dass seit dem Einbau der Dioden-basierten ESD-Schutzschaltung das schnelle Rücksetzen des ladungsempfindlichen Vorverstärkers (CSA) nicht wie erwartet funktioniert. Es ist jedoch möglich, den Chip auch ohne die schnelle Rücksetzfunktion mit hoher Rate zu betreiben, indem man die Entladezeitkonstante des CSA geeignet reduziert. Es wurde gezeigt, dass der ASIC auf diese Weise betrieben werden kann, ohne

Eigenschaften wie das ballistische Defizit oder den Rauschpegel zu beeinträchtigen.

Unter den vielfältigen Betriebsanforderungen des STS-XYTER v2.2 ASIC ist gutes Rauschverhalten eine der wichtigsten. Das Rauschverhalten des ASIC wurde als Funktion verschiedener Parameter wie Eingangskapazität, CSA-Bias-Strom, CSA-Rückkopplungs-Widerstand (IFED), Shaping-Zeit, Shaping-Strom sowie Langzeitstabilität charakterisiert. Die Ergebnisse zeigen einen stabilen und zuverlässigen Betrieb des ASIC ohne signifikante Verschlechterung des Rauschpegels über einen großen Bereich möglicher Einstellungen.

Eine Voraussetzung für den Bau funktionsfähiger Detektoreinheiten in jedem Experiment ist eine strenge Qualitätssicherung (QA) der Komponenten. Für die Tests einzelner ASICs wurde ein spezieller Aufbau verwendet, der auf einer speziellen Pogo-Pin-Station basiert, in der eine große Anzahl von ASICs und Chipkabeln getestet wurde. QA-Protokolle wurden entwickelt und optimiert, um die Testverfahren zu verbessern. Für jeden ASIC und jedes Chipkabel wurde, basierend auf den Erfahrungen, die beim Testen früherer Versionen des Chips gesammelt worden waren, eine Qualitätsstufe ermittelt. Es wurde eine grafische Benutzeroberfläche in PyQt Version 4.0 entwickelt, um den Testprozess so benutzerfreundlich wie möglich zu gestalten. Die implementierte Software zum Testen von Chips und Chipkabeln wird seit 2021 verwendet, wodurch erhebliche Verbesserungen bei der Montage der Detektormodule im Hinblick auf die STS-Serienproduktion erreicht wurden.

Der Test und die Charakterisierung vollständig montierter Module ist von grundlegender Bedeutung für die Verifizierung der Montagekonzepte für den endgültigen STS-Detektor. In den letzten Jahren hat das CBM-STS-Projekt wichtige Meilensteine in Bezug auf den Zusammenbau und den erfolgreichen Betrieb der ersten Module erreicht. Systematische Tests der vollständig montierten STS-Module ermöglichten die Überprüfung der Leistung der neuesten Version der Front-End-ASIC-Funktionen und die elektrischen Eigenschaften der Module. Parameter wie z.B. die ASIC-Kommunikation und die Kontroll-Funktionalität wurden bei allen Messungen durchgehend überwacht. Die Ergebnisse der Ladungskalibrierung zeigten ein gutes und homogenes Verhalten für alle produzierten Module. Die Resultate sind unabhängig von den Gesamtabmessungen (Kabel- und Sensorlänge) der Module bzw. der verwendeten Version der Front-End-Elektronik.

Die Rauschmessungen haben gezeigt, dass ein Gesamtpegel von etwa 1000 e^- ENC für die meisten der größten produzierten Module ein erreichbares Ziel ist. Die Scans des CSA-Bias-Stroms haben ein großes und stabiles Plateau aufgezeigt, in dem die Module betrieben werden können, ohne dass sich das Systemrauschen verschlechtert. Die Messungen der Rauschpegel für verschiedene Shaping-Zeiten zeigen die Dominanz der Spannungs-Rauschkomponente bei kleinen Shaping-Zeiten (90 ns).

An einem ausgewählten Modul wurde die Signalauslese mit einer ^{241}Am-Gammaquelle untersucht. Dies ermöglichte die Verifizierung des Kalibrierungsverfahrens und die Bewertung der Übertragungsfunktion des ADC-Schwellenwertregisters auf dem Chip. Die Ladungssammel-Effizienz wurde für dieses ausgewählte Modul mit einem Wert von etwa 96% abgeschätzt. Es wurde ein durchschnittliches Signal-Rausch-Verhältnis von über 13 für beide Polaritäten bestimmt.

Das iterative Testen von STS-Modulen ist ein wesentlicher Schritt zur Entwicklung eines zuverlässigen Qualitätskontrollverfahren und zur Festlegung von Klassifizierungskriterien für die Serienproduktion. Diese Studien brachten wichtige Erkenntnisse über den Anteil nicht verbundener oder anderweitig nicht funktionierender Kanäle in den Modulen und folglich für die Fertigungsausbeute bei der Montage.

Im Rahmen der CBM-Phase 0 wurde ein kleiner Prototyp des vollständigen Detektors, der so genannte Mini-STS (mSTS), gebaut. Dieser Aufbau war während der Strahlzeit-Kampagne im Juli 2021 mit O + Ni bei 2 AGeV am Schwerionensynchrotron SIS18 an der GSI Darmstadt in Betrieb. Zum ersten Mal wurde ein Aufbau mit zwei Tracking-Stationen und insgesamt 11 Modulen gebaut und in einer realistischen Experimentumgebung betrieben.

In der zeitlichen Verteilung der Daten aller mSTS-Module wurden periodische Strukturen beobachtet. Diese sogenannten Replika-Treffer werden durch ein starkes Rauschen im MHz-Bereich im schnellen Diskriminator verursacht. Es ist möglich, dieses Verhalten aus den Eigenschaften des ASIC-Designs zu verstehen. Der Replika-Effekt kann deutlich reduziert werden, indem der Schwellenwert des schnellen Diskriminators so niedrig wie möglich eingestellt wird, ohne die Zeitauflösung des Systems zu beeinträchtigen, und indem externe Rauschquellen im relevanten Frequenzbereich so weit wie möglich reduziert werden.

Für die mSTS-Daten wurde erfolgreich eine Zeitkalibrierung durchgeführt. Die Zeitauflösung des Systems wurde zu 5.9 ns abgeschätzt, was auf eine gute Zeitauflösung der Detektoren schliessen lässt. Der Rauschbeitrag des schnellen Shapers (σ_n) wurde berechnet. Die Ladungsverteilungen der rekonstruierten Treffer wurden für Cluster verschiedener Streifenanzahl ermittelt und zeigen eine klare Trennung zwischen Rauschverteilung und MIP-Signal. Das durchschnittliche SNR wurde für 1-Streifen-Cluster-Signale für einige Module ausgewertet und ergibt einen Wert von etwa 21. Dieses Ergebnis ist ein wichtiger Meilenstein für den STS-Detektor, da die in mSTS verwendeten Module zu den größten mit höchster Eingangskapazität und damit stärkstem Rauschen in STS gehören. Der Betrieb von mSTS in einer gemeinsamen mCBM-Auslesekette bei Strahlintensitäten von bis zu 10^9 ions/s hilft, das STS-Konzept unter Bedingungen zu verifizieren, die dem endgültigen Betrieb nahekommen.

Chapter 1

Introduction

The understanding of the universe, and more specifically its evolution, have been some of the most important questions to be answered for the scientific community. With the progress in technology during the last centuries and the development of more sophisticated devices, the theories and discoveries of thousands of physicists have resulted in a remarkable insight into the fundamental structure of matter. Everything in the universe is found to be made from a few basic building blocks called fundamental particles, governed by four fundamental forces: gravity, electromagnetism, strong and weak interactions. Putting aside the gravitational force, which is described by Einstein's general relativity theory, the other three forces can be described by the Standard Model [1].

The Standard Model was developed in stages throughout the end of 20th century, taking into account the work of many scientists worldwide. The current formulation has been developed in the early 1970s, providing a uniform framework for understanding the electromagnetic, weak, and strong interactions. Although the Standard Model is believed to be theoretically self-consistent and it is the most successful theory of elementary particles and their interactions, it falls short of being a complete theory of fundamental interactions.

While the theory describing week interactions is called quantum flavourdynamics (QFD), the weak force is better understood by the electroweak theory (EWT) [2]. The electroweak theory inherits the phenomenological successes of the four-fermion low-energy description of weak interactions, and provides a well-defined and consistent theoretical framework including weak interactions and quantum electrodynamics in a unified picture. The underlying fundamental theory for strong nuclear interaction is called Quantum Chromodynamics (QCD) [3].

There are two key fundamental phenomena associated with QCD. The first one is *asymptotic freedom*, which states that quarks interact weakly at large energies (or equivalently at short distances). As the distance between quarks in hadrons increases, their interaction energy increases as well, which prevents the quarks from hadrons to be separated. The second fundamental property of QCD is *confinement*, which refers to the experimental observation that quarks and antiquarks can not be found isolated in nature. Namely, quarks and antiquarks are found only confined in hadrons, the composite objects they form. This is a consequence of the constant force between the color charges, as they are separated, resulting from the self interaction of gluons, as they also carry charge. Analytically, confinement is unproven, however, Lattice QCD calculations have predicted, that at certain conditions the confinement of quarks in hadrons vanishes, forming a new state of matter, the quark-gluon plasma (QGP) [4], where the quarks and gluons can move freely in the region where a QGP exists, on the scales larger than the size of hadrons (about 10^{-15} m). The nuclear matter under such extreme conditions may exist also in the interior of compact stellar objects like neutron stars.

As every field theory of particle physics, QCD is based on certain symmetries of nature, deduced by observation. Chiral symmetry exists as an exact symmetry only in the limit of vanishing quark masses. However, the actual quark masses, and the strong interaction of quarks and gluons cause the explicit and spontaneous breaking of chiral symmetry, responsible for the generation of hadron masses. Chiral symmetry is approximately restored when quark masses are reduced from their large effective values in hadronic matter to their small bare ones at sufficiently high temperatures and energy densities.

1.1 The QCD phase diagram

Different substances exist in the universe across phases such as gas, liquid, and solid, depending on the temperature and pressure. A variation of these conditions might cause a transition from one phase to another one. The boundaries between different transition lines can be described in a diagram of temperature as function of the pressure. Significant efforts have been made so far to explore the phase diagram of strongly interacting matter [5]. In contrast to the countless, very distinct phase diagrams found in condensed matter physics, the phase diagram probed in heavy-ion collisions is a unique and fundamental feature of QCD. The most common way to characterize the QCD phase diagram is in the plane of temperature (T) and the baryon chemical potential (μ_B). The hypothetical phases of strongly interacting matter and their boundaries are illustrated in Fig. 1.1.

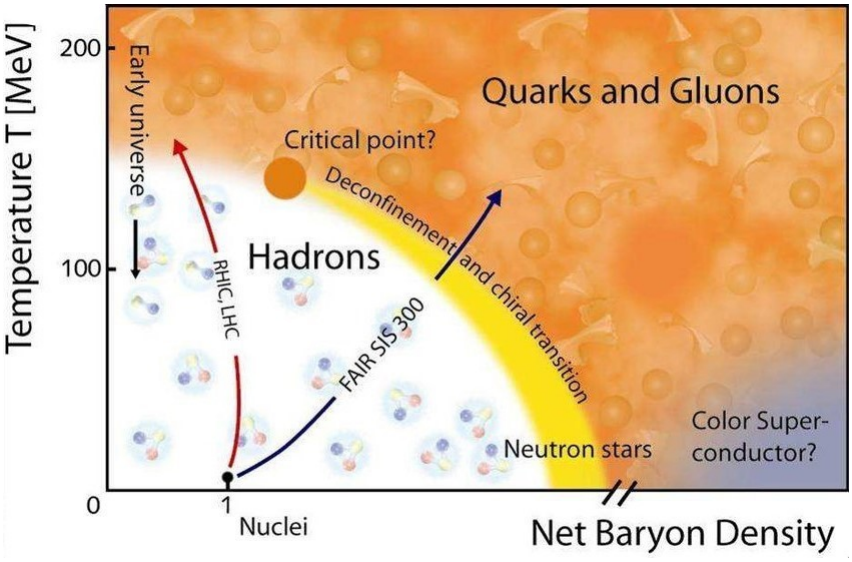


Figure 1.1: *Schematic phase diagram of dense nuclear matter, in the baryon chemical potential μ_B - temperature (T) plane.*

In the region of low temperatures and baryon chemical potential, partons are bound to form hadronic matter (protons, neutrons, mesons, etc). When temperature rises, space is filled with a dilute gas of hadrons; as the temperature increases this hadronic gas gradually fills the space, until the hadrons begin to merge, continuously transforming the matter structure and leading to a breakdown of its description purely in terms of hadrons. Figure 1.2 shows a schematic of the transition from hadronic to quark-gluon plasma phase with increasing the temperature. Yet, a quasiparticle description based on quarks and gluons does not apply either, for while the hadrons have broken down, the strong correlations remain. Thus, the system may be described as a strongly correlated quark-gluon plasma in which both hadronic-like and quark-like degrees of freedom can exist. These conditions, where the number of baryons and antibaryons is almost equal, existed in

the early Universe several microseconds after the Big Bang [6]. In this region a smooth crossover from partonic to hadronic matter is expected. Experiments at the Relativistic Heavy Ion Collider (RHIC) and the Large Hadron Collider (LHC) have provided compelling evidence of the formation of a deconfined state of quarks and gluons for matter close to $\mu B = 0$ and temperatures above 156 MeV.

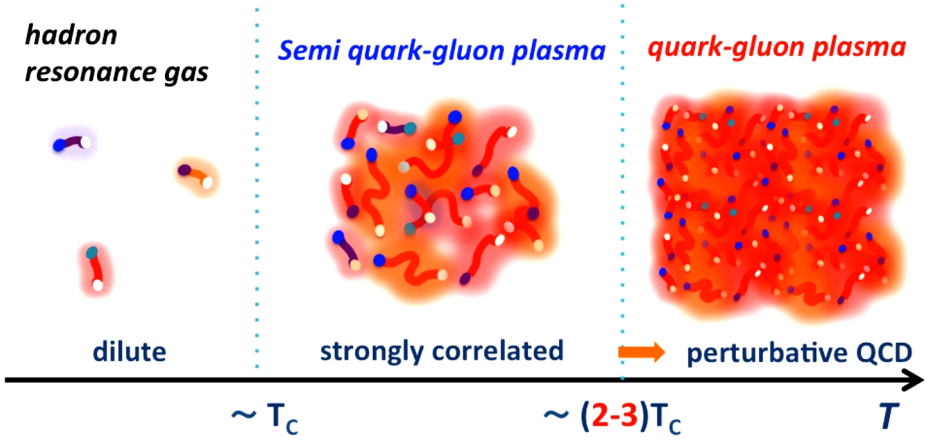


Figure 1.2: *Schematic picture of the crossover transition from the hadronic to quark-gluon plasma phase with increasing temperature [7].*

In the region of moderate temperatures and large baryon densities, a first order phase transition has been predicted from hadronic to partonic matter [8]. These predictions, together with the existence of an end point or critical point at high μB have been proposed for several QCD-based models. However, the locations of the phase boundary, the existence of a critical point and a first order phase transition at higher μB remains to be confirmed experimentally.

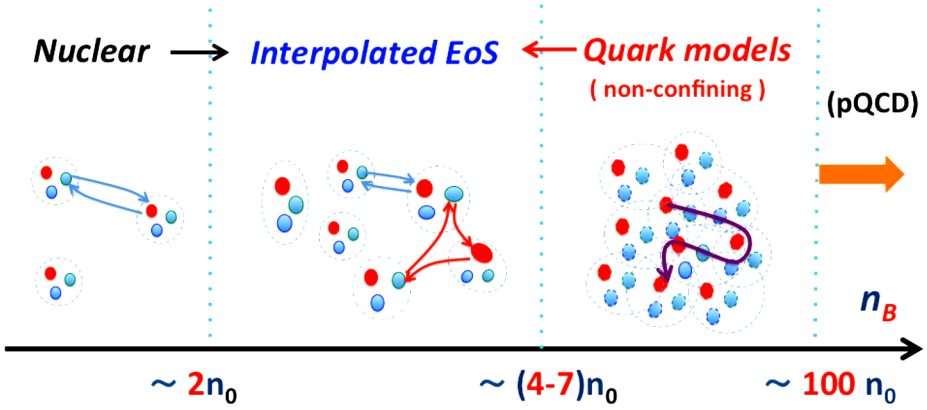


Figure 1.3: *Schematic picture of the transition from nuclear to deconfined quark matter with increasing density [7].*

At very high baryon densities and low temperatures, the distance between nucleons becomes smaller, making these ones to crush into each other. At a sufficiently high density the matter should percolate, in the sense that their quark constituents are able to propagate throughout the system. Figure 1.3 shows the transition from nuclear to deconfined quark matter with the increasing density.

The deconfinement of nuclear matter with increasing density has many similarities to the manner in which atomic gases, when compressed, become gases of itinerant electrons in a background of ions. This state of matter is possibly existing in the interior of the neutron stars.

The phases of QCD are characterized by a variety of condensates in which a macroscopic number of particles (and antiparticles) are strongly correlated by the strong interaction. The emergence of condensates reduces the energy of the system, and in addition, condensates break symmetries in QCD, leading to states with lower symmetry than in the QCD Hamiltonian. The condensates, which depend on temperature and baryon density, play an important role in the structure of hadrons, as well as in neutron stars, since the condensation energies are a large fraction of the energy density in a neutron star core.

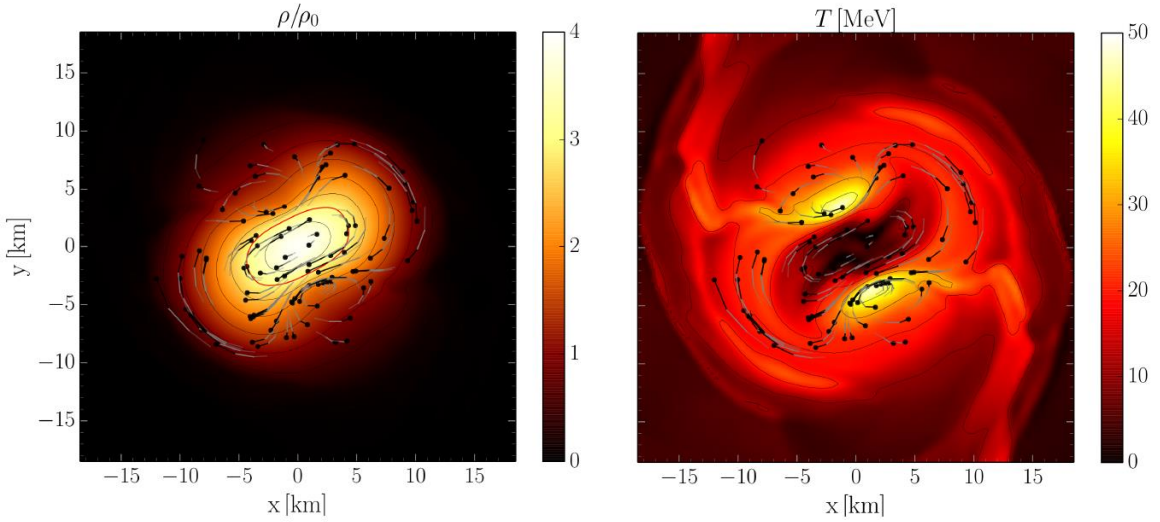
1.2 QCD at high baryon densities: neutron stars

In the hadronic regime, three quarks bind together to produce a color singlet object. In the regime between hadronic and quark matter, colored quarks and diquarks appear virtually during quark exchanges between baryons (essentially the baryon-baryon interactions). In the quark matter regime, a diquark or a pair of quarks can easily find an extra quark nearby to produce local color neutrality, so that the extra quark is weakly correlated with the diquark or pair. With increasing baryon density or temperature, the effective degrees of freedom of matter change, possibly accompanied by phase transitions. Neutron stars are some of the densest manifestations of massive objects in the universe. They are ideal laboratories for testing theories of dense matter physics and provide connections among nuclear and particle physics and astrophysics. They might exhibit conditions and phenomena not observed elsewhere, such as hyperon-dominated matter, deconfined quark matter, superfluidity and superconductivity, opaqueness to neutrinos, and magnetic fields in excess of 10^{13} Gauss.

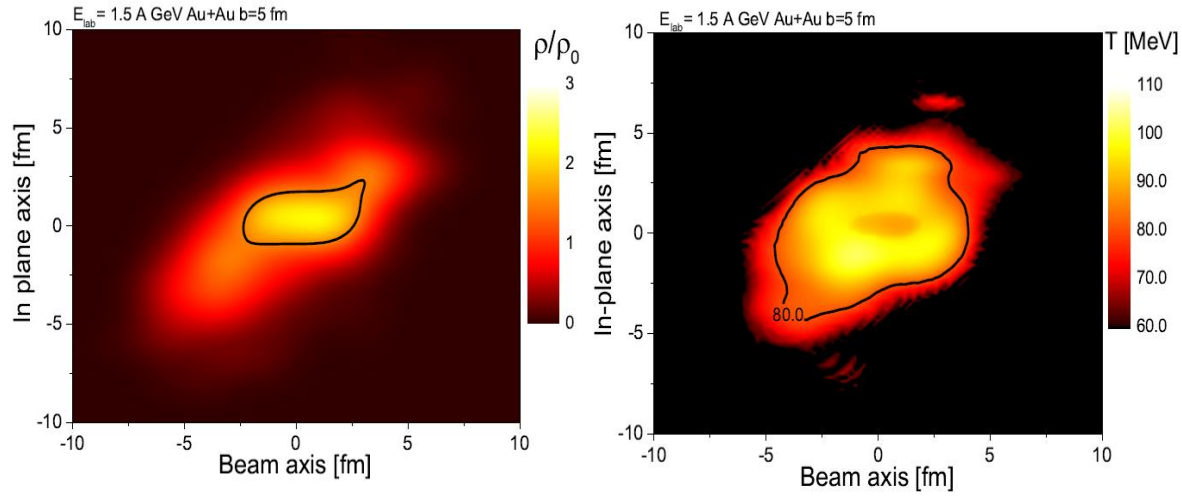
Neutron stars are created in the aftermath of the gravitational collapse of the core of a massive star (larger than 8 Solar masses) at the end of its life, which triggers a Type II supernova explosion [10]. Typical neutron stars masses are about 1.4 solar masses, while the radii are in the range of 10 to 14 km. The density can reach values between 5 to 10 times nuclear saturation density and the temperature can go up to 10^{10} kelvins (around 1 MeV). The exception is at neutron star births in supernovae, where temperatures can be tens of MeV, and in final gravitational mergers where temperatures could reach values up to 100 MeV. The bulk properties of neutron stars (e.g., mass, radius, moment of inertia, mass-shed frequency, tidal deformability, etc.) chiefly depend on the equation of state (EOS) describing the macroscopic properties of stellar matter. The EOS of dense matter is also one of the main ingredients for the study of various astrophysical phenomena related to neutron stars, as core-collapse supernovae and binary neutron star (BNS) mergers.

In August 2017, the LIGO-Virgo Scientific Collaboration reported the milestone detection of gravitational waves (GW) from binary neutron stars (BNS) merger GW170817 [11] and since then, the interest in dense matter physics has increased substantially. Although the gravitational waves from this discovery event seen by LIGO only reveal the inspiraling incident neutron stars, with coming improvements to LIGO's sensitivity, future events will give a view of the collision itself, making it possible to learn about the compactness and density profile of the incident neutron stars and, conceivably, whether or not they feature dense quark matter cores. If they do, present constraints on heat transport in neutron stars coming from X-ray observations of how they cool down will turn into constraints on the equation of state and the transport properties of cold dense quark matter.

The densities created in the mergers of compact stars can exceed several times the nuclear ground state density. Furthermore, in the early time of the merger, high temperatures close to 100 MeV are obtained. The properties of matter at such high temperature and density are very



(a) *Distributions of the rest-mass density ρ in units of ρ_0 (left panel) and the temperature (right panel) on the equatorial plane at a post-merger time of $t = 6.34$ ms for the neutron stars binary merge LS220-M132.*



(b) *Net baryon density contour in the reaction plane of a non-central Au + Au collision ($b = 5$ fm) at a beam energy of $E_{lab} = 1.5$ AGeV (left panel) and the respective temperature (right panel).*

Figure 1.4: *Comparison between neutron stars binary merge LS220-M132 and Au + Au collision at SIS100. Densities for the heavy ion collisions were calculated using the UrQMD transport model and the temperatures were calculated from the density and energy density using the QχP model for the equation of state [9].*

different from what it's expected from cold nuclear matter. Similar densities and temperatures can be created in the relativistic collisions of heavy nuclei at different particle accelerators. In such heavy ion experiments the heavy nuclei are accelerated to relativistic velocities. It is therefore very intriguing to study QCD matter at similar temperatures and densities in two rather different experimental setups, in neutron star mergers and heavy ion collisions. Figure 1.4 illustrates a comparison between neutron stars binary merge LS220-M132 and Au + Au collision at SIS100, where multiple similarities between both systems can be observed. By combining the findings from

both observations one can be able to deduce information about the properties of the QCD matter at high densities and its phase structure. The properties of the equation of state of QCD are the link connecting neutron star mergers and relativistic nuclear collisions. Consequently the goal of such studies aim to find a description for the EOS that should be able to describe neutron star merger and nuclear collision observables and therefore, establish the connection.

1.2.1 Equation of state

The physics of neutron stars represents a way to test our understanding of matter under extreme conditions of density and temperature. This requires the modeling of systems in very different physical conditions such as heavy neutron rich nuclei arranged to form a lattice structure as in the outer crust of the star, or a charge neutral system of interacting hadrons (nucleons, and possibly hyperons or a phase with deconfined quarks) and leptons forming a quantum fluid as in the stellar core [10].

The main ingredient needed to describe the structure of neutron stars is the equation of state. The EOS refers to the equations describing how the pressure and other thermodynamic variables, such as the free energy and entropy, depend upon the quantities of density, temperature and composition. For high density matter, for instance found in neutron stars, the composition is not well understood and the equation of state remains highly uncertain. In the past decades, several approaches have been developed to derive the dense matter EOS. Among non-relativistic approaches, some of the most popular models are based on effective Skyrme interactions, which can be used to describe finite nuclei as well as nuclear matter and neutron stars. The general relativity and causality set important constraints to the neutron stars compactness [11]. In addition, analytic general relativity solutions are useful for understanding the relationships that exist among the maximum mass, radii, moments of inertia, and tidal Love numbers of neutron stars, which are accessible to observation. Some of these relations are independent of the underlying dense matter equation of state, while others are very sensitive to the equation of state.

The EOS of dense matter below nuclear saturation densities can be well approximated by the use of the liquid droplet model, while at higher densities, it can be described by the EOS of bulk nucleonic matter. Bulk neutron star matter differs from bulk matter in ordinary atomic nuclei largely because of the different equilibrium values of the proton fraction. Neutron star matter near and above nuclear saturation densities has very few protons, and is nearly pure neutron matter. The difference between neutron and nuclear matter with nearly equal proton and neutron concentrations is described by the nuclear symmetry energy. The greatest uncertainty in the description of neutron star matter is due to uncertainties in the nuclear symmetry energy, however experiments are beginning to closely constrain those properties.

Recent observations of neutron stars from pulsar timing, quiescent X-ray emission from binaries, and Type I X-ray bursts can set important constraints on the structure of neutron stars and the underlying equation of state. In addition, measurements of thermal radiation from neutron stars have uncovered the possible existence of neutron and proton superfluidity/superconductivity in the core of a neutron star, as well as offering powerful evidence that typical neutron stars have significant crusts. These observations impose constraints on the existence of strange quark matter stars, and limit the possibility that abundant deconfined quark matter or hyperons exist in the core of the stars.

As the only source of data on cold high density matter in QCD, neutron stars are a rich testing ground for microscopic theories of dense nuclear matter, providing an approach complementary to probe dense matter in ultrarelativistic heavy ion collision experiments.

1.3 Heavy ion collisions

Heavy ion collision experiments at relativistic energies create extreme states of strongly interacting matter and allow their investigation in the laboratory. In order to search for features like the predicted first-order phase transition, the chiral phase transition and the critical endpoint, moderate temperatures and high baryochemical potentials must be achieved and experimentally accessed. High-energy heavy ion collision experiments worldwide have been investigating the strongly interacting matter under extreme conditions. The RHIC in Brookhaven National Laboratory and the LHC in CERN have been running heavy ion programs to explore the QGP at small baryon chemical potentials and high temperatures, where matter is produced with almost equal numbers of particles and antiparticles, simulating several microseconds after the Big Bang. The efforts made from this collaborations opens the gate for claiming that partonic degrees of freedom prevail in the early phase of the fireball evolution.

Most of the experimental observables, which are sensitive to the properties of dense nuclear matter, like the flow of some identified particles, higher moments of event-by-event multiplicity distributions of conserved quantities, multi-strange hyperons, and di-leptons demand very high statistics. Therefore, one of the key feature for future experiments is the rate capability, which allows to measure the above mentioned observables with high precision. The interaction rates of existing and planned heavy-ion experiments are presented in Fig 1.5 as a function of center-of-mass energy [12].

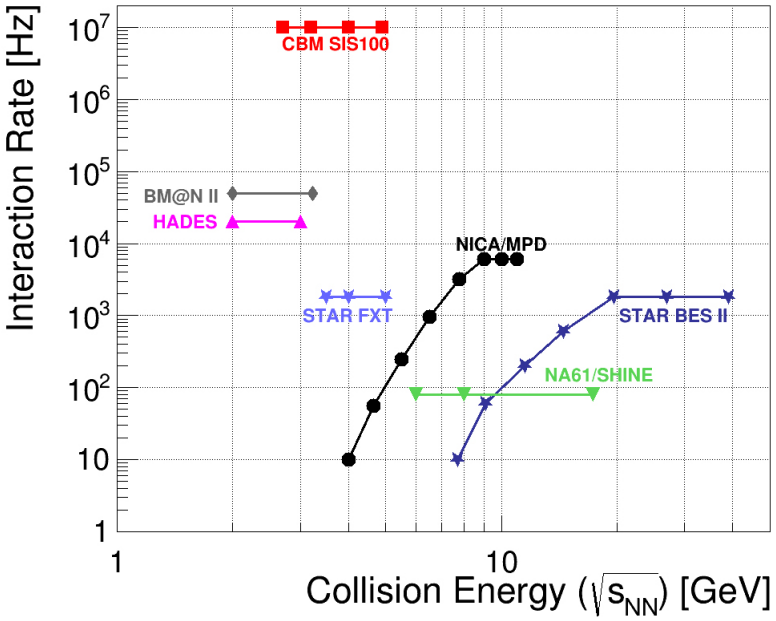


Figure 1.5: *Comparison of the interaction rates of existing and planned heavy-ion experiments as a function of the center-of-mass energy [12].*

The QCD phase diagram at large baryon chemical potentials has been explored by pioneering heavy-ion experiments. Due to the detector technologies available back then when these experiments were designed, their measurements were restricted to abundantly produced hadrons and to di-electron spectra with limited statistics. At the CERN-SPS, the NA61/SHINE experiment continues to search for the first-order phase transition by measuring hadrons using light and medium heavy ion beams. This detector setup is limited to reaction rates of about 80 Hz. The existing HADES detector at SIS18 measures hadrons and electron pairs in heavy-ion collision systems with

reaction rates up to 20 kHz. The STAR collaboration at RHIC has been performing a beam energy scan from energies down to $\sqrt{S_{NN}} = 3.3$ GeV by modifying the collider geometry experiment to a fix target one. At beam energies above $\sqrt{S_{NN}} = 20$ GeV, the reaction rates of STAR are limited to 800 Hz due to the TPC read-out, and drop down to a few Hz at beam energies below $\sqrt{S_{NN}} = 8$ GeV because of the decreasing beam luminosity provided by the RHIC accelerator. At the Joint Institute for Nuclear Research (JINR) in Dubna, the fixed-target experiment BM@N is being developed at the Nuclotron to study heavy-ion collisions at gold beam energies up to 4 AGeV. Moreover, at JINR the Nuclotron-based Ion Collider facility NICA with the Multi-Purpose Detector (MPD) is already under operation. The NICA collider is designed to run at a maximum luminosity of $L = 10^{27}$ cm^{-2}s^{-1} at collision energies between $\sqrt{S_{NN}} = 8$ and 11 GeV corresponding to a reaction rate of 6 kHz for minimum bias Au + Au collisions. The interaction rate at NICA decreases to about 100 Hz because of low luminosity at $\sqrt{S_{NN}} = 5$ GeV.

The Facility for Antiproton and Ion Research (FAIR), currently under construction in Darmstadt, Germany, will offer the opportunity to study nuclear collisions at extreme interactions rates. The FAIR Modularized Start Version (MSV) comprises the SIS100 ring, which provides energies for gold beams up to 11 AGeV ($\sqrt{S_{NN}} = 4.9$ GeV), for Z = N nuclei up to 15 AGeV, and for protons up to 30 GeV.

1.4 The FAIR facility

The international FAIR facility will provide unique research opportunities in the fields of nuclear, atomic and plasma physics, and applications in the fields of materials research and radiation biophysics including novel medical treatments and space science. The upgraded existing GSI (GSI Helmholtzzentrum für Schwerionenforschung) accelerators UNILAC (Universal Linear Accelerator) and SIS18 (SchwerIonenSynchrotron) will serve as injectors. They will be followed by a superconducting double-synchrotron SIS100 with a circumference of 1084 m and a magnetic rigidity of 100 Tm. The energies of the SIS100 will be up to 30 GeV for protons and up to 11 AGeV for Au ions. The beam intensity will be up to 10^9 ions per second resulting in 10^7 interactions per second using a 1% interaction probability in target. Figure 1.6 illustrates the existing and future installations of the FAIR facility.

FAIR will have the unique ability to provide particle beams of all chemical elements and their ions, as well as protons and antiprotons. The research program of the FAIR facility is grouped in the following experimental collaborations: APPA (Atomic, Plasma Physics and Applications), CBM (Compressed Baryonic Matter), NuSTAR (NUclear STructure, Astrophysics and Reactions) and PANDA (anti-Proton ANihilation at DArmstadt). The APPA experiment will perform tests of fundamental interactions and symmetries as well as applications of nuclear physics in medicine. The wide program of APPA will cover atomic physics, plasma, medical and space radiation physics. NuSTAR will investigate nuclear structure and dynamics of nuclear astrophysics. PANDA will focus on antimatter research, the weak and the strong forces, exotic states of matter, and the structure of hadrons.

The Compressed Baryonic Matter experiment is a next-generation experiment to be operated at FAIR. The CBM experiment proposes one of the richest and leading research programs in the field of heavy-ion physics. Its physics program aims to explore the QCD phase diagram at high baryon densities, where a first-order phase transition from hadronic to partonic matter and a chiral phase transition is expected to occur. The setup consist of a fix target forward spectrometer with fast and radiation hard detectors employing free-streaming readout electronics with a novel online reconstruction concept. For high-statistic measurements of rare probes, CBM is designed to cope with very high interaction rates up to 10 MHz [12]. The experiment is currently being developed by an international collaboration between institutes from Germany, India, Poland and other countries.

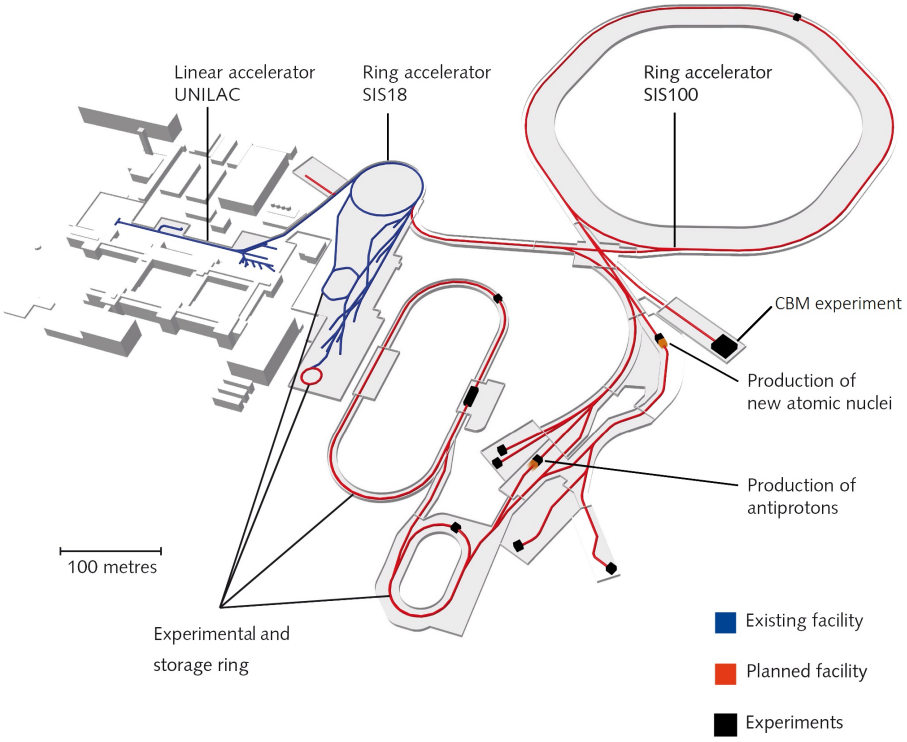


Figure 1.6: *Layout of the FAIR facility. Blue lines represents existing GSI facilities, the new accelerator complex is shown with red. The superconducting synchrotron SIS100 will provide ion beams for the CBM experiment.*

1.5 The physics program of the CBM experiment

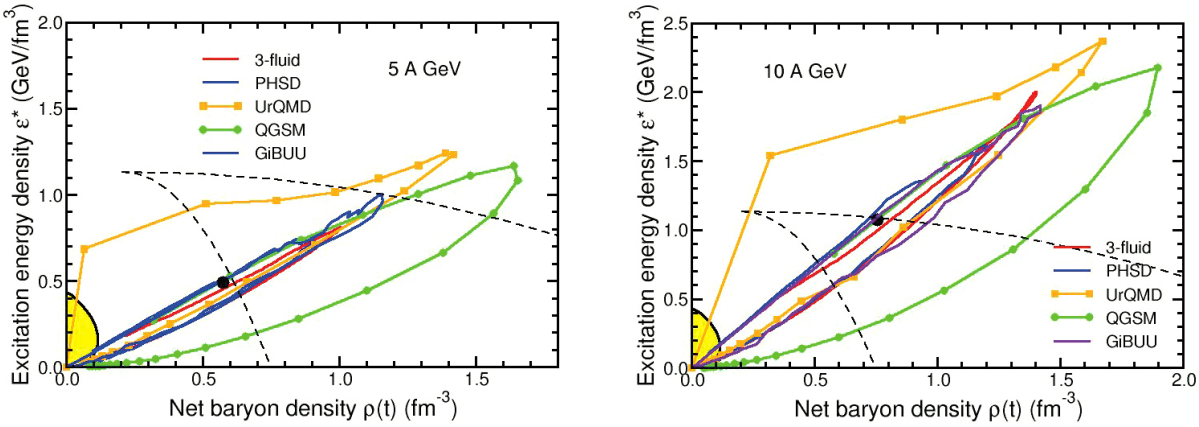
The rich physics program of the CBM experiment aims to investigate the equation-of-state of QCD matter at densities similar to the densities in the core of neutron stars, and search for a possible phase transition from hadronic to quark-gluon matter, a critical point of the QCD phase diagram, existence of quarkyonic matter, and signatures of chiral symmetry restoration [12, 13].

The CBM physics program will be able to address the following fundamental questions:

- The equation of state of QCD matter and the relevant degrees of freedom at high net-baryon densities. Is there a phase transition from hadronic to quark-gluon matter, or a region of phase coexistence? Do exotic QCD phases exist? Is there a critical point?
- To what extent are the properties of hadrons modified in dense baryonic matter? Are we able to find indications of chiral symmetry restoration?
- How far can we extend the chart of nuclei towards the strange dimension by producing single? and double-strange hypernuclei? Does strange matter exist in the form of heavy multi-strange objects?

To address these questions CBM will investigate collisions of heavy ion and proton beams, with fixed, heavy element targets, at beam energies between 2 and 14 AGeV (up to 14 AGeV for light nuclei and 29 AGeV for protons). The combination of high-intensity beams with a high-rate

detector system provides unique conditions for a comprehensive study of QCD matter at the highest net-baryon densities achievable in the laboratory.



(a) *5 AGeV* (b) *10 AGeV*

Figure 1.7: *Evolution of the excitation energy in the center of the fireball as a function of the baryon-net density calculated by different transport models and a 3-fluid hydrodynamics code. The Au+Au collision system is simulated for two different running scenarios, at 5 and 10 AGeV respectively [12].*

Figure 1.7 illustrates the excitation energy density in the center of the collision zone is shown as a function of the net-baryon density for central Au + Au collisions at beam energies of 5 AGeV and 10 AGeV, as predicted by several transport models and a hydrodynamic calculation [14]. The excitation energy is defined as a function of the energy density and the mass density. The solid lines correspond to the time evolution of the system and the dots on the curves labeled UrQMD and QGSM correspond to steps of 1 fm/c in collision time. The expected region of phase coexistence is enclosed by dashed lines.

Some significant observables that are particularly relevant for addressing the questions above will be briefly describe in the following subsections.

1.5.1 Event by event fluctuations

Event by event fluctuations of conserved quantities such as baryon number, strangeness and electrical charge can be related to the thermodynamical susceptibilities and hence provide insight into the properties of matter created in high-energy nuclear collisions [15]. Lattice QCD calculations suggest that higher moments of these distributions are more sensitive to the phase structure of the hot and dense matter created in such collisions. Non-Gaussian moments (cumulants) of these fluctuations are expected to be sensitive to the proximity of the critical point since they are proportional to powers of the correlation length, with increasing sensitivity for higher-order moments [16, 17].

Measurements of these fluctuations have been performed by other collaborations in order to search for the critical point. Figure 1.8 shows results from STAR collaboration, which depicts the volume-independent cumulant ratio $\kappa\sigma^2$ (excess kurtosis times squared standard deviation) of the net-proton multiplicity distribution as a function of the collision energy, measured in Au + Au collisions.

However, up to date no higher-order event by event fluctuations have been measured at SIS100 energies. The CBM experiment will, for the first time, perform a high-precision study of higher-order fluctuations at various beam energies in order to search for the elusive QCD critical point

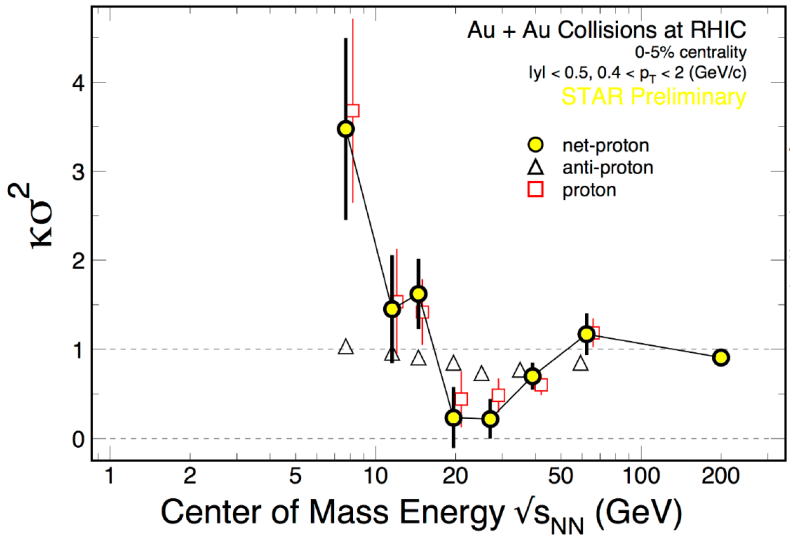


Figure 1.8: *Energy dependence of the product $\kappa\sigma^2$ (excess kurtosis times variance) of the net-proton multiplicity distribution (yellow circles) for top 0 - 5% central Au + Au collisions. The Poisson expectation is denoted as dotted line at $\kappa\sigma^2 = 1$ [12].*

in the high net-baryon density range $\sqrt{S_{NN}}$ = 2.7 - 4.9 GeV, corresponding to $\mu_B \simeq$ 800 - 500 MeV [12].

1.5.2 Collective flow

The collective flow of hadrons, resulting from heavy-ion reactions, is driven by the pressure gradient created in the early fireball and provides important information on the dense phase of the collision. The isotropic, radial flow allows to characterize the collision system at kinetic freeze-out, i.e. when elastic collisions of the produced particles come to an end. On the other hand, anisotropic flow is produced from the conversion into pressure gradients of anisotropies in the density distribution [18]. Flow effects can be characterized by the azimuthal distribution of the emitted particles in the plane transverse to the beam axis:

$$\frac{dN}{d\varphi} \propto 1 + 2\sum_{n=1}^{\infty} v_n cos[n(\varphi - \Psi_n)] \tag{1.1}$$

where N is the number of produced particles, φ is the azimuthal angle of each particle, Ψ_n is the n^{th} order symmetry plane and the v_n coefficients are related to the magnitude of the flow-vector [19].

Important observables like multi-differential flow measurements for several hadron species, in particular strange hadrons and anti-baryons, the equation of state and the properties of strange particles, are mandatory for a variety of collision systems and beam energies in the SIS100 energy range in order to address the degree of thermalization.

The direct flow (v_1) is important to understand the role of partonic degrees of freedom and it is sensitive to the softening of the QCD matter EOS, as well as to the phase transition details [21]. Figure 1.9 shows the performance for directed flow (v_1) of strange hyperons for the STAR collaboration. The directed flow slope (dv_1/dv_y) is represented as a function of the beam energy for intermediate centrality (10 - 40%) Au + Au collisions for net-protons, net-Λ's and net-Kaons. The error bars define statistical uncertainties, while the caps are systematic uncertainties [20].

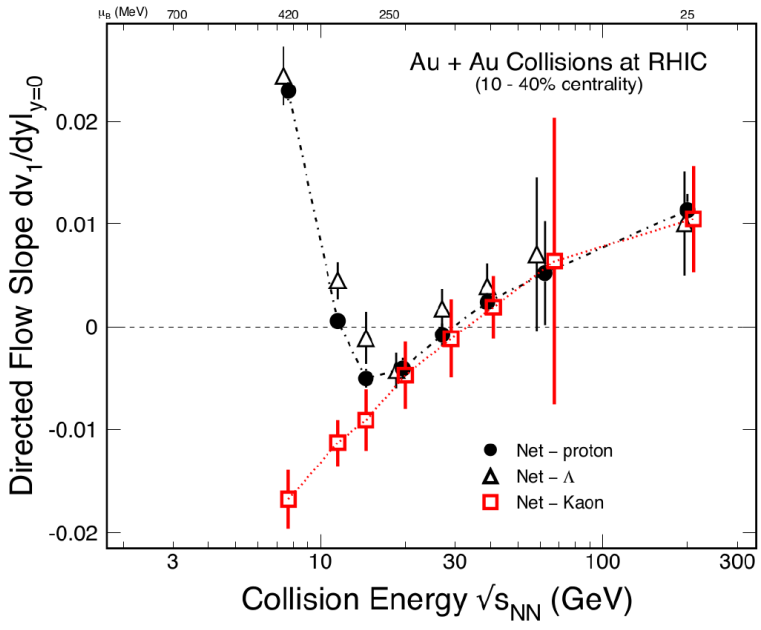


Figure 1.9: *Directed flow slope (dv_1/dv_y) versus beam energy for intermediate centrality (10 - 40%) Au + Au collisions for net-protons, net-Λ's and net-Kaons [20].*

The elliptic flow (v_2) depends on the particle transverse momentum, which can bring insights about the degrees of freedom prevailing in the early stage of the collision. At low collision energies, close to the SIS100 energy range, (v_2) measurements are only available for pions, protons, antiprotons, charged kaons, with relatively poor precision. The CBM experiment will improve this situation by measuring the flow of identified particles including multistrange hyperons and di-leptons. On the other hand, one of the main goals is to measure the flow of particles not significantly suffering from re-scattering like hyperons or mesons, for which no experimental data exist. These measurements will significantly contribute to our understanding of the QCD matter equation of state at neutron star core densities [12].

1.5.3 Lepton pairs

One of the most important goals of heavy-ion collision experiments is the search for signatures of chiral symmetry restoration at very high baryon-net densities and temperatures. Di-leptons offer a unique opportunity to investigate the microscopic properties of strongly interacting matter. Virtual photons are radiated off during the whole time evolution of a heavy-ion collision. Once produced, they decouple from the collision zone and materialize as muon or electron pairs. Hence, leptonic decay channels offer the possibility to look into the fireball and to probe the hadronic currents of strongly interacting systems in a state of high temperature and density. The degeneration of the spectral functions of chiral partners, such as the ρ-meson and the a_1-meson, is a consequence of the restoration of the chiral symmetry. While the a_1-meson is very difficult to measure in the nuclear medium, the in-medium spectral function of the ρ-meson is accessible via the measurement of its decay into lepton pairs [22]. Moreover, the excess yield of lepton pairs in the energy range ($M \leq 1$ GeV/c^2) is sensitive to the temperature of the created matter and its space-time extension. This observable should be sensitive to chiral symmetry restoration, and it is expected to be a measure of the fireball lifetime.

Figure 1.10 shows the invariant-mass spectrum of e^+e^- pairs radiated from a central Au + Au collision at 10 AGeV. The slope of the di-lepton invariant-mass spectrum between 1 and 2.5 GeV/c^2 directly reflects the average temperature of the fireball [23]. The solid red curve shows the contribution of the thermal radiation, which includes in-medium ρ, ω, 4-π spectral functions and QGP spectrum calculated using the many-body approach. The freeze-out hadron cocktail, represented with a solid grey curve, is calculated using the Pluto event generator and includes two body and Dalitz decays of π^0, ω and ϕ.

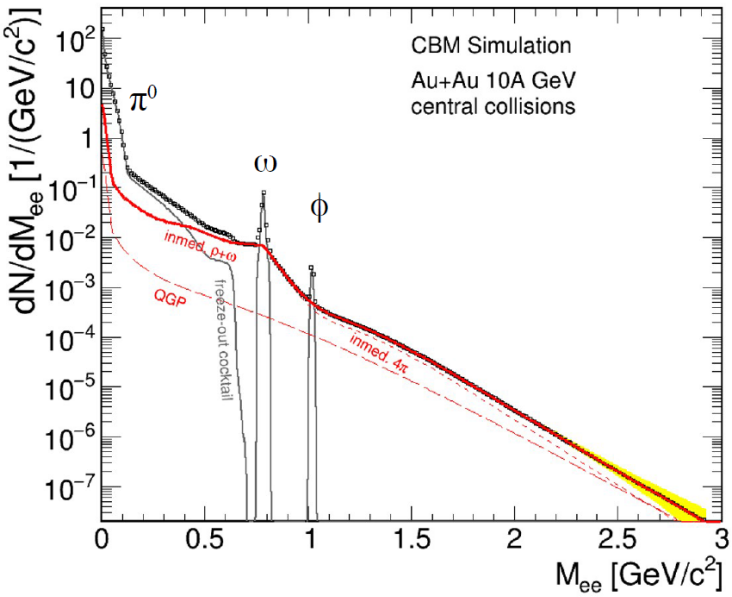


Figure 1.10: *Invariant-mass spectrum of e^+e^- pairs radiated from a central Au + Au collision at 10 AGeV [12].*

Heavy ion collision experiments have no data measured in the range of energies between 2 and 40 AGeV. The CBM experiment will perform pionering multi-differential measurements of lepton pairs over the whole range of invariant masses emitted from a hot and dense fireball. The main experimental challenges are the very low signal cross sections, decay probabilities in the order of 10^{-4} and high combinatorial background [12].

1.5.4 Strangeness and hypernuclei

High precision measurements of excitation functions of multi-strange hyperons in symmetric nucleus-nucleus collisions at SIS100 energies will allow to study the degree of equilibration of the fireball, and, hence, open the possibility to find a signal for the onset of deconfinement in QCD matter at high net-baryon densities. Strangeness production is an essential observable with possible connection to a phase transition.

According to hadronic transport models, which do not feature a partonic phase, multi-strange anti-hyperons are produced in sequential collisions involving kaons and lambdas, therefore, they are sensitive to the density in the fireball. This sensitivity is largest at beam energies close to, or even below, the production threshold in elementary collisions and is expected to shed light on the compressibility of nuclear matter.

The CBM experiment will open a new era of multi-differential precision measurements of strange hadrons including multi-strange hyperons. The expected particle yields will be sufficient to study,

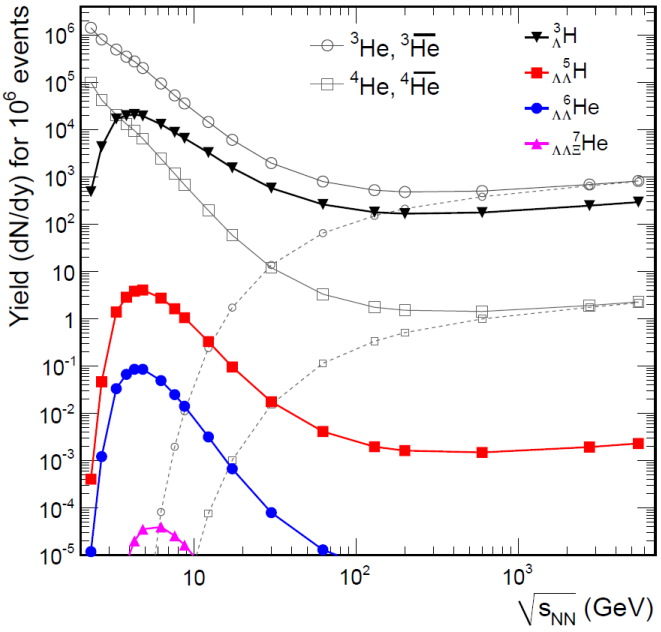


Figure 1.11: *Energy dependence of predicted hypernuclei yields at mid-rapidity for* 10^6 *central collisions. The predicted yields of* ^{3}*He and* ^{4}*He nuclei are included for comparison, along with the corresponding anti-nuclei (dashed lines) [12].*

with excellent statistical significance, the production and propagation of heavy strange and anti-strange baryons up to Ω^+ in dense nuclear matter. It will also open possibilities to identify excited hyperon states and to study hyperon-nucleon and hyperon-hyperon correlations in order to explore the role of hyperons in neutron stars, helping to reconcile the measured masses of neutron stars with the presence of hyperons in their interiors (the so-called hyperon puzzle).

Thermal model calculations show that the maximum of the hypernuclei excitation function is at SIS100 energies, see Fig 1.11. This is due to the superposition of two main effects: the increase of light nuclei production with decreasing beam energy, and the increase of hyperons production with increasing beam energy [24]. The CBM experiment has also substantial discovery potential for light double-Λ hypernuclei. Information about hyperon-hyperon and hyperon-nucleon interaction can be deduced from measuring double-Λ hypernuclei and their lifetimes, which will further our understanding of the nuclear matter EOS at high densities.

1.5.5 Open and hidden charm

Particles containing charm quarks are expected to be created in the very first stage of the reaction, and, therefore, offer the possibility to probe the degrees-of-freedom over the entire collision history. Depending on their interaction with the medium, the charm and anti-charm quarks hadronize into D mesons, charmed baryons, or charmonium [25].

There is no available data on open and hidden charm production in heavy-ion collisions at beam energies below 158 AGeV. The interpretation of existing data is complicated due to the lack of knowledge of interactions between charmed particles and the cold hadronic medium [12]. Figure 1.12 shows the energy dependence of the total nucleon-nucleon charm production cross section. In case of proton-nucleus (pA) or deuteron-nucleus (dA) collisions, the measured cross

sections have been scaled down by the number of binary nucleon-nucleon collisions calculated in a Glauber model of the proton-nucleus or deuteron-nucleus collision geometry. The NLO MNR calculation (and its uncertainties) is represented by solid (dashed) lines [26].

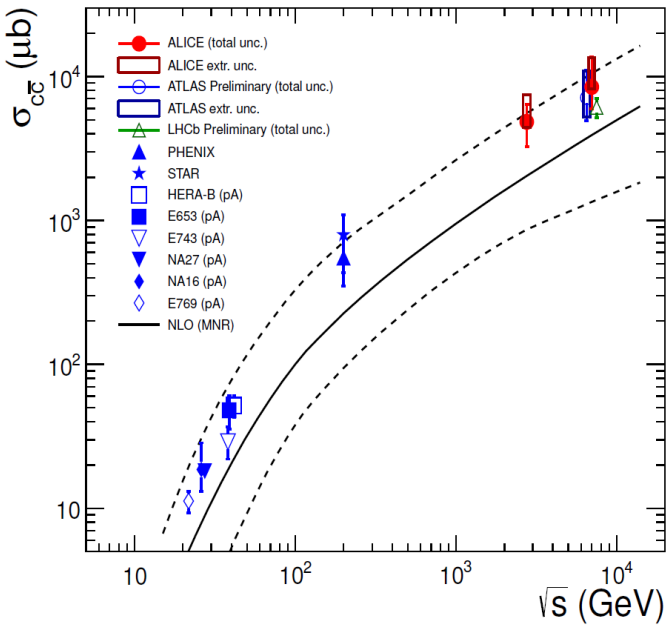


Figure 1.12: *Energy dependence of the total nucleon-nucleon charm production cross section [26].*

With CBM-SIS100, hidden and open charm production will be studied for the first time in proton-induced reactions at beam energies close to production threshold (up to 29 GeV) and different targets. At these energies, the formation time of charmonium is small compared to the lifetime of the reaction system. Systematic measurements of open charm will shed light on the charmonium interaction with cold nuclear matter and constitute an important baseline for measurements in nuclear collisions.

In a deconfined medium, charmonium states are expected to dissociate into c and $\bar{c}$ quarks due to color screening effects. This has been the first predicted signature for the QGP formation [25]. At SIS100, charmonium will be measured in collisions of symmetric nuclei up to 15 AGeV and, more challenging even, below threshold in Au + Au collisions at 10 AGeV. In order to detect this specific observable, very high interaction rates and a dedicated experimental configuration, optimized for the identification of the J/ψ, will be used in the CBM experiment [12].

1.6 The CBM experimental setup

The CBM experiment possesses a wide and challenging physics program. Many of the important observables are rare diagnostic probes carrying the information of the dense stage of the fireball evolution. The CBM detector system is designed to measure the collective behavior of hadrons, together with rare diagnostic probes such as multi-strange hyperons, charmed particles and vector mesons decaying into lepton pairs with unprecedented precision and statistics. Most of these particles will be studied for the first time in the FAIR energy range. In order to achieve the required precision, the measurements will be performed at reaction rates up to 10 MHz. This requires very fast and radiation hard detectors, a novel data readout and analysis concept including free streaming

front-end electronics, and a high performance computing cluster for online event selection [15].

The CBM detector has an angular acceptance between 2.5° and 25° to cover mid and forward rapidity hemisphere for symmetric collision systems at beam energies between 2 and 40 AGeV. The estimated data rate for the whole experiment in Au + Au collisions is approximately 1 TB/s, therefore, fast algorithms for reconstruction and event selection will be performed in real time in order to reduce by two order of magnitude the stored data.

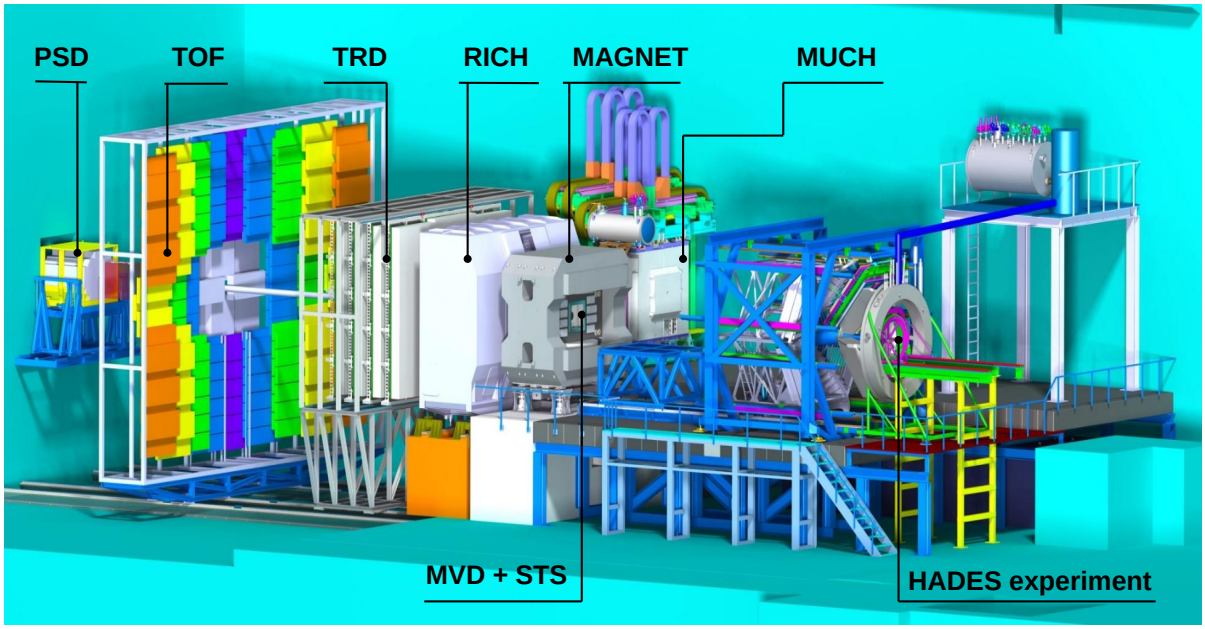


Figure 1.13: *The CBM experimental setup as part of the FAIR facility.*

The full schematic view of the CBM experimental setup concept, including the HADES (High-Angle Di-Electron Spectrometer) experiment, is shown in Fig. 1.13. It comprises the following subsystems:

- a dipole magnet for momentum measurements;
- a Micro Vertex Detector (MVD) to measure short-lived decay vertices and low-momentum particles;
- a Silicon Tracking System (STS) to provide tracking of charged particles and to measure their momentum;
- a Muon Chamber (MUCH) for muon identification and track reconstruction;
- a Ring Imaging Cherenkov detector (RICH) to provide electron/pion identification;
- a Transition Radiation Detector (TRD) to suppress pions and to support track reconstruction;
- a Time-of-Flight (ToF) wall for hadrons identification;
- a Projectile Spectator Detector (PSD) for the collision centrality and event plane determination.

The CBM detector system can be used in two operation modes: the first one is optimized for electron identification (all the subsystems apart from MUCH will be involved) and the second is specialized for muon identification (the RICH detector will be replaced by MUCH).

Superconducting dipole magnet

The superconducting dipole magnet serves to bend charged particle trajectories in order to determine their momenta. The device is essential for particle momenta determination of all charged particles for the CBM experiment. It will be superconducting in order to reduce the operation costs. The superconducting dipole magnet provides a vertical magnetic field with a field integral of 1 Tm from the interaction point to approximately 1 m downstream the target [27].

Micro Vertex Detector (MVD)

The main task of the MVD is to distinguish between primary vertex and displaced vertices, for example, to reconstruct decays of charmed hadrons: D-mesons or Λ_c baryons. This task requires a high resolution along the position vector of approximately 70 μm, which turns to 5 μm spatial resolution and low material budget.

The MVD is located directly behind the target (5 - 20 cm downstream) inside the dipole magnet. The MVD is placed in vacuum, thus it is able to reconstruct low-momentum tracks that helps to reject background for di-electrons [28]. Due to the limited readout speed, the MVD will participate only in data taking with the interaction rate up to 10^5 Hz [28, 29]. The requirements of high spatial resolution, low material budget and high radiation tolerance are fulfilled with CMOS Monolithic Active Pixel Sensors (MAPS) with fine pixel size of several dozens of μm. Being operated in the target chamber vacuum, the sensors need to be cooled, with the total anticipated power of 300 W.

Muon Chambers Detector (MUCH)

The experimental challenge for muon measurements in heavy ion collisions at FAIR energies is to identify low-momentum muons in an environment of high particle densities [15]. It is experimentally challenging to identify low-momentum muons in heavy ion collisions due to the high particle multiplicity [15]. The reconstruction of di-muon decay channels of vector mesons like ρ, ω, ϕ and J/ψ requires a very precise muon identification. The MUCH system in combination with STS are the main detectors in CBM to perform this task [30]. The MUCH is located downstream the STS detector and it will be replacing the RICH detector in the CBM muon configuration. It will be operated in different setup configurations by varying the positions of the absorber-detector combinations. The design of the MUCH detector system consists of 5 hadron absorber layers (60 cm thick carbon plate followed by four iron plates of 20 cm, 20 cm, 30 cm and 100 cm thickness) and several gaseous tracking chambers located in triplets behind each iron slab. The tracking planes are based on Gas Electron Multiplication (GEM) [31] and Resistive Plate Chambers (RPC) detectors.

Ring-Imaging Cherenkov Detector (RICH)

The RICH detector is designed to provide identification, via Cherenkov radiation [32], of electrons and suppression of pions in the momentum range below 8 GeV/c. The electron identification efficiency reaches values above 85% and the suppression factor for pions is above 300, which in combination with TRD will allow to reduce drastically the pion contamination. The RICH detector, located behind the dipole magnet, about 1.6 m downstream of the target, will be used in the electron-hadron configuration of the CBM setup. The detector design consist of a 1.7 m long CO_2 gas radiator and two arrays of mirrors and photo detector planes. The gas constituents and its pressure are chosen to cover the largest possible momentum range. The photo detector planes

are based on Multi-Anode Photo-Multipliers (MAPMTs) (Hamamatsu H12700) in order to provide high granularity, high geometrical acceptance and high photon detection efficiency. In order to direct the light to the high granularity photon detectors the mirrors of the RICH detector are constructed with a reflective Al + MgF_2 coating [33].

Transition Radiation Detector (TRD)

The TRD is a particle identification detector complementary to the RICH setup. In order to allow a measurement of dielectrons with good signal to background ratio, a pion suppression factor in the range 10 - 20 and an electron efficiency of 90% have to be achieved. Additionally, TRD will provide tracking between the RICH and the TOF detector and it will be used as tracking station in the muon configuration of CBM, providing spatial resolution about 300 μm. The detector system will be located at approximately 5 m downstream the target and it will be composed of one station with four layers. The detector will be based on Multi-Wire Proportional Chambers (MWPCs) in combination with a radiator and it will separate the electron and positron candidates from the pion background for momenta above 2 GeV/c. The readout will be realized in rectangular pads. The particle identification concept is based on the fact that ultra-relativistic charged particles are going to produce transition radiation when traversing a boundary between media with different dielectric constants [15].

Time of Flight Detector (ToF)

An array of Multi-gap Resistive Plate Chambers (MRPCs), which provides an efficiency higher than 95% and a time resolution of approximately 60 ps, will be used for hadron identification via ToF measurements. The detector will posses a granularity in the range from 2 kHz (in the periphery) to 25 kHz (in the central region) depending on the hit rate variations. The ToF wall will be placed at 6 m downstream the target (for SIS100 energies) [34] and it will cover an area of 120 m^2. In order to achieve the required rate capability, MRPCs are built using low-resistivity glass [35]. The main task of the ToF detector is hadrons identification: pions, kaons and protons.

Particle Spectator Detector (PSD)

The PSD is a full compensating modular lead-scintillator calorimeter which provides very good and uniform energy resolution. The detector is designed to measure the number of non-interacting nucleons from a projectile nucleus in nucleus-nucleus collisions. PSD detector system will be used to determine the centrality and the orientation of the reaction plane. A precise characterization of the event class is of crucial importance for the analysis of event-by-event observables. The study of collective flow requires a well defined reaction plane, which has to be determined by a method not involving particles participating in the collision [15]. It will comprise 44 individual modules, each consisting of 60 lead/scintillator layers with a surface of 20 $\times$ 20 cm^2. The scintillation light will be read out via wavelength shifting (WLS) fibers by Multi-Avalanche Photo-Diodes (MAPD) with an active area of 3 $\times$ 3 mm^2 [36].

First Level Event Selector (FLES)

The CBM physics program requires high-statistics measurements, which lead to high interaction rate and high data rate. For a traditional data acquisition and storage architecture a maximum interaction rate of 100 kHz can be achieved. The data readout concept for the CBM experiment employs no hardware trigger, thus it will push all detector raw data to an online computing farm. For high interaction rates, an online event selection algorithm, which rejects the background events at least by a factor of 100 before the data can be stored is required.

The First Level Event Selector is a dedicated computing farm intended to reduce online the raw data volume by more than two orders of magnitude, but still making possible the online reconstruction of full event topology including long-lived charged and short-lived particles. The basis for the online event selection will comprise fast and fully parallelized algorithms for reconstruction of hits, tracks and short-lived particles. The online CBM FLES will consist of nodes equipped with modern many-core central processing units (CPU) and graphic cards with the total power of about 60 000 CPU cores equivalent [37].

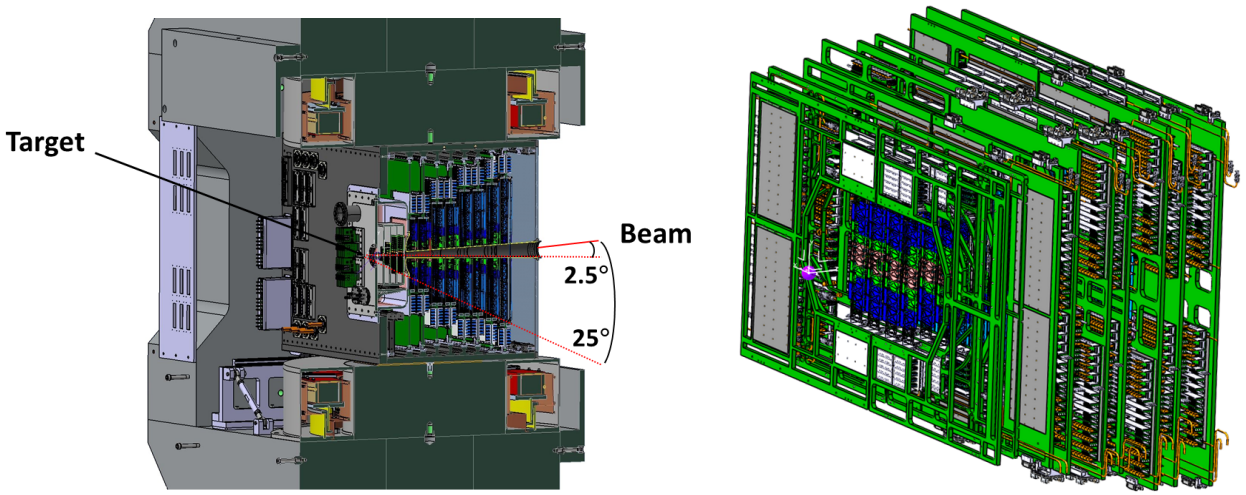
1.7 The Silicon Tracking System

The Silicon Tracking System (STS) main task is to measure charged particles momenta with high resolutions (1.5% for p $\geq$ 1 GeV/c), and to reconstruct their tracks with an efficiency higher than 95% for p $\geq$ 1 GeV/c. In order to minimize the multiple Coulomb scattering and the production of delta electrons and conversion electrons, the tracker needs to have a low material budget. The experimental conditions pose demanding requirements in terms of channel density and readout bandwidth to be met by the front-end electronics. The main requirements for the STS design can be summarized below:

- The detector is contained in a volume of approximately 1.4 $\times$ 2.3 $\times$ 1.3 m^3 inside the superconducting CBM dipole magnet.
- It must be capable of measuring up to 1000 particles per central Au + Au collision at interaction rates up to 10 MHz at SIS100.
- It requires radiation hard silicon sensors, which should be able to stand up to 10^{13} 1 MeV n_{eq} during the operation.
- The material budget should be kept as small as possible.
- The sensors will be readout using fast and self-triggered front-end electronics (FEE),
- The FEE must keep a reliable performance in a radiation environment of up to 100 krad/yr.
- The cooling system should be capable of removing up to 50 kW of dissipated heat from inside the detector box.

The detector system consists of 876 double-sided silicon micro-strip sensors arranged in 8 tracking stations covering a physics aperture of 2.5° $\leqslant \Theta \leqslant$ 25°. It is placed between 30 and 100 cm downstream the target, inside 1 Tm dipole magnetic field [38]. Detector modules are mounted on low mass carbon-fiber support structures [39], keeping the readout electronics in the periphery of the detector, out of the physics acceptance. The signals from the sensors are transferred to the FEE via ultralight readout cables with up to 50 cm length. Figure 1.14 (a) shows a schematic of the eight STS tracking stations inside the dipole magnet and the detector modules mounted on low mass carbon-fiber support structures (b).

The STS detector is installed in a thermally isolated box and inserted into the dipole magnet. This box serves as supporting structure for target, beam pipe and for the STS and MVD detectors. During operation, a thermal power of about 50 kW will be continuously dissipated by the whole system. The front-end and readout electronics contribute with the largest amount (approximately 40 kW), while the rest is mostly generated by low voltage power cables, heat transfer via the walls of the STS box and a small amount from the sensors itself (approximately 6 mW/cm^2). In order to keep the operation temperature in the desired range, the cooling system is to ensure that sensors are operated at a temperatures below -5° C. The use of gas convection for the sensors will ensure



(a) *The STS inside the dipole magnet* (b) *Eight tracking stations for the STS detector.*

Figure 1.14: *Design concept of the STS. The detector is placed inside the superconductive dipole magnet between 30 cm and 100 cm downstream the target. The 8 tracking stations cover the physics aperture between 2.5° and 25°.*

minimal material budget inside the physics acceptance. Humidity levels should be kept very low in order to avoid condensations in the sensors. For cooling the readout electronics, the cooling blocks will be tightly connected to the boxes holding the FEE at the top and bottom sides of the STS [38].

1.7.1 The STS detector module

The STS building block is the detector module, which consists of a double-sided silicon microstrip sensor connected through a stack of low-mass aluminum polyimide readout cables (microcables) to the custom-developed ASICs on two front-end boards (FEBs).

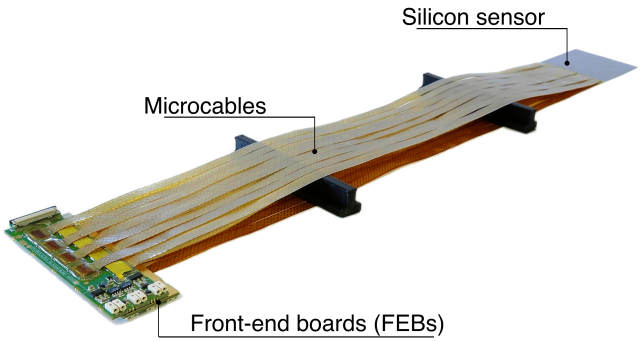


Figure 1.15: *The detector module is the functional building block of STS. Every module consits of a double-sided silicon sensor, connected via a stack of microcables to the FEBs. The photo illustrates the module before the shielding layers are soldered [43].*

Figure 1.15 represents a full detector module before the shielding layers are applied. The sensors, produced by Hamamatsu Photonics K.K with 320 μm thickness, have been designed on a common base layout in four different strip lengths in order to adjust the detector granularity to the expected particle densities [38]. For the signal transmission, two layers of microcables with aluminium strips

and a pitch of 116 μm are used to interconnect the sensors with the STS-XYTER ASICs bonded onto a FEB type 8 carrying 8 chips, each of them reading 128 channels (for more details about the STS-XYTER ASICs see section: General description of the STS-XYTER v2.2 ASIC). The microcables are separated with a meshed spacer in order to reduce the parasitic inter-layer capacitance and they are covered with two shielding layers in order to reduce the electromagnetic interference.

1.7.2 Silicon micro-strip sensor

Silicon sensors play a central role in modern High Energy Particle Physics experiments for tracking and momentum determination of charged particles due to their fast response, high radiation tolerance and good spatial resolution. STS sensors have been designed on a common base layout in four different strip lengths using double-sided micro-strip sensors technology. Each sensor side has 1024 strips (two interconnected short-length strips in the p-side are counted as one), positioned with a pitch of 58 μm. The double-side technology has the advantage of providing 2D tracking position in the same amount of silicon material, while sensors segmented into strips on one side only, require twice the sensitive material. The sensors are produced on 320 μm thickness n-type wafers, by Hamamatsu Photonics K.K., Japan. Figure 1.16 shows the double-sided silicon micro-strip sensors family that will be used for the STS detector.

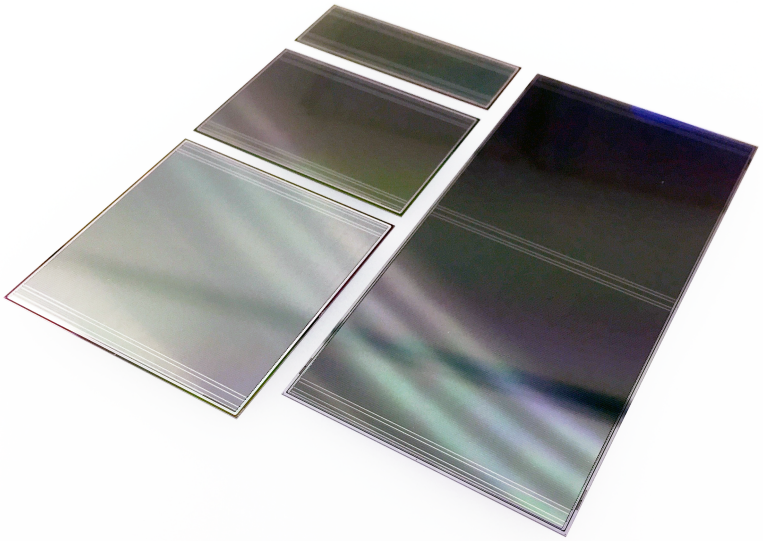


Figure 1.16: *STS detector silicon sensors family. They will be produced with the same width of 6.2 cm and four different strip lengths (2.2 cm, 4.2 cm, 6.2 cm and 12.4 cm), matching the track densities in the STS detector.*

The strip implants (p+, n+) are 10 μm wide and each strip is connected to the bias line with a poly-Si resistor. The strips are AC-coupled to the readout electrodes via a thin SiO_2 insulation layer in order to avoid the need of the leakage current compensation circuitry in the front-end electronics. On the n-side of the sensors, strips are at right angle with respect to the sensor edges, while on the p-side strips will be inclined by 7.5° in order to keep the number of ghost hits at minimum values. Stereo angle of 7.5° results in having shorter strips at the edges of the sensor. The short strips in the upper left and lower right corners are interconnected between their readout layers through horizontal routing lines on a metal layer. In this way, they can be readout from the same edge. The number of corner strips will depend on the sensor variant [40]. Guard rings shape the field inside the sensitive area to minimize edge effects and to guarantee a defined homogeneous potential

for all strips, including the edge ones. The guard rings are p and n-type implants, DC-coupled to aluminum electrodes on floating potential.

The radiation tolerance is a vital quality for the silicon micro-strip sensors due to the severe radiation conditions in the STS environment. It is expected that the innermost sensors in the STS detector have to withstand a NIEL (Non-Ionizing Energy Loss) damage up to 10^{14} 1 MeV $n_{eq}cm^{-2}$ and an ionizing dose around 11 Mrad during the SIS100 operation. The radiation hardness was confirmed up to twice the expected lifetime fluence [39, 40]. The sensor's charge collection efficiency decreases by 15 - 20% after irradiation to twice this level.

1.7.3 Al-polyimide low mass microcables

In order to transfer the analogue signals from the sensors to the front-end electronics, low mass aluminum microcables are used. The front-end electronics are mounted in the detector periphery due to material budget constraints. For the final STS detector, microcables up to 50 cm length are foreseen to be used inside the physics acceptance. They are manufactured at Research and Production Enterprise LTU through a lithographic process from polyimide-coated aluminum foil. The base material for this microcables is 14 μm aluminum covered with a 10 μm thick insulating polyimide (PI) substrate layer. Each microcable has 64 aluminum traces with a width of 30 μm and a pitch of 112 μm, structured with a photo lithographic process and wet etching. In the TAB-bonding area the width is 45 μm and the pitch is 116 μm. This results in $2048/64 = 32$ cables, eight different cable types, which have to be connected to each sensor in order to complete a module [38].

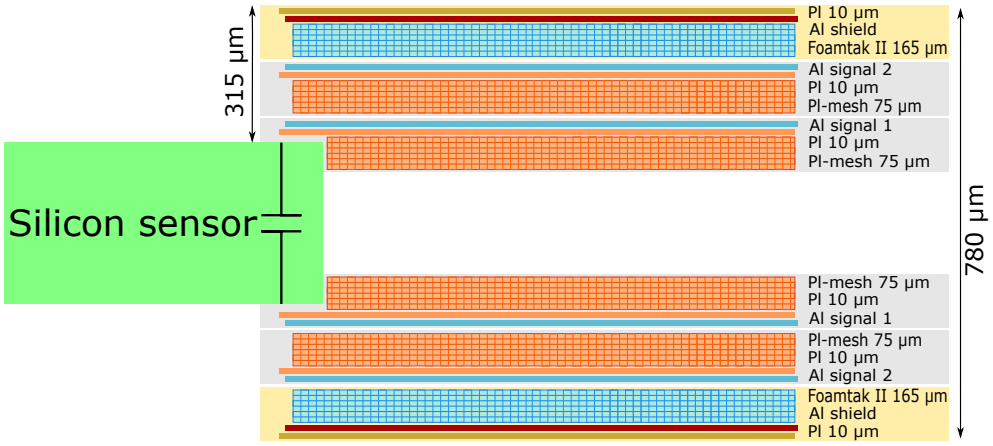


Figure 1.17: *Cross section of two layers of microcables connected to a silicon sensor.*

Figure 1.17 illustrates the cross section of microcables attached to a silicon sensor. Each multi-layer analog cable consists of two signal layers built from aluminum-polyimide adhesiveless, two meshed spacers based on Kapton (75 μm thick) and a shielding layer with Foamtak II spacer. The shielding layers are needed in order to reduce the electromagnetic interference and electrically insulate the stacked modules on a ladder. They are built from the raw material 14 μm aluminum covered with 10 μm Polyimide and a foamed Polystyrol with 165 μm thickness, leading to a total thickness of about 780 μm for the stack.

For the signal transmission, two layers of microcables with aluminum strips with a pitch of 116 μm are used. They are separated with a meshed spacer in order to reduce the parasitic inter-layer capacitance. To reduce the material budget, meshed spacers are used with a cross-shaped structure. The supporting material for the aluminum strips is 20 μm polyimide.

1.8 The STS readout chain

The CBM physics program, only achievable with a very high interaction rates, impose strong constraints on the detector performance and the Data Acquisition (DAQ) system capabilities. CBM will implement a free-streaming DAQ with no hardware trigger, which means a combination of self-triggered front-end electronics (FEE), fast free-streaming data transport, online event selection and event reconstruction [41, 42].

The STS readout chain needs to assure all controls and functionalities required by the system and sufficient data throughout to store all relevant information. For this purpose, the readout chain will contain more than 14000 STS-XYTER ASICs, around 1792 front-end boards (FEBs), 600 readout boards (ROBs) and 2400 optical links between the common readout interfaces (CRIs) and the ROBs. STS will produce around 500 GB/s of data with a signal rate up to 150 kHz/channel. All the data have to be read out by thousands of high-speed optical links from the detector for further processing and data reduction algorithms. Figure 1.18 shows a general readout chain scheme for the STS detector. The digitized data from the FEBs are aggregated in the ROBs and shipped out from the detector box via high-speed optical links. Afterwards the CRIs, placed in the experiment service building, will execute the pre-processing data together with the clock and control commands distribution. A very fast and efficient computer farm, located 700 m away from the experiment, will implement the online selection using high parallelized algorithms. The main components of the CBM readout chain can be described as:

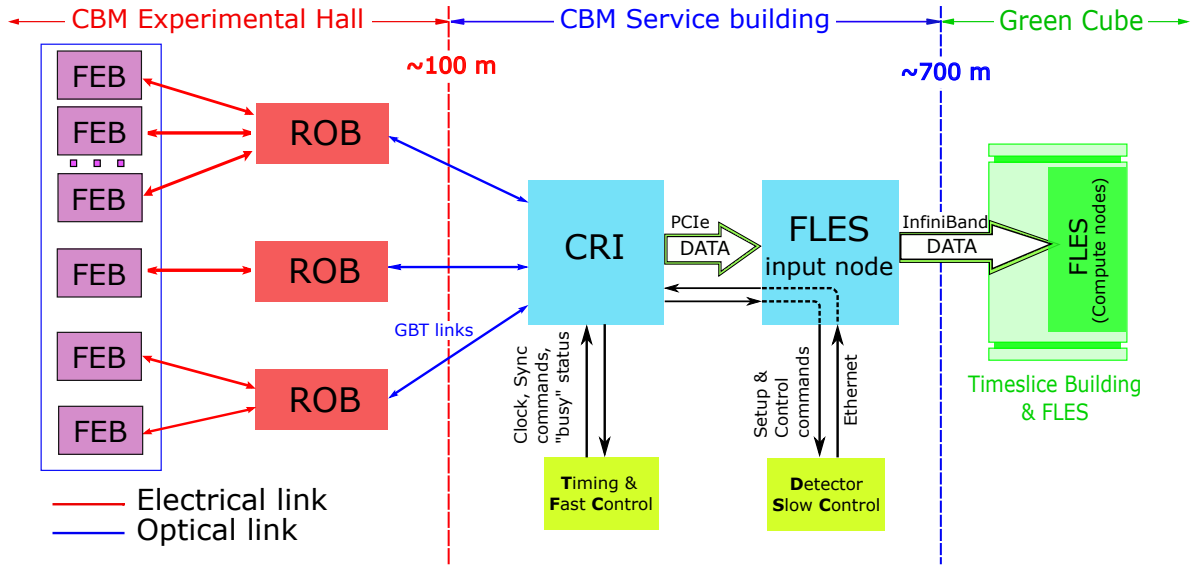


Figure 1.18: *Block diagram of the STS readout chain concept [43].*

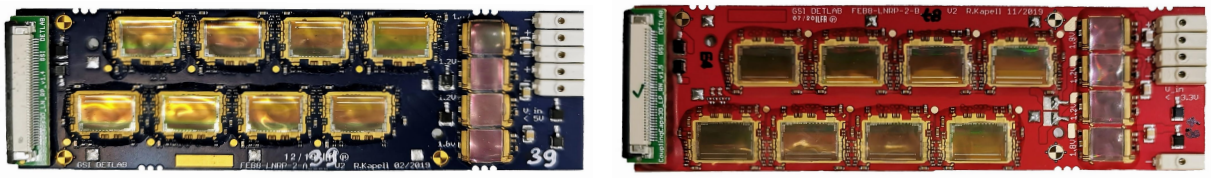
- **Front-end board (FEB):** carrying 8 STS-XYTER ASICs with 128 channels each [44]. The ASICs provide an electrical interface (Low Voltage Differential Signal (LVDS)) to the readout as well as the generation of individual hit data with ADC and timestamp information;
- **Readout board (ROB):** based on the CERN GBT (Giga Bit Transceiver) ASIC, aggregates the data from one or several FEBs and implements an electrical to optical interface. On the front-end interface, the ROB supports up to six clocks and down-link for front-end control and up to 42 readout links on three GBTX devices [45];

- **Common readout interface (CRI):** a Field Programmable Gate Array (FPGA) based board, for data pre-processing, timing distribution and interface to slow and fast control. The CRI also acts as interface for the detector control and the CBM first level event selector (FLES);
- **First level event selector (FLES):** responsible for time slice building, online event selection and full event reconstruction.

1.8.1 Front-end board

Sensors of varying lengths (from 2.2 to 12.4 cm) will be connected with the readout electronics via bundles of dedicated ultra-light and shielded microcables. A custom-designed STS-XYTER ASIC will be performing the signal readout of the silicon sensors. Further details regarding the chip design, operation and performance are shown in chapter 2: Test and characterization of the STS-XYTER v2.2.

Eight STS-XYTER ASICs are mounted on a front-end board (FEB), reading out 1024 channels of one sensor side. The chips are positioned in a staggered scheme in order to match the sensor width and strip pitch. To enable sufficient bandwidth allocation, each chip can be configured to provide 1, 2 or 5 readout links at 320 Mb/s each depending on the expected local data load. The FEBs will be located at the perimeter of the detector stations (outside the physics acceptance), mounted in a shelf structure that is in contact with a cooling plate to remove the power dissipated by the electronics. The main function of the FEB board is to apply appropriate power supply voltages to the ASICs and to provide a capacitive coupled data interface, which establishes the connection of the LVDS lines (clock, down-link and up-links) to the readout board.



(a) *Prototype design of the FEB-8 type A.* (b) *Prototype design of the FEB-8 type B.*

Figure 1.19: *Prototype design of the FEBs-8 for reading out 1024 channels from the silicon sensors for p- and n-side.*

Figure 1.19 shows a prototype design of the FEB-8 type A (left side) and type B (right side) with dimensions of approximately 10 × 3 cm^2. On the left side of the PCB of each FEB, there is a 40-pin ZIF connector on an adapter PCB, in order to connect a flat cable with LVDS signal lines to the readout board. The capacitive coupling of the data signals is realized with 36 high voltage SMD capacitors vertically arranged below the ZIF connector PCB. Right next to the ASICs, four custom designed radiation hard linear regulators developed at the Semiconductor Laboratory SCL Chandigarh in India [46] are mounted on the board, providing three low noise supply voltages to the chips. The input voltages for the FEB-8 can be applied to five single wire clamps at the upper right edge of the PCB. For operating each silicon micro-strip sensor, two FEBs-8 are needed: one is assigned to the p-side and the other one to the n-side of the sensor [38]. The e-links between FEBs and ROBs will be AC-coupled in order to allow the connection of a single ROB to multiple FEBs operated at the different high voltage biasing potentials.

1.8.2 Readout board

The electrical interface between FEB and Readout board (ROB) is realized using flexible flat cables (FFCs) for the e-links in order to provide control and clock distribution in down-link direction and for data readout and control responses in the up-link direction. The main purpose of the ROB is the data aggregation from many electrical readout links and multiple FEBs and ASICs, together with the electrical-to-optical interface to connect the experimental area in the underground cavern to the CRIs on the surface. In addition, clock as well as slow and fast control commands are distributed to the front-ends [47].

The ROBs will be located out of the physics acceptance but inside the STS detector box and the CBM dipole magnet. They are arranged in stacks outside the sensor acceptance where radiation exposure from interactions at the highest design rates reaches levels up to 100 krad for Total Irradiation Dose (TID), and around 2×10^{13} n_{eq}/cm^2 for NIEL over 10 years of operation. Therefore, the devices of the CERN Gigabit Transceiver (GBT) and Versatile Link project have been elected to provide the functionality and the radiation tolerance required.

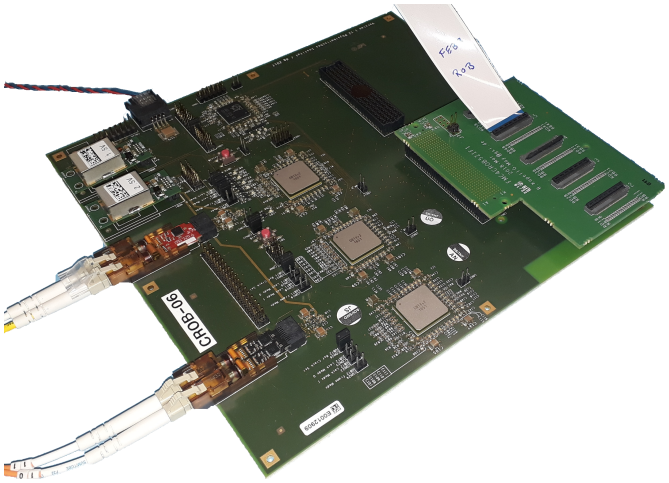


Figure 1.20: *The C-ROB board including three GBTx chips, a GBT-SCA ASIC and Versatile Links components [43].*

The STS-ROB will implement three GBTX chips. The first GBTX (master), connected to a Versatile Link VTRX bidirectional optical transceiver module and two additional GBTX (slaves), connected to the second type of Versatile Link module. The VTTX twin transmitter module will provide two optical interfaces for unidirectional data transmission in the up-link direction from the detector to the data acquisition system [45]. Each ROB will provide six phase adjustable clocks and six down-links at 160 MHz, which allow to connect up to six FEBs. It will support 42 readout links at the maximum supported rate of 320 MHz, but only 40 of those will be used in the STS system. The optical up-links provide a user bandwidth of 4.48 Mb/s/link, which matches by design the E-Link bandwidth on the front-end side. The ROBs will be externally supplied with 1.5 V (GBTX, SCA) and 2.5 V (VTRX, VTTX) from FEAST modules on dedicated POBs similar to the FEB powering [47].

The CBM Common Readout Board (C-ROB) is an approach for all CBM GBTX based readout chains. It is an early prototype of the final ROB with a different form factor that includes other functionalities that can be exploited during the testing phase. It uses concepts, hardware, protocol and firmware solutions that can be shared among various readout chains to the largest possible extent. Figure 1.20 shows the existing C-ROB populated with the optical transceivers and the custom-designed ZIF-to-FMC card.

1.8.3 Common readout interface

Data readout from a ROB will be done through the three available optical up-link fibers: one from the master GBTX via the VTRX transceiver, and two from the slave GBTX via the VTTX transceivers. The control access to the ROB will be exclusively via the optical down-link on the VTRX to the master GBTX device.

The Common Readout Interface (CRI) is a common FPGA hardware platform for CBM with system specific firmware. The CRI will implement the back-ends of the optical interfaces to multiple readout boards. This includes adaptations of the GBT-FPGA core, which handles the communication with the GBTX devices as well as the back-end of the ASIC communication protocol. Preprocessing of the hit data stream includes address expansion, time alignment of data from multiple sources and building of micro slices, which are data containers for all hit data created in a given time interval. The CRI implements the interface to the detector control system (DCS) connected to the back-end of the communication protocol for the front-end ASICs. In addition, the CRI also implements the interface to the Timing and Fast Control System (TFC), which merges synchronization and fast control commands such as Start/Stop of acquisition or throttling commands coming from the TFC master into the local down-link streams [45].

The the Data Processing Board (DPB) is a multipurpose platform for testing and developing the readout chain of different detectors. The DPB consist of an FPGA-based board, a dedicated firmware and a custom-designed interface card to connect the FEE or the ROB. The hardware solution adopted by several CBM subsystems is based on the AMC FMC carrier Kintex 7 (AFCK) board [48, 49]. Even when the DPBs are widely used for development and test purposes, the final solution for the CBM readout will be the CRI board.

Chapter 2

Test and characterization of the STS-XYTER v2.2

The custom developed front-end chip for reading out the double-sided silicon sensors in the STS detector is the STS-XYTER ASIC. It is a low power, self-triggering ASIC with 128 channels, 5-bit ADC charge and 14-bit timing information. The experimental conditions pose demanding requirements in terms of channel density, readout bandwidth and low noise levels for the front-end electronics. The chip also needs to be fully integrated into a confined space and it should perform in a high radiation environment. Other versions of the STS-XYTER ASIC have been produced and characterized before [43, 50, 51]. Since this is the final version aiming to be used in the STS detector, a full characterization of the chip is a key aspect for the future experiment.

This chapter aims to verify the STS-XYTER v2.2 functionalities. It is structured in several sections and it will cover from the characterization of the analog front-end until a detailed study of the noise performance, including validation of the calibration procedures.

2.1 General description of the STS-XYTER v2.2 ASIC

The STS-XYTER v2.2 ASIC is a multichannel integrated circuit designed for the STS and MUCH detectors readout. The chip enables time and amplitude measurement in each of the 128 channels and fast data readout via a dedicated protocol over a GBTx-based DAQ structure [52]. It is fabricated in a UMC 180 nm CMOS process, occupies an area of 10.0×6.7 mm^2 and it uses enclosed layout transistors (ELT) nMOS as a trial for enhancing the radiation hardness. It uses a redesigned set of input amplifiers, improved shapers, enhanced testing features, reference sources with enhanced stability of the analog to digital converter (ADC), new back-end and a pad layout to meet specific conditions in the STS assembly procedure [53, 54].

The ASIC includes 128 Analog Front-End (AFE) channels with 14-bit time and 5-bit amplitude measuring circuits. It has a set of full-custom configuration registers, calibration circuits, common biasing blocks and a band-gap reference voltage. The digital back-end is designed for a maximum clock frequency of 160 MHz, providing access to configuration registers, free streaming digital readout, time stamp wise sorting of acquired hits and multiple diagnostic features. Two additional test channels located at the two sides of the chip are supplied with buffered outputs of internal signals [55].

The chip uses a charge sensitive amplifier (CSA) with ELT NMOS input transistor biased with nominal 2 mA drain current and supplied from a separate, lower 1.2 V power supply (VDDM). The amplifier uses gain switching: 9.2 mV/fC (STS) and 1.6 mV/fC (MUCH) to address the different dynamic range requirements. There is a polarity selection circuit (PSC) with the purpose of having only one pulse polarity in the proceeding stages, although there is a possibility to work with both

input signal polarities. A pulse is fed directly to the shapers if positive charges are integrated or inverted by the differential amplifier for negative input charges. Two parallel signals paths are used for pulse processing. A *fast* path, built from a CR-RC filter with 30 ns peaking time, followed by a comparator for the determination of the input charge arrival time. A *slow* path, using a filter of two amplifiers with a CR-$(RC)^2$ characteristic, followed by a 5-bit flash ADC for low noise energy discrimination and measurement. Figure. 2.1 shows a functional diagram of the ASIC.

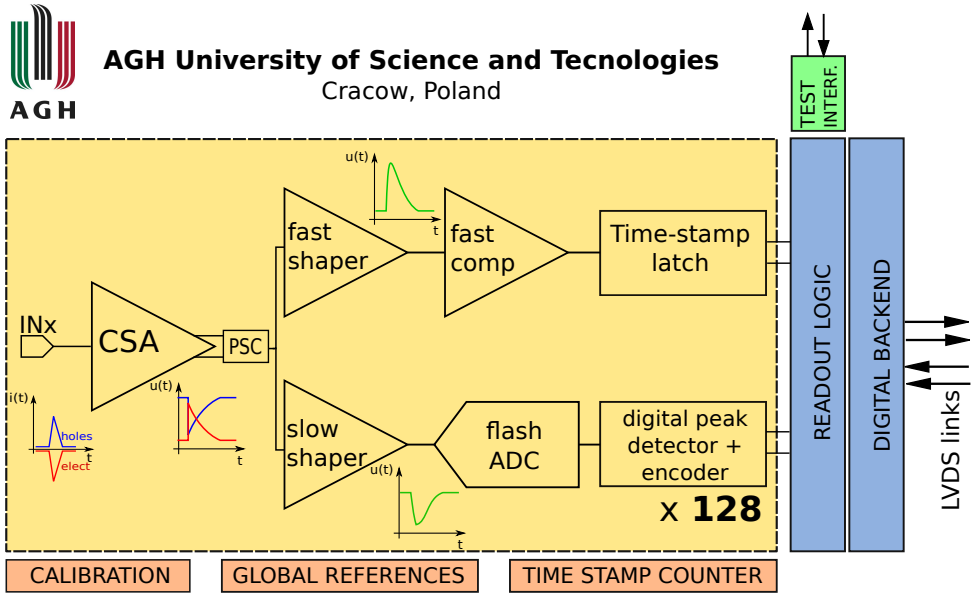


Figure 2.1: *A functional diagram of one channel of the STS-XYTER v2.2 ASIC [53].*

The back-end logic serves for register access, data read-out and streaming. It additionally provides some diagnostic features like single event upset (SEU) counters, a link error monitor, link diagnostics and deterministic test hit generation. For the purpose of efficient hit data transfer in the STS and the MUCH detectors, a dedicated protocol, named STS-HCTSP [56], has been developed. Specific features of this protocol are a novel, low-level link reset and synchronization method, deterministic delay and asymmetrically optimized data transfer and finally a quite small effective compression factor. The full chip storage capacity is approximately 1024 hits, which take between 123 μs and 26 μs to empty, depending on the number of active serializers from 1 to 5. The number of active serializers is related to the physical structure of the detector DAQ structure and depends on the chip location in the detector and the local data rate.

2.1.1 Hit generation mechanism

The STS-XYTER v2.2 operates in self-triggered mode. The hit information contains: 14-bit timestamp, 5-bit amplitude, 7-bit channel information and 1-bit event missed flag. The hit mechanism diagram is illustrated in Fig. 2.2. For the hit generation mechanism, every time the fast comparator fires, the new 14-bit timestamp value is stored in the timestamp latch. Once a slow shaper signal crosses the ADC's first comparator threshold, which typically occurs a few tens of ns later, the timestamp latching is blocked by means of the *block_ts* signal. During the following several hundreds of nanoseconds, the pulse driving the ADC reaches its peak and returns to the baseline. The peak detector keeps the maximum of the slow shaper's output (the highest discriminator). As soon as the slow path signal falls below the lowest threshold discriminator, the *data_valid* flag is asserted and the hit data are ready to be written into the 8 word deep channel FIFO. All signals

are then synchronized with the back-end clock in the channel logic. If the channel FIFO is not full and the channel is not masked, the hit is written into the FIFO and the channel is reset once the operation is completed. When this happens, the channel is reset and becomes ready for the next hit. The event missed flag is asserted if, in between, the ADC's first comparator goes high again or if the channel FIFO is full when a new hit should be written. For the successful operation of the AFE, the timing comparator threshold should be configured low enough to ensure latching of timestamp values whenever the first ADC comparator threshold is exceeded [53].

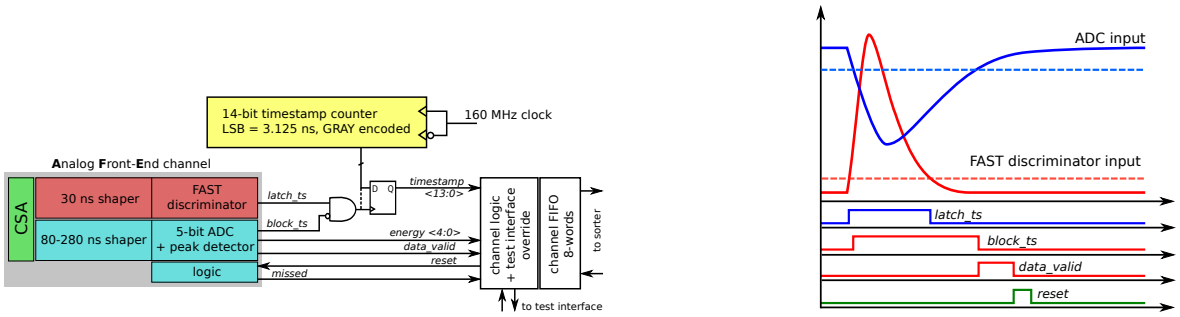


Figure 2.2: *Schematic of the hit generation mechanism. The hit generation logic is represented in the left side and the timing scheme of the hit generation is represented in the right side [53].*

2.1.2 Overview of the changes implemented in the STS-XYTER v2.1

Due to the evolution of the experiment specifications, the STS-XYTER has undergone several iterations, being the version 2.2 the one with relatively minor changes compared to its predecessors [53, 57]. The most significant changes are related to problems with reading back global registers and unnecessary delay built into the fifo-clear command. A diode-based ESD protection has also been included. The full modifications list that have been implemented in the analog front-end is shown below:

- Fix the issue on the readout of global registers that were introduced like new in the STS-XYTER v2.1;
- The layout has been slightly modified in order to reduce risk of short during bonding of digital power;
- Fast reset timing modification;
- Implemented diode-based ESD protection;
- A fifo clear will be automatically released after a fifo-clear command;
- More potentials have been added to the internal diagnostic circuit for on chip monitoring;

Although some of the changes can be considered minors, the full characterization of the STS-XYTER v2.2 will be used as a reference for the STS detector operation. Some of the analog front-end tests and operation tuning will be described in next sections.

2.2 STS-XYTER v2.2 operation setup

For operating and characterizing the STS-XYTER v2.2 ASIC, a dedicated readout chain has been set up at the GSI-STS laboratory. Its main components are:

- a prototype FEB type C with a single STS-XYTER v2.2 ASIC;
- an FPGA-based data processing board (DPB), which implements the communication protocol back-end;
- gDPB FMC mezzanine card, for interfacing the front-end board with the DPB;
- a control PC;

A prototype custom designed FEB-C, with two ERNI connectors have been equipped with a single ASIC. The test channels have been connected to the ERNI connectors. This is very useful for monitoring channels performance while connecting external sensor boards or capacitor boards via the ERNI connectors. The board design allows to monitor multiple analog signals as well as to check the reference biasing potentials via external LEMO connectors (see Appendix A: The prototype FEB-C). A low voltage power supply provides 2.5 V for powering the 1.2 V for the analog front-end (AFE) and the 1.8 V for the digital part. The hardware platform for implementing the readout back-end is based on the AFCK board [58], which was the development and prototyping platform for the CBM DPB during last years. The communication with the controller back-end is provided by the IPBus protocol using a 1 Gbps Ethernet link [59]. Figure. 2.3 shows the main components of the prototype readout chain.

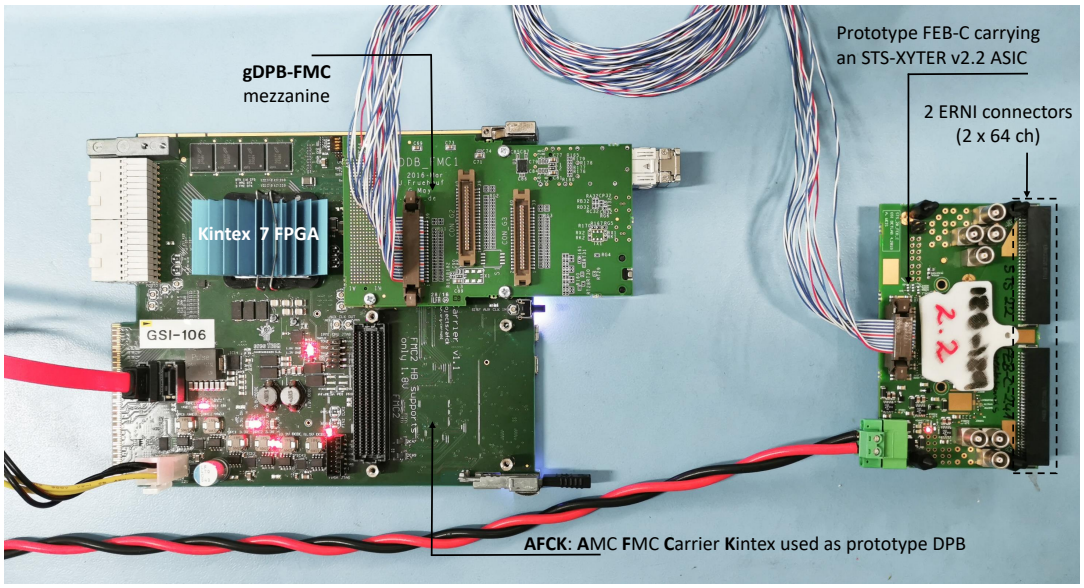


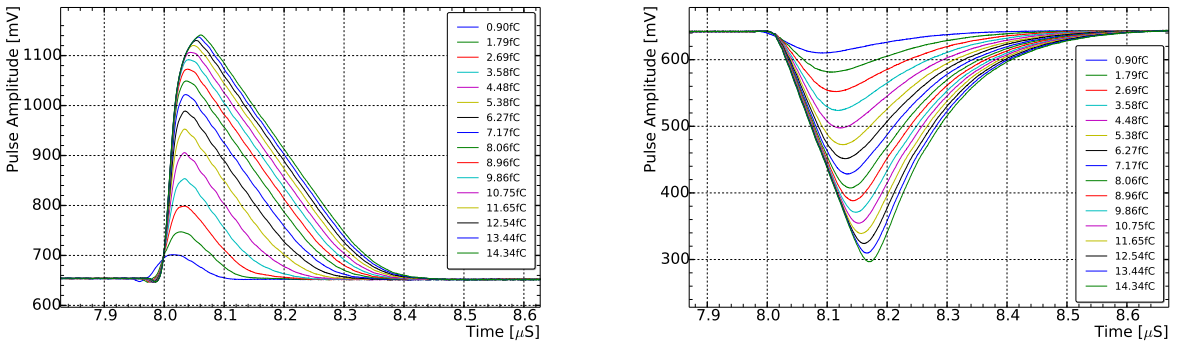
Figure 2.3: *Readout chain used for testing the STS-XYTER v2.2.*

2.3 Characterization of the analog front-end

The test of the STS-XYTER v2.2 ASIC [60] is an essential step carried out in order to characterize the chip before using it in the readout of the silicon micro-strips sensors. These procedures are intended to study and check some of the most important features and functionalities of the analog front-end that will have a direct impact on the STS detector performance. Several relevant AFE tests will be discussed below.

2.3.1 Gain estimation for the shapers

One of the first steps to characterize the AFE is the acquisition of the waveforms for the fast shaper, slow shaper and CSA for both polarities. For this purpose, FEB-C testing features, where two test channels are routed to external connectors on the board, are used. The analog waveforms are acquired using 1.5 GHz active probes via a Tektronik 4054 oscilloscope. Fig. 2.4 represents the response to injected pulses of different amplitudes in the range 1 - 14 fC. The waveforms are shown only for holes polarity (see Appendix B: Waveforms of the STS-XYTER v2.2 shapers for electron polarity).



(a) *Fast shaper waveforms for holes polarity.* (b) *Slow shaper waveforms for holes polarity.*

Figure 2.4: *Signal waveforms measured at the shapers output in test channel for different injected charges.*

The shapers gain can be measured by evaluating the output signal amplitude. A first order polynomial fit is used to adjust the data and extract the gain parameters. Results for the shapers gain characteristic values are shown in Fig. 2.5.

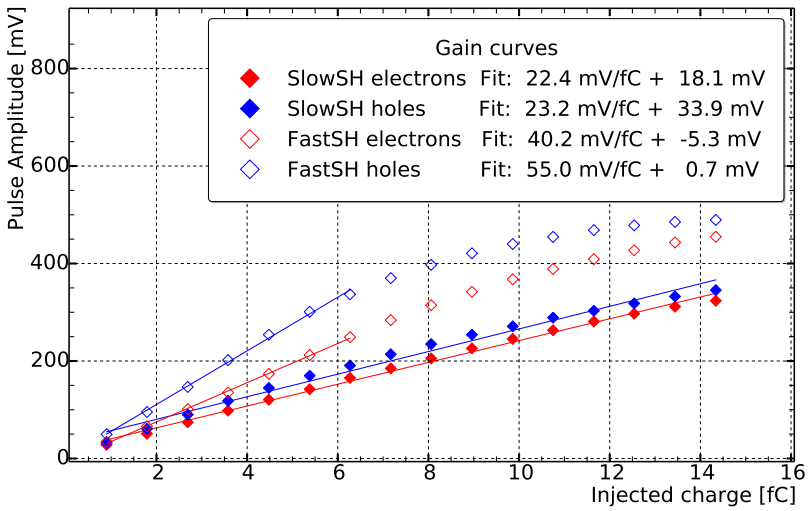


Figure 2.5: *Gain characteristic for the STS-XYTER v2.2 shapers.*

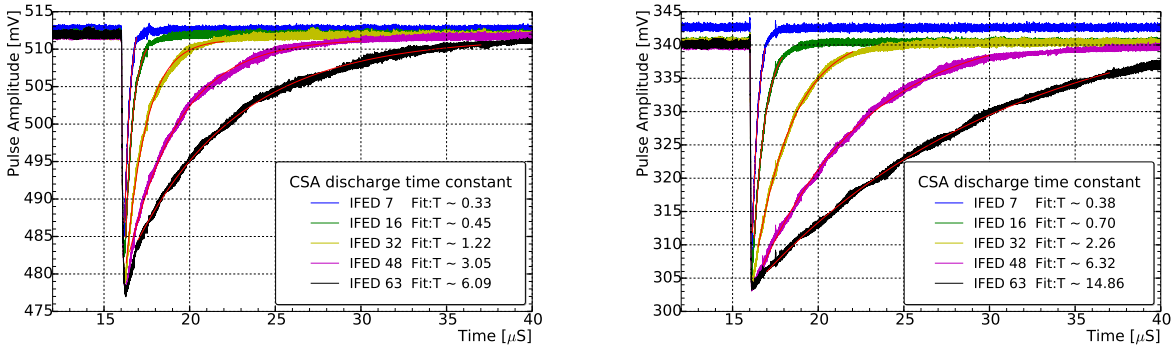
For the slow path the linearity is kept up to 13 fC, which is expected, since it is optimized for charge measurements. This range is considered sufficient since the passage through an active volume of non-irradiated silicon sensors, creates charge pulses with an average amplitude of approximately 4 fC. The linearity of the fast path is kept up to approximately 6 fC, which is considered enough for time-stamping purposes.

2.3.2 CSA discharge time constant estimation

Any circuit suffers from time delay between its input and output terminals when either a signal or voltage is applied to it. This delay is generally known as the circuits time constant, which represents the time response of the circuit when an input step voltage or signal is applied. In order to adjust the CSA feedback resistance, a 6-bit register (IFED) is implemented in the ASIC. Higher register values correspond to a higher feedback resistance. Figure 2.6 shows the CSA waveforms collected for different IFED values for both signal polarities. The discharge time constant (τ) can be estimated for each IFED value applying an exponential fit to the data. The estimated values are larger for holes polarity and this difference becomes more pronounced for higher values of the feedback resistance. Assuming that the capacitance used in STS mode is approximately 100 fF, the feedback resistance can be estimated based on the relation:

$$\tau = RC \tag{2.1}$$

The calculated values are between 3.3 MΩ and 60.9 MΩ for electrons polarity and between 3.8 MΩ and 148.6 MΩ for holes polarity.



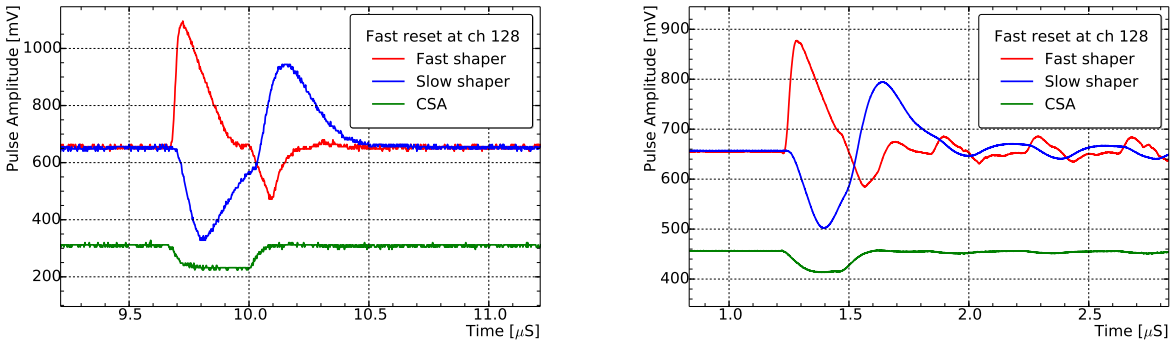
(a) *Electrons polarity.* (b) *Holes polarity.*

Figure 2.6: *CSA discharge time constant estimation for different feedback resistor (IFED) values.*

2.3.3 Charge sensitive amplifier fast reset

The STS-XYTER v2.2 ASIC has a "fast reset" feature, which is an optional pulsed reset of the charge sensitive amplifier for quickly bringing the CSA output voltage back to the baseline. The reset time delay is the time from the first appearance of the signal at the CSA, until the reset is triggered. This feature is controlled by a 250 ns pulse, triggered by the fast shaper leading edge delayed by 150 ns. The fast reset helps to shorten the baseline restoration in the slow shaper output, aiming to increase the rate capabilities of the experiment. Figure 2.7 shows a comparison of the waveforms for the slow shaper, fast shaper, and CSA with the fast reset turned on for the STS-XYTER v2.1 and STS-XYTER v2.2. It was observed for the STS-XYTER v2.1 that the fast

reset is activated close in time to the moment when the slow shaper reaches its peak for the two longest shaping times. For this reason, was decided to implement a timing modification in the fast reset that will act earlier and for a shorter period of time to enable a faster recovery to the baseline. As mentioned in section: Overview of the changes implemented in the STS-XYTER v2.1, one of the main modifications of the STS-XYTER v2.2 was the implementation of the timing corrections for the fast reset. Figure 2.7(b) illustrates that the fast reset feature is oscillating, not shorten the baseline restoration for the slow shaper when compared to its predecessor (Fig. 2.7(a)). The cause of this behavior is not yet understood and still under investigation. However, it is possible to operate the chip at high rate without the fast reset feature, by reducing the discharge time constant of the CSA. This solution could introduce other issues during the ASIC operation, such as a ballistic deficit of the CSA if the discharging time is not slow enough for not allowing a full pulse formation, or a serious degradation of the noise performance of the detector. These topics will be study in next sections.



(a) *Waveforms with fast reset active for ASIC v2.1.* (b) *Waveforms with fast reset active for ASIC v2.2.*

Figure 2.7: *Operation of the fast reset feature after time and amplitude measurements for holes polarity.*

2.3.4 Ballistic deficit estimation

The ballistic deficit effect refers to the incomplete integration of the output signals of radiation detectors, which can deteriorate the systems performance. This effect primarily stems from the sensitivity of the pulse shaping network to the duration of the detector pulses, but it may also result from the finite time constant of the pulse readout circuit. The latter effect is also known as pulse height loss due to the capacitive decay in the pulse readout circuit [61]. A good trade-off between the ballistic deficit effect, noise, and pulse pile-up in the detector systems is key for the STS detector system.

The signal at the output of the charge sensitive amplifier usually has a long decay time constant due to the need for a large R_f to minimize its thermal noise contribution. A long decay time constant is not desirable in terms of high rate capabilities because it will lead to pile up effects, missing pulses and improper estimation of the signal amplitude. The STS-XYTER possess a fast reset feature to quickly bring the CSA output voltage back to the baseline after time and amplitude measurement. Since this option is not properly working for the STS-XTER v2.2 (see section: Charge sensitive amplifier fast reset); an alternative solution might be reducing the decay time constant as much as possible, without compromising the signal amplitude for the giving peaking time. Figure 2.8 represents the dependency of the pulse amplitude at the output of the slow shaper as a function of the feedback resistor. A peaking time of 90 ns is used for this measurements in order to reduce as

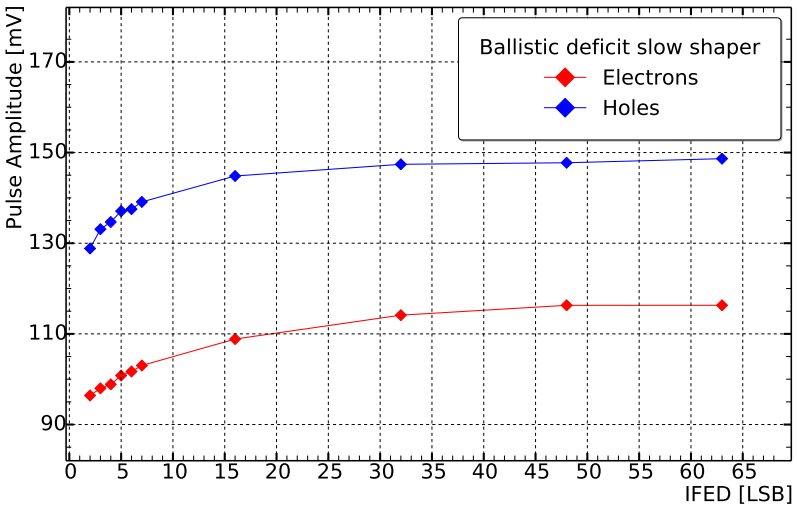


Figure 2.8: *Ballistic deficit in the ADC for different IFED values.*

much as possible dead time and pile up. For an IFED value of 20 LSB units (approximately 10 MΩ) the signal formation starts reaching the plateau. This value is a good compromise between full signal formation and small discharge time constant for avoiding ballistic deficit. Further studies about noise contributions due to the reduction of the discharge time constant will be presented in this work.

2.3.5 Slow shaper peaking time

Pulse shapers typically transform a narrow sensor pulse into a broader pulse with a gradually rounded maximum at the peaking time. The optimum choice of a shaper relies on the design requirements and it is a trade between different factors such as counting rate, sensitivity of rise time fluctuations and signal to noise ratio.

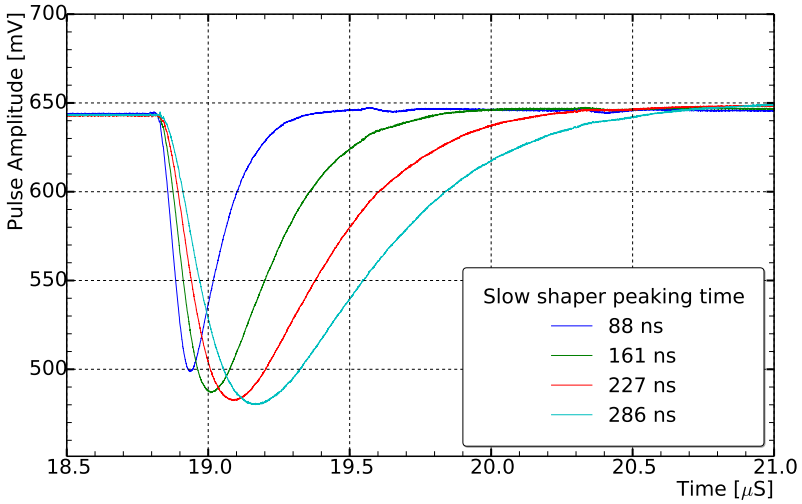


Figure 2.9: *Slow shaper waveforms for different peaking times.*

The peaking time is a key design parameter, as it dominates the noise bandwidth and must also accommodate the sensor response time and the hit rate. The signal peaking time in the STS-XYTER can be controlled via a 2-bit configuration register (FS = 0..3). The slow shaper $CR-(RC)^2$ design allows to select multiples peaking times modifying the resistance values in the pulse processing chain [62].

The output waveforms for all possible shaping times are shown in Fig. 2.9. The waveforms are collected with a Tektronik 4054 oscilloscope. Positive input signals of approximately 4.5 fC are applied in a test channel. The CSA input current and the feedback resistor are kept to typical values. The estimated peaking time values are 88 ns, 161 ns, 227 ns, 286 ns.

2.4 Validation of the ADC calibration using an external pulse generator

The STS-XYTER v2.2 ASIC calibration aims to determine the individual correction settings for the ADC and the FAST discriminator in every channel. Like its predecessor [43, 63], the chip has an internal calibration circuit, which allows to inject charge pulses into the analog front-end. For the calibration procedure, in a first step, the reference potentials ($VRef\_P$ and $VRef\_N$), the polarity and the calibration range of the ADC, i.e., the threshold of the first and last discriminator, should be defined. For the $VRef\_P$ and $VRef\_N$, a method of successive approximations have been implemented in order to find the best value for the desired range. The range is equally distributed in 31 steps, resulting in the corresponding threshold for each comparator. The effective threshold is adjusted by scanning the trim DAC of every discriminator while the threshold of the timing discriminator is adjusted to be very close to the first ADC level. The threshold is adjusted by scanning the trim DAC of every discriminator and the response function is read out using the diagnostic counters.

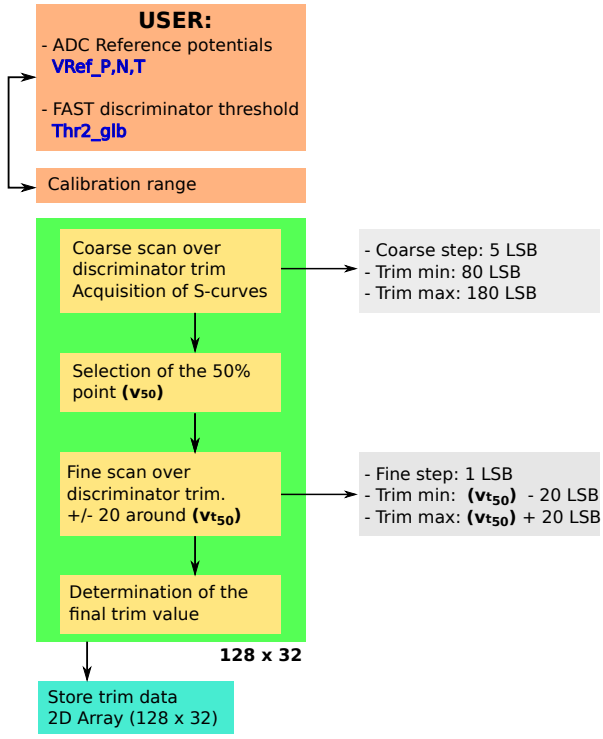


Figure 2.10: *Diagram of the calibration procedure for the STS-XYTER v2.2 ASIC [43].*

Figure 2.10 represents the main steps of the calibration procedure. A detailed description of the procedures, as well as optimization of the main calibration parameters will be described in other chapter for an STS module (see section: Calibration procedures for modules testing). This section intends to validate the ADC response using external and internal pulse calibration. For this purpose, a prototype FEB-C with a single STS-XYTER v2.2 have been used. The ADC was calibrated in advance for both polarities resulting in:

- Holes: Dynamic range of 12.03 fC (30-247 *amp_cal* LSB). ADC gain of 0.41 fC/ADC;
- Electrons: Dynamic range of 12.03 fC (30-247 *amp_cal* LSB). ADC gain of 0.40 fC/ADC;

The ADC response function have been calculate by injecting external pulses into the ASIC channel inputs using an attenuator board. The use of an external pulse generator offers some advantages in terms of speed compared to the internal pulse generator integrated in the chip, since higher frequencies can be used for the injected pulses and all channels can be accessed simultaneously. The voltage pulses are generated via an Agilent 33250A arbitrary waveform generator and injected at 10 kHz in the first 64 channels. The signal charge can be estimated as $Q = C \cdot \Delta V$. To correct parasitic capacitances, the capacitors, as well as the voltage divider resistors were measured using a Peak Tech 2155 LCR meter.

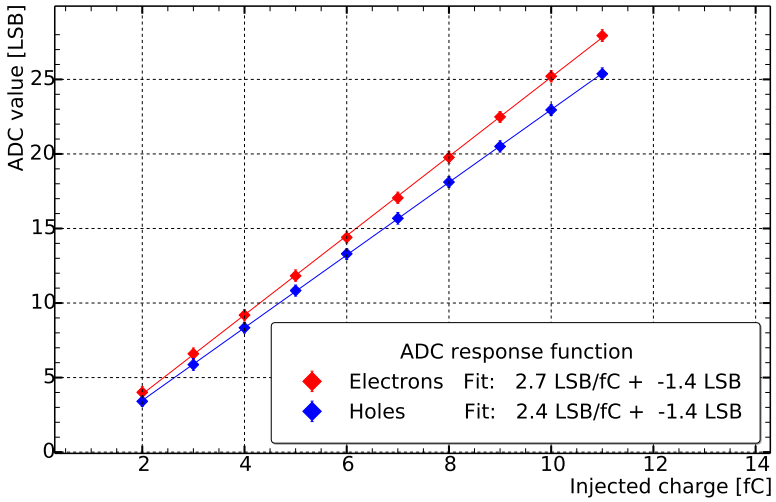
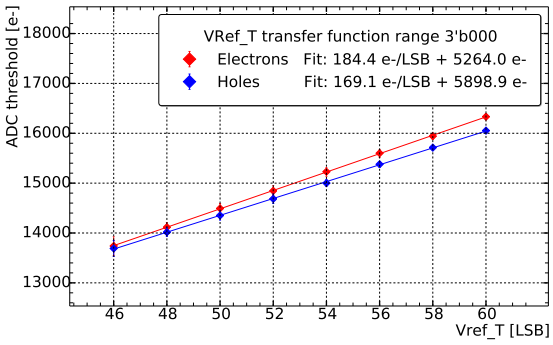


Figure 2.11: *ADC transfer function for both polarities using external pulse generator.*

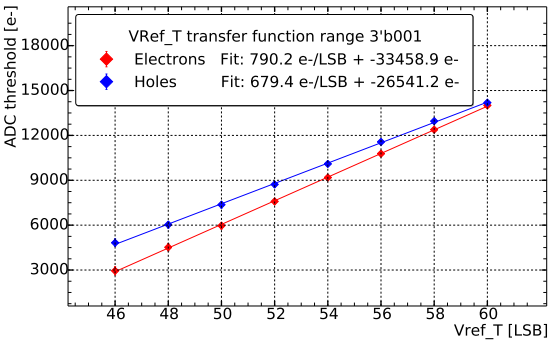
Figure 2.11 shows the ADC response function for electrons and holes polarities. A lineal regression is used for fitting. Each point corresponds to the average amount the even channels and the error bars represent the standard deviation. With this, it is possible to determine that 1 *amp_cal* LSB, from the internal pulse generator, is equivalent to 0.056 fC for holes polarity and 0.053 fC for electrons polarity, or approximately 349 and 330 electrons respectively. These results are consistent for both polarities and independent of the ADC range used.

2.5 Linearity of the *VRef_T* transfer function

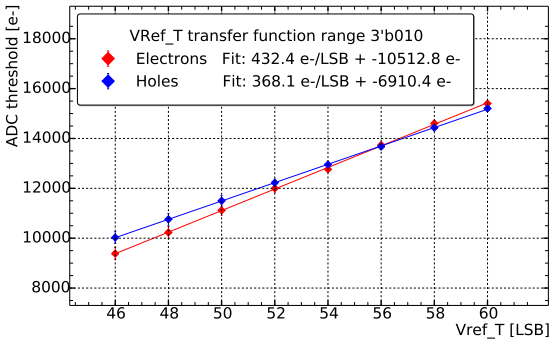
One of the features implemented in the STS-XYTER v2.2 is the capability to choose between different ranges of the ADC global threshold, determined by the *VRef_T* potential. The *VRef_T* is a global DAC that allows to adjust the position of the signal baseline relative to the ADC, i.e., to set the ADC effective threshold without modifying the transfer function. The four possible operating ranges of the chip are referenced with 3'b000, 3'b001, 3'b010, and 3'b100, and can be chosen via a combination of two global registers, as described in Ref. [55]. Each range has a 6-bit resolution (0 to 63). A full characterization of the transfer function for the four ranges is necessary for a correct operation of the ASIC in the detector readout. With this purpose, the ADC global threshold response was measured and its linearity evaluated.



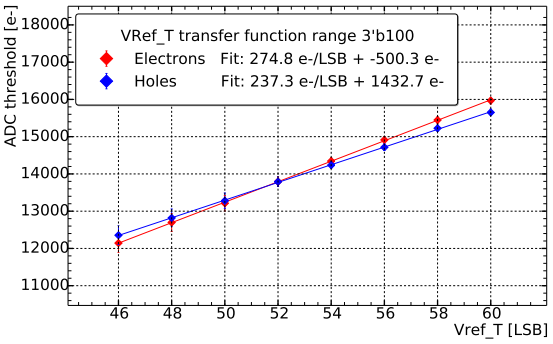
(a) *Range 3'b000.*



(b) *Range 3'b001.*



(c) *Range 3'b010.*



(d) *Range 3'b100.*

Figure 2.12: *ADC threshold scan for both signal polarities for the four selectable dynamic ranges.*

The method is based on s-curves scan for the ADC discriminators at different values of the *VRef_T* register (between 46 and 60). Figure 2.12 shows the results of the threshold scans for both signal polarities and all ranges of the *VRef_T* potential. Each data point represents the average response among all channels of the ASIC, the error bars represent the standard deviation with respect to the main value. Each data set is fitted with a first degree polynomial. For all measurements, the CSA current and the IFED feedback resistance are kept to the typical value [55].

2.6 Summary of noise measurements

In any physical system, measurable quantities come with unavoidable superimposed fluctuations, due to the discrete nature of matter, the quantity itself or the randomness of the constituting processes [62]. All these fluctuations are referred to as noise and are statistical properties of the system that can be estimated and measured. Generally, the most important feature limiting the performances of a system is its inherent level of noise. This is a measurable quantity and can be expressed in different ways. The signal to noise ratio (SNR) indicates, for a specific type of event, the ratio between the signal (assumed to be noise-free) and the measured noise. Since most detectors rely on the measurement of the charge delivered by an ionization event, the most common parameter used to characterize the noise is the equivalent noise charge (ENC), defined as the input charge that produces at the output a signal amplitude equal to the RMS noise. It is the minimum charge detectable by the system, the one making the SNR equal to 1. Excessive noise can introduce a large background making very difficult the data analysis and could also obstruct the data taking by overloading the data acquisition system. This is specially important for self-triggering systems, like the STS detector, where noise hits are digitized as soon as the amplitude exceeds the given threshold.

In the STS modules, there are three main contributions to the noise: the intrinsic noise of the charge sensitive amplifier (CSA), the shot noise generated by the detector leakage current and the thermal noise of the resistive structures (biasing resistors, readout electrodes, microcable traces). An equivalent circuit of the STS detector module showing the main elements contributing to the system noise is shown in Fig 2.13 [64].

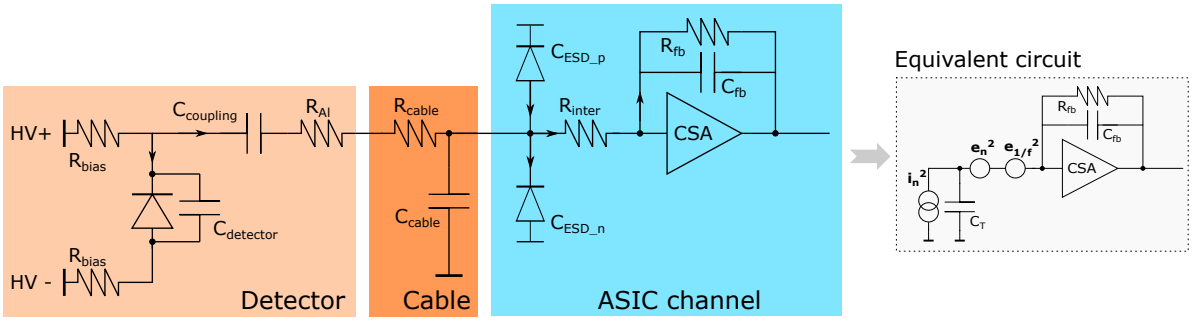


Figure 2.13: *Noise sources in the detector readout system. Simplified schematic [43, 64].*

The noise for the STS detector modules can be grouped in three equivalent noise sources:

- parallel current noise (i_n^2)

$$i_n^2 = \frac{4k_BT}{R_{bias}} + \frac{4k_BT}{R_{fb}} + 2eI_{det} + 2eI_{Diode} \tag{2.2}$$

- series voltage noise (e_n^2)

$$e_n^2 = 4k_BTR_{Al} + 4k_BTR_{cable} + 4k_BTR_{inter} + e_{na}^2, \tag{2.3}$$

- series $1/f$ noise (e_{nf}^2)

$$e_{nf}^2 = \frac{K_f}{f} \tag{2.4}$$

The total noise can be obtained by integrating over the total range of the amplifier with frequency dependent gain $A(f)$:

$$ENC^2 = \int_0^\infty \left(i_n^2 + e_n^2 + e_{nf}^2\right) A(f) df \tag{2.5}$$

After performing the integration over the whole frequency range and considering the total detector capacitance $C_T = C_{det} + C_{cable} + C_{ESDn/p} + C_{PCB}$, the noise of the full detector modules (ENC_T) can be estimated:

$$ENC_T^2 = i_n^2 F_i \tau_s + e_n^2 F_v \frac{C_T^2}{\tau_s} + F_{vf} A_f C_T^2 \tag{2.6}$$

where F_i, F_v and F_{vf} are numerical values depending mainly on the shaper order and τ_s is the time constant of the shapers. This equation can also be written in a simplified way:

$$ENC_T = \sqrt{ENC_i^2 + ENC_e^2 + ENC_{1/f}^2} \tag{2.7}$$

The noise measurements for the STS-XYTER v2.2 that are discussed in this section, are made using a single ASIC bonded onto a prototype FEB-C. This configuration allows to perform a characterization, optimization and detection of possible issues at the ASIC level in a relatively simple system (see Fig. 2.3).

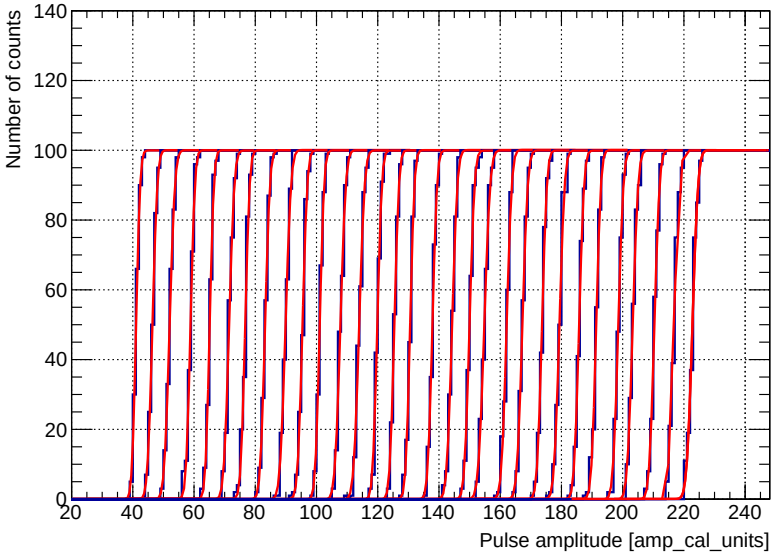


Figure 2.14: *Error function fitting for the 31 discriminators in one channel.*

For the noise estimations, pulses of different amplitudes are injected at the input of the CSA. Ideally, the discriminator response should be a step function, but in reality the distribution is smeared by the electronic noise. The discriminator response looks like a s-curve and it is fitted using a complementary error function:

$$F(x) = \frac{N}{2}\left(1 + erfc\left(\frac{x-\mu}{\sqrt{2}\sigma}\right)\right) + Y_0 \tag{2.8}$$

where N is the number of injected pulses, Y_0 an arbitrary offset, the width (σ) is a measurement of the ENC noise amplitude and the mean value (μ) indicates the effective discriminator threshold. Figure 2.14 shows the s-curves, for the 31 discriminators in one channel, fitted using an error function.

The noise levels are calculated for every channel as an average among all discriminators. Results for a single ASIC in a prototype FEB-C are shown in Fig. 2.15 for both polarities. The average noise levels are approximately (487 ± 29) e- for holes and (503 ± 35) e- for electrons polarity. The noise for holes is smaller than for electrons, this effect is well known an it is associate with the polarity selection circuit, which bypasses the signal for holes polarity and not for the case of electrons. Results are comparable with previous version of the ASIC [50].

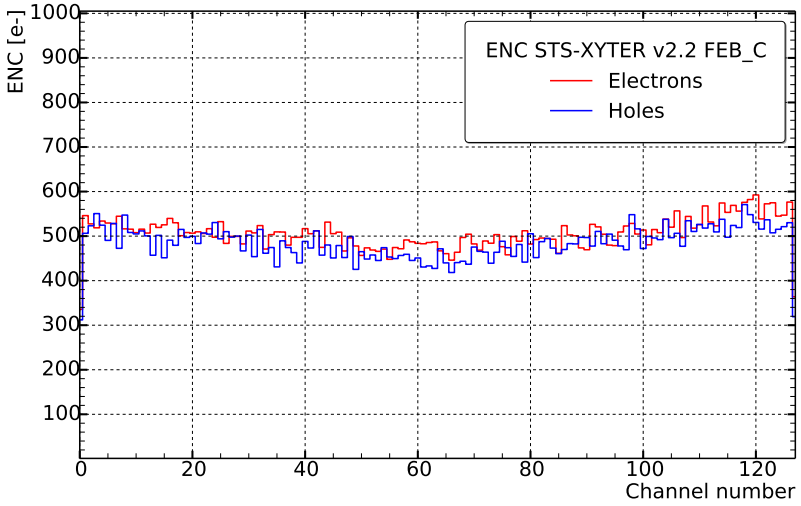


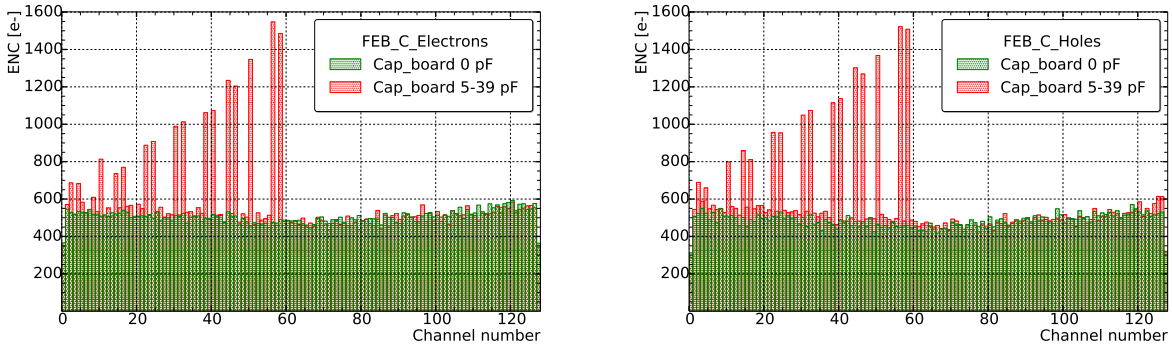
Figure 2.15: *Noise level measurement for a single ASIC bonded onto a prototype FEB-C.*

2.6.1 Noise dependence on input load capacitance

The STS detector, in the final design, will carry several combinations of sensor sizes and micro-cables length with and estimated load capacitance in between 12 and 40 pF [65, 66]. The noise of the detector sytem strongly depends on the total capacitive load seen by the CSA input transistor. For non irradiated sensors, with low leakage current, the contributions to the total system noise is expected to be mostly due to the load capacitance. Therefore, the noise dependence on the load capacitance is an important criteria in order to characterize the detector system.

For this purpose, a test board built from ERNI connectors with 64 pins and a set of low leakage C0G SMD capacitors, ranging from 5 to 39 pF, was used. The capacitors were soldered to different channels in the board. Every capacitance value was cross checked using a Peak Tech 2155 LCR meter, in order to correct parasitic values. During measurements, the board was connected to the first ERNI connector of the FEB-C, i.e., channels 0 - 63. Pulses of different amplitudes are injected at the channel's input using the internal pulse generator.

Figure 2.16 shows the ENC levels for all channels in the ASIC, with two different capacitor boards attached to the FEB-C. As reference, a background measurement (green line) is taken for the FEB-C with a single board where no capacitors had been attached. The noise as a function of the input load capacitance is shown in Fig. 2.17. A first order polynomial fit is used for fitting the data, resulting in a slope of 24.9 ENC(e-)/pF for the electrons polarity and 24.7 ENC(e-)/pF for



(a) *Electrons polarity.* (b) *Holes polarity.*

Figure 2.16: *Noise level measured with different capacitor boards.*

the holes polarity. The offset values reproduce the average noise levels measured for the FEB-C. Since the voltage and the $1/f$ components of the noise rise with the capacitance, the noise levels, as expected, increase as a function of the input capacitance.

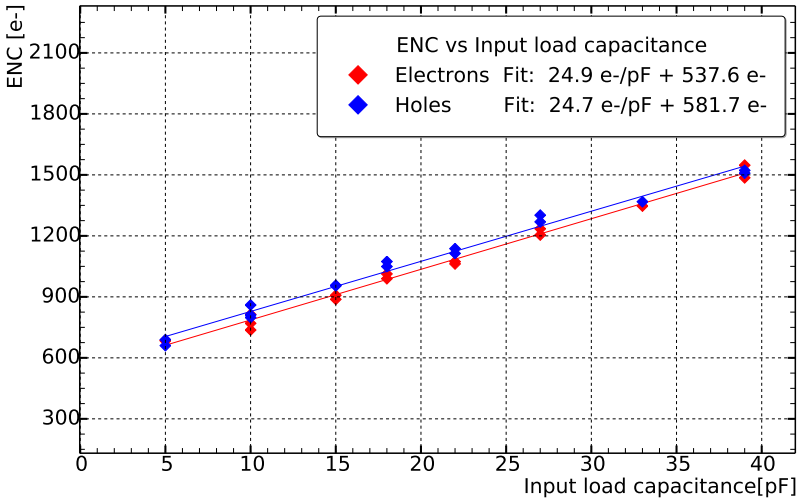


Figure 2.17: *Noise level estimation as a function of the load capacitance.*

2.6.2 Noise dependence on CSA bias current

The main role of the CSAs, for radiation detector systems, is to extract signals induced by the incident radiation and amplify them to obtain a better signal to noise ratio. Therefore, the proper operation of the CSA bias current has a significantly influence on the chip performance and noise reduction. The CSA architecture uses a 2500 μm/320 nm ELT NMOS input transistor biased with nominal 2 mA drain current and supplied from a separate, lower 1.2 V power supply (VDDM) [53]. The amplifier bias current can be selected by two dedicated 6-bit DACs. This allows to set the bias current in the range 0 to 4 mA, with a typical value of 31 LSB units, which corresponds to

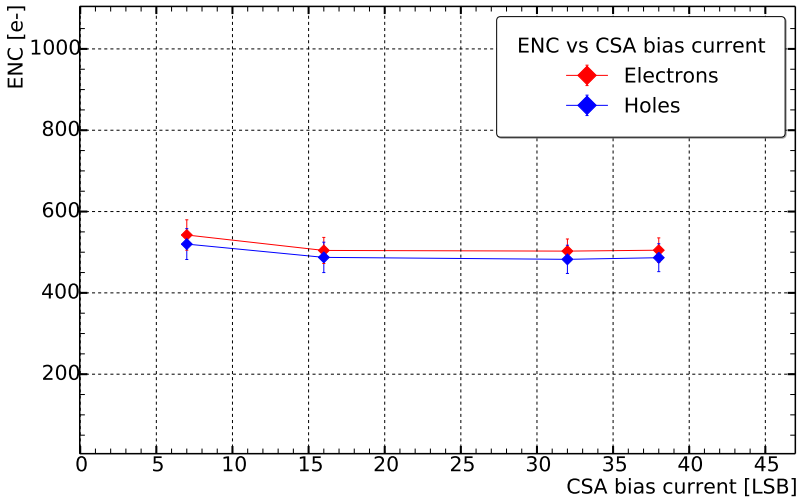


Figure 2.18: *Noise level estimation as a function of the CSA bias current for both polarities.*

2 mA/channel. Figure 2.18 represents the noise in the chip as a function of the CSA bias current for a single ASIC bonded on a prototype FEB-C. Every point represents the average across all channels and the error bars correspond to the standard deviation with respect to the main value. For values below 16 LSB units a small increase of approximately 50 electrons is visible compared to larger values of the CSA bias current. The differences are significantly small and its safe to say that the noise levels are approximately constant for the full range of the CSA bias current. This study is extended to a fully assembled module and it will discussed in chapter 4 section: Study of the STS-XYTER v2.2 settings in the module readout.

2.6.3 Noise dependence on the IFED resistor values

The feedback resistor discharges the capacitor and establishes a well defined operating point for the charge sensitive amplifier. The thermal noise associated with the feedback resistor is a major contributor to the overall noise. As presented previously, it can defined by the expression:

$$i_n^2 = \frac{4k_B T}{R_{fb}} \tag{2.9}$$

were k_B is the Boltzmann constant, T is the temperature and R_{fb} is the feedback resistor. The noise is minimized by maximizing R_{fb}. Because of the large resistance required for low noise, a long decay time constant is created, which might not be suitable if the detector operation demands a high rate capability, like the CBM experiment. Pile up happens when radiation events occur before the output of the system is able to return to the baseline. Since the fast reset feature, implemented for the fast return of the signal to the baseline, is not properly working in this version of the ASIC (see section: Charge sensitive amplifier fast reset); a good compromise have to be found between noise and pile up. Figure 2.19 shows the noise dependence on the feedback resistor (IFED) value for a single ASIC bonded onto a prototype FEB-C. The noise level is reduced by around 100 electrons for the first part of the IFED range under study (until 32 LSB). For values of IFED bigger than 32 LSB, there are not significant improvements in the noise performance of the system. Since 100 electrons is a relatively small deterioration, it allows to operate the chip at low feedback resistor values, if needed, as far as it does not introduce ballistic deficits into the system.

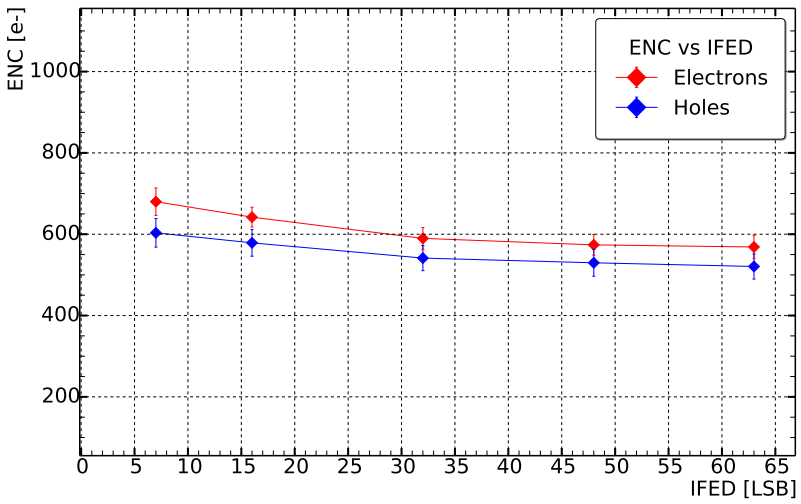


Figure 2.19: *Noise level estimation as a function of the feedback resistor for a single ASIC.*

2.6.4 Noise dependence on shaping times and shaper current

The slow shaper design $CR-(RC)^2$ enables the selection of multiple peaking times in order to find the optimum trade-off between speed and noise. Four different peaking times, 88 ns, 161 ns, 227 ns, and 286 ns can be selected via a 2-bit DAC by modifying the appropriate feedback resistance values in the chip (see section: Slow shaper peaking time). Figure 2.20 represents the noise as a function of the slow shaper peaking time for a prototype FEB-C. Parameters like the CSA current and the IFED have been kept to the typical values.

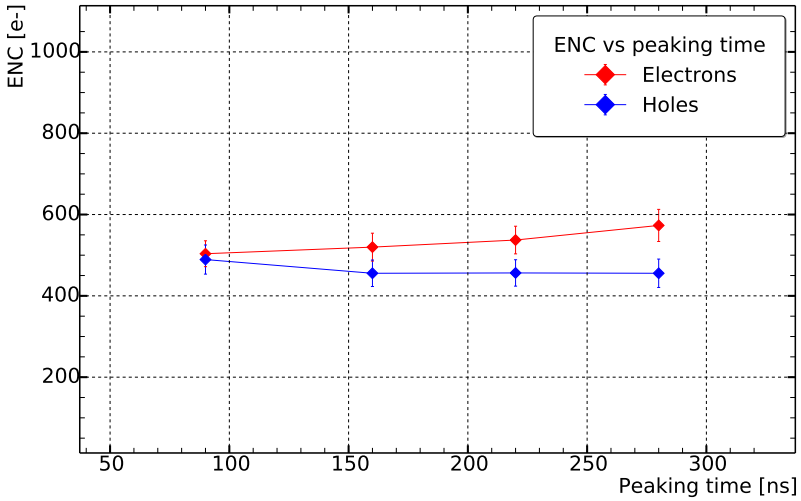


Figure 2.20: *Noise level estimation as a function of the slow shaper peaking time.*

The noise levels remain approximately constant among all possibles peaking times. There is a significant difference between electrons and holes polarity, mainly due to the contribution of the polarity selection circuit (PSC), which is present in the electron processing chain.

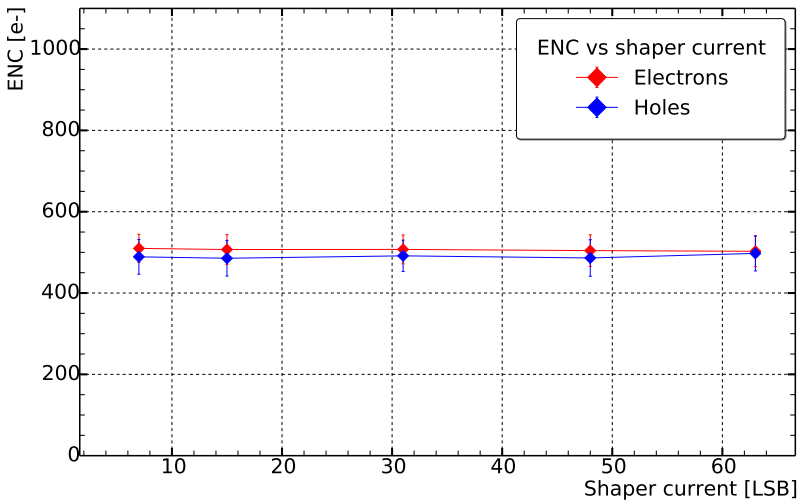


Figure 2.21: *Noise level estimation as a function of the slow shaper current.*

Another important parameter to take into account is the the shapers current. The noise contribution from the shapers will not be analyzed here. Although, if the slow shaper is working properly, this value should stay approximately constant across the full range. This value can be set in the ASIC configuration and it can be modified in the range between 0 and 63 LSB units or from 102 μA to 300 μA. Figure 2.21 shows the noise as a function of the slow shaper current for a FEB-C. Other parameters like the shaping time, CSA current and IFED have been set to the typical values. As expected, the slow shaper current stays constant across the possible range with a deviation of less than 5% with respect to the main value.

2.6.5 Noise stability tests

CBM will be a long standing experiment in which a reliable performance in time is considered mandatory. The noise evaluation over time for an STS-XYTER v2.2 ASIC can contribute to identify malfunctions that are not easy to observe during short running periods. These variations can be a consequence of electromagnetic interference, uneatable biasing, faulty ground connections, unstable temperatures. For this test, a single ASIC bonded on a prototype FEB-C have been used. The measurements were taken for both polarities every 18 minutes for approximately 72 hours. The temperature was registered after each measurement to be able to detect noise fluctuations due to drastic changes in temperatures.

Figure 4.18 shows the noise dependence with the time. Every point represents the average noise values among all channels in the chip and the error bars indicate the spread. The variations along the monitoring period were below 10%, which is considered a good result.

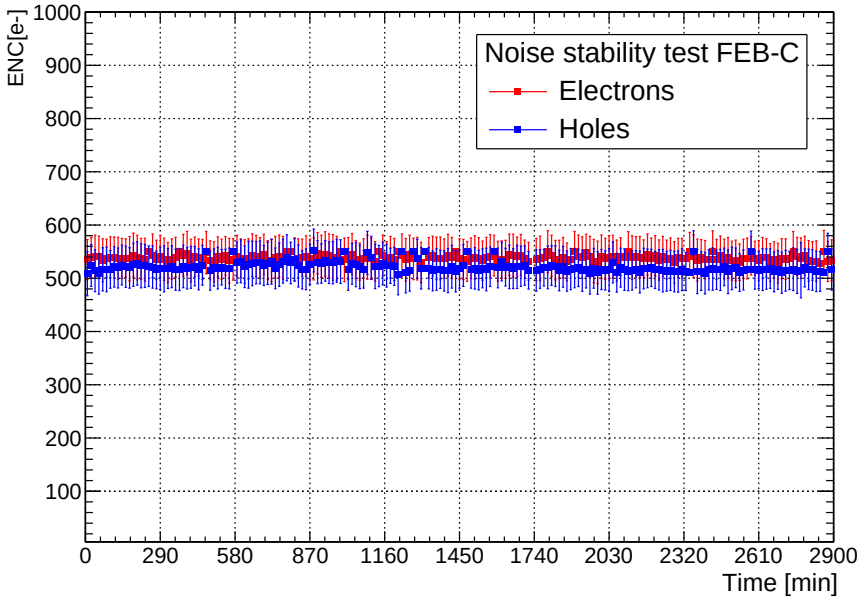


Figure 2.22: *Noise stability test for a single ASIC bonded in a prototype FEB-C.*

2.7 Summary

The characterization of the STS-XYTER v2.2 is one of the major steps before its operation in the full readout chain. Some of the most important requirements in the chip design, tests and operation results have been highlighted. The collection and analysis of the analog waveforms, with gain values of 22.4 mV/fC for electrons and 23.2 mV/fC for holes polarity were extracted for the slow shaper. Values of 40.2 mV/fC for electrons and 55.0 mV/fC for holes were also extracted for the fast shaper. The slow shaper peaking time was also estimated for all possible values.

The discharge time constant was estimated and the feedback resistor values were calculated obtaining larger values for holes polarity. This difference becomes more pronounced for higher values of the feedback resistance.

Since the inclusion of the diode-based ESD protection circuit, the CSA fast reset is not working as expected. However, it is possible to operate the chip at high rate without the fast reset feature, by reducing the discharge time constant of the CSA. This solution could introduce other problems during the ASIC operation such as a ballistic deficit or a serious degradation of the noise performance of the detector. It was shown that without the fast reset feature it is possible to operate the chip at high rates without compromising the performance in terms of ballistic deficit or noise levels.

The STS-XYTER v2.2 has the ability to choose between four different dynamic ranges of the global ADC threshold. A full characterization of the transfer function for the four ranges is necessary for a correct operation of the ASIC in the detector readout. With this purpose, the ADC global threshold response was measured and its linearity evaluated for all possible ranges.

Among the multiple operation requirements of the STS-XYTER v2.2 ASIC, the noise performance is one of the most important. The chip was characterized in terms of noise for different parameters such as: input capacitance, CSA bias current, IFED resistor and shaping time. All these studies allow the optimization of the chip parameters as well as the detection of possible malfunctions that could lead to serious problems during the STS operation. The noise stability

was also tested showing a dispersion below 10% over 72 hours of continuous testing. The tests and procedures discussed in this chapter represent essential elements to understand and operate successfully the STS detector.

Chapter 3

Development of procedures and software tools for the ASIC quality control

A prerequisite for the assembly of functional detector modules, in any experiment, is a rigorous Quality Assurance (QA) of the components. These procedures aim to ensure the functionalities of all the components in order to fulfill the detector specifications. As the main tracking detector of the CBM experiment, the STS has high performance requirements in terms of reconstruction efficiency and momentum resolution. These observables are determined, among other factors, by the quality of the detector modules assembly and its components [67].

This chapter aims to describe the software developments and implementation of quality control (QC) procedures in order to evaluate the correct functionality of the STS-XYTER and the bonding quality of the chipcable (ASIC + microcable). In addition, a decision criteria based on the number of defective channels, power consumption and other operational aspects will be established.

3.1 Basics considerations

The STS-XYTER v2.2 ASIC, as one of the fundamental components of the detector module, has also high constraints in terms of electrical functionalities for reading out the double-sided silicon sensors. The fraction of defective (dead or broken) channels on the STS tracking performance is an important element to consider. Several simulations have been performed in order to check the impact of the number of defective channels in the reconstruction efficiency and momentum resolution [68].

Figure 3.1 shows simulations of how the detector efficiency depends on the percent of broken channels [69]. Having 5% of dead channels drops the track reconstruction efficiency to 90% for all tracks and around 95% and 94% for primary tracks and D0 decays respectively. However, dead channel means the whole readout channel, where problems can appear at any state during the assembly procedures. Thus, having 5% of defective strips for the sensors, would put a requirement of no defective channels for microcables and ASICs. On the other hand, setting a request of zero bad strips would decrease the number of accepted sensors and, consequently, would increase considerably the total production cost.

Realistic number of bad strips for sensors is below 1% per sensor on average [68]. Relying on this factor, a safety margin around 3% of bad strips can be established like criteria selection for the sensors QA. This is equivalent to 30 strips per sensor side. Sensors with a number of bad strips larger than this value are rejected and not assembled into detector modules.

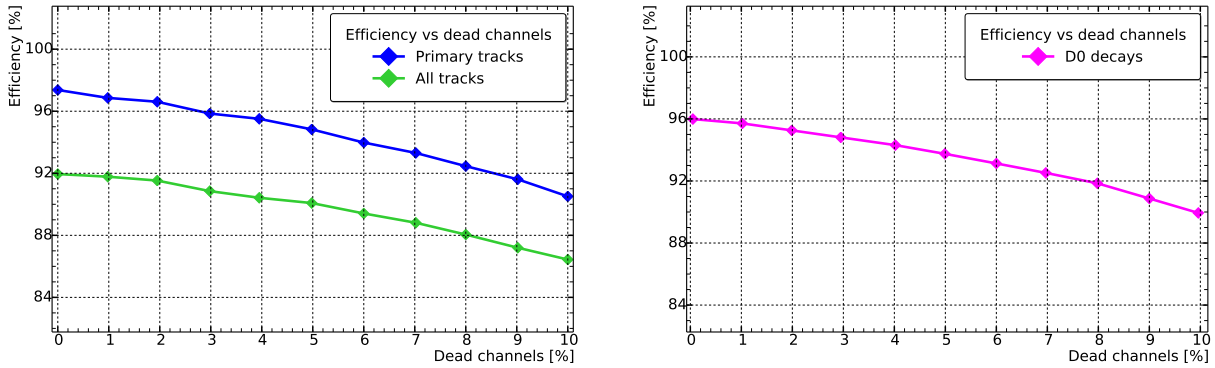


Figure 3.1: *Efficiency as a function of the dead channels for all tracks and primary tracks in the left side and from D0 decays in the right side.*

These elements allow to set the limits of QA in terms of broken channels for the ASICs and chipcable tests in around 15 to 20 broken channels. This criteria is not absolute since the total number of broken channels for a full assembled module should be below 3%, making possible to combine ASICs and microcables with different amounts of broken channels to fill the final QA criteria.

Not only the amount of broken channels is important to ensure the correct functionality of STS components, but also elements like power consumption, correct e-fused ID, data readout for the back-end and the correct functionality of the analog front-end needs. Therefore, the importance of developing and elaborating reliable QA procedures to ensure high production yield and the correct performance of the final STS detector.

3.2 The STS-XYTER pogo prober interface

The ASICs designers have elaborated a minimal set of 63 larger test pads for essential connectivity, which are placed near to the ordinary bonding pads. It allows the full operation of the chip and the test of different functionalities [70]. The test pads for a Pogo Pin has to be at least 150×150 μm^2 in size, with a pitch of at least 200 μm.

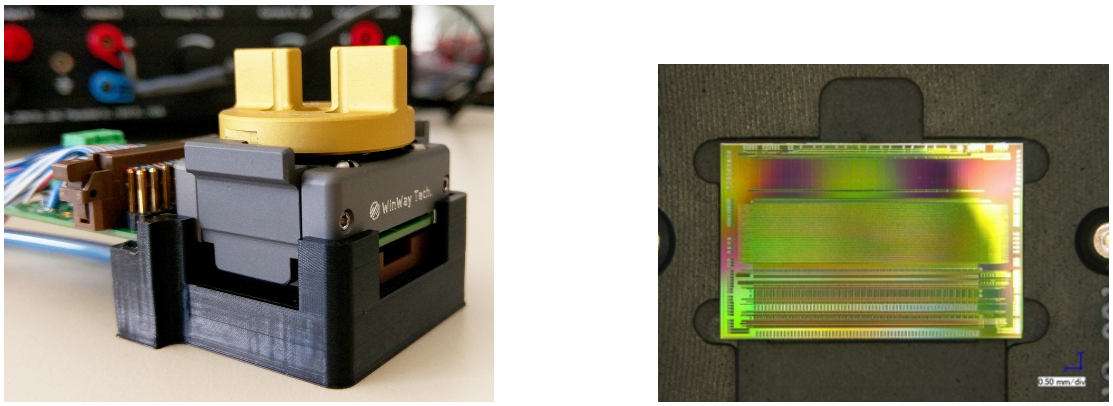


Figure 3.2: *Pogo pin station setup (left side). STS-XYTER ASIC inside the pogo pin (right side).*

Figure 3.2 shows the custom designed socket developed by the WinWay Technology Company [71] in the left side. The chip is placed in a bottom socket manually and can be fixed using vacuum if needed (see Fig. 3.2 right side). The top lid contains a set of needles that interfaces the chip via dedicated pogo pads. An entrance window on the side of the channel's input allows testing the ASICs with bonded microcables. A custom-designed PCB interfaces the test station with a standard STS-XYTER v2.2 readout chain.

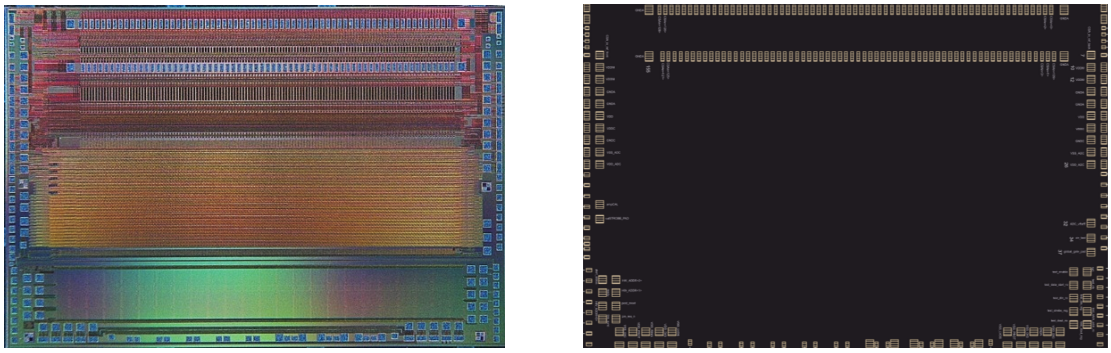


Figure 3.3: *The STS-XYTER with its available pad layout [55].*

Figure 3.3 shows the available pads for the STS-XYTER. Since these pads for pogo-probes are much larger than typical wire-bonding pads (100×65 μm^2), it is required to provide only a minimum connectivity essential for performing the tests on this level. This brings some limitations to the pogo prober setup like:

- No direct interaction with the channels input;
- It is possible to test only one up-link for the ASIC;
- Can be a problem for the assembly of the FEB8-5 with five up-links per ASIC. This FEB8-5 will be used in the high occupancy region of the detector;

3.3 Experimental setup

The custom-designed STS-XYTER implements a testing interface for evaluating the chip functionalities at the wafer level. For the final ASIC production, the chips will be tested in a wafer-probe station and given a unique identification number [72]. At the moment, those tests are carried out at GSI laboratory using a pogo-pin station. The PCB design allows the LVDS signals to be routed to an external connector. This feature permits to make use of the same firmware used for prototypes FEBs-C testing without further modifications (see section: STS-XYTER v2.2 operation setup). The tests are performed for every ASIC that will be used in the assembly of STS modules or prototype FEBs-C. Figure 3.4 shows the main components of the setup; it features:

- prototype pogo prober for carrying one STS-XYTER ASIC;
- data processing board (DPB), FPGA based board, which implements the communication protocol back-end (AFCK board);
- power supplies providing the voltage for the pogo pin station and AFCK;
- external pulse generator for doing the ASIC E-Fusing process;

- vacuum pump to help positioning the ASIC inside the pogo prober station;
- testing computer;

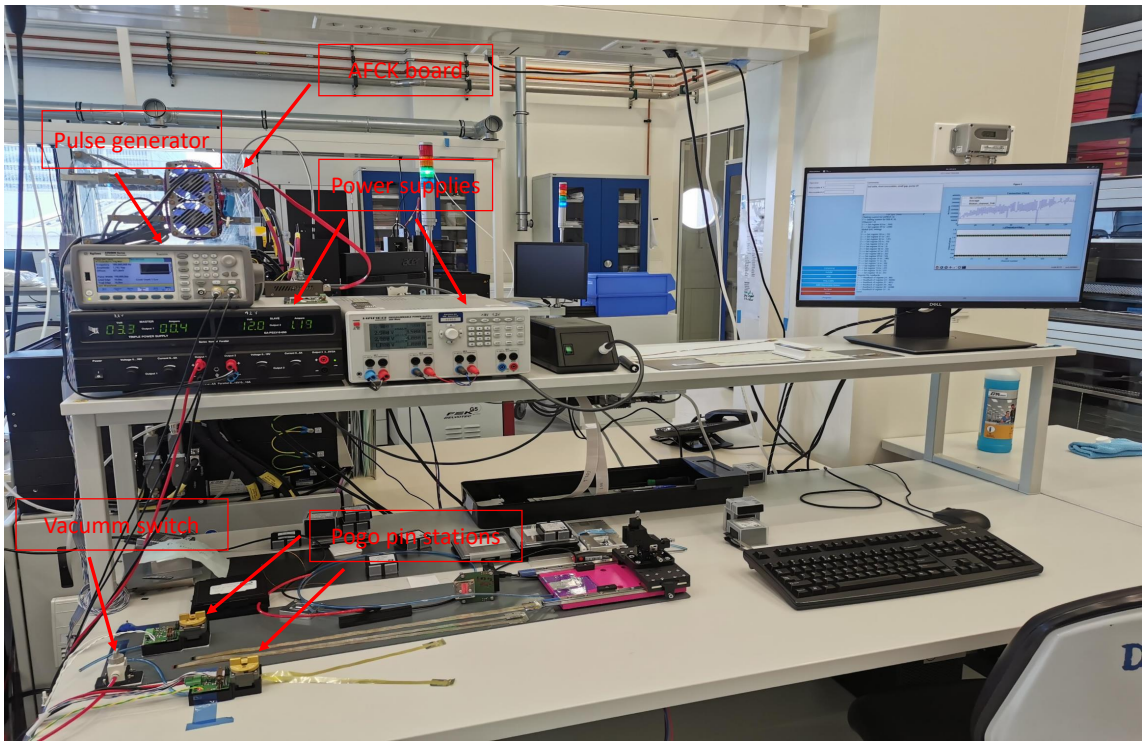


Figure 3.4: Main components of the Pogo prober test setup.

3.4 ASIC testing protocol

The STS-XYTER v2.2 QA procedures focus on testing some of the most important functionalities of the chip. It checks for any damage caused during wafer tests, ASICs dicing, handling and production issues that can result in malfunctions. The testing protocol is divided in several phases or steps, addressing critical points in the ASIC operation [72]. These steps are organized according to the operational order and complexity. The full ASIC testing takes approximately one minute of computing time. Some of the most important elements checked during this process are presented in the flow diagram shown in Fig. 3.6. The main phases are described below:

- Synchronization: This is the first step in the testing chain, after powering on the setup, and it checks that communication with the ASIC via the digital back-end is possible. If a failure takes place during this stage, the synchronization process is relaunched. In case of three consecutive failures, the chip under test is marked with communication problems and the entire QA procedure is ended at this moment (Table 3.1).
- Configuration: All analog front-end and digital back-end registers are written and readout multiple times. In this step, each ASIC is configured with typical operational values. If discrepancies appear among what is written and readout, values are re-checked to confirm the mismatch. Problems are recorded in the log file step by step.

- Current consumption: The chip, from default, has many randomly configured registers, which bring a significant dispersion in the initial current consumption. This step is executed typically after synchronization and immediately after the configuration is loaded. The standard current value after configuring depends mostly on the CSA bias settings.
- ASIC E-Fuse. This process normally will be done at the wafer level, where a unique ID is written into the chip. At this step the ASIC ID is read back. More details about the e-fusing process will be given below.
- Analog front-end check and broken channels: The first step of the signal processing is checked by injecting large amplitude signals at the input of every channel. Values are read on the auxiliary counters of every discriminator. The process is performed for both polarities, which also allows to test the operation of the polarity selection circuit. A successful results is built on two steps:

  1. To record the signals on FAST and ADC counters. This implies that the analog front-end circuit is properly powered and working. A correlation to the measured current after configuration can be found here: if the value is lower than 0.4 A, it indicates that the chip amplifier is not properly working, and therefore, it will not sample the injected signals.
  2. Since every channel is checked, it requires that for such large injected signals, at least 26 out of 31 discriminators of the ADC are fired, as well as the FAST discriminator. If one of these two conditions is not achieved, the channels is labeled broken and its number, together with the cause (FAST or ADC issue), are recorded.

The collected data are initially stored in the format of txt file that also contains the date and time of the measurement as well as the assembly stage. Afterwards, the test data is saved in FAIRDB [73], a dedicated data base branch for storing the QA results of every assembly components in the CBM experiment. The STS-XYTER E-Fuse ID is a unique number that can be permanently

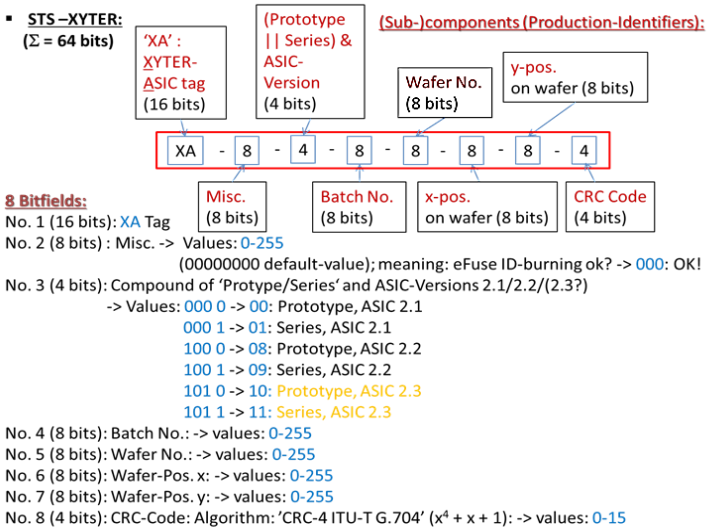


Figure 3.5: Detail schematic of the 64-bits format for the e-fused ID of the STS-XYTER [72].

written into the device by means of electronic fuses (e-fuse). This ID can be read from the ASIC via regular control interface. It allows to identify and track each individual device over the full life

cycle from QA tests over assembly stages to operation. Figure 3.5 shows the 64-bits format for the e-fused ID where features like the ASIC version, batch number, wafer number and position will be stored [72]. This unique ID is very important for the quality control of the detector modules components since it will be used to build a database for storing calibration parameters and different testing results during the detector modules assembly.

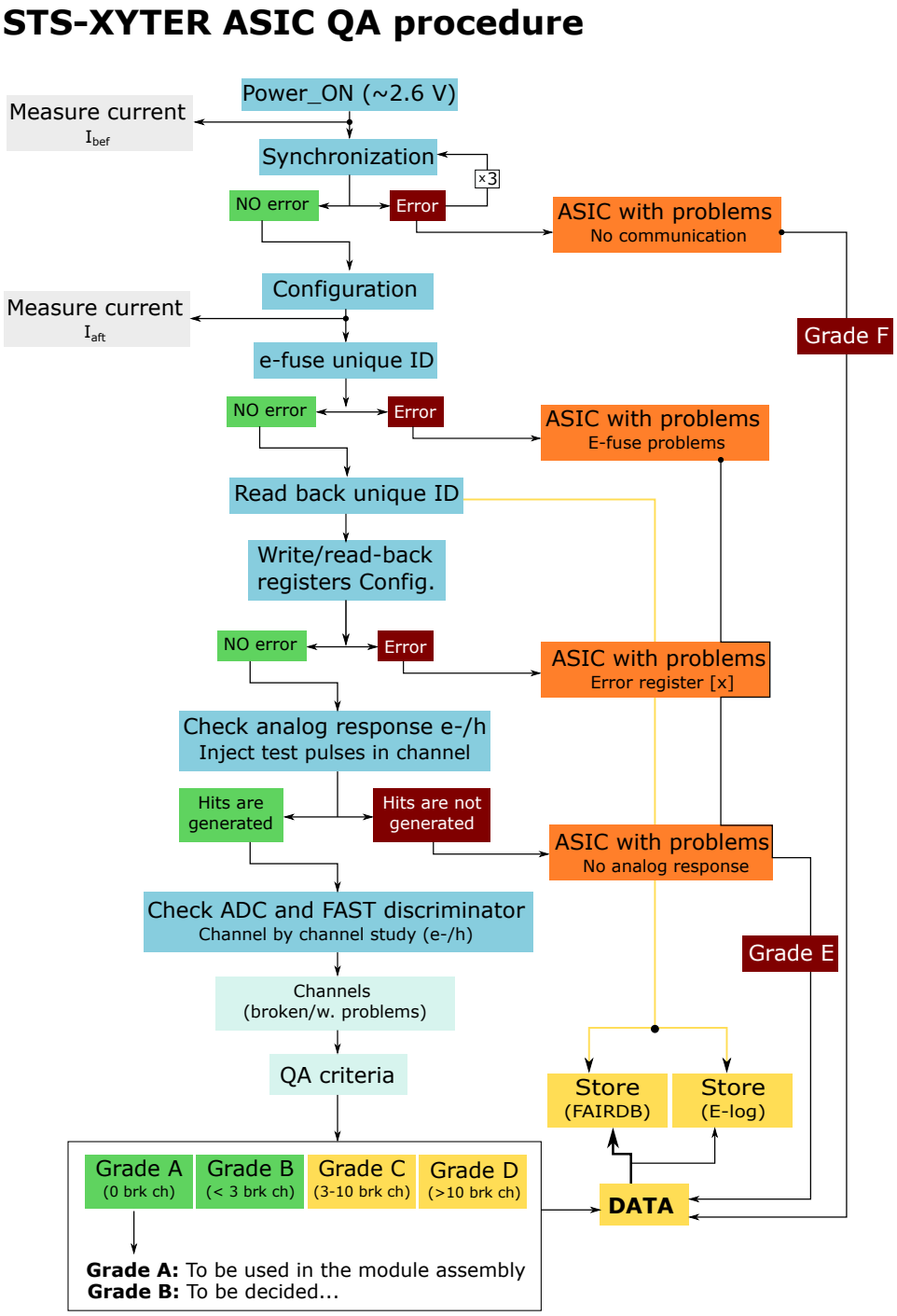


Figure 3.6: Flow diagram of the ASIC test procedure.

3.4.1 Evaluation of the ASIC quality

This process is based on the gained experience testing the previous versions of the STS-XYTER ASIC. The entire procedure checks important chip functionalities and intends to provide a quality grade for every chip. In addition, every ASIC is e-fused with an unique ID that will be retrieved and used during the next assembly and testing steps. At the end of the tests, each ASIC is graded according to its performance. The grading categories are described in the Table 3.1 below. The results of such tests are stored in the directory in a local computer and afterwards in the FAIRDB.

Table 3.1: *ASIC QC grades based on the test results. The tests marked with (*) indicate that they are mutually exclusive.*

	Test				
QA Grade	**Sync**	**E-fuse**	**R/W Config**	**Analog resp**	**Broken ch**
A	✓	✓	✓	✓	0
B	✓	✓	✓	✓	< 3
C	✓	✓	✓	✓	$3 - 10$
D	✓	✓	✓	✓	> 10
E	✓	–*	–*	–*	–
F	–	——— No test performed ———			

Grade B, ASICs with only one or two broken channels, is reserved for those chips that might be used for modules assembly if unexpected problems appears on the STS production. Due to the very good yield (more than 90%) shown for the STS-XYTER previous versions [43], only ASICs with no issues will be taken into account for module assembly. Chips with more than two broken channels will be graded in the categories C or D, depending on the amount of broken channels.

Grades E and F describe ASICs that can not be used under any circumstance; they imply the failure of one of the fundamental chip functionalities. In case of grade F, the ASIC fails the most fundamental tests, i.e., no synchronization or communication with the chip is possible. This type of failure is identified at the beginning of the procedure, and immediately terminated. However, it requires the intervention of the user, who must try to check possible causes for the synchronization failures. After three iterations of the test, if the issue persists, the user should set the synchronization failure flag, which appears in the shape of a buttom in the graphical interface. The information regarding the ASIC is then stored in another file, where a unique ID is established based on the testing date and time **DATE_TIME**.

- **QA grade A:** ASIC ready for module assembly. The chip passed the tests flawless and no issues were found.
- **QA grade B:** ASIC can also be considered for the module readout. The chip passed the tests but there are up to two broken channels.
- **QA grades C and D:** The ASIC has multiple broken channels (three or more). It is not recommended to be used in the module assembly.
- **QA grade E:** This category is issued when:
  - the ASIC has one or multiple essential registers not operating properly (errors were encountered while writing and reading the main configuration register of the ASIC);
  - the ASIC can not be e-fused or have a corrupted E-fuse ID;

- the ASIC did not respond to injected pulses. Therefore, its analog front-end is not properly working.

- **QA grade F:** No possible communication with the ASIC.

Further investigations can be done for these ASICs to confirm the problems and if it is possible to restore them to their regular performance.

3.4.2 Evaluation of the chipcable quality

After the ASIC is fully tested, the next step in the assembly process is the bonding of microcables onto the chip. The ultra-thin microcables are used to interconnect the silicon sensors and the readout electronics, providing minimized material budget [74, 75]. They are composed of a stack of analog signal cables, meshed spacers and shielding layers. Figure 3.7 shows a magnified picture of a microcable bonded onto the STS-XYTER ASIC on the left side and its positioning inside the pogo pin station on the right. For setting properly the chipcable inside the pogo prober, a vacuum pump is used to ensure its correct position. This process was conceived to be performed in two steps, where the bonding quality is tested for each of the microcables. However, the test is executed only once. There are two main reasons for this: first, the reliability of the TAB-bonding process during precious tests, second, the use of another testing interface called testfan, which is more suitable to be used in the bonding machine since it uses the microcable technological zone. The control procedure for the pogo prober uses the same experimental setup described above for the ASIC test. In addition, the chipcable layers (one or two) are placed on a dissipative ESD surface for more stable results during the quality control. When the two microcables are bonded, they are spread apart on the surface to avoid electromagnetic shielding from the top cable to the bottom one.

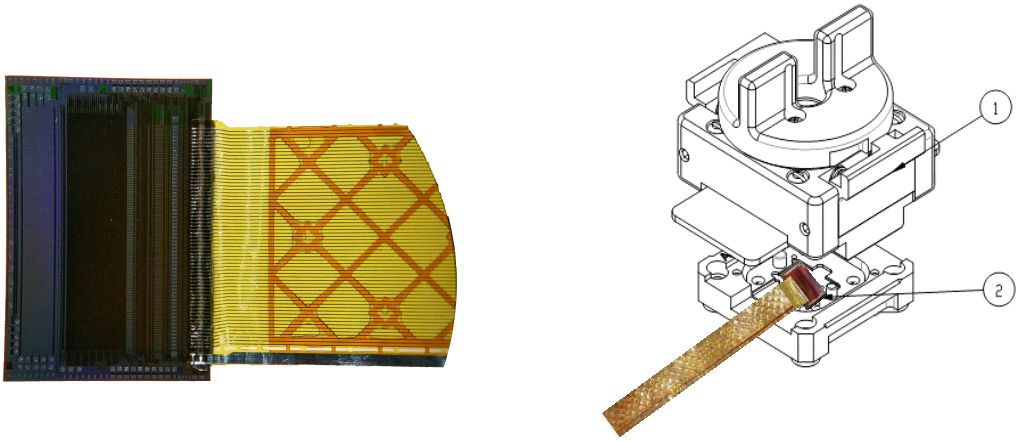


Figure 3.7: *Detail of a microcable layer bonded onto the STS-XYTER ASIC (left side) and its positioning inside the pogo prober (right side).*

To evaluate the bonding quality process, noise hits are collected in every channel. The microcable structure is sensitive to electromagnetic pick up in a large frequency spectrum and also its capacitance (in the order of a few pF) is responsible for the thermal noise contribution that can be measured in the ASIC. This allows to use the noise hits generated to identify defective bonds and broken channels.

The procedure can be described as follows: At a relative low threshold, multiple noise hits will be stored in all channels counters of the ASIC. Due to their limited buffer size (12-bit/counter = 4096 hits), they are read and reset at least 5 times continuously. The noise counts are then summed

up for all discriminators in a channel. The channels distribution of noise counts is then analyzed by an algorithm that controls the average noise level and identify defective channels due to their lower noise counts. Among the broken channels, it is possible to identify two type of defects: if the channel shows 0 counts, or if a few entries are present. The first one implies that the ASIC analog front-end is not working and no hit in the charge sensitive amplifier will be amplified. This is mostly a consequence of an ESD problem during the handling and bonding of the microcable onto the chip. This ESD situation has been heavily reduced with the implementation of the diode based protection for the STS-XYTER v2.2 [76, 77]. The second one reflects that the ASIC channel is shown, but the bond between ASIC and microcable is broken. Figure 3.8 shows an example of the procedure for checking the chipcable quality. The top plot shows the total number of counts for the chipcable with the established thresholds for detecting broken channels. The bottom plot describes the two rows of bonded channels. If a broken channel appears, the color will turn red, otherwise it will remain green. In addition to the displayed graphics, an output file in txt format is also generated, storing the details of the tests. The data are saved afterwards in the FAIRDB.

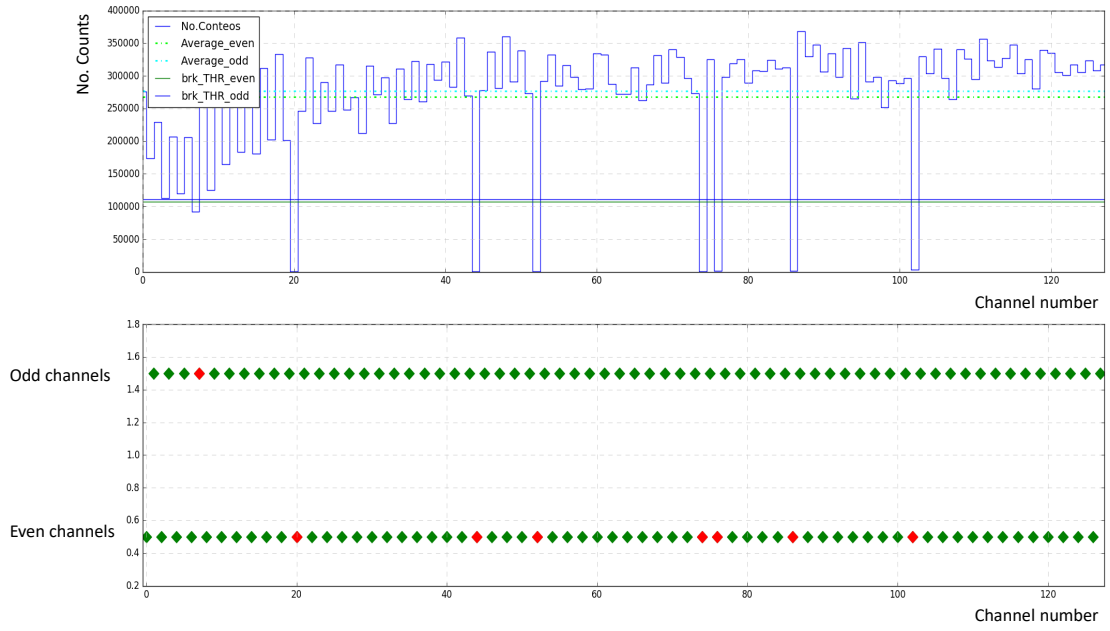


Figure 3.8: Noise counts channels distribution measured on the pogo-prober station.

3.5 Software developments and GUI implementation

The software installed with the purpose of executing the ASIC and microcable testing is based on Python version 2.7.18 running on Kubuntu 20.04 LTS. This version was selected due to compatibility issues between the IPbus libraries and higher version of Python. The IPbus protocol implemented in the version 2.8 is a simple packet-based control for reading and modifying memory-mapped resources within FPGA-based hardware devices. The IPbus suite of software and firmware implements reliable high performance control for particle physics electronics [59]. It consists of a firmware for implementing the protocol within end-user hardware, a ControlHub that acts like software application mediating simultaneous hardware access from multiple uHAL clients, a Hard-

ware Access Library (HAL) providing an end-user C++/Python API for IPbus read, write and read-modify-write transactions.

The existing software, for ASIC and microcable testing, needs to be optimized and automatized in order to bring a user friendly experience, aiming towards the series production. For this purpose a Graphical User Interface (GUI) has been developed. A GUI is an interface through which users interact with electronic devices via visual indicator representations. It uses a combination of technologies and devices to provide a platform that users can interact with, for the tasks of gathering and producing information. Replacing the code with icons, users can quickly and easily accomplish their tasks.

3.5.1 GUI characterization

Graphical user interface design principles conform to the model-view-controller software pattern, which separates internal representations of information from the manner in which information is presented to the user, resulting in a platform where users can immediately access the possible functionalities rather than inputting command codes. Users interact with information by manipulating visual widgets, which are designed to respond in accordance with the type of data they hold and support the actions necessary to complete the user's task. The GUI is running on PyQt4, which is a library that allows using the Qt GUI framework from Python. Qt itself is written in C++, by using it from Python, applications can be build much more quickly without sacrificing much of the speed of C++. Some of the main advantages of using PyQt are: a flexible code, since

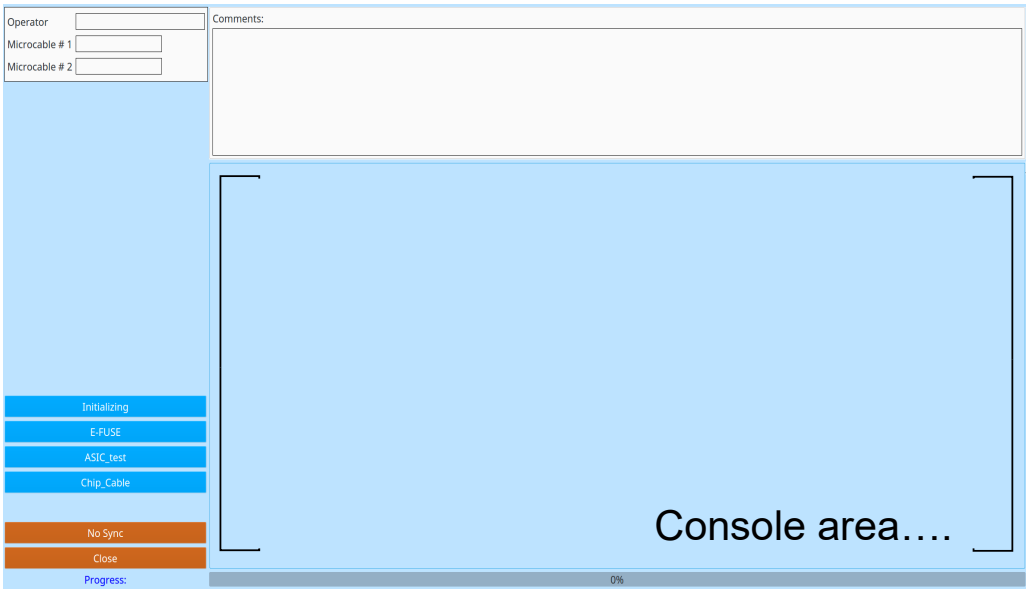


Figure 3.9: Graphical User Interface (GUI) under use in the pogo pin setup

programming with Qt is designed around the concept of signals and slots for establishing communication among objects that permit flexibility when dealing with GUI events and results. Qt uses a wide array of native platform APIs for the purpose of networking, database creation, among other. It offers primary access to them via a unique API, with several widgets, such as buttons or menus, all designed with a basic appearance across all supported platforms. Since PyQt is one of the most used UI frameworks for Python, a wide array of documentation can be easily access.

Figure 3.9 shows an schematic of the implemented GUI. Some of the most important parts are described below:

- Operator Box: This label is important for having a reference of whom performed the test.
- Comments Box: After the test is done, if the user considers that some special notes about the test should be written.
- Console: It has the same function and features of a terminal. In this case, it is running all the sub processes in the GUI, i.e., prints, errors.
- **Buttons**:
    1. **Initializing**. It will set all the environmental variables and establish communication with the ASIC. It will also establish a running configuration on the ASIC which mostly includes setting the proper analog front-end registers. At this point the operator should take note of the current drawn by each ASIC after the full configuration, which should be very similar among them and approximately 0.4 A. These statistics will help to identify possible issues with the ASICs.
    2. **E-Fuse**. It will execute the ASIC E-Fusing. This step can be skipped if the ASIC has been tested before in the pogo station. If the ASIC has already been E-Fused, it will not be possible to assign another ID.
    3. **ASIC_test**. It will execute all necessary tests to evaluate the ASIC quality (see Figure 3.6). A QA grade will be assigned to the chip after the testing is done (see section: Evaluation of the ASIC quality).
    4. **Chip_cable**. It will run the test to evaluate the microcables QA. It will provide two plots as a result of the tests. The first one, with the total number of counts per channel and the respective threshold set for detecting broken channels. The second one, with all the channels divided in odd and even. The operational channels will be green, while the broken ones will be red (see Figure 3.8).
    5. **No Sync**. If there is an error during the sync procedures, the program will stop and raise a flag. If the problem can't be solve, after trying to re-initialize several times, the operator should press the button **No Sync**. The program will activate an automatic counter to keep the statistics of ASICs with no synchronization.
    6. **Close**. It will close the GUI together with all sub processes running behind.
- Progress bar: It will provide a visual effect of the running test.

All the buttons in the GUI are linked to the python scripts executing the described tests. These scripts are sub processes of the main GUI, keeping all the functionalities of the original test.

3.6 Results and statistics

Since January 2021, many STS-XTYTER v2.2 ASICs have been tested and used in the assembly of detector modules and prototype FEBs-C. For this chapter a sample of 450 ASICs was analyzed uniformly using the new procedure which offers the highest standards of robustness and reliability. The main findings are summarized in Table 3.2. Out of the total number used like sample, only 27 have shown problems, which represents 6% of the total. Out of the total number of ASICs with problems, 13 were identified with issues and will not be used in the assembly procedures. These crucial problems are mostly related to communication with the digital interface of the ASIC and the

response of the analog front-end. From the 12 ASICs with no analog response, 2 present issues with the fast discriminator and 10 with the ADC. Only one chip presents synchronization problems. The 10 chips identified with multiple broken channels have been selected for the assembly of prototype FEBs-C, used afterwards for research purposes.

Table 3.2: *Sample of statistics on STS-XYTER v2.2 testing.*

Total number of tested ASICs	450
ASICs with problems	27
Synchronization problem	1
No analog response	12
Single broken channel	4
Multiple broken channels	10

Since the ASIC yield is larger than 90% (see Figure 3.10), the acceptance criteria to be used in the module assembly is set such that only chips without problems are going to be selected. The ASICs with only one broken channel will be kept in reserve for being used during module assembly in case of needed. This decision is made considering that during the next phases of the assembly procedures, some additional channels might be damaged, making the object not usable for the final STS detector.

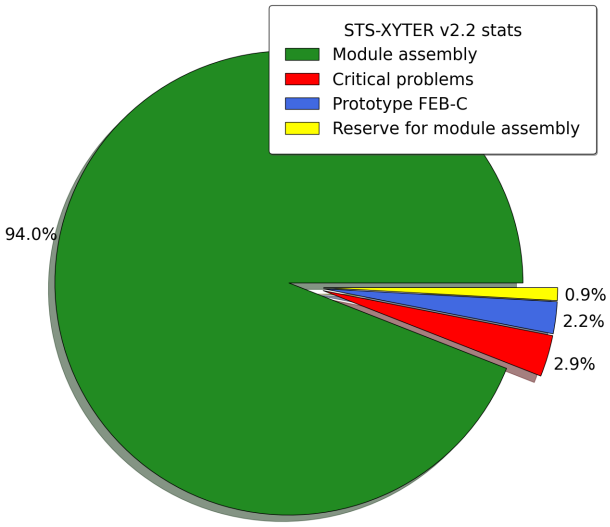


Figure 3.10: STS-XYTER v2.2 stats in percent from the 450 used like sample.

A sample of 450 chipcables was also considered for this analysis, since the test procedures have been changed multiple times, the last format of tests offer more reliability. Figure 3.11 shows the broken channels distribution in logarithmic scale in the Y axis. Out of the total sampled used:

- 342 have shown no broken channels;
- 73 with one broken channel;
- 26 with two broken channels;
- 4 with three broken channels;
- 5 with four broken channels;

Out of the total, 76% of the tested chipcables have no broken channels and 16.2% have only one. The broken channels are positioned arbitrary, with no specific patterns visible. If a total of 15 to 20 broken channels per module is considered, only chipcables with a maximum of one broken channel can be selected. This represent, the 92.2% of the total tested, which corresponds to a very good yield. Although this selection criteria could be costly for the experiment, since the components are expensive and also there are some restrictions in the microcables availability. Besides, since 16 chipcables are used in one module, it is possible to mix no broken channel ones with more than one broken channel chipcables in order to match the final criteria of around 3% of broken channels.

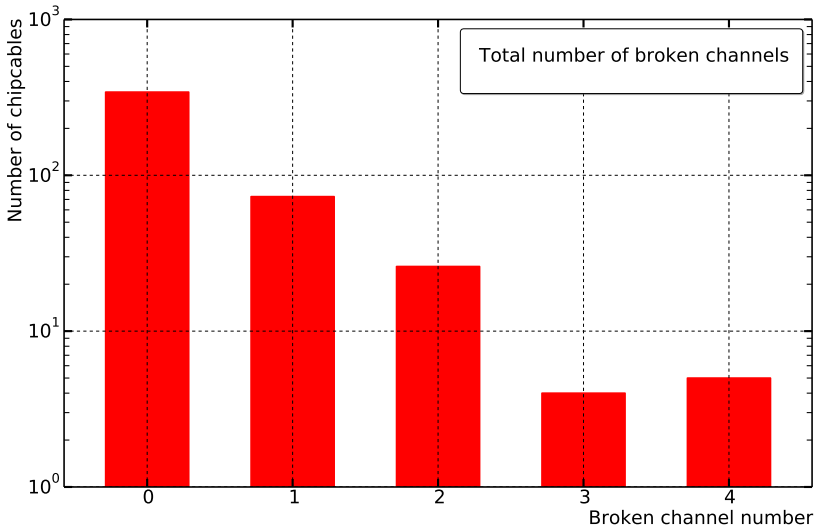


Figure 3.11: Broken channel distribution for the 450 chipcables used during testing.

Some of the next steps in the quality control processes, aiming to the future STS production, are the implementation of a new EMU-board for the readout chain like substitution of the data processing (FPGA based) board. This means a migration of the software to a new platform based on Python version 3, making possible the use of PyQt5 with all its advantages over previous versions. The readout of the temperature and the VDDM will also be integrated in the QA procedures. It will allow the association of non regular effects during measurements with parameters like the temperature or the VDDM potential on the chip.

3.7 Summary

This chapter has presented different results, aiming to check the ASIC and chipcable functionalities and also establish a possible decision criteria based on the number of defective channels, power consumption and other operational aspects.

A dedicated setup has been used, based on a custom designed pogo-pin station, where a total of 450 ASICs and chipcables were tested. QA protocols have been designed and optimized in order to improve the testing procedures. Several assembly issues are coming from factory defects, or appear after transportation or incorrect handling during the test procedures. Therefore, the quality grade for every ASIC is also based on the gained experience form previous versions of the chip. In the sample of chips used for the test, more than 90% were in perfect condition, which represents a very good yield. A decision criteria has been proposed for the chipcable quality tests. Out of the total sampled used, more than 90% presents one or none broken channels, being a very good result. A GUI has been developed in PyQt version 4.0 for making the testing process as user friendly as possible. The procedures take around 1 minute for ASIC testing and similar time for the chipcable test. The implemented software for testing the chips and chips with microcables has been in use since 2021, making significant improvements in the detector modules assembly aiming to the STS production.

Chapter 4

Performance of STS fully assembled modules

4.1 Introduction to the STS module as main building block

The main STS building block is the detector module, which consists of a double-sided silicon microstrip sensor connected through a stack of microcables to the custom-developed ASICs on two front-end boards (FEBs). The sensors have been produced by Hamamatsu Photonics K.K with a thickness of 320 μm. The signals from the double-sided silicon sensors are read out by the custom-designed STS-XYTER ASIC [53, 78]. For more information see section: The STS detector module.

The test and characterization of fully assembled modules is fundamental for proving assembly concepts for the final STS detector. Across the last years, the CBM-STS project has achieved important milestones related to the assembly and successful operation of the first modules [79]. These objects have been used in multiple studies to demonstrate the performance and also to characterize the latest versions of the STS front-end electronics [80, 81]. In parallel to these developments, it became necessary to work out a general testing procedure with the following purposes: to evaluate the functionalities of the modules with the final version of the components, to determine the optimal operating parameters for each individual module, to identify flaws in the final produced objects prior to further integration and to optimize the quality control procedures. This last one can also be understood as the first step towards a more robust quality control concept, which aims to ensure reliable performance of the modules in the final STS detector and high production yield.

The assembly of STS modules is a complex process carried out in multiple steps. Before their assembly, all components are thoroughly tested, graded and selected [82, 83, 84]. Through the process, the quality of the components, bonds and compound objects, as well as the basic functionalities of the front-end electronics are regularly checked. Figure 4.1 shows the workflow diagram for detector modules assembly with the main QA steps in between.

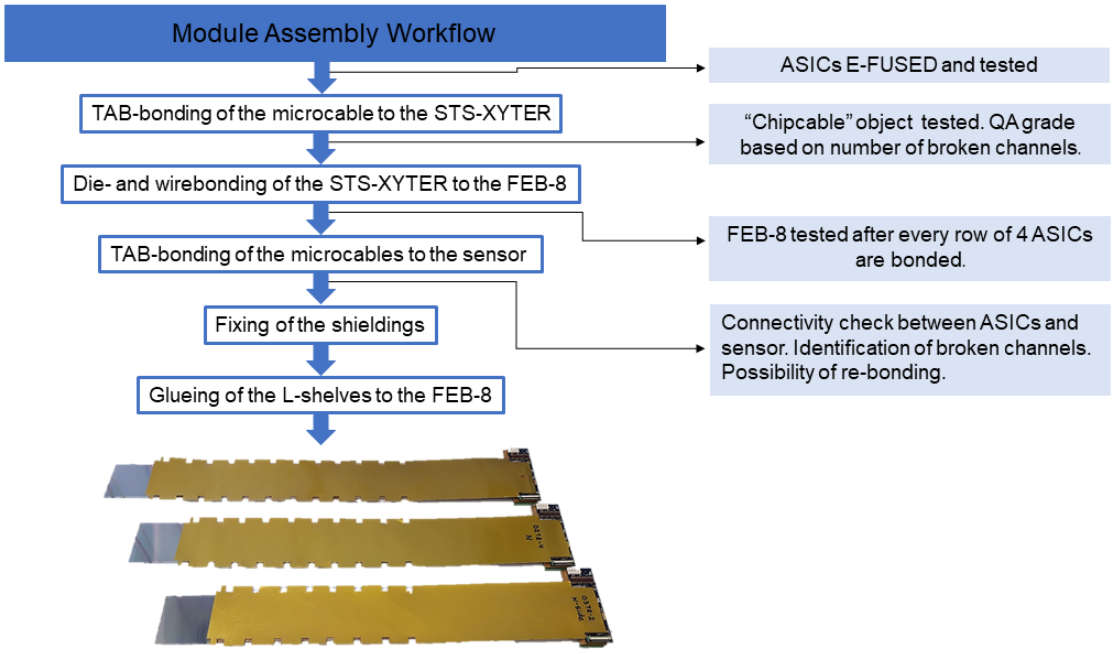


Figure 4.1: *Module assembly workflow showing also the sequential test procedures.*

This chapter presents a series of tests, which aim to evaluate the module's operation, and establish the basic elements for quality control criteria. The performance of several fully assembled modules has been checked highlighting results of calibrating the measured circuits and other electrical properties such as: the overall noise levels, optimization of the different ASIC parameters as a function of the noise levels, signal readout, high voltage scans and noise stability tests. In addition, it includes a study on the channel's yield and the main issues affecting their performance. The results of this work are considered the first steps for developing a quality control concept towards pre-series and series production.

4.2 Experimental setup

When modules are fully assembled, they are moved carefully to the STS laboratory, where a detailed characterization of the object is performed. This is done in the so-called module test-box, a precursor of the module quality control setup. The setup consists of a light-tight shielded enclosure box, made of aluminum, which can easily accommodate modules with different dimensions mounted in close-to-final position. It also implements all necessary services: low and high voltage, readout components and FEB cooling. In addition, it has a thin aluminum window that can be used for measurements with radioactive sources. Figure 4.2 shows a detailed view of the described setup.

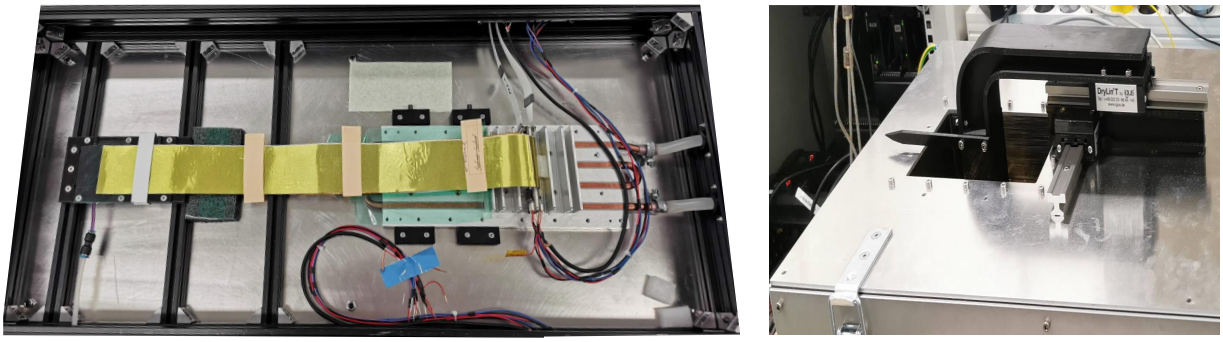


Figure 4.2: *The detector module test box with services in the left side. Window with holder for installing a radioactive source in the right side.*

The readout chain used in the module test setup consists of three main components:

- The FEBs, carrying 8 ASICs each of them, are connected to the 1024 channels of one sensor side. ASICs are positioned in a staggered scheme for matching the sensor width and strip pitch. In addition the FEB contains 4 voltage regulators for the LV supply of the chips, connectivity pads for shielding of the analog sensor cables and the readout interface and termination components for clock and down-links.

- The Common Readout Board (C-ROB), providing data aggregation and electric to optical interface. The board will provide 6 phase adjustable clocks and 6 down-links at 160 MHz. An FPGA mezzanine card is connected to the C-ROB, the STS FMC card carries 5 ZIF connectors, each connected to 8 up-links allowing to connect 5 FEBs with one up-link per ASIC. It also includes the bias resistors for the up-links which guarantee a well-defined potential to the GBTX E-link inputs behind the AC coupling capacitors [47].

- The Data Processing Board (DPB), an FPGA based board, where incoming data are processed via multiple lower speed short distance links, concentrated, and then forwarded to the FLES via higher-speed, long distance links. As part of the Timing and Fast Control (TFC) system, the DPB ensures transmission of the reference clock and synchronous commands necessary to synchronize the front end electronics. It also provides an interface for the Detector Control System (DCS) to configure readout and front-end electronics (FEE) [78, 56].

Noise problems are often not encountered during the design phase of a detector system, but in the case of silicon microstrip sensors, the very low signal levels and the high number of channels make them very sensitive to noise sources. External electromagnetic fields introducing pickup currents into the systems can be one of the main noise causes. The ground currents from a large scale power supply network may also create additional noise. Therefore, a good design of grounding, shielding and power distribution is essential to achieve a good performance. In the module test box setup, a symmetric and floating ground scheme for the sensor bias and the front-end electronics is implemented. Each module side has a separate power domain [85] and a DC-decoupling interface is also implemented between the floating FEB and the data transport hardware (C-ROB). The low voltage power lines use radiation hard and magnetic field tolerant DC-DC converters before the linear regulators on the board [86]. They are used to provide the required potential for operating the front-end electronics on each side. The microcable shields are connected to the FEB grounds. The test box is grounded and electrically insulated from the support table and the HV common

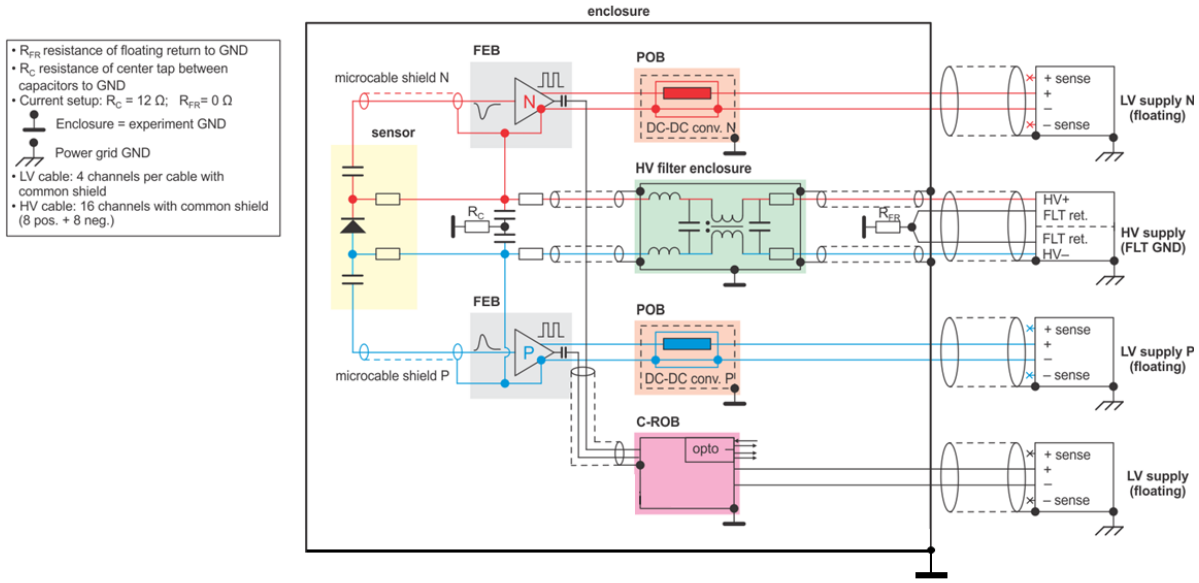


Figure 4.3: *Power distribution scheme for testing the STS modules in the test box setup.*

return is not connected to the box enclosure. Figure 4.3 shows the powering scheme implemented in module test box, including the POB and the sensors.

4.3 Test and characterization of fully assembled modules

During the module test, multiple operation parameters are checked. These include FEB verification, charge calibration, noise levels, signal readout and functional channel yield. These checks aim to examine a broad range of the ASIC functionalities and to directly assess crucial electric characteristics of the entire module. The collected data allow to optimize the ASIC settings for a better module performance and to identify possible reasons for module malfunctions. In addition, they bring valuable feedback for improving the testing procedures.

Initially, each module is visually inspected, in search for possible damages that could occur during the handling and installation in the test box. If no issue is found, the module is connected to the power supplies and low voltage is applied. Figure 4.4 shows the main steps in the working flow diagram for the modules testing procedures. The testing procedure starts with a check on the electrical connections and the power consumption of each FEB. Afterwards, a data link initialization and synchronization process is launched, allowing the user to directly communicate with each ASIC on the module. Register configuration, multiple write/readback actions, power consumption after configuration are some of the parameters initially verified for each ASIC. The analog response is then checked for each ASIC individually. At this point, the sensor is biased up to 150 V for the first time, paying special attention to the leakage current and any possible electrical short circuits between the shielding layers.

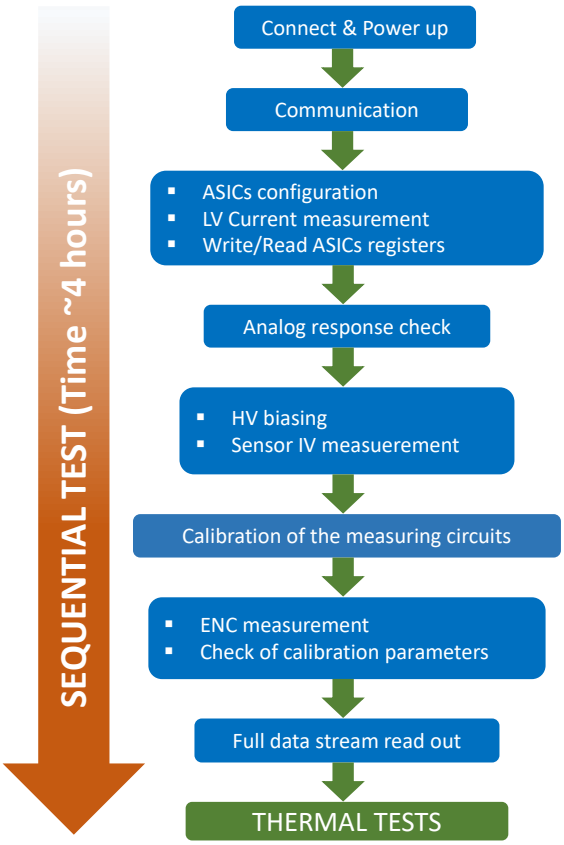


Figure 4.4: *Module tests diagram showing the sequential test procedures.*

4.3.1 Calibration procedures for modules testing

The next step is devoted to the calibration of the analog front-end (AFE) measuring circuits. This procedure aims to determine channel-to-channel threshold corrections using the built-in ASIC functionalities as described in chapter 2 section: Validation of the ADC calibration using an external pulse generator. Charge pulses of fixed amplitude are injected at the input of each channel using the internal pulse generator, and the recorded discriminator counter values are analyzed for the 31 discriminators. Corrections are then individually applied using dedicated trimming digital-to-analog converters (DACs). For more details see Appendix C: ADC calibration. Output files are then generated for each ASIC containing the calibration matrix. These files will be used in the next testing steps [53, 63].

The charge calibration is a crucial step in module testing. The ADC gain and threshold spreads are among the parameters that characterize the correct calibration of the module, and therefore, its response. ADC gain and threshold are determined for each channel by performing a so called S-curve scan, where pulses with varying amplitudes are injected at the input of the analog front-ends. The response function of each discriminator to a scan of pulse amplitudes is recorded in dedicated counters, and individually analyzed. The data are fitted with a Gaussian-Error function to extract the inflection point of each curve, which is considered to be the effective discriminator's threshold. The threshold of the first discriminator also represents the effective detection threshold. The gain, on the other hand, is extracted from a linear fit of the thresholds versus the injected charge. This process also allows to verify the ADC linearity after calibration. Figure 4.5 (left side) illustrates the distribution of the ADC gain across all channels for a typical module. The average gain values

for each sensor side are displayed on Fig. 4.5 (right side), where histograms show a good agreement between both polarities. The gain deviation, for all channels, with respect to the main value is below 10% for both polarities.

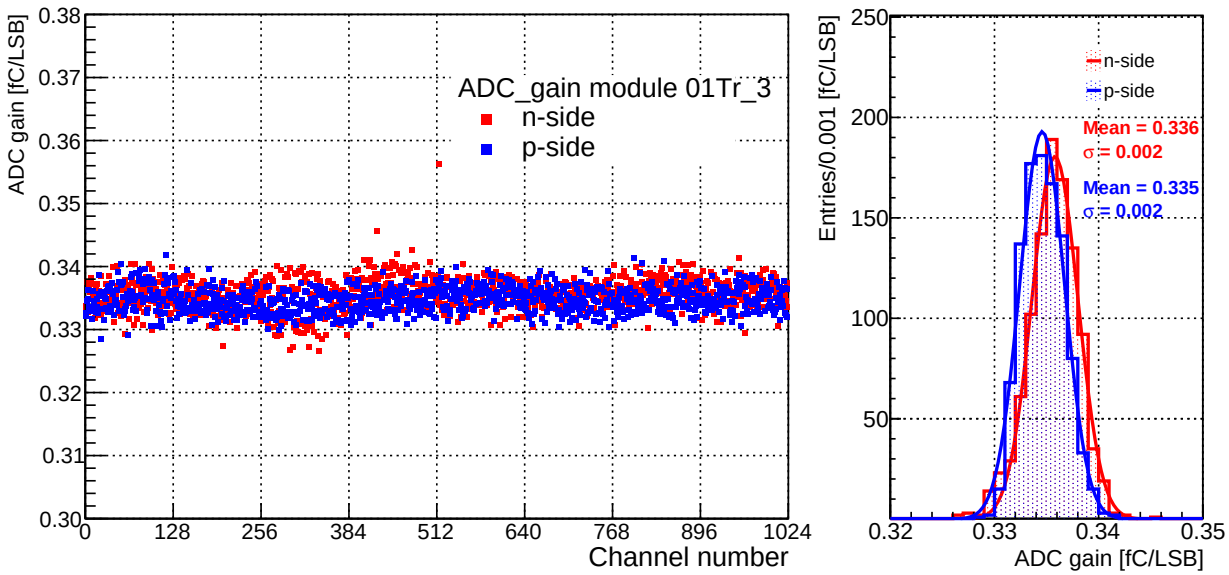


Figure 4.5: *Left: ADC gain distribution for all channels across a typical STS module. Right: ADC gain corresponding histograms, with mean and sigma values determined for each side through a Gaussian fit.*

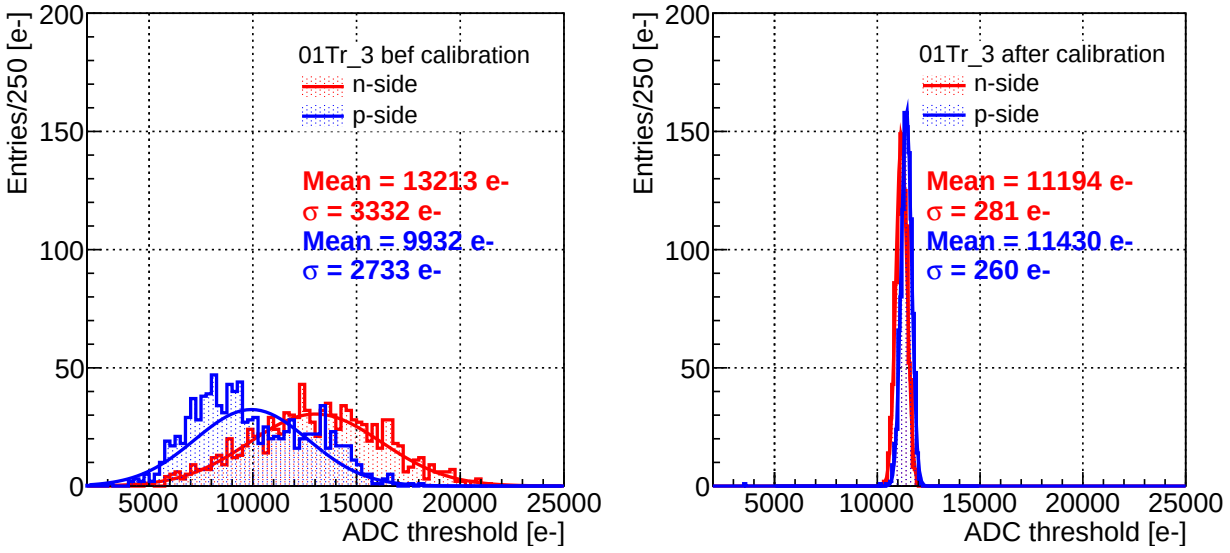


Figure 4.6: *ADC threshold distribution comparison, before (left side) and after (right side) calibration. Channel-to-channel threshold differences are reduced by a factor of 10 after calibration.*

A comparison of the channel's threshold before and after calibration is shown in Fig. 4.6, for the biggest operating range of the ASIC (see section: Linearity of the *VRef_T* transfer function). The comparison between the width of the distributions demonstrates how channel-to-channel spread is

reduced up to 10 times through the calibration. These results are considered sufficient to ensure an adequate and homogeneous detector performance. Similar statistics on the parameters of the ADC are summarized in Table 4.2 for other tested modules.

4.3.2 ENC investigations

For each channel, noise levels are also extracted from the same S-curve scan, as described above. Although, ideally the discriminator response would follow a step function, in reality, the transition is smeared by the electronic noise. The width of the channels response (number of counts vs injected pulses) is an effective measurement of the overall noise. Figure 4.7 shows the equivalent noise charge (ENC) values across all channels. The selected module was symmetrically biased at 150 V to ensure full depletion of the sensor. The system noise, around 1000 e- ENC, is in agreement with an estimation based mainly on the total detector capacitance (Equation. 4.1) [87, 88], depicted with a green dashed line. The different terms in Eq. 4.1 are labeled according to their contribution, and the factor 25 (e-)/pF represents the ASIC noise dependence on the input capacitance (see section: Noise dependence on input load capacitance). The 6.2 cm and 49 cm values correspond to the sensor and microcable dimensions for the specific module under test. The intrinsic ASIC noise level of approximately 350 e- ENC is also shown for reference with a yellow dashed line.

$$\begin{aligned} ENC &= \left[\underbrace{6.2\ cm \cdot 1.02\ \frac{pF}{cm}}_{sensor} + \underbrace{49\ cm \cdot 0.38\ \frac{pF}{cm}}_{microcable} \right] \cdot 25\ \frac{e^-}{pF} + \underbrace{350\ e^-}_{ASIC} \\ &= 974\ e^- \end{aligned} \tag{4.1}$$

Across the entire distribution, different structures can be observed. Unconnected channels can be distinguished by the reduced noise level compared to the connected ones. The significantly larger noise levels in the first group of channels on the p-side corresponds to the corner strips (see section: Z-strips studies).

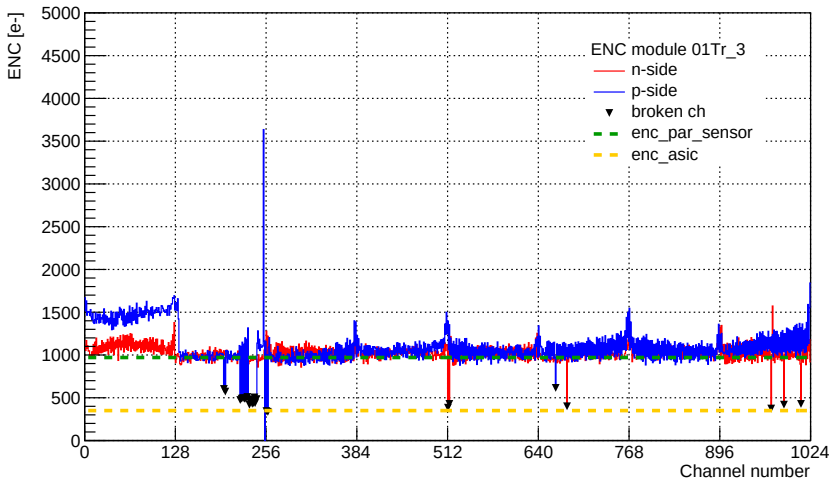


Figure 4.7: *Average noise levels across all channels in module 01Tr_3 in the test box setup.*

Small discrepancies between odd and even channels can also be distinguished for both polarities. This effect is clearly visible when looking at the ENC distributions for odd and even channels separately, see Fig. 4.8. The differences are related to the routing and stretching of the microcables

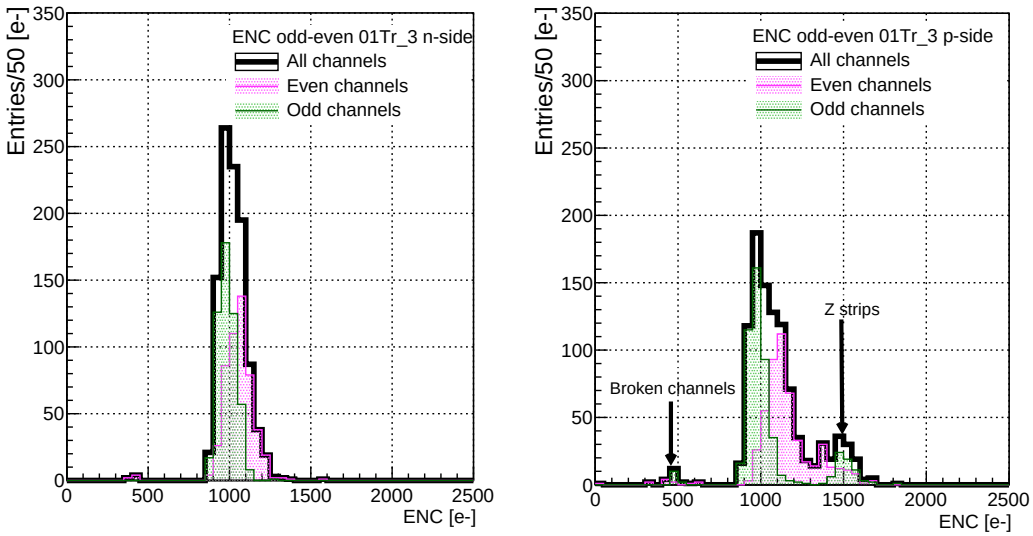


Figure 4.8: *Difference between odd and even channels on module 01Tr_3 for both polarities.*

during the measurements. On each ASIC, signals for odd and even channels are routed in different microcables. The inhomogeneous spaces between them and in relation to the shielding layers, affect the effective capacitance of each signal line, leading to different noise levels for the inner and outer channels. An effective way to reduce this issue is by stretching the microcables and shielding layers properly. This odd-even differences disappear when the modules are mounted in a carbon fiber ladder, as in the final detector setup (see Appendix D: Noise comparison for module 01Tr_3 in different setups).

4.3.3 Z-strips studies

On the STS sensors, it is well known that the n-side strips are oriented parallel to the side edges of the sensor, while the p-side strips are arranged under 7.5 degree with respect to the n-strips. On the p-side, where the strips are inclined, the short strips in the upper left and lower right corners are interconnected between their readout layers through horizontal routing lines on a second metal layer. Therefore, they can be read out from the same edge. The strips orientation scheme and the interconnections on the p-side are shown in Fig. 4.9, while Table 4.1 summarizes the number of Z-strips for the different sensor sizes.

Table 4.1: *Z-strips number for different sensor sizes.*

Sensor variant (cm^2)	Number of Z-strips
6.2 × 2.2	42
6.2 × 4.2	88
6.2 × 6.2	134
6.2 × 12.4	274

These strips are hereafter referred to as Z-strips due to their geometrical shape. For the Z-strips, the overall length is larger and consequently the series resistance and capacitive load at the input of the amplifier are bigger. Therefore, the series voltage noise component is larger compared to the rest of the strips. This can be observed in the first 134 strips of the p-side in Fig. 4.7.

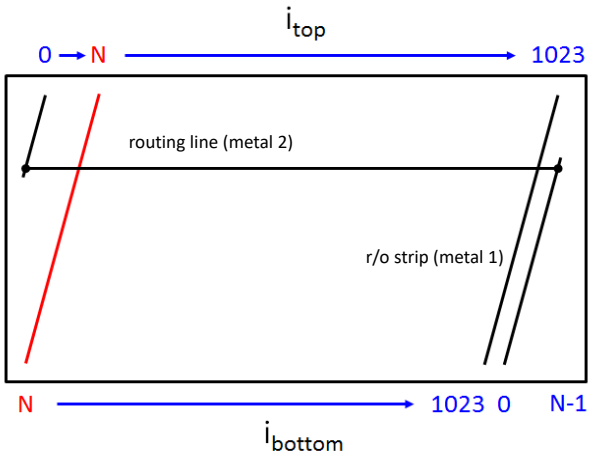


Figure 4.9: *Schematic of the p-side strips distribution for the STS sensors.*

Figure 4.10 shows the difference between the average noise calculation for each module (see Table 4.2) and its respective noise average for the Z-strips. The error bars, shown in the green area, correspond to the standard deviation with respect to the main value. The average noise difference across all modules is approximately 516 e-, with a standard deviation of 16.3%. There is a relativity large spread among the ENC differences for all modules. Since the modules were not tested consecutively, the measurements conditions in the laboratory might change slightly from module to module. If the overall capacitance of the double metal layer is considered as the only responsible for the noise excess, the average capacitance for the Z-strips in the double metal layer could be approximated to 20.6 ± 3.4 pF.

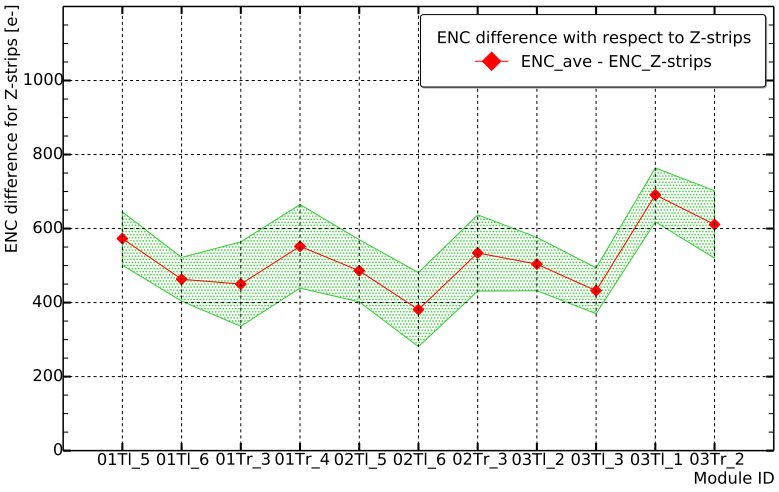


Figure 4.10: *ENC difference between the standard noise average and the Z-strips noise for different modules.*

4.4 Study of the STS-XYTER v2.2 settings in the module readout

This section summarizes the results of multiple tests, oriented to measure the noise levels in the STS-XYTER v2.2 at the modules level. The scan of a group of user-controlled settings (current on the CSA, magnitude of the feedback resistor and shaping time) intends to check and optimize some of the main operation settings that could influence the overall performance of the STS detector.

The proper operation of the CSA bias current has a significant influence on the chip performance and noise reduction since it is in charge of amplifying the extracted signals, induced by the incident radiation in the detector. The CSA bias current is related to the VDDM potential in the ASIC. The amplifier bias current can be selected in the range 0 to 4 mA, with a typical value of 31 LSB units, which corresponds to approximately 2 mA/channel. Figure 4.11 represents the noise in two different ASICs as a function of the CSA bias current for module 01Tr_3. Every point represents the average across all channels and the error bars correspond to the standard deviation with respect to the main value. A stable operation range can be observed for the p-side. For the n-side, after values above 16 LSB units, an increase of approximately 70 electrons compared to smaller values of the CSA bias current is visible. This difference is significantly small and it is safe to say that the noise levels are approximately constant for both polarities in the measured range of the CSA bias current.

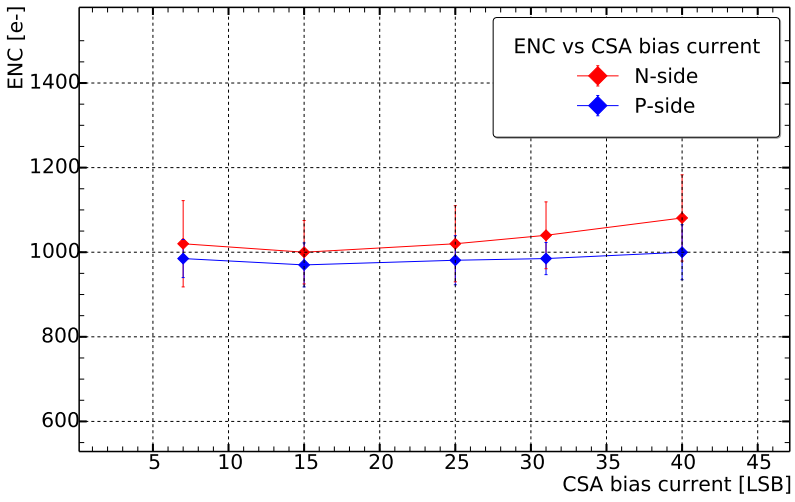


Figure 4.11: *Measured ENC for selected ASICs as a function of the CSA bias current for module 01Tr_3.*

The feedback resistance determines the time required for the CSA baseline to be restored after a signal is amplified (see section: CSA discharge time constant estimation). Therefore, it is a key feature for operating the modules in a high rate environment. In an ideal system, the signal amplitude in the CSA should remain constant while the signal is being processed in the shapers, however, this implies a very large feedback resistance, and it can lead to a large pile up effect. As an alternative, the ASICs could be operated using a reset circuit that discharges the CSA quickly to the baseline, called fast reset. Several issues were found during the characterization of the STS-XYTER v2.2, making fast reset circuit unusable for operating purposes (see section: Charge sensitive amplifier fast reset). The ASICs operation in a high rate scenario is still possible without this functionality, simply by reducing the discharge time constant of the CSA. Theoretical estimations of the noise contribution suggest that lower feedback resistance can be responsible for more than 15% of the parallel current noise in the chip for non-irradiated sensors [64]. Consequently, it is important to consider the influence of this parameter in the overall system noise.

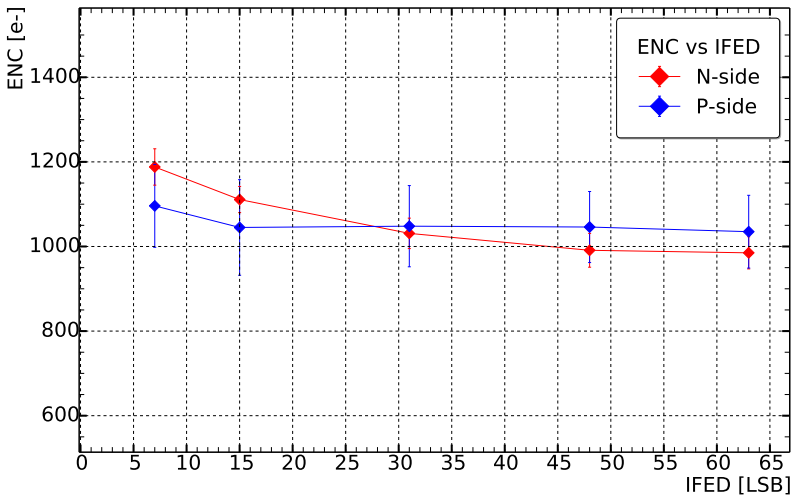


Figure 4.12: *Measured ENC for selected ASICs as a function of the IFED bias current for module 01Tr_3.*

Figure 4.12 shows the dependence of the noise as a function of the feedback resistance for different ASICs, each of them connected to the p and n-side. Higher register values correspond to higher feedback resistance. For n-side, the noise levels are slightly larger at lower feedback resistance (around 100 electrons) in comparison with larger values. For the p-side, it is visible that around 15 LSB the noise remains stable for the full feedback resistor range. This allows to say that even with an increase of the noise levels of 100 electrons for lower values of the feedback resistor, it is possible to operate the modules without big compromises in terms of noise for an IFED value of 20 LSB.

Another design feature of the STS-XYTER ASIC is the user-controlled selection of the shaping times in the amplitude measuring path [55]. This is an important parameter as it dominates the noise bandwidth, and it must accommodate the ASIC response time and the hit rate. To reduce the dead time and pile-up effects, the detector modules will be operated at the smallest shaping times. The slow shaper $CR-(RC)^2$ design allows to select multiples peaking times modifying the resistance values in the pulse processing chain.

Figure 4.13 illustrates the noise dependence as a function of the shaping time for two different ASICs for p and n-side in module 01Tr_3. The noise levels show the dominance of the voltage noise component at smaller shaping times (90 ns), getting an increase of approximately 100 electrons with respect to the main value. This implies a slightly larger system noise during the first years of the STS detector operation. This situation will be reversed as the parallel current noise will dominate the noise distribution, due to larger sensor leakage current after irradiation (shot noise).

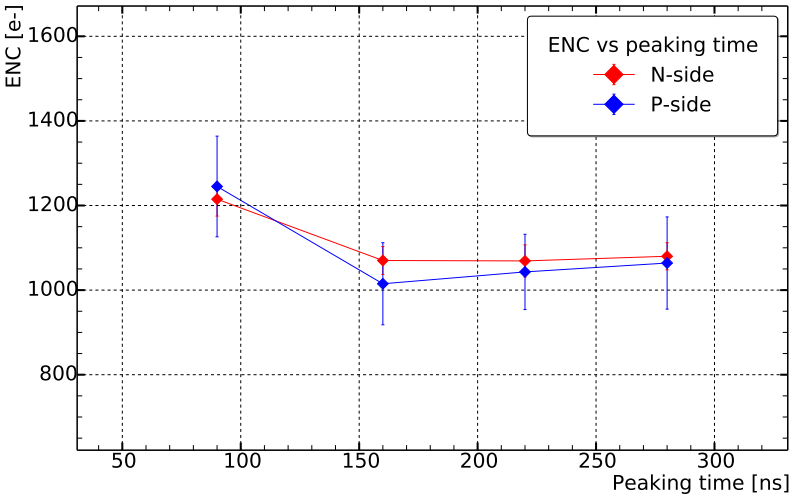


Figure 4.13: *Measured ENC for selected ASICs as a function of the shaping time for module 01Tr_3.*

4.5 Measurement of the response to a gamma source

To evaluate the detector performance in terms of signal readout, charge collection efficiency and signal to noise ratio, the module response was studied using a gamma radioactive source of ^{241}Am with an activity of 37 MBq. The non-collimated source was placed outside of the test box, at a distance of approximately 3 cm, to illuminate the complete sensor area. Figure. 4.14 shows the hit map, at the DIGIs level, for the full illuminated sensor area. The DIGIs are raw signals from the detector, containing information on charge and time (5-bit amplitude and the 14-bit timestamp respectively) together with the address (channel and module) of the read strips. The sensor strip structures (vertical and 7.5 degree) are visible in the hit map. This can be explained based on the fact that the edge channels for the ASICs are masked due to their high noise levels.

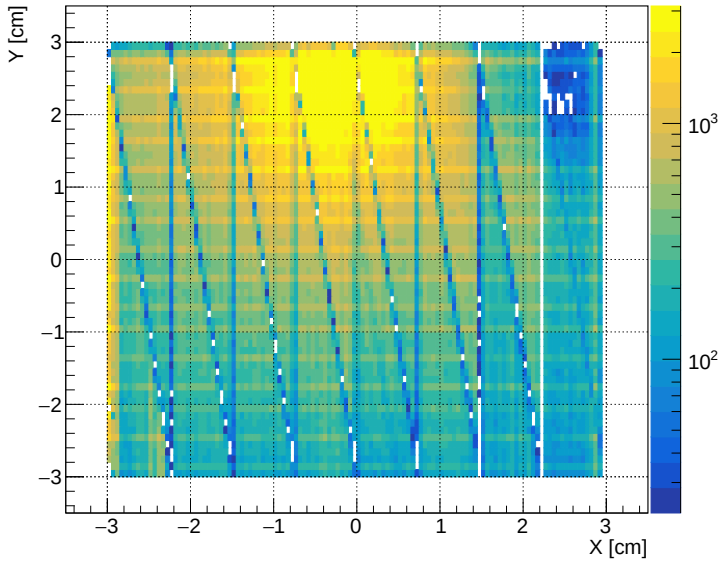
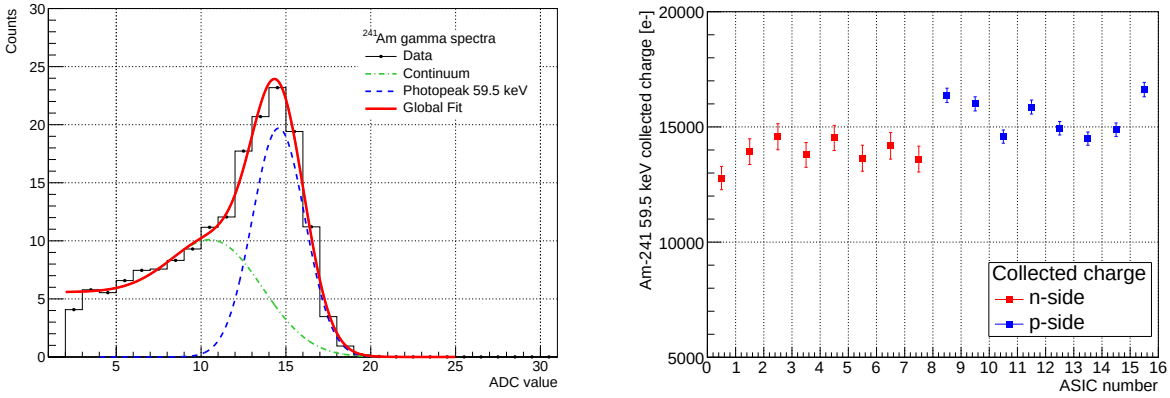


Figure 4.14: *Hit map of the full illuminated 6.2 × 6.2 cm^2 sensor in module 01Tr_3.*

These studies were conducted with the module 03Tl_3, symmetrically biased at 150 V. In order to have a better energy resolution, the readout ASICs were calibrated in a reduced ADC range of approximately 3.4 fC, with ADC gain of 0.113 ± 0.006 fC/LSB and 0.103 ± 0.002 fC/LSB for n- and p-side, respectively. The fine calibration of the ADC allows to reconstruct the source spectrum, and identify the gamma photopeak of 59.5 keV. Figure 4.15(b) shows the collected charge across all ASICs at a threshold of approximately 6400 e-. The error bars correspond to the standard deviation. There is a bigger dispersion among ASICs in the p-side compared to the n-side. This effect is not well understood and is still under investigations. The deposited energy spectrum measured on the p-side at a threshold of approximately 6450 e- is shown in Fig. 4.15(a). The low energy peaks of ^{241}Am, such as 13.6 keV and 26.3 keV, were not observed because of the high threshold value. To extract the peak centroid, the data was fitted with a Gaussian function around the expected position of the photopeak, and a convoluted *Erfc* and Gaussian functions were used to reproduce the continuum.



(a) (b)

Figure 4.15: *^{241}Am spectrum measured with module 03Tl_3 at an effective threshold of approximately 6450 e^- (a). Charge distribution across all ASICs (b).*

The peak position yields an average ADC value of 14.5 LSB. According to the ADC transfer function, the deposited charge can be calculated as 14574 and 15385 e- for the n and p-side, respectively. Using the corresponding noise measurements, see Table 4.2, whose average values are 1112 and 991 e-, excluding the Z-strips, an average signal-to-noise ratio of 13.1 and 15.5 can be calculated for the n and p-side, respectively.

To have an estimate of the module charge collection efficiency, the measured charge was compared to the expected charge deposited by a photon of 59.5 keV in silicon material. However, the collected charge in the sensor and the one amplified in the front-end are slightly different, due to the fact that the input capacitance of the electronics is not infinitely large compared to the detector one. To determine what fraction of the collected charge is really sampled by the ASIC, it is necessary to consider, in a first approximation, the total capacitance in the signal path. The latter can be estimated by knowing the sensor's and microcables capacitance, i.e., $C_{det} = C_{sensor} + C_{mic} = 22.2$ pF for the module investigated [87, 88].

If we assume that all the charge is collected on the sensor, which is fully depleted and not irradiated, the expected charge is approximately 16400 e-. This value must be corrected by the factor $1/(1 + C_{detect}/C_{CSA})$, where C_{CSA} represents the dynamic input capacitance of the charge sensitive amplifier (CSA). The latter can be estimated based on the open-loop gain relationship

$C_{CSA} = AC_{fbck}$, where $A = 4.8$ kV/V is the amplifier gain and $C_{fbck} = 100$ fF is the CSA feedback capacitance [89]. These corrections yield a value that corresponds to an expected collected charge of 15680 e-. Therefore, the measured charge collection efficiency can be estimated to be approximately 96%, slightly below the expected value.

4.5.1 Response function of the ADC threshold

The channels' flash ADC uses two main reference potentials, which determine its dynamic range. In addition, the effective threshold is established through a third potential, hereafter called *VRef_T* (see section: Linearity of the *VRef_T* transfer function). This is implemented in the ASIC as a 6-bit register controlling a digital to analog (DAC) that allows to adjust the position of the signal baseline relative to the ADC discriminator levels, i.e., setting the effective threshold without the need to modify the ADC transfer function or the trim calibration values. The functionality of the *VRef_T* provides a convenient degree of freedom that can be exploited during calibration or in case of noise saturation. Therefore, for a correct operation of the ASIC in the detector readout, a proper understanding of the transfer function of the DAC is essential. Although the *VRef_T* is designed to operate in four possible ranges, this work targets the largest range, which is typically used in the module operation. To assess the DAC response and to evaluate its linearity, the 59.5 keV reference signal from the ^{241}Am gamma source was measured at different *VRef_T* values, as described in the previous section. Using the module 03Tl_3 calibrated in the same high resolution range as

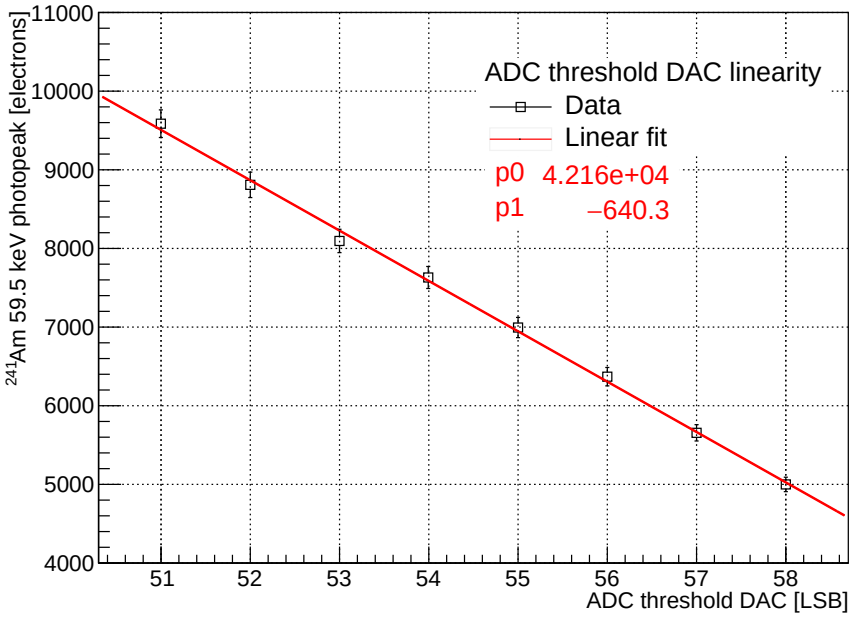


Figure 4.16: *Linearity check of the threshold DAC using the 59.5 keV gamma line of a reference ^{241}Am source. The data correspond to ASIC 6 of p-side. Fitting parameters are also shown in the plot, being p1 the slope of the curve and also representing 1 LSB equivalence.*

mentioned before, the response function of the register controlling the effective ADC threshold was also verified. Figure 4.16 illustrates the linearity of the DAC, where every point corresponds to the centroid of the 59.5 keV photopeak in units of charge. Since the ADC measures the signal above threshold, the peak position moves to larger values with decreasing threshold. The slope of the linear regression allows to estimate the equivalence of 1 LSB, resulting in approximately 740 ± 77 e-

and 640 ± 56 e- for the n- and p-side, respectively. These parameters are in the acceptance range compared to the previously calculated values for the largest range of the threshold DAC (see section: Linearity of the *VRef_T* transfer function).

4.6 High voltage scan and stability tests

Figure 4.17 shows the results of a bias scan for a group of selected ASICs attached to the n- and p-side of the sensor, along with the sensor current-voltage dependence. Each point illustrates the average noise in the ASIC, and the error bars represent the standard deviation across the channels. While the noise remains approximately constant for the p-side, the effect of the bias voltage is clearly visible for the n-side at voltages lower than 60 V. This behavior can be explained as follows: when increasing the reverse bias of the sensor, the depletion zone expands from the p-side towards the n-side. At 40 V, the region surrounding the p-side implants is already depleted, therefore, the ENC values remain constant around the value of 1000 e-. The n-side curves show how the depletion volume gradually extends between the n-side strips to insulate them. The sensor full depletion is then reached at 60 V, in agreement with the measured current values for the sensor.

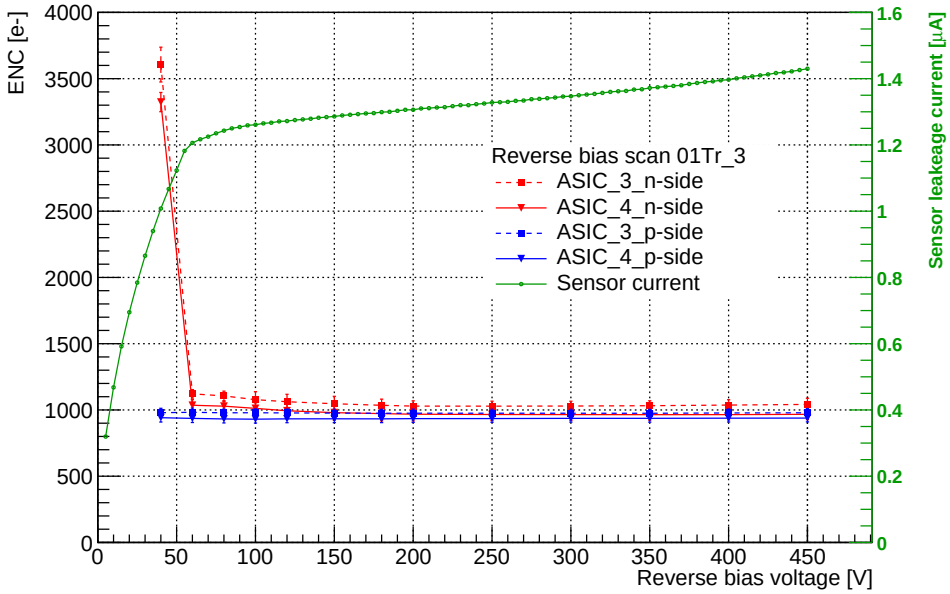


Figure 4.17: *Measured ENC for selected ASICs as a function of the sensor reverse bias voltage of module 01Tr_3. The ENC values for the n-side ASICs reached saturation from 60 V, signaling the sensor full depletion. This result is in agreement with the depletion voltage measured via the sensor current-voltage characteristics, and here depicted for reference.*

CBM is going to be a long-standing experiment, therefore, a reliable performance is considered a very important parameter. The noise evaluation over time for a full assembly module can contribute to identify malfunctions or operation problems that might not be easy to observe during short testing periods. These variations can be a consequence of electromagnetic interference, uneatable biasing, faulty ground connections or unstable temperatures.

The module 03Tl_2 was selected to study the stability of the detector. During a period longer than 72 hours, the noise of the module was continuously monitored. The measurements were taken for three ASICs in both polarities. Each noise scan takes approximately 5 minutes per ASIC. The

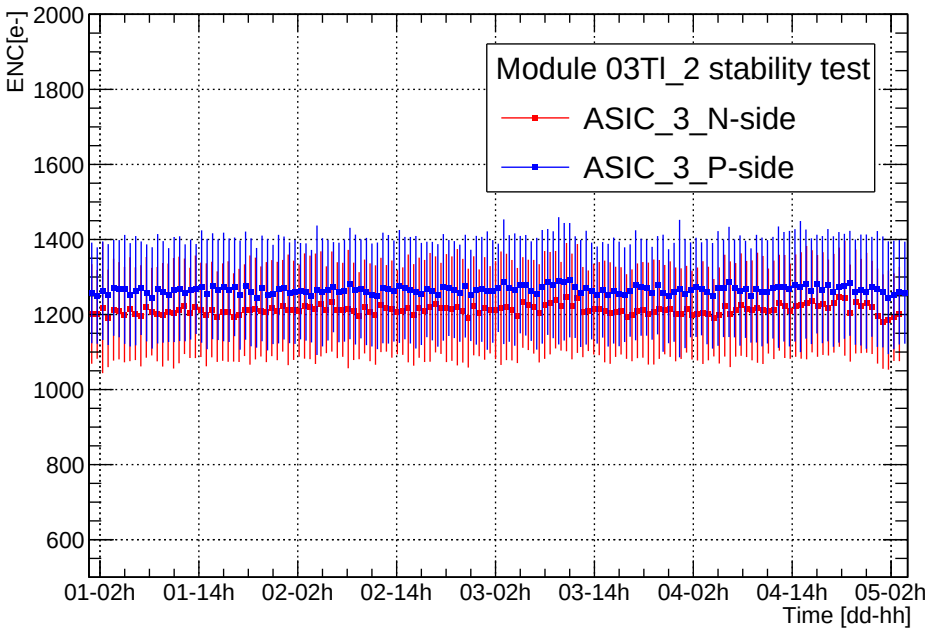


Figure 4.18: *Noise stability test for module 03TI_2 for a period longer than 72 hours. The noise of the module was continuously monitored.*

ASICs temperature were registered after each measurement, using a dedicated ADC implemented for monitoring temperature and potentials in the chip, to be able to detect noise fluctuations due to this factor. The temperature variations were not significant, with deviations with respect to the main value below 1%. Figure 4.18 illustrates the noise dependence with the time for two ASICs corresponding to p- and n-side respectively. Every point represents the average noise value among all channels in the chip and the error bars indicate the spread. The variation along the monitoring period was below 10%, which is considered a good result.

4.7 Statistics on module tests

Another important parameter for good module performance is the overall channel yield. During the module assembly, there are multiple steps where it is possible to damage the bonding connections between the sensor and microcables and/or between the microcables and the ASICs. In addition, it is also possible to compromise the operation of the chip itself by electrostatic discharges (ESD) or physical damage. When the bonds are broken, either at the ASIC or sensor side, noise levels appear relatively low compared to well connected channels, see Fig. 4.7. In case of a permanent damage to the analog front-end channel, no signal is amplified or further digitized. Therefore, the identification of a broken channel becomes relatively easy by comparing its noise level to the average amount the connected channels. Even if the quality of the bonding and the basic ASIC functionalities have been monitored during the assembly, inappropriate handling, thermal or electrical shocks could damage the module. Therefore, these investigations are necessary to consider when building an acceptance criteria for the modules.

In Fig. 4.7, a group of channels with lower noise levels have been identified and labeled as broken. Their absolute noise can be related to the position where the bond or the entire channel was damaged. Following this reasoning, it is possible to classify them as follow:

- No analog response: broken channel with ENC = 0. The channel AFE was permanently damaged, no hits are amplified (NoAnalogResponse).
- Broken bond at the ASIC. Faulty connection between ASIC and microcable. Only the intrinsic ASIC noise is visible (@ASIC).
- Broken bond at the sensor. Faulty connection between the microcable and the sensor or across the signal line in the microcable. The expected noise is larger than the intrinsic noise of the ASIC and below the module average (@Mic+sensor).

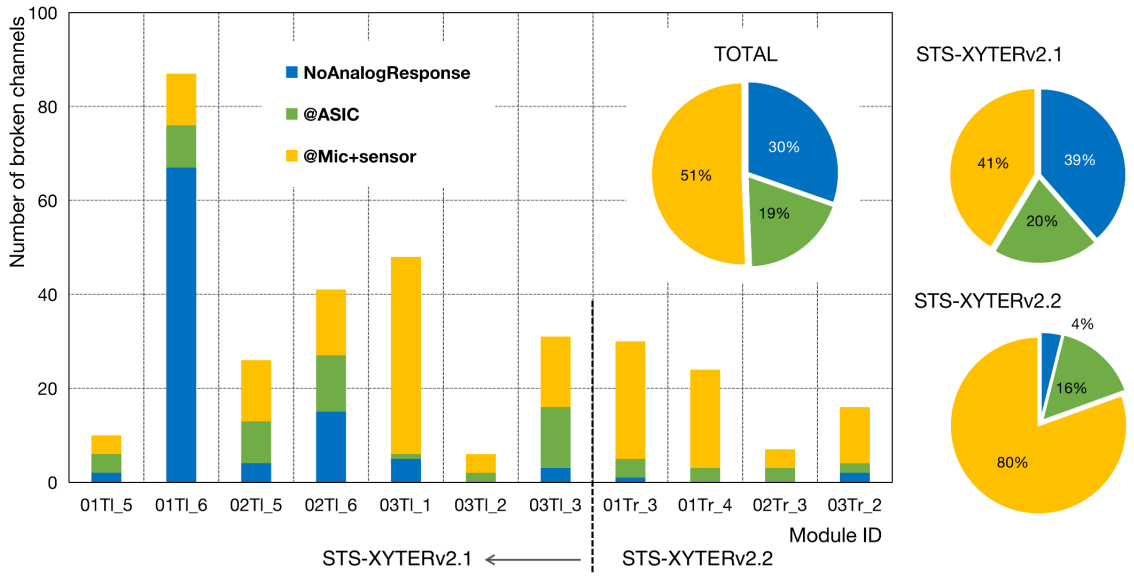


Figure 4.19: *Distribution of broken channels in STS modules. Statistics on the different problems are also illustrated for the two versions of the front-end electronics in use. The implementation of an ESD protection structure in the STS-XYTER v2.2 ASIC contributes to supress the damage of electrostatic discharges.*

Figure 4.19 illustrates the distribution of broken channels for 11 assembled modules. They are classified according to their absolute noise level, and hence, the place where the channel was identified as broken. The statistics correspond to modules built with different versions of the ASIC. During the assembly procedure, multiple measures were implemented to avoid damaging the devices by electrostatic discharges. This problem was identified as the main cause for having channels with no analog response. Its effect is clearly visible in the overall statistics, and more significant in the modules produced with the v2.1 of the ASIC. In this case, channels with no analog response represent 39% of the total number of broken channels. A marked reduction of this problem is observed for the modules produced with the ASIC v2.2, where the contribution has been reduced to 4%. This was expected since, in the last version of the chip, an ESD protection circuit at the input of the channels' AFE has been implemented (see section: Overview of the changes implemented in the STS-XYTER v2.1).

For the broken channels statistics, not only the absolute amount is important, but also their spatial distribution in the modules. Consecutive broken channels can affect significantly the track

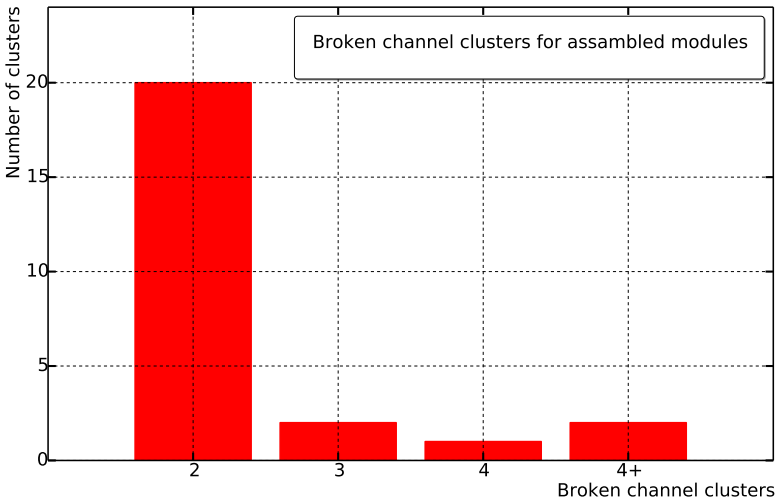


Figure 4.20: *Broken channels cluster distribution for assembled modules.*

efficiency and the detector resolution. Figure 4.20 shows the cluster size distribution for broken channels. The clusters are based on the readout position in the sensor. The higher amount of broken channels is for clusters fo size 2, representing approximately 12% of the total number of broken channels. Higher cluster sizes represent a more dangerous situation for the modules performance, but the amount found is very small.

When comparing the results of the modules produced with the STS-XYTER v2.2 and the requirements for the sensor production (below 1.5% of defective channels) [83], it can be understood that the module assembly is a reliable procedure which do not compromise the overall channel's yield. This benefit can be exploited during the assembly, and it allows to tentatively establish the production goal, in terms of broken channels, in approximately 1.5% or 30 defective channels per module.

Table 4.2 summarizes some of the most important electrical parameters of each tested modules. The results are grouped according to the sensor and microcables dimensions. In general, they correspond to some of the largest objects to be assembled for the future STS detector [90]. The reported values are extracted from a series of checks performed on each module, as shown across this work. For each polarity, a unique parameter value is given. They correspond to the average across all channels, while errors represent their standard deviation.

4.8 Summary

The systematic testing of fully assembled STS modules allowed to verify the performance of the latest version of the front-end ASIC functionalities and the electrical properties of the modules. Several parameters such as ASIC communication and control functionalities as well as the integrity of the signal path have been continuously monitored across all checks. The noise measurements demonstrated that an overall level of approximately 1000 e- ENC is an achievable goal for most of the largest produced modules. The scans of the CSA bias current have exposed a large and stable plateau, in which the modules can be operated without deteriorating the system noise. The selection of the feedback resistance and the shaping time is subjected to several requirements, such as the dead time of the ASIC, pile-up effects, and absolute noise levels. The results of the charge

calibration have shown a good and homogeneous response for all produced modules, with spread around the target values below 10%. These results are independent of the overall dimensions of the modules or the version of the front-end electronics in use. On a selected module, signal readout, charge collection efficiency and signal to noise ratio were studied. This allowed to verify the calibration procedure and to assess the transfer function of the ADC threshold registers in the chip. In addition, these studies brought important insights regarding the fraction of broken and non-operational channels in the modules, and consequently assembly yield. The implementation of an ESD protection circuit in the latest version of the ASIC has improved the assembly yield, making possible to reach the production aim of approximately 1.5% defective channels per module. The iterative testing of STS modules is, in general, an essential step for developing a reliable quality control procedure and establishing classification criteria towards series production.

Table 4.2: *Test results for STS fully assembled modules.*

Module ID	Features†		ENC [e-]	ADC gain [fC/LSB]	Threshold spread [e-]	Broken channels
01Tl_5	S6M49	n	1276 ± 160	0.349 ± 0.005	231	4
		p	1278 ± 83	0.357 ± 0.004	243	6
01Tl_6		n	1190 ± 138	0.368 ± 0.019	344	53
		p	1115 ± 120	0.311 ± 0.005	337	34
01Tr_3		n	1021 ± 73	0.336 ± 0.002	281	6
		p	1052 ± 100	0.335 ± 0.002	261	24
01Tr_4		n	1095 ± 79	0.336 ± 0.002	369	8
		p	1048 ± 93	0.334 ± 0.002	346	16
02Tl_5	S6M45	n	1165 ± 139	0.330 ± 0.019	440	11
		p	1100 ± 84	0.310 ± 0.005	324	15
02Tl_6		n	960 ± 77	0.338 ± 0.002	200	13
		p	958 ± 75	0.338 ± 0.003	255	28
02Tr_3		n	1034 ± 75	0.336 ± 0.005	348	2
		p	1028 ± 72	0.335 ± 0.004	263	5
03Tl_2	S6M42	n	1117 ± 90	0.346 ± 0.005	226	4
		p	1142 ± 67	0.356 ± 0.003	252	2
03Tl_3		n	1112 ± 98	0.340 ± 0.009	245	11
		p	991 ± 86	0.337 ± 0.007	251	20
03Tl_1	S12M42	n	1586 ± 135	0.346 ± 0.005	271	23
		p	1631 ± 88	0.357 ± 0.003	330	25
03Tr_2		n	1431 ± 136	0.337 ± 0.007	360	5
		p	1440 ± 167	0.335 ± 0.003	260	11

†*Sensor size SX (cm) and microcable length MXX (cm).*

Chapter 5

Assembly, test, operation and performance of the mSTS

The operation of fully assembled modules in a realistic scenario is a very important step towards the production of the STS detector. Following this idea, a small-scale prototype of the full detector, named mini-STS (mSTS), has been built as part of the CBM Phase 0 activities. The setup has been operated in various beam conditions, at the Heavy Ion Synchrotron SIS18 in GSI, Darmstadt. This chapter describes the recent activities of the mSTS project, the construction of the current setup, the installation in the beam line, the operation during July 2021 campaign with O + Ni at 2 AGeV and some experimental results.

5.1 The mCBM experiment

As part of FAIR phase 0 activities, a test setup named mini-CBM (mCBM) has been constructed at the GSI facility [91]. The setup aims at commission, optimization and preparation for the series production of the CBM detectors, together with proving the concept of free streaming data generation under realistic experimental conditions.

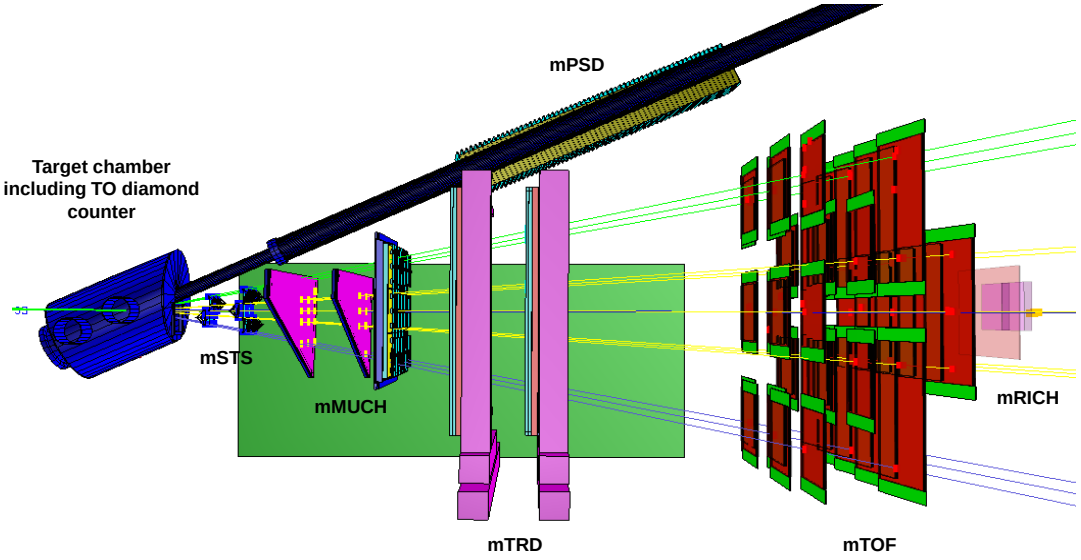


Figure 5.1: *Schematic of the mCBM setup for July 2021 beam campaign.*

The mCBM project has been running since 2018 using heavy ion beams of a wide range of species from SIS18 at energies between 1 and 2 AGeV and intensities up to 10^9 ions/s. The setup has dimensions of approximately 3 m in length and it is set under a polar angle of about 25° with respect to the primary beam axis. Figure 5.1 shows a geometrical scheme of the mCBM experiment for July 2021. The setup comprises of final prototypes and pre-series components of all CBM detector subsystems and their readout chains. There is no magnetic field in the mCBM system, therefore, it is possible to measure only charged particles produced in nucleus-nucleus collisions traversing the detector stations under straight trajectories. It includes detector modules from STS, RICH, MUCH, TRD, TOF, PSD and has been successfully installed in the detector test area HTD, situated at the beam entrance of the experimental area Cave-C (HTC) [92]. The primary aim of mCBM is to commission and optimize:

- the operation of the detector prototypes in a high-rate nucleus-nucleus collision environment;
- the detector control system;
- the free-streaming readout chain including the data transport to a high-performance computer farm inside the Green IT Cube at GSI;
- the online track and event reconstruction as well as event selection algorithms;
- the offline data analysis;

The experience gained during mCBM campaign will significantly shorten the commissioning period of the CBM experiment at SIS100. The results obtained from the commissioning phase show the key role of mCBM as a powerful tool towards the realization of the CBM experiment.

5.1.1 mSTS as part of mCBM

The mSTS detector consists of two tracking stations, built from prototype elements of the final STS detector. Some simplifications have been made, with respect to the final STS system, in order to focus on a few essential components and system design aspects [93]. The mSTS setup comprises a total of 11 detector modules, arranged in four units. Every detector module consists of a double-sided silicon microstrip sensor, segmented into 1024 strips per side and connected to a custom designed FEB-8 via a stack of Al-polyimide readout cables (see section: The STS detector module).

The modules are glued onto carbon fiber support structures named ladders, where every ladder is mounted into an aluminum C-frame. Figure 5.2 shows the mSTS design concept with the C-frame and electronic cooling services. The stations are housed in a box that provides shielding against light and electromagnetic radiation. The box has a low-mass entrance window directly in front of the sensors. Inside the box, the sensors are operated at room temperature [93].

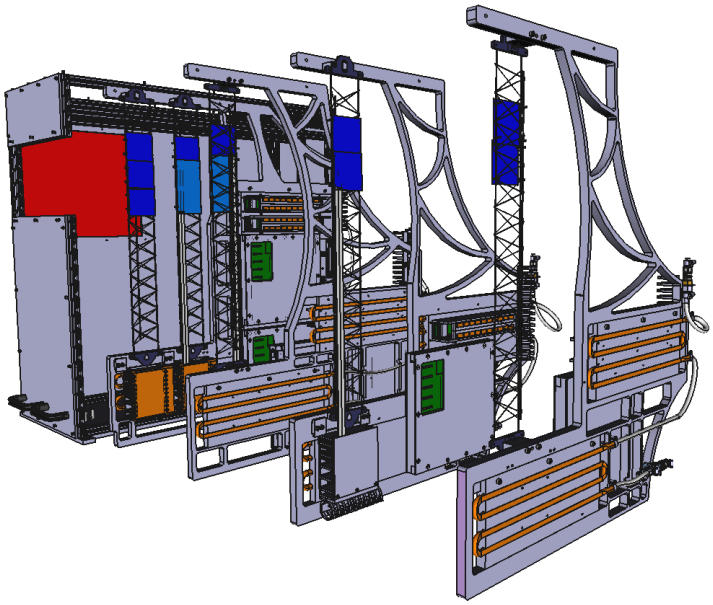


Figure 5.2: *mSTS design concept in the C-frame.*

5.2 Assembling and installation

The mSTS setup covers an area of 12 × 12 cm^2 and 18 × 18 cm^2 respectively, arranged in 4 units consisting in a total of 11 modules: 2 with 6.2 × 12.4 cm^2 and 9 with 6.2 × 6.2 cm^2 double-sided silicon sensors. The 11 microstrip sensors represent a total of 11 × 2048 readout strips and thus more than 22 000 readout channels grouped in 176 STS-XYTER ASICs bonded onto 22 FEB-8, plus two service FEBs for pulser signal injection, 5 CROBs for readout, and 5 POBs providing LV for FEBs [92, 93]. From the four operational units:

- Unit 0 and Unit 2 are produced with the last version of the components (STS-XYTER v2.2 and LDOs);
- Unit 1 and Unit 3 are produced with older version of the components (STS-XYTER v2.1);
- From Unit 0 to Unit 2, out of 96 ASICs, 2 are non operational;
- From Unit 3, out of 80 ASICs, 17 are non operational;

The tested STS modules were mounted onto a carbon fiber structure (CF-ladder) using different tools and jigs produced on standard milling machines. Afterwards, the ladder and other components like the POBs and C-ROB were mounted into a C-frame [94, 95]. The full system was integrated in a light-tight aluminum box that provides shielding against electromagnetic interference, power connections, cooling pipes and interfaces for data. Figure 5.3 shows the mSTS setup with all ladders inside the box with services and cooling (left side) and the setup in the beam line inside the cave (right side).

The integration of the units include mounting of the readout boards (C-ROBs) in shielded enclosures, high and low voltage cabling for the front-end electronics, installation of the circuit to provide a signal return path for every detector module and routing of the data cables between the front-end boards and the C-ROBs. The front-end boards are attached to water cooling plates to dissipate the heat. The low voltage lines were made using flat cables with 0.3 mm^2 cross section

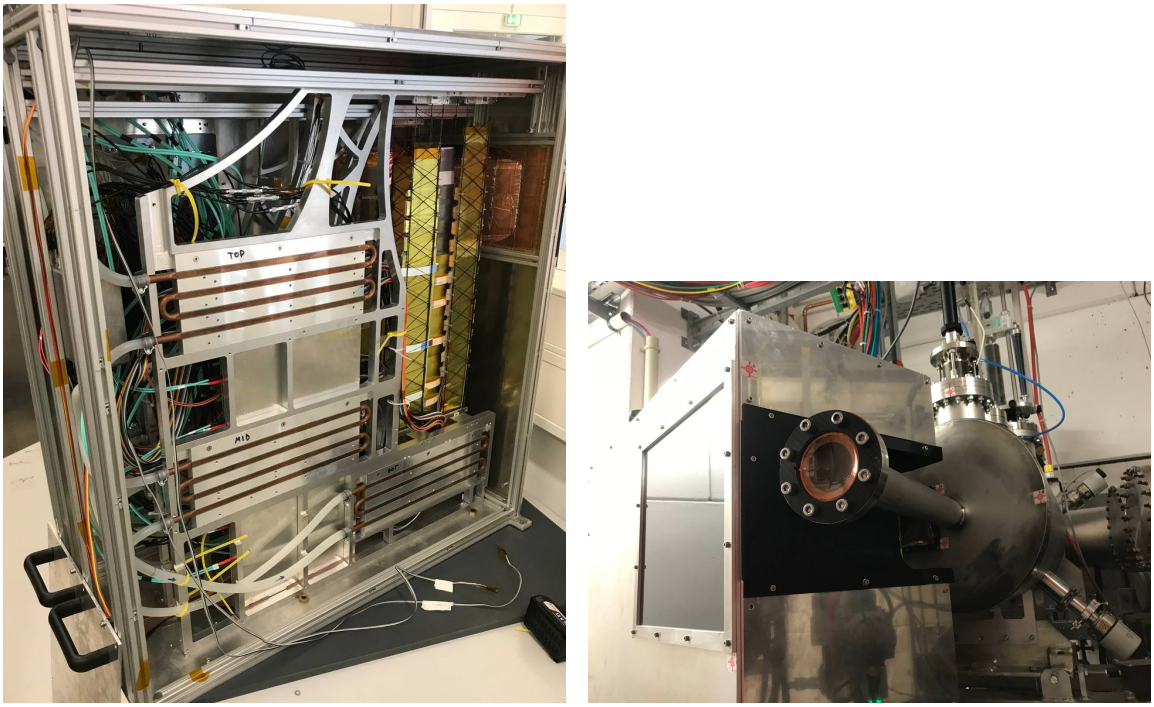


Figure 5.3: *mSTS detector with the 2 stations (left side). The setup is placed in the beam line inside the cave (right side).*

of individual strands. High voltage has been provided over shielded coaxial cables, whereas cable shields have been connected to the enclosure (detector ground). In order to provide the return path for the signal, FEB ground points on the p- and n-sides have been connected with two capacitors in series and with their center tap connected to the detector ground. To protect the sensitive analog lines from transients in the digital electronics, the data cables have been routed far away from the LV/HV lines and shielded. Their shields have been referenced to the ground of the C-ROBs [96]. The full system was installed in the mCBM experiment cave in June 2021 for commissioning and operation.

5.3 Commissioning and operation

In order to operate the setup, one of the first steps is the loading of the configuration parameters for each ASIC. Beyond the typical settings that include the global registers, each ASIC is configured with the unique calibration parameters [97]. These parameters were determined during the module testing (see section: Calibration procedures for modules testing). Table 5.1 shows the results of the calibration for each module used in mSTS, together with their respective ENC values, measured in the laboratory before installation.

For the data readout, the mCBM detector front-ends are synchronized by the Timing and Synchronization (TS) system, which relies on a clock and pulse-per-second (PPS) distribution. The detector front-end digitizes signals above threshold and assigns a timestamp to the hit. The data are then forwarded via an electrical connection to the GBTX readout board, where the signals acquired through a large number of e-links are converted and merged into an optical GBT link operating at 4.48 Gbit/s. These GBT links are the detector interface to the Data Acquisition

Table 5.1: Results of the calibration settings for the modules used in the mSTS setup.

mSTS	Module ID	Polarity	ENC [e-]	Error	ADC Gain [fC/LSB]	Error	Thr [e-]	Error
UNIT 0	01Tr_3	n	1021	73	0.336	0.002	10830	273
		p	1052	100	0.335	0.002	11115	252
	02Tr_3	n	1034	75	0.336	0.005	10932	347
		p	1028	72	0.335	0.004	10230	238
UNIT 1	01Tl_4	n	1506	196	0.406	0.012	12720	220
		p	1278	98	0.358	0.003	12420	292
	02Tl_3	n	1609	191	0.336	0.007	12455	440
		p	1431	208	0.335	0.004	11832	263
UNIT 2	01Tr_4	n	1095	79	0.336	0.002	10578	347
		p	1048	93	0.334	0.002	11216	470
	03Tr_2	n	1431	136	0.337	0.007	11436	369
		p	1440	167	0.335	0.003	11320	262
UNIT 3	01Tl_6	n	1190	138	0.368	0.019	11367	294
		p	1115	120	0.311	0.005	12145	342
	02Tl_5	n	1165	139	0.330	0.019	11335	417
		p	1110	84	0.310	0.005	12048	337
	03Tl_3	n	1112	98	0.340	0.009	11019	225
		p	991	86	0.337	0.007	11938	266
	COSY	n	977	76	0.323	0.004	10545	268
		p	1050	45	0.404	0.004	10086	245
	03Tl_1	n	1586	135	0.346	0.005	12646	275
		p	1631	88	0.357	0.003	12216	326

(DAQ) chain. The detector subsystems are presently read out using readout chains based on the CRI board as backend [98].

The ground and powering scheme used in the mSTS setup is shown in Figure. 5.4. The scheme follows the same logic than the one used in the module testing setup. The only difference is the addition of pulser FEBs in the mSTS setup (for more details see section: Experimental setup).

During the few hours of main data taking, the first tracking station was fully operational, except for a few channels and 2 ASICs. It was operated with different thresholds in order to allow systematic performance studies. In the second station, parts of the last unit could not be brought into stable operating conditions, therefore, the Unit 3 was not operated during the data tacking.

Periodic structures were observed in the time distribution of all modules. Figure 5.5 shows the time difference with respect to the previous DIGI in the same channel. A narrow peak, with the width of a single 3.125 ns bin, can be observed at exactly 0 indicating the presence, in the data stream, of multiple copies of the same hit with the same time in the same channel (replica hits). This peak is also visible every 51.2 μs, which is the turnover point of the 14-bit ASIC time stamp. This effect was studied in the laboratory varying the amplitude and frequency of a mixture of fixed signal pulses with an induced noise contribution [99].

The replica hits are generated due to significant noise in the MHz range, which keeps the fast discriminator below its trigger threshold even in case of a signal, while the slow shaper still generates a hit with a non-updated timestamp value identical to a previous hit in the same channel. The replica hits can be produced not only at low signal amplitudes, which can be attributed to wrong settings in the fast discriminator, but also at high signal amplitudes. Even when this effect increases with the noise amplitude, its strongest contribution comes from the noise frequency, being

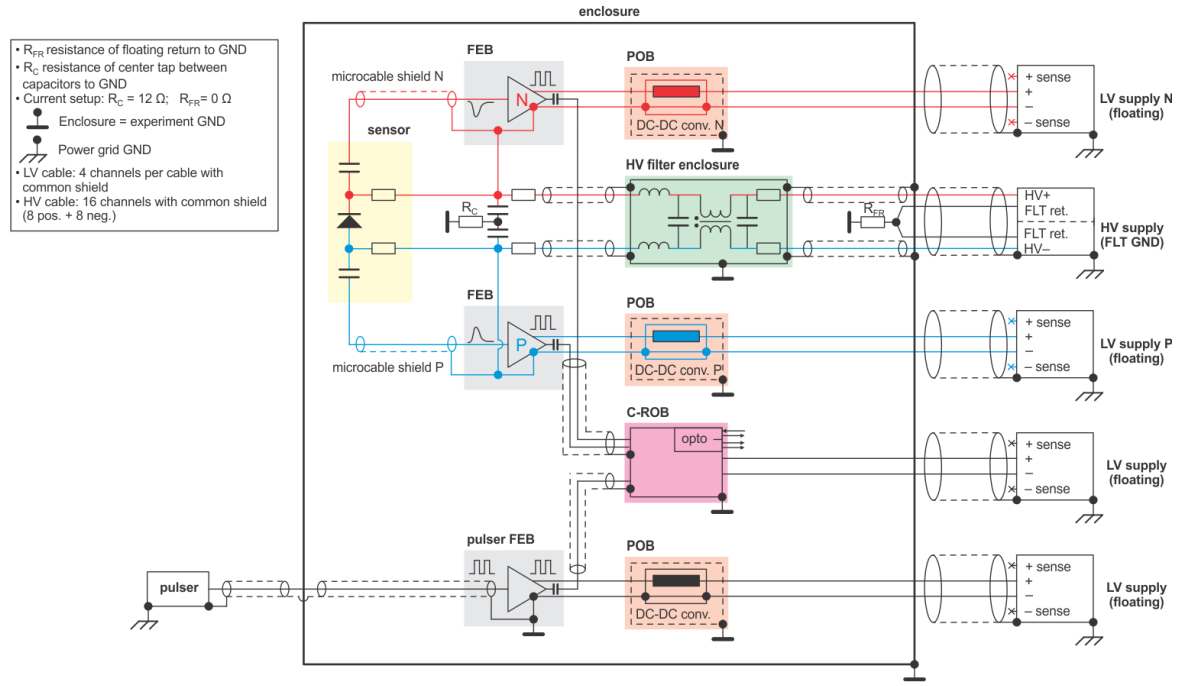


Figure 5.4: Ground and powering scheme used in the mSTS setup on July 2021.

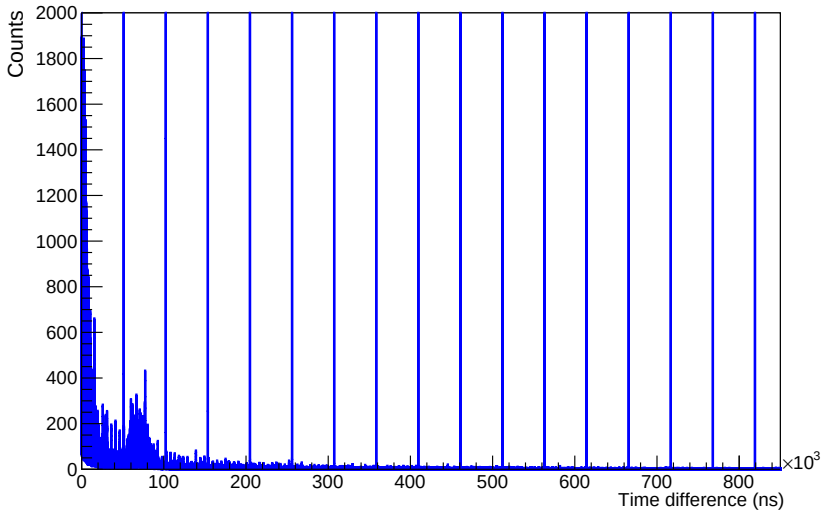


Figure 5.5: Replica hits observed in mSTS. They appear as spikes due to an artifact in the online time sorting of these hits.

especially present in the range of 1 to 6 MHz approximately. This behavior is well understood and consistent with the ASIC design where the bandwidth difference between the slow and fast shaper is located in this frequency range. The replica effect can be significantly reduced by setting the fast discriminator threshold as low as possible without affecting the time resolution of the system. Although, reducing to the largest possible extent the pick up from external noise sources in the relevant frequency range will also help to reduce the replica effect [99].

5.4 Data analysis

The data collected during the beam time campaign of July 2021 are very important since for the first time a setup with two stations and multiple modules, with close-to-final components, has been operated in the beam line. This section summarizes some of the main findings and preliminary results from the analyzed data.

5.4.1 Reconstruction chain

In order to understand the following sections, it is important to introduce some specific nomenclatures and concepts used in the data analysis and reconstruction chain. Figure 5.6 shows a basic block diagram of the individual data containers and the reconstruction chain.

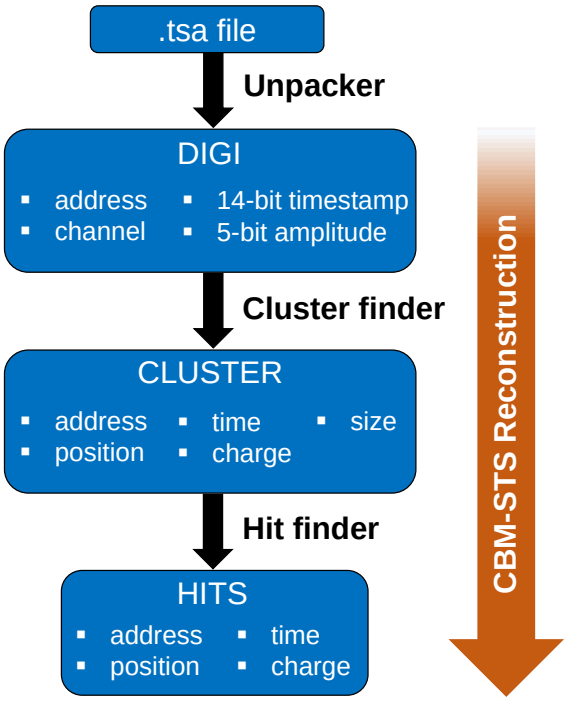


Figure 5.6: CBM-STS reconstruction chain concept.

The raw data from the detector are stored in a set of time slices written into a Time Slice Archive (TSA-file). These time slices contain the full data recorded by the DAQ in a defined time frame (5.12 μs in this case). The TSA-files are first unpacked and written in a CbmRoot tree, which contains the so-called DIGIs. If a signal crosses the lowest discriminator threshold of the slow shaper path, it will be digitized and stored in the DIGIs. Next, the CBM cluster finder algorithm combines DIGIs in neighboring fired strips in a given time window into a cluster. After that, hits are derived from the clusters correlation for the p- and n-side. The events are then defined using a seed detector (ToF in this case) and including all DIGIs within a symmetric time window: $(-50, +50)$ ns. Additionally, a software trigger might be applied, in this case, three ToF DIGIs was set in order to accept the events [100].

5.4.2 Beam characterization

In the mCBM 2021 beam time campaign at SIS18 (GSI), O + Ni collisions at 1.96 AGeV were measured under fixed and stable conditions for around 2.37 hours. The total amount of collected data was approximately 5 TB. The achieved mSTS data rates were up to 280 MB/s, which correspond to an average of 125 kHits/ASIC/s with a beam intensity up to 10^9 ions per spill and approximately 500 kHz interaction rate. The extraction time was approximately 10 s with an effective spill length of 7.5 - 8.0 s. Figure 5.7 shows the spill structure of the ion beam where the DIGIs rate is plotted as a function of the number of time slices. The modules operational threshold was set to 2500 e- for Unit 0, and 12000 e- approximately for Units 1 and 2. The modules with higher noise were set at higher thresholds in order to get a reasonable data rate. The ToF was also included in the plot as reference.

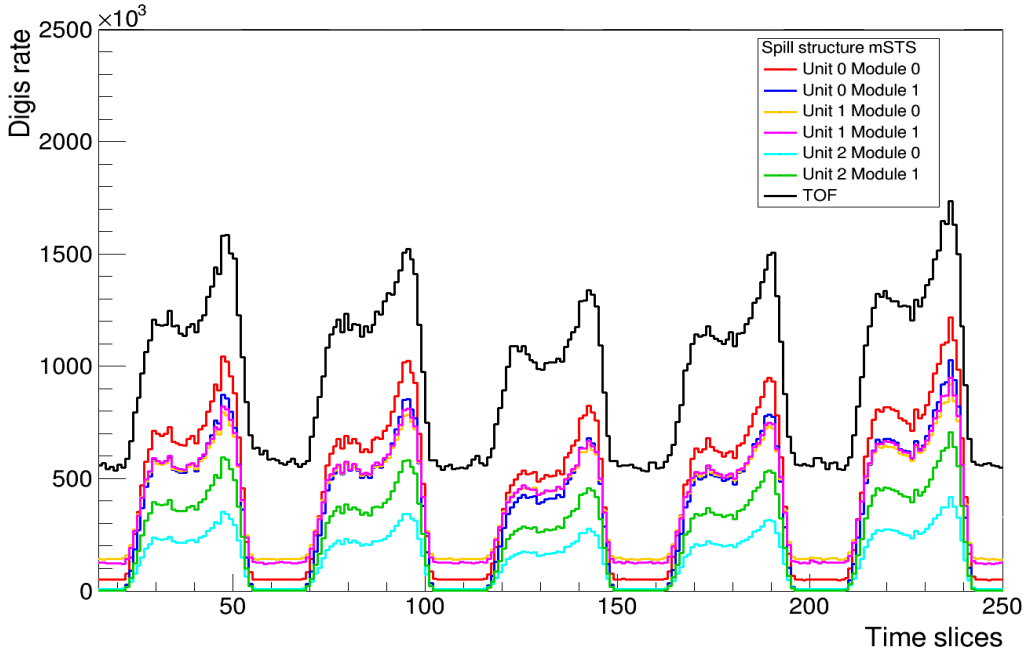


Figure 5.7: Detector rate as a function of time slices, for all STS modules, and the ToF detector as reference.

5.4.3 Time resolution

Precise timing information of the hits is necessary to establish a correct time correlations between the mCBM systems. In order to avoid the hits reconstruction from non-correlated clusters, it is necessary to adjust individually the ASICs offset to ensure a correct synchronization. The hit reconstruction algorithm looks for pairs of clusters, from the front and back side of the sensor, within a specific time window. For a precise time tuning, a detector with a good time resolution should be used as reference. The detector with the highest time resolution available during the July 2021 beam campaign was the mToF, which was used as time reference for the measurements. Time correlations between mSTS and mToF have been built for a time slice, from where the global time offset between the two subsystems was extracted after fitting the correlation peak. The charge dependence of the signal timing, also called time walk effect, it is very important to check, since this effect can be considerably large ($\approx$ 20 ns) for the STS detector. Clusters are formed combining

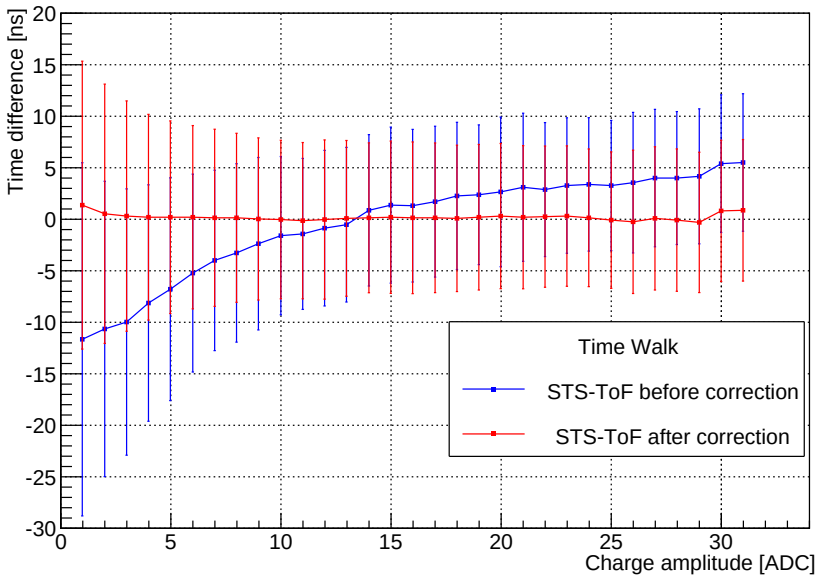


Figure 5.8: Time-walk correction: Time difference between STS and Tof DIGIs as a function of the STS signal amplitude (blue). Time difference after Time-walk correction (red).

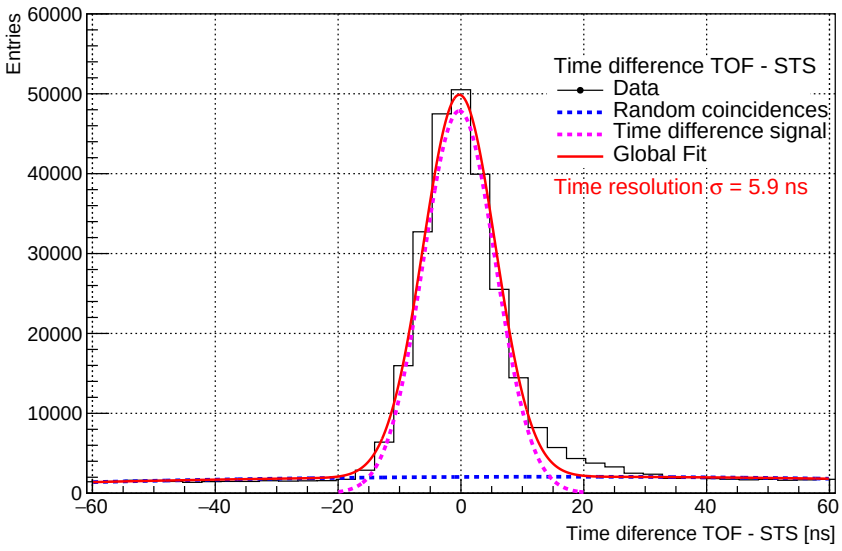


Figure 5.9: Fitted time difference between mSTS and mToF DIGIs.

signals from neighboring fired strips and hits are formed combining correlated clusters in the n- and p- side, both in a narrow time window. Therefore, it is important to synchronize the signals from all detector readout boards [100].

Figure 5.8 shows the mean time difference between mSTS and the ToF detector signals as a function of the signal amplitude before and after time walk correction. The data correspond to an ASIC in module 1 of Unit 0 for the p-side and the error bars indicate the sigma of the distribution. At low amplitudes, the signal is broader and an expected delay of up to 20 ns can be seen before time walk corrections (below 5 ADC units) compared to larger amplitudes. These values are in

agreement with previous estimations of the ASIC time-walk [43]. A charge-dependent time-shift correction is applied at the DIGI level in the time calibration procedure.

After time calibration, the time resolution of the mSTS can be extracted. Figure 5.9 shows the time difference distribution between the STS and ToF DIGIs. For large signal's amplitudes, the measured time resolution (σ) obtained from a Gaussian fit is 5.9 ns, which indicates a good time resolution achieved by the detectors. This value is the combination of the mSTS module's contribution. The right side tail corresponds to the events for which the time-walk correction did not apply correctly, even though they are a very small fraction of the total number of events. Since mToF time resolution is estimated to be around 60 ps, the overall RMS is mostly dominated by the mSTS contribution.
The total time resolution is determined as a contribution of the mSTS and mToF detector systems:

$$\sigma_T^2 = \sigma_{mSTS}^2 + \sigma_{mToF}^2 \tag{5.1}$$

since $\sigma_{mToF} \ll \sigma_{mSTS}$, $\sigma_T \approx \sigma_{mSTS} = 5.9$ ns.
The overall time resolution (σ_T) can also be mathematically expressed as the sum of uncorrelated sources and hence added quadratically:

$$\sigma_T^2 = \underbrace{\left(\frac{TS_{bin}}{\sqrt{12}}\right)^2}_{\text{timestamp}} + \underbrace{\left(\frac{\sigma_n}{\frac{dV}{dt}\,|_{V_{thr}}}\right)^2}_{\text{jitter}} + \underbrace{\left(\frac{V_{thr}}{\frac{dV}{dt}}\right)^2}_{\text{time walk}} \tag{5.2}$$

where σ_n is the noise level, V_{thr} the threshold level of the discriminator and dV/dt the slope of the leading edge at the measured threshold.
After time-walk correction, the time resolution can be expressed as:

$$\sigma_T^2 = \left(\frac{TS_{bin}}{\sqrt{12}}\right)^2 + \left(\frac{\sigma_n}{\frac{dV}{dt}\,|_{V_{thr}}}\right)^2 \tag{5.3}$$

where the noise level of the fast discriminator can be estimated:

$$\sigma_n = \frac{dV}{dt}\,|_{V_{thr}} \times \sqrt{\sigma_T^2 - \left(\frac{TS_{bin}}{\sqrt{12}}\right)^2} \tag{5.4}$$

where: the clock frequency (LSB of the timestamp counter) is $\mathrm{TS}_{bin} = 3.125$ ns and the dV/dt for a threshold of approximately 0.9 fC is 9.0 V/μs [43]. The noise contribution from the fast shaper (σ_n) is approximately 5950 e-. This value corresponds with the expected noise from the fast discriminator, since during operation, the threshold was set to low operational values (see section: Commissioning and operation).

5.4.4 Charge distribution

In a self-triggered system, the digitization threshold plays a very important role. If the threshold is kept too high, the signal remains undetected. However, if the level is too low, noise-related hits would overflow the channels and create dead time. Moreover, in a silicon sensor, a fraction of the collected charge always couples to the neighboring strips. This implies that the full signal amplitude can be only reconstructed if the threshold is sufficiently low [100].

In order to test the STS concept under realistic conditions, mSTS modules were operated at different thresholds based on their respective noise levels. The threshold level was set as low as possible for each individual ASIC, paying attention to not over-saturating the readout bandwidth. The following study will focus mostly on the performance of Unit 0 and Unit 2 since they are built with the last version of the STS detector components.

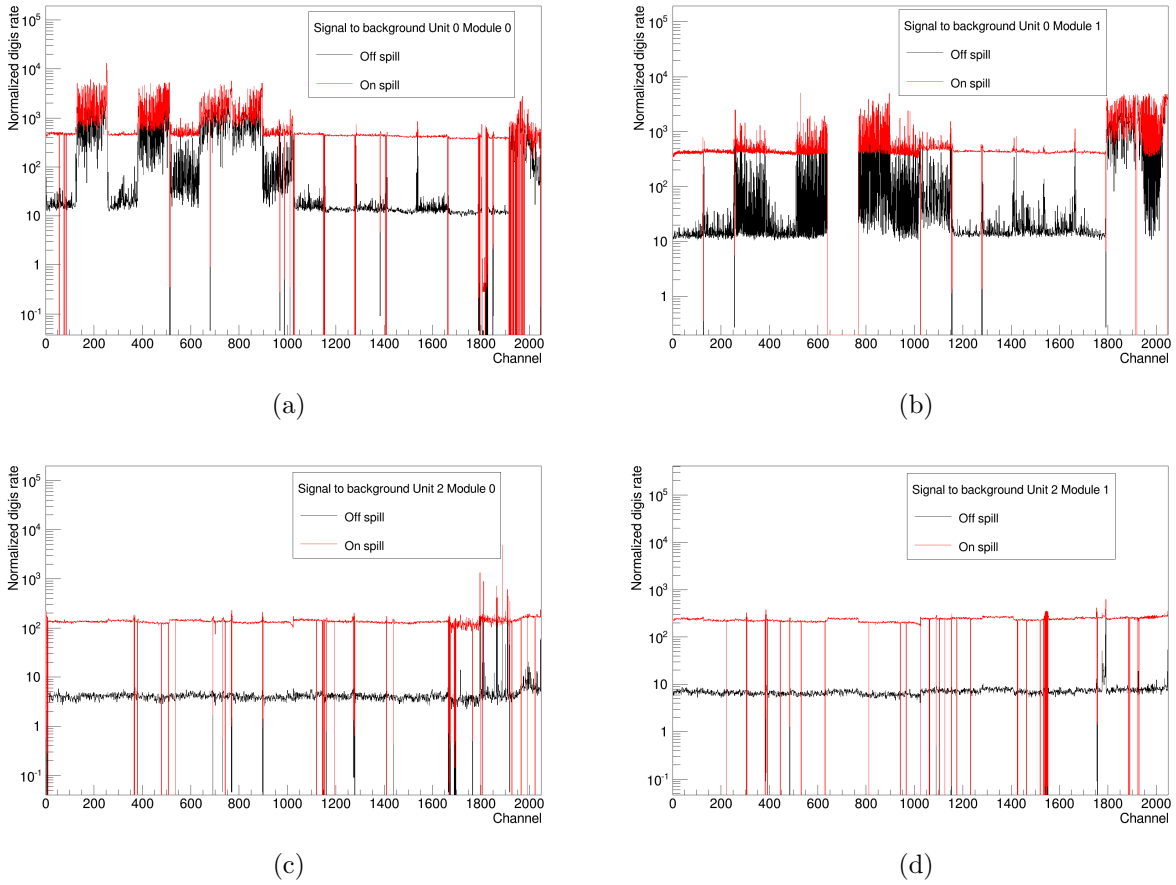


Figure 5.10: *Channel distribution for Unit 0 (a, b) and Unit 2 (c, d), in spill (red) and off spill (black) for the different mSTS modules.*

At the moment of setting the operational threshold levels as low as possible, the noise contribution might increase drastically until the point that it could affect severely the reconstruction. A software cut is necessary at this point in order to deal with this problem. From the spill structure plot (see Fig. 5.7), can be decided if a time slice is in or off spill. Figure 5.10 shows a comparison between the channel distribution in and off spill for different modules of Unit 0 (top) and Unit 2 (bottom). The first 1024 channels of each plot correspond to the n-side while the remaining 1024 correspond to the p-side. The two modules in Unit 0 have a substantial noise increase compared to the ones in Unit 2, making the signal to background significantly smaller in this case. This can be explained from the fact that the data taking threshold was set to approximately 2800 e- for Unit 0, while for Unit 2 it was set to around 12000 e-.

If a cut is applied on the first ADC discriminator (around 2080 e-) the noise in Unit 0 is substantially removed. Figure 5.11 shows the comparison between the channel distribution in and off spill for different modules after the first ADC discriminator cut. A considerable improvement is visible, but it is still questionable if further ADC cuts will further improve the signal to background ratio in the system. In order to verify how the performance can be improved by means of discriminator cuts, the signal to background was studied for different ADC cuts. The noise hits are concentrated at low ADC values, for values ≥ 3 ADC the signal to background remains approximately constant. Therefore, one up to two ADC cuts should be enough to restore considerably the detector system performance in terms of signal to background.

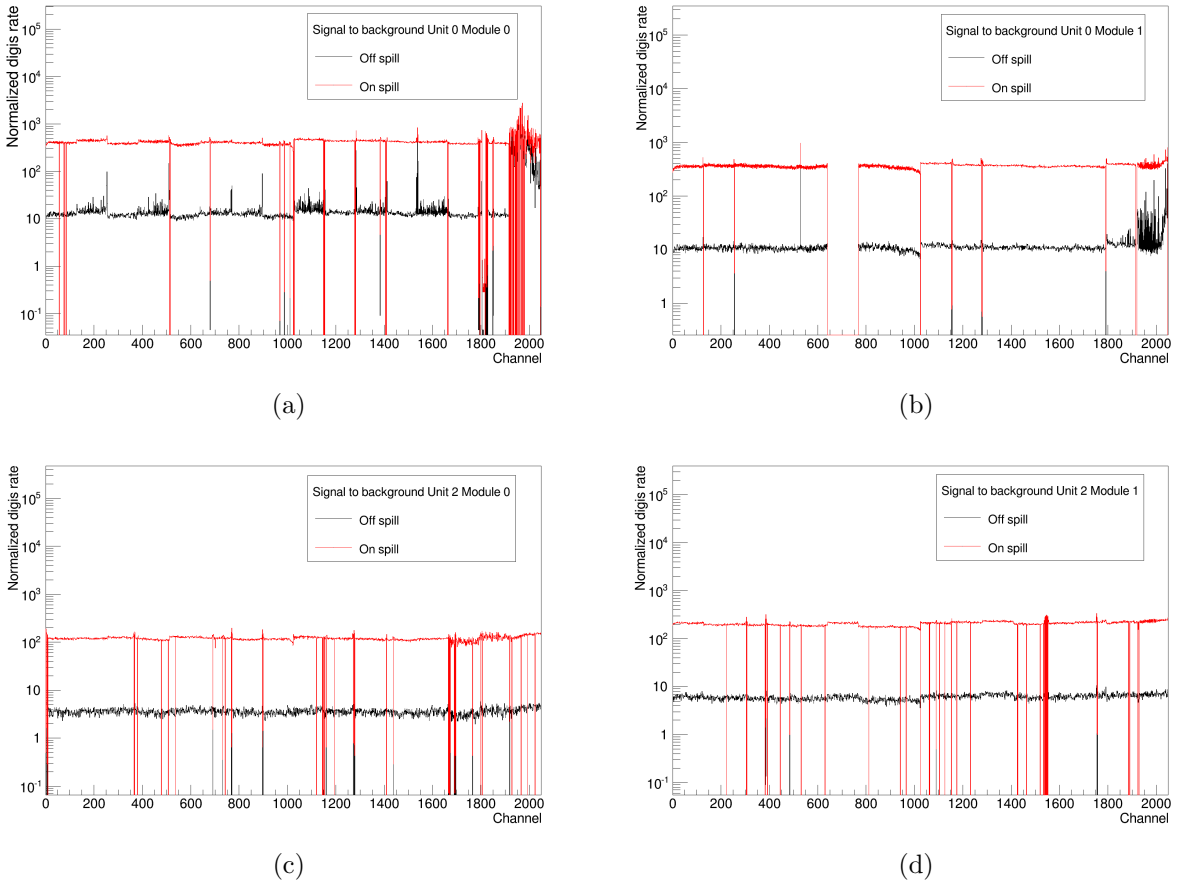


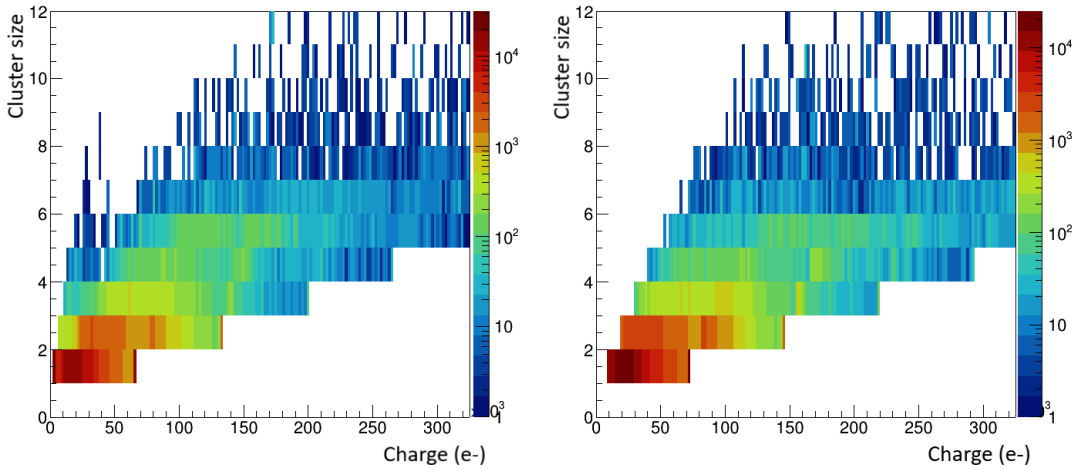
Figure 5.11: *Channel distribution for Unit 0 (a, b) and Unit 2 (c, d), in spill (red) and off spill (black) for the different mSTS modules after a cut of the first discriminator.*

5.4.5 Calibrated charge distribution

The charge calibration is one of the main steps before proceeding to the reconstruction. For the event build, only event with at least two hits in ToF were kept. Figure 5.12 shows the cluster size for Unit 0 and Unit 2 as a function of the charge distribution of all clusters. The reconstruction yields mostly 1 strip-cluster. Two and three strip-clusters are one to two orders of magnitude lower.

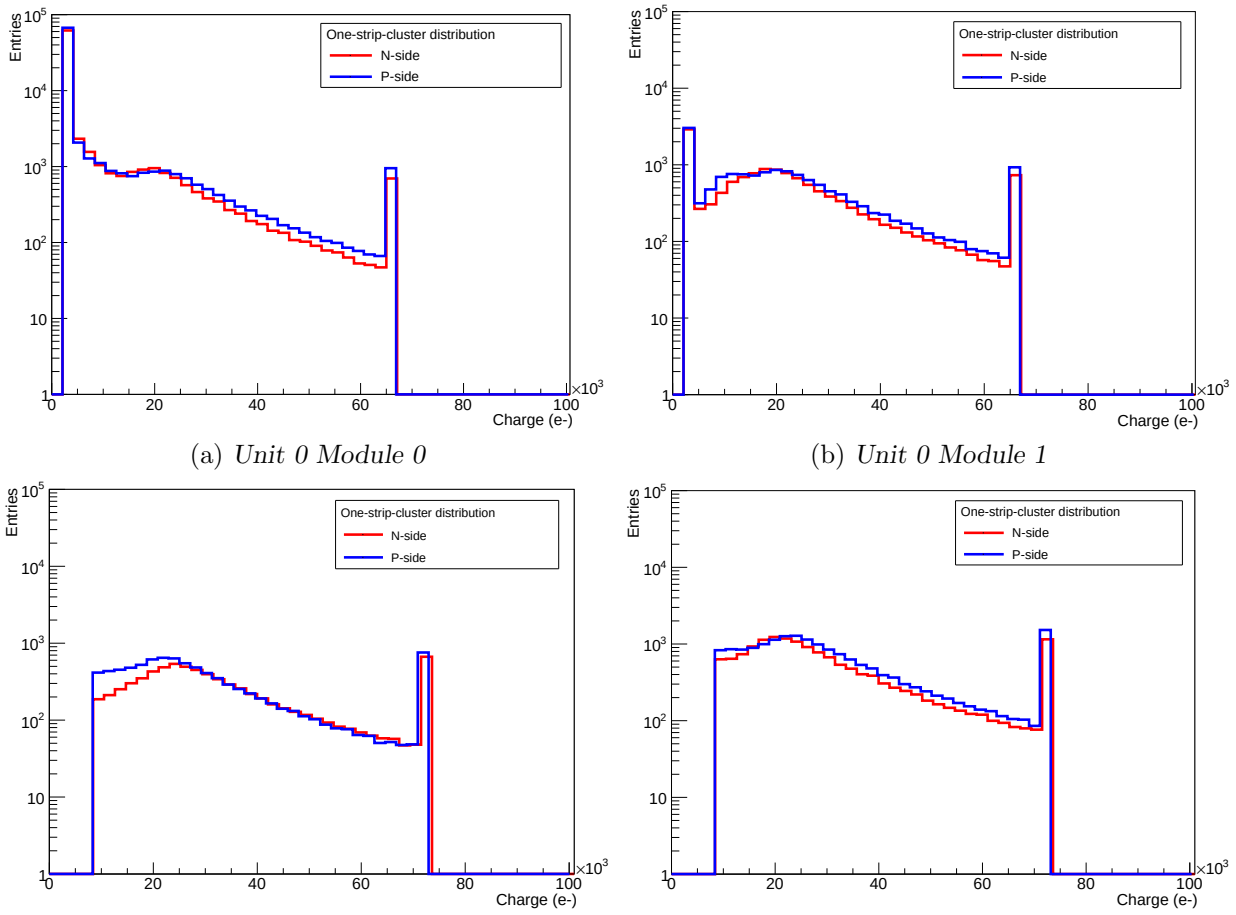
Figure 5.13 shows the distribution of one-strip-cluster signals, for p- and n-side, for Units 0 and 2. There are visible differences between the units, this is due to the fact that the lower threshold of the two units is not the same and the overflow bins are not at the same charge values. The overall distributions are very similar, with a clear peak around 24000 e-, which corresponds to the charge deposited on 320 μm silicon sensor by MIP, clearly separated from the noise contribution. This is especially visible for Unit 0 where the hardware threshold was set to 2800 e-.

If the average noise values determined for modules of Unit 0 is considered (around 1100 e-), the average signal to noise ratio can be estimated, resulting in a value above 21. This value is an important result for the detector since the modules used in mSTS represents some of the largest, and therefore, higher capacitance objects in the detector system.



(a) *Charge distribution for Unit 0* (b) *Charge distribution for Unit 2*

Figure 5.12: *Cluster size as a function of the charge distribution for Unit 0 and Unit 2.*



(a) *Unit 0 Module 0* (b) *Unit 0 Module 1*

(c) *Unit 2 Module 0* (d) *Unit 2 Module 1*

Figure 5.13: *One-strip-cluster charge distribution for p- and n-side for all modules in Unit 0 and Unit 2.*

5.5 Summary

This chapter presented results about the assembly, operation and performance of the STS modules in a realistic environment. For the first time in the beamtime of July 2021, a setup comprising of two tracking stations and a total of 11 modules was built. Two Units were assembled with the most up to date components, using the last version of the STS-XYTER v2.2 and the final versions of the low voltage regulators. During operation, besides a few unconnected channels (typically less than 1%) and two broken ASICs, three detector units were operational. An effective ground and powering scheme have been used for operating the detector modules in a symmetric and floating configuration.

Periodic structures were observed in the time distribution of all modules. These replica hits are generated due to significant noise in the MHz range in the fast discriminator. This behavior is well understood and consistent with the ASIC design. The replica effect can be significantly reduced by setting the fast discriminator threshold as low as possible without affecting the time resolution of the system and also by reducing the noise in the relevant frequency range to the largest possible extent.

A time calibration was performed at the ASIC level for all operational units. The system time resolution was estimated to 5.9 ns, which indicates a good time resolution achieved by the detectors. The noise contribution from the fast shaper (σ_n) was calculated in approximately 5950 e-. This result corresponds to the expected noise from the fast discriminator under the specific operation settings used in mSTS. The charge distribution of reconstructed hits was presented for different strip clusters and shows a clear separation between noise and MIP position. The average SNR was evaluated for 1 strip-cluster signals for Unit 0, resulting in a value of approximately 21. This value is an important result for the STS detector since the mSTS modules are some of the largest, and therefore, higher capacitance objects in the detector system. In addition, another important achievement was the operation of mSTS in a common, high-speed, free-streaming readout chain at intensities up to 10^9 ions/s, proving the DAQ concept in conditions close to the final STS operation.

Chapter 6

Summary and conclusions

The CBM experiment, with its rich physics program, will investigate collisions of heavy ion and proton beams, with fixed, heavy element targets, at beam energies between 2 and 14 AGeV (up to 14 AGeV for light nuclei and 29 AGeV for protons). The combination of high-intensity beams with unprecedented interaction rates and a novel free-streaming readout concept impose strong constraints in the STS as main core tracking detector. The experimental conditions pose demanding requirements in terms of channel density, readout bandwidth and low noise levels for the front-end electronics. The custom-developed front-end chip for reading out the double-sided silicon sensors in the STS detector is the STS-XYTER ASIC. It is a low-power, self-triggering ASIC with 128 channels, 5-bit ADC charge and 14-bit timing information. The chip is optimized for amplitude and time measurements in a heavily irradiated environment.

The main goal of this thesis is the test and characterization of the STS front-end electronics, which includes: the integration of the readout chain and detector components, the development of quality control procedures during the different assembly stages, and the commissioning and operation of the detector modules within dedicated beamtime campaigns.

Within this work, the operation, test and characterization of the STS-XYTER v2.2 have been achieved. A set of procedures and software tools, used during the ASIC characterization, were implemented and optimized. Among the different tested functionalities, the collection and analysis of the analog waveforms, where gain values of 22.4 mV/fC for electrons and 23.2 mV/fC for holes polarity were extracted for the slow shaper. Values of 40.2 mV/fC for electrons and 55.0 mV/fC for holes were also extracted for the fast shaper. The slow shaper peaking time was estimated for all possible values. The discharge time constant was calculated, obtaining larger values for holes polarities compare with electrons polarity. This difference becomes more pronounced for higher values of the feedback resistance. The ADC global threshold response was measured and its linearity evaluated for all possible ranges with the purpose of characterizing the transfer function for all available ranges in the chip.

In the last version of the ASIC (v2.2), it was found that, due to the inclusion of the diode-based ESD protection circuit, the CSA fast reset is not working as expected. However, it is possible to operate the chip at high rate without the fast reset feature, by reducing the discharge time constant of the CSA. This solution could introduce other problems during the operation such as a ballistic deficit or a serious degradation of the noise performance of the detector. It has been demonstrated that without the fast reset feature it is possible to operate the ASIC without compromising the performance in terms of ballistic deficit or noise levels.

An extensive investigation has been carried out to check the dependence of the ASIC's noise with different parameters such as: input capacitance, CSA bias current, IFED resistor, shaping time and shaping current, stability tests. From the results, it can be highlighted that:

- the average ENC(e-) level for holes is approximately (487 ± 29) e- and (503 ± 35) e- for electrons polarity. These values are comparable with previous versions of the chip mounted in a prototype FEB-C;
- the ENC(e-) increases linearly with the input capacitance in a ratio of 24.7 ENC(e-)/pF. This value is larger than predicted by simulations;
- the noise level increases by approximately 50 electrons for CSA values below 16 LSB units (around 1 mA/channel). For larger values of CSA current, the ENC(e-) remains stable;
- the ENC(e-) decreases with the increasing of the IFEB values until 32 LSB (around 100 electrons). For larger values of the IFED, no significant improvements in the noise performance of the system are visible;
- the ENC(e-) remains approximately constant among the different peaking times for holes polarity. There is a noticeable difference between electrons and holes behavior in terms of noise as a function of the peaking times;
- the noise stability showed a dispersion below 10% over 72 hours of continuous testing for both polarities;

A dedicated test setup has been used, based on a custom designed pogo-pin station, for testing the STS-XYTER v2.2 ASICs, which will be used in the assembly of the detector modules. QA protocols have been designed and optimized in order to improve the testing procedures to identify broken or unconnected channels from ASICs and chipcables. In the sample of chips used for the test, more than 90% were in perfect condition, which represents a very good yield. From the sample of chipcables used for the test, more than 90% presents one or none broken channels, representing a very good result. A decision criteria, to be used in STS production, has been proposed for the chipcable quality tests.

A GUI has been developed in PyQt version 4.0 for making the testing procedure as user friendly as possible. The procedures take around 1 minute for ASIC testing and similar time for the chipcable test. The implemented software for testing the chips and chips with microcables has been in use since 2021, making significant improvements in the detector modules assembly aiming to the STS production.

Within this work, a systematic testing of fully assembled STS modules has been performed. These tests allow to verify the performance of the latest version of the front-end ASIC functionalities and the electrical properties of the modules. Several parameters such as ASIC communication and control functionalities as well as the integrity of the signal path have been continuously monitored across all checks.

The noise measurements demonstrated that an overall level of approximately 1000 e- ENC is an achievable goal for most of the largest produced modules. The scans of the CSA bias current have exposed a large and stable plateau, at which the modules can be operated without deteriorating the system noise. For the feedback resistance, the noise levels are slightly larger at lower values of IFED (around 100 electrons) in comparison with larger values. There are small differences between p- and n-side. The noise levels for different shaping times show the dominance of the voltage noise component at smaller shaping time (90 ns), getting an increase of approximately 100 electrons with respect to the main value for larger values.

The results of the charge calibration have shown a good and homogeneous response for all produced modules, with a spread around the target values below 10%. These results are independent of the overall dimensions of the modules or the version of the front-end electronics in use.

For a selected module, signal readouts have been studied using an ^{241}Am gamma source. This allows to verify the calibration procedures and to assess the transfer function of the ADC threshold register in the ASIC. The measured charge collection efficiency can also be estimated, for this selected module, with a value of approximately 96%, slightly below the expected value. An average signal-to-noise ratio of 13.1 and 15.5 was calculated for the n- and p-side, respectively.

In addition, the module testing studies brought important insights regarding the fraction of broken and non-operational channels and consequently, assembly yield. The implementation of an ESD protection circuit in the latest version of the ASIC has improved the assembly yield, making possible to reach the production aim of approximately 1.5% of defective channels per module. The iterative testing of STS modules is, in general, an essential step for developing a reliable quality control procedure and establishing classification criteria towards series production.

Based on a common effort, for the first time during the beamtime of July 2021, a setup comprising of two tracking stations and a total of 11 modules was built and operated in a realistic environment. Besides a few unconnected channels (typically less than 1%) and two broken ASICs, three detector units were operational. An effective ground and powering scheme has been used for operating the detector modules in a symmetric and floating configuration.

Periodic structures were observed in the time distribution of all modules. These replica hits are generated due to significant noise in the MHz range in the fast discriminator. This behavior is well understood and consistent with the ASIC design. The replica effect can be significantly reduced by setting the fast discriminator threshold as low as possible without affecting the time resolution of the system and also by reducing the noise in the relevant frequency range to the largest possible extent.

A time calibration was performed at the ASIC level for all operational units. The system time resolution was estimated to 5.9 ns, which indicates a good time resolution achieved by the detectors. The noise contribution from the fast shaper (σ_n) was calculated in approximately 5950 e-. The charge distributions of reconstructed hits were presented for different strip clusters and show a clear separation between noise and MIP position. The average SNR was evaluated for 1 strip-cluster signals for Unit 0, resulting in a value of approximately 21.

The operation of mSTS in a common, high-speed, free-streaming readout chain at intensities up to 10^9 ions/s, helps to prove the STS concept in conditions close to the final operation.

Zusammenfassung

Das Compressed Baryonic Matter Experiment

Das umfangreiche Physikprogramm des CBM-Experiments zielt auf die Untersuchung der Zustandsgleichung von QCD-Materie bei Dichten, die denen im Kern von Neutronensternen ähneln, sowie auf die Suche nach einem möglichen Phasenübergang von hadronischer zu einer Quark-Gluon-Materie, nach dem kritischen Punkt des QCD-Phasendiagramms, nach der Existenz von quarkonischer Materie sowie von Anzeichen für die Wiederherstellung der chiralen Symmetrie.

CBM wird Kollisionen von Schwerionen bei Strahlenergien zwischen 2 und 14 AGeV (für leichte Kerne) sowie von Protonen bis zu 29 AGeV mit festem Target untersuchen. Das Experiment befindet sich derzeit im Aufbau als eine der vier wissenschaftlichen Säulen der zukünftigen FAIR-Anlage in Darmstadt, Deutschland. Das CBM-Detektorsystem ist darauf ausgelegt, das kollektive Verhalten von Hadronen zu messen, daneben auch mit noch nie dagewesener Präzision und Statistik seltene Sonden wie Multi-Strange-Hyperonen, Charm-Teilchen sowie Vektormesonen, die in Leptonenpaare zerfallen. Um die erforderliche Präzision und Statistik zu erreichen, werden die Messungen bei Kollisionsraten von bis zu 10 MHz durchgeführt. Dies erfordert sehr schnelle und strahlungsresistente Detektoren, ein neuartiges Datenauslese-und Analysekonzept einschließlich einer Free-Streaming-Frontend-Elektronik und eines Hochleistungscomputerclusters für eine Online-Ereignisauswahl. Die Kombination von hochintensiven Strahlen mit einem Hochraten-Detektorsystem bietet weltweit einzigartige Bedingungen für eine umfassende Untersuchung von QCD-Materie bei den höchsten im Labor erreichbaren Baryonendichten.

Das Silizium-Spurverfolgungssystem

Das Silicon Tracking System (STS) ist der zentrale Detektor für die Spurverfolgung und Impulsmessung im CBM-Experiment. Seine Hauptaufgabe ist die Messung der Impulse geladener Teilchen mit einer hohen Auflösung (1.5% for p$\geq$1 GeV/c) und deren Spurrekonstruktion mit einer Effizienz von mehr als 95% für p$\geq$1 GeV/c. Um Mehrfach-Coulomb-Streuung sowie die Produktion von Delta-Elektronen und Konversionselektronen zu minimieren, muss der Tracker ein niedriges Materialbudget haben. Die experimentellen Bedingungen stellen hohe Anforderungen an die Kanaldichte und Auslesebandbreite der Front-End-Elektronik. Die wichtigsten Anforderungen an das STS-Design lassen sich wie folgt zusammenfassen:

- Der Detektor befindet sich in einem Volumen von etwa 1.4×2.3×1.3 m^3 im Inneren des supraleitenden CBM-Dipolmagneten.
- Er muss in der Lage sein, bis zu 1000 Teilchen pro zentraler Au + Au-Kollision bei Wechselwirkungsraten von bis zu 10 MHz im SIS100 zu messen.
- Er benötigt strahlungsharte Siliziumsensoren, die bis zu 10^{13} 1 MeV n_{eq} während des Betriebs aushalten.
- Das Materialbudget sollte so klein wie möglich sein.

- Die Sensoren werden mit einer schnellen und selbstgetriggerten Front-End-Elektronik (FEE) ausgelesen.
- Die FEE muss in einer Strahlungsumgebung von bis zu 100 krad/Jahr zuverlässig arbeiten.
- Das Kühlsystem muss in der Lage sein, bis zu 50 kW Verlustleistung aus dem Inneren der STS-Detektorbox abzuführen.

Das Detektorsystem besteht aus 876 doppelseitigen Silizium-Mikrostreifensensoren, die in 8 aufeinanderfolgenden Detektorlagen (Stationen) angeordnet sind und den Polarwinkelbereich von $2.5° \leqslant \Theta \leqslant 25°$ abdecken. Die STS-Stationen befinden sich zwischen 30 cm und 100 cm hinter dem Target und innerhalb eines 1 Tm Dipol-Magnetfeldes. Die wichtigste funktionale Einheit des STS-Detektors ist das Modul, welches aus einem Sensor, Mikrokabeln und zwei Front-End-Boards mit jeweils 8 STS-XYTER Frontend-ASICs besteht. Der speziell entwickelte ASIC implementiert das analoge Front-End mit Vorverstärkung und Pulsformung, die Digitalisierung sowie die Erzeugung individueller Treffer-Datenworte für jedes Sensorsignal. Die Detektormodule sind auf Trägerstrukturen ("Leitern") aus Kohlenstoff mit geringer Masse montiert, so dass sich die Ausleseelektronik in der Peripherie des Detektors außerhalb der physikalischen Akzeptanz befindet. Die Signale der Sensoren werden über ultraleichte Auslesekabel mit bis zu 50 cm Länge zur FEE übertragen.

Motivation für diese Arbeit

Das CBM-Physikprogramm, das nur mit sehr hohen Wechselwirkungsraten realisierbar ist, stellt starke Anforderungen an die Detektorleistung und die Fähigkeiten des Datenerfassungssystems(DAQ). CBM wird ein Free-Streaming-Auslesesystem ohne Hardware-Trigger nutzen, d.h. eine Kombination aus selbstgetriggerter Front-End-Elektronik (FEE), schnellem Free-Streaming-Datentransport sowie einer Online-Ereignisauswahl und-rekonstruktion.

Der STS-XYTER ist ein speziell entwickelter Front-End-ASIC zum Auslesen der doppelseitigen Silizium Sensoren im STS-Detektor. Sein Einsatz im STS erforderte die Entwicklung von Software-Werkzeugen und Methoden zur Evaluierung des analogen Front-Ends, der gesamten Signalverarbeitungskette und zur optimalen Kalibrierung der Zeit- und Amplitudenmessungen.

Es wurden bereits Vorgänger-Versionen des STS-XYTER-ASIC hergestellt und charakterisiert. Da nun die finale Version vorliegt, die im CBM-STS-Detektor verwendet werden wird, ist eine vollständige Charakterisierung des Chips in Bezug auf die Auslese- und Rauschleistung ein wichtiger Aspekt für das zukünftige Experiment.

Eine effiziente Qualitätskontrolle (QC) der Einzelkomponenten ist eine wichtige Voraussetzung für den Zusammenbau von funktionierenden Detektormodulen. Um dieses Ziel zu erreichen, sind Softwareentwicklungen notwendig sowie die Implementierung von Verfahren der Qualitätskontrolle, um unter anderem die korrekte Funktionalität des STS-XYTERs und die Qualität der Bond-Verbindungen der Chipkabel (ASIC + Mikrokabel) zu überprüfen. Darüber hinaus ist es wichtig, ein Entscheidungskriterium zur Akzeptanz der fertigen Modulen festzulegen auf Grundlage der Anzahl defekter Kanäle, des Stromverbrauchs sowie weiterer Betriebsparameter.

Der Bau kompletter Detektormodule mit finalen Komponenten und deren Betrieb innerhalb der Auslesekette in verschiedenen Betriebs-Szenarien ist ein wichtiger Meilenstein für das STS-Experiment. Das systematische Testen der vollständig montierten Module ermöglicht die Überprüfung der Leistung der neuesten Version der Front-End-ASIC-Funktionen sowie der elektrischen Eigenschaften der Module. Verschiedene Parameter wie die ASIC-Kommunikations- und Steuerungsfunktionen sowie die Integrität des Signalpfads und das Rauschverhalten müssen kontinuierlich überwacht werden.

Einer der wichtigsten Schritte auf dem Weg zur Herstellung des STS-Detektors ist der Betrieb der vollständig montierten Module in einem realistischen Szenario. Dieser Idee folgend wurde ein kleiner Prototyp des vollständigen Detektors, genannt mini-STS (mSTS), als Teil der mini-CBM-Aktivitäten gebaut. Der mSTS-Aufbau wurde für die Strahlzeit im Juli 2021 in der Strahllinie installiert und mit O + Ni Kollisionen bei 2 AGeV am Schwerionen-Synchrotron SIS18 an der GSI Darmstadt betrieben. Diese Studien brachten wertvolle Erkenntnisse und Erfahrungen für Montage und Test der Detektormodule. Daneben konnten mittels dieses Aufbaus, der aus zwei Tracking-Stationen und insgesamt 11 Modulen bestand, Leistungsstudien in einer realistischen Betriebsumgebung durchgeführt werden.

Test und Charakterisierung des STS-XYTER v2.2

Die Charakterisierung des STS-XYTER Version 2.2 ist einer der wichtigsten Schritte vor seinem Einsatz in der Auslesekette. Im Rahmen dieser Arbeit wurde der Betrieb und die Charakterisierung des STS-XYTER v2.2 erfolgreich durchgeführt. Eine Reihe von Verfahren und Software-Tools, die bei der ASIC-Charakterisierung verwendet werden, wurden implementiert und optimiert. Zu den verschiedenen getesteten Funktionalitäten gehören die Erfassung und Analyse der ASIC-internen analogen Signalformen, aus denen Verstärkungsfaktoren von 22.4 mV/fC für Elektronen und 23.2 mV/fC für die Polarität der Löcher im langsamen Pulsformungs-Pfad (Slow Shaper) extrahiert wurden. Werte von 40.2 mV/fC für Elektronen und 55.0 mV/fC für Löcher wurden für den schnellen Shaper ermittelt. Die Peaking-Zeiten im langsamen Shaper wurde ebenfalls für alle möglichen Konfigurationen experimentell bestimmt. Die Entladungszeitkonstante im CSA wurde bestimmt und ergab größere Werte für die Polarität der Löcher im Vergleich zur Zeitkonstante für Elektronen. Dieser Unterschied wird noch deutlicher für höhere Werte des Rückkopplungswiderstands. Das Antwortverhalten des ADC als Funktion der globalen Digitalisierungs-Schwelle wurde gemessen und seine Linearität für alle Messbereiche bestimmmt, um die Übertragungsfunktion für alle verfügbaren Messbereiche des Chips zu charakterisieren.

In der neuesten Version 2.2 des ASICs wurde festgestellt, dass seit der Implementierung einer diodenbasierten ESD-Schutzschaltung der schnelle CSA-Reset nicht wie erwartet funktioniert. Es ist jedoch möglich, den Chip auch ohne die Fast-Reset-Funktion mit hoher Rate zu betreiben, indem die Zeitkonstante des CSA verringert wird. Potentielle Probleme dieses Lösungsansatzes wie z. B. ein ballistisches Defizit oder eine Verschlechterung der Rauschleistung des Detektors wurden untersucht. Es wurde gezeigt, dass der ASIC auch ohne die schnelle Rücksetzfunktion betrieben werden kann ohne Beeinträchtigung der Leistung in Bezug auf ballistisches Defizit oder Rauschpegel. Für den Betrieb des STS-XYTER v2.2 ASIC ist ein gutes Rauschverhalten eine der wichtigsten Anforderungen.

Der Chip wurde in Bezug auf das Rauschen als Funktion verschiedener Betriebsparameter wie Eingangskapazität, CSA-Bias-Strom, Rückkopplungswiderstand (IFED), Shaping-Zeit, Shaping-Strom und Langzeit-Stabilität charakterisiert. All diese Untersuchungen ermöglichen die Optimierung der Chip-Parameter sowie die Erkennung möglicher Fehlfunktionen, die zu ernsthaften Problemen während des STS-Betriebs führen könnten. Aus den Ergebnissen dieser ASIC-Studien kann hervorgehoben werden:

- das durchschnittliche ENC(e-)-Rauschniveau beträgt ungefähr (487 ± 29) $e-$ für Löcher und (503 ± 35) $e-$ für Elektronen-Polarität. Diese Werte sind kompatibel mit früheren Versionen des Chips, die mit dem FEB-C Prototyp-FEB bestimmt wurden;
- der ENC(e-)-Wert steigt wie erwartet linear mit der Eingangskapazität. Der Wert von 24.7 $e-$/pF ist größer als durch Simulationen vorhergesagt;

- das Rauschniveau steigt um etwa 50 Elektronen für CSA-Werte unter 16 LSB-Einheiten (d.h. unterhalb von ca. 1 mA/Kanal). Für größere Werte des CSA-Stroms bleiben die ENC(e-)-Werte stabil;
- die ENC(e-)-Werte nehmen mit der Erhöhung der IFED-Werte bis auf 32 LSB um etwa 100 Elektronen ab. Bei größeren IFED-Werten sind keine nennenswerten Verbesserungen des Rauschverhaltens des Systems sichtbar;
- die ENC(e-)-Werte bleiben bei den verschiedenen Peaking-Zeiten für Löcher ungefähr konstant. Es gibt einen deutlichen Unterschied zwischen dem Verhalten von Elektronen und Löchern in Bezug auf das Rauschen als Funktion der Peaking-Zeiten;
- die Rauschstabilität zeigt eine Streuung von weniger als 10% über 72 Stunden Dauertest für beide Polaritäten;

Entwicklung von Software-Tools und Verfahren für die ASIC-Qualitätskontrolle

Voraussetzung für den Zusammenbau funktionsfähiger Detektormodule in jedem Experiment ist eine strenge Qualitätssicherung (QC) der Komponenten. Diese Verfahren zielen darauf ab, die Funktionalitäten aller Komponenten zu gewährleisten, um die Detektorspezifikationen zu erfüllen. Als Haupt-Spurverfolgungsdetektor des CBM-Experiments stellt der STS hohe Anforderungen an die Rekonstruktionsleistung und Impulsauflösung. Diese Kenngrößen werden neben anderen Faktoren durch die Qualität der Detektormodule und ihrer Komponenten bestimmt.

Für Tests der ASICs wurde ein spezieller Aufbau verwendet, der auf einer speziell entwickelten Pogo-Pin-Station basiert, in der insgesamt 450 ASICs und Chipkabel (d.h. ASICs mit gebondetem Mikrokabel) einzeln getestet wurden. Es wurden Qualitätssicherungsprotokolle entwickelt und optimiert, um die Testverfahren zu verbessern. Viele der auftretenden Fehler beim Modulbau sind auf Produktionsfehler der Komponenten zurückzuführen, oder sie erscheinen nach Transport oder durch unsachgemäße Handhabung während der Testverfahren. Deshalb basiert die Ausbeute gut getesteter ASICs auch auf den Erfahrungen mit früheren Versionen des Chips und den resultierenden Optimierungen aller Prozessschritte. Von der Gesamtzahl der getesteten Chips waren mehr als 90% in einwandfreiem Zustand, was eine sehr gute Ausbeute darstellt.

Es wurden auch Entscheidungskriterien für die Qualitätsprüfung der Chipkabel entwickelt. Von der Gesamtzahl der verwendeten Stichproben wiesen mehr als 90% nur einen oder keinen defekten Kanal auf, was ein sehr gutes Ergebnis ist.

Ein GUI wurde in PyQt Version 4.0 entwickelt, um den Testprozess so benutzerfreundlich wie möglich zu gestalten. Die Testprozedur dauert etwa 1 Minute für ASIC-Tests und ähnlich lange für den Chipkabeltest. Die implementierte Software zum Testen der ASICs und der Chipkabel ist seit 2021 im Einsatz und hat die Montage der Detektormodule im Hinblick auf die STS-Produktion deutlich verbessert.

Charakterisierung von vollständig montierten STS-Modulen

Die wesentliche STS-Detektoreinheit ist das Detektormodul, das aus einem doppelseitigen Silizium-Mikrostreifensensor besteht, der über mehrere gestapelte Mikrokabel mit 16 der speziell entwickelten ASICs auf zwei Front-End-Platinen (FEBs) verbunden ist. Die Sensoren wurden von Hamamatsu Photonics K.K. mit einer Dicke von 320 μm hergestellt.

Der Test und die Charakterisierung der fertig montierten Module sind von grundlegender Bedeutung für den Nachweis der Montagekonzepte und der Leistungsfähigkeit der Module für den endgültigen STS-Detektor. In den letzten Jahren hat das CBM-STS-Projekt wichtige Meilensteine in Bezug auf den Zusammenbau und den erfolgreichen Betrieb der ersten Module erreicht. Diese

Module wurden in mehreren Studien verwendet, um ihre Leistungsfähigkeit zu demonstrieren und auch die der neuesten Versionen der STS-Frontend-Elektronik zu charakterisieren. Parallel zu diesen Entwicklungen war es notwendig, ein allgemeines Testverfahren für Module auszuarbeiten, das folgende Ziele verfolgt:

- die Funktionalität jedes Moduls inklusive aller seiner Komponenten zu bewerten;
- die optimalen Betriebsparameter für jedes einzelne Modul zu bestimmen;
- fehler in den gebauten Objekten vor der weiteren Integration zu identifizieren und die Qualitätskontrolle zu optimieren;

Dieser letzte Punkt kann auch als erster Schritt auf dem Weg zu einem robusteren Qualitätskontrollkonzept verstanden werden, das darauf abzielt, eine zuverlässige Leistung der Module im endgültigen STS-Detektor und eine hohe Produktionsausbeute sicherzustellen.

Die systematische Prüfung vollständig montierter STS-Module ermöglicht die Überprüfung der Leistung der neuesten Version des Front-End-ASICs und der elektrischen Eigenschaften der Module. Verschiedene Parameter wie die ASIC-Kommunikations- und Konfigurationsfunktionen sowie die Integrität des Signalpfads wurden bei allen Tests kontinuierlich überwacht. Die Ergebnisse der Ladungskalibrierung zeigen ein gutes und homogenes Verhalten für alle getesteten Module, mit einer Streuung um die Zielwerte von unter 10%. Diese Ergebnisse sind unabhängig von den Art der Module (Sensorgröße, Kabellänge) und der Version der verwendeten Frontend-Elektronik. Die Rauschmessungen zeigen, dass ein Gesamtpegel von ca. 1000 $e-$ ENC ein erreichbares Ziel auch für die größten produzierten Module ist. Die systematische Variation des CSA-Bias-Stroms zeigt ein breites und stabiles Plateau, in dem die Module ohne Verschlechterung des Systemrauschens betrieben werden können. Als Funktion des Rückkopplungswiderstand ist das Rauschen bei niedrigeren IFED-Werten etwas größer (bis zu ca. 100 Elektronen) im Vergleich zu größeren IFED-Werten. Die Unterschiede zwischen p- und n-Seite sind gering. Die Rauschpegel für verschiedene Shaping-Zeiten zeigen die Dominanz des Spannungs-Rauschens bei der kleinsten Shaping-Zeit (90 ns) mit einem etwa 100 Elektronen größeren Rauschen verglichen mit längeren Shaping-Zeiten.

An einem ausgewählten Modul wurde die Signalauslese mit einer ^{241}Am-Gammaquelle untersucht. Dies ermöglichte die Überprüfung des Kalibrierungsverfahrens und die Bewertung der Übertragungsfunktion der ADC-Schwellenwertsetzung im Chip. Die Ladungssammel-Effizienz wurde für dieses ausgewählte Modul mit einem Wert von etwa 96% gemessen, was leicht unter dem Erwartungswert liegt. Für die n- und p-Seite wurde ein durchschnittliches Signal-Rausch-Verhältnis von 13.1 bzw. 15.5 für Signale von der Gamma-Quelle berechnet.

Darüber hinaus brachten diese Untersuchungen wichtige Erkenntnisse über den Anteil der defekten und nicht funktionsfähigen Kanäle in den Modulen und folglich über die Ausbeute des Modulbaus. Die Implementierung einer ESD-Schutzschaltung in der neuesten Version des ASIC hat die Ausbeute bei der Montage verbessert, so dass das Produktionsziel von weniger als 1.5% defekter Kanäle pro Modul erreicht werden kann. Die iterative Prüfung der STS-Module ist ein wesentlicher Schritt zur Entwicklung eines zuverlässigen Qualitätskontrollverfahren und für die Festlegung von Klassifizierungskriterien für die Serienproduktion.

Montage, Test, Betrieb und Charakterisierung des mSTS-Detektors

Der Betrieb mehrerer vollständig montierter Module in einem realistischen experimentellen Szenario ist ein sehr wichtiger Schritt auf dem Weg zur Produktion des vollständigen STS-Detektors. Ein kleiner Prototyp des vollständigen Detektors, genannt mini-STS (mSTS), wurde im Rahmen der CBM Phase 0 gebaut. Der Aufbau war in Betrieb während der Strahlzeit-Kampagne im Juli 2021 mit O + Ni Kollisionen bei 2 AGeV am Schwerionen-Synchrotron SIS18 in GSI Darmstadt.

Zum ersten Mal wurde während der Strahlzeit im Juli 2021 ein Aufbau bestehend aus zwei Trackingstationen und insgesamt 11 Modulen aufgebaut und in einer realistischen Umgebung betrieben. Zwei Einheiten (4 Module) waren aus den neuesten Komponenten aufgebaut, darunter die letzte Version des STS-XYTER v2.2 und die finalen Spannungsregler-ASICs. Während der Strahlzeit waren, abgesehen von einigen defekten Kanälen (typischerweise weniger als 1%) und zwei defekten ASICs, drei Detektoreinheiten betriebsbereit. Für den Betrieb der Detektormodule wurde ein effektives Erdungs- und Spannungsversorgungs-Schema verwendet mit einer symmetrischen Versorgung aus potentialfreien Netzgeräten.

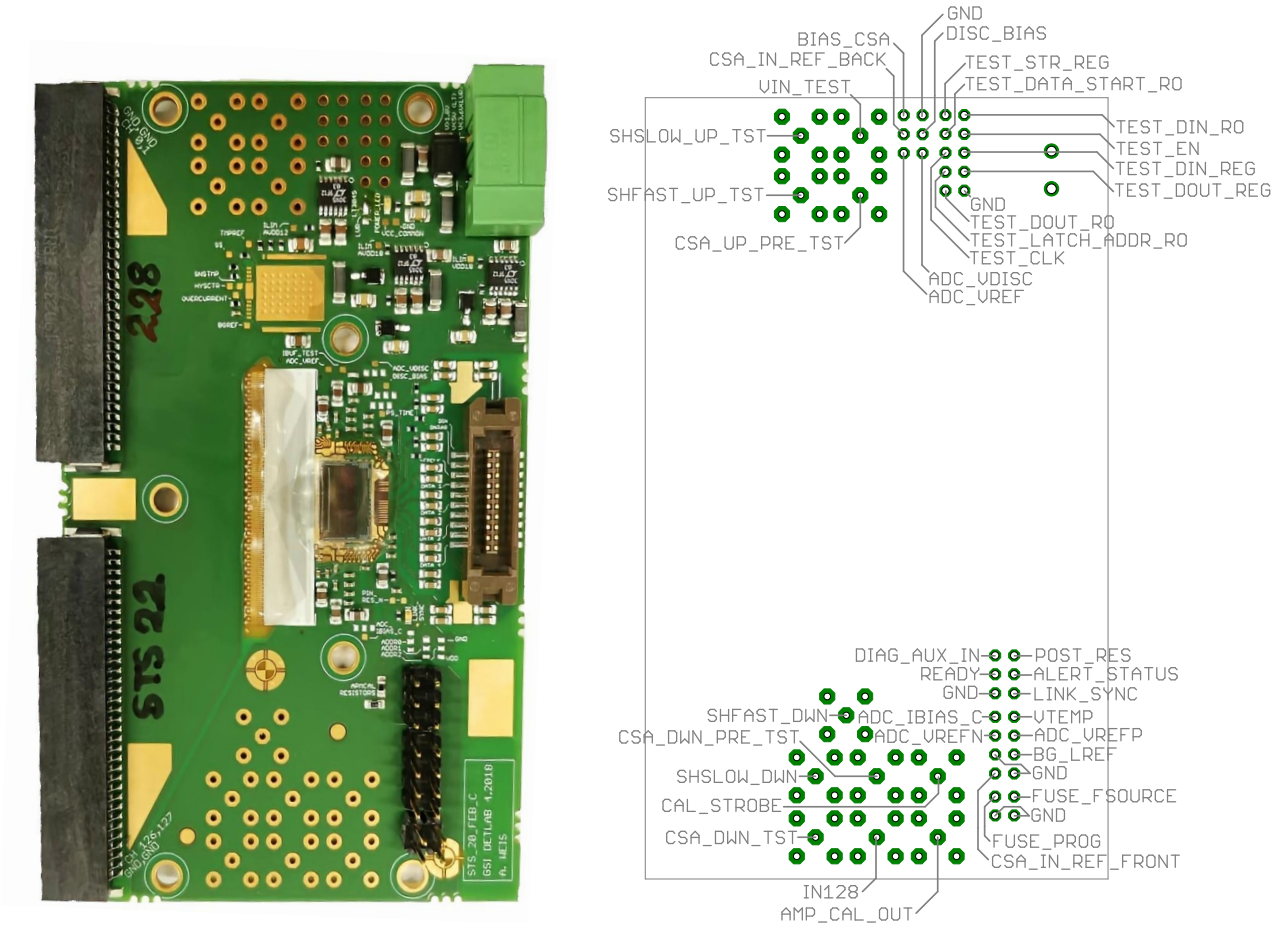
In allen Modulen wurden periodische Strukturen in der zeitlichen Verteilung der Daten beobachtet. Diese unphysikalischen Replikat-Treffer wurden durch ein erhebliches Rauschen im MHz-Bereich im schnellen Diskriminator erzeugt. Dieses Verhalten ist aufgrund der unterschiedlichen Bandbreiten des schnellen und langsamen Diskriminators im ASIC-Design verständlich. Dieser Replika-Effekt kann deutlich reduziert werden, indem der Schwellenwert des schnellen Diskriminators möglichst niedrig eingestellt wird, ohne die Zeitauflösung des Systems zu beeinträchtigen, und indem das Rauschen (v.a. aus externen Quellen) spezifisch im relevanten Frequenzbereich so weit wie möglich reduziert wird.

Für die Zeitkalibrierung wurden zwei Detektormodule der Einheit 0 verwendet. Die Zeitauflösung des Systems wurde zu 5.9 ns ermittelt, was eine gute Zeitauflösung für die STS-Module darstellt. Der Rauschbeitrag des schnellen Shapers wurde zu etwa $5950e-$ (σ_n) bestimmt. Dieses Ergebnis entspricht dem erwarteten Rauschen des schnellen Diskriminators unter den spezifischen Einstellungen in mSTS. Die Ladungsverteilungen der rekonstruierten Treffer wurden für Ladungscluster mit verschiedener Streifenanzahl bestimmt und zeigen eine klare Trennung zwischen Rauschen und der Signalverteilung um die MIP-Position herum. Das durchschnittliche SNR wurde für Signale mit 1-Streifen-Clustern in der Einheit 0 ausgewertet und ergibt einen Wert von ungefähr 21. Dieser Wert ist ein wichtiges Ergebnis für den STS-Detektor, da die im mSTS verwendeten Module zu den größten Modulen mit höchsten Rauschwerten des STS-Detektorsystems gehören.

Der Betrieb von mSTS in einem gemeinsamen mCBM-System mit einer Hochgeschwindigkeits-Auslesekette und den Daten von Kollisionen mit Intensitäten von bis zu 10^9 ions/s hilft, das STS-Konzept unter Bedingungen zu verifizieren, die dem realen Betrieb in CBM nahe kommen.

Appendix A

The prototype FEB-C



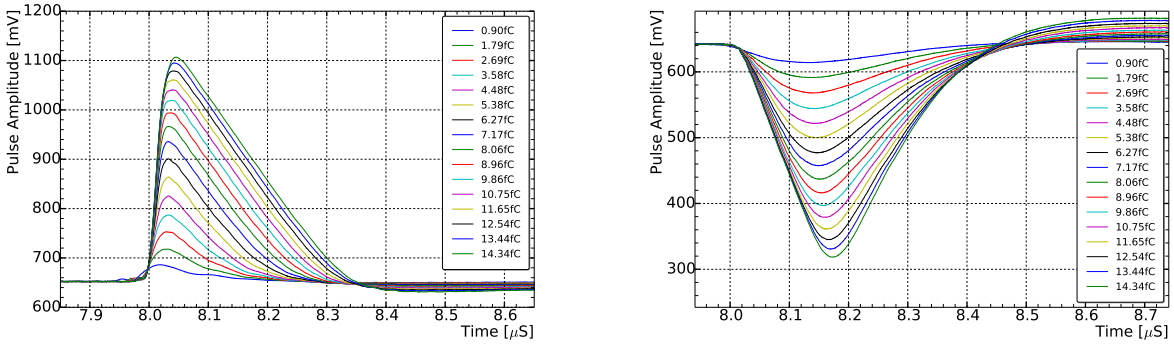
(a) *Prototype FEB-C fully equipped.* (b) *Schematics of main signals in the FEB-C.*

Figure A.1: *Photo and schematics of the prototype FEB-C used for testing the STS-XYTER v2.2. Two ERNI connectors are used for interfacing up to 128 channels in the detectors with the chip. The FEB-C is fabricated with commercial components including linear regulators.*

Appendix B

Waveforms of the STS-XYTER v2.2 shapers for electron polarity

Part of the characterization procedure of the STS-XYTER v2.2 is the acquisition of the shapers waveforms and estimation of the gain for holes and electrons polarities. Figure B.1 shows the waveforms acquired from a test channel in the STS-XYTER v2.2. The charge pulses are injected at the input of the CSA using the internal calibration pulse existing in the chip.



(a) *Fast shaper waveforms.* (b) *Slow shaper waveforms.*

Figure B.1: *Waveforms of the ASIC's shapers measured for electrons polarity.*

Appendix C

ADC calibration

The STS-XYTER v2.2 implements in each channel a 5-bit continuous type, flash ADC with digital peak detector. Figure C.1 illustrates the block diagram of the STS-XYTER ASIC flash ADC, where the *VRef_P,N,T* are the ADC reference potentials. *VRef_P* and *VRef_N* determine the coarse dynamic range of the ADC. The common global threshold of the discriminators, are generated by a resistor ladder stretched between these potentials. In order to correct the mismatch offset of every ADC, trimming corrections are used to adjust the effective threshold of each discriminator for all channels i.e., achieving the linearity of the system. The discriminator outputs are connected to the peak detector logic, which provides thermometric encoding for all the 31 cells. The *VRef_T* reference potential controls the position of the signal baseline relative to the ADC, acting as the effective system threshold.

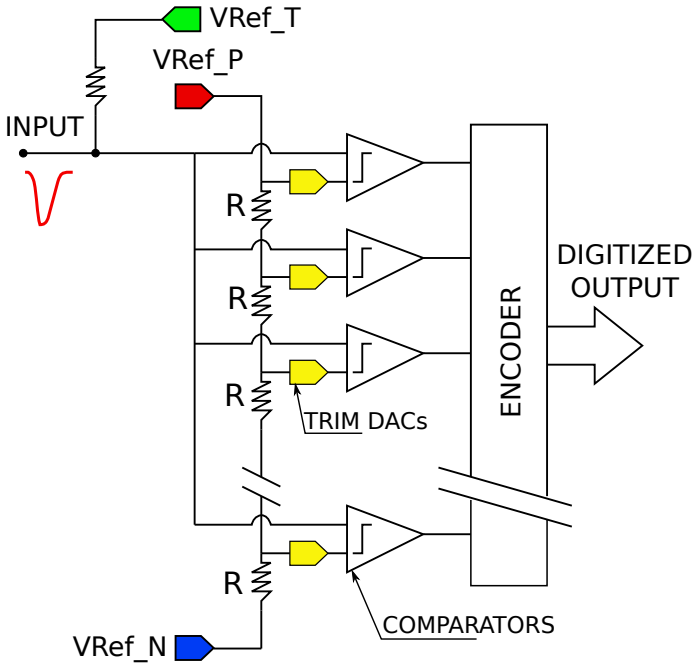
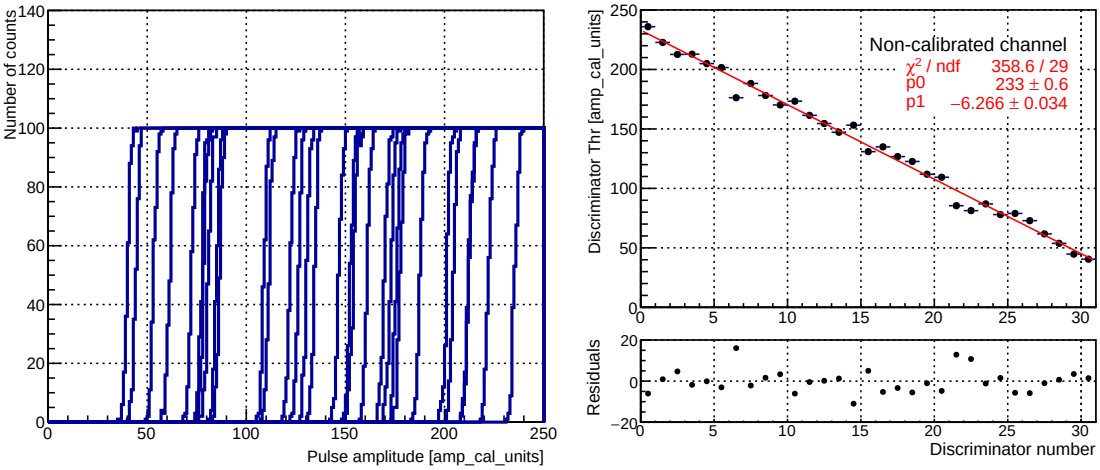
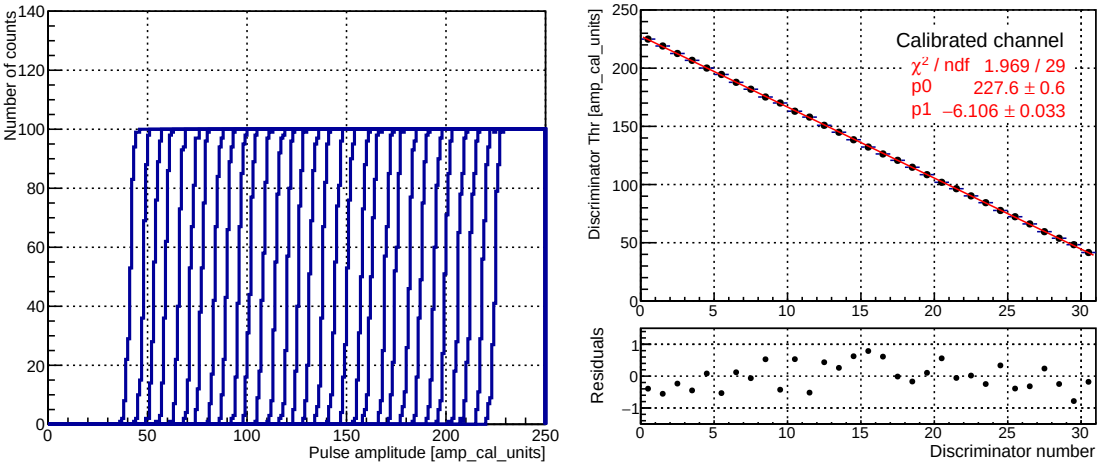


Figure C.1: Block diagram of the STS-XYTER ASIC flash ADC [43].

Figure C.2 shows the s-curves and linearity with the fitting residuals, before and after calibration, for the 31 discriminators in one channel. The linearity of the ADC is verified by plotting the discriminators threshold, obtained via the error function fitting, as a function of the discriminator number.



(a) *S-curves for a non calibrated channel (left side). Linearity of the ADC before calibration (right).*



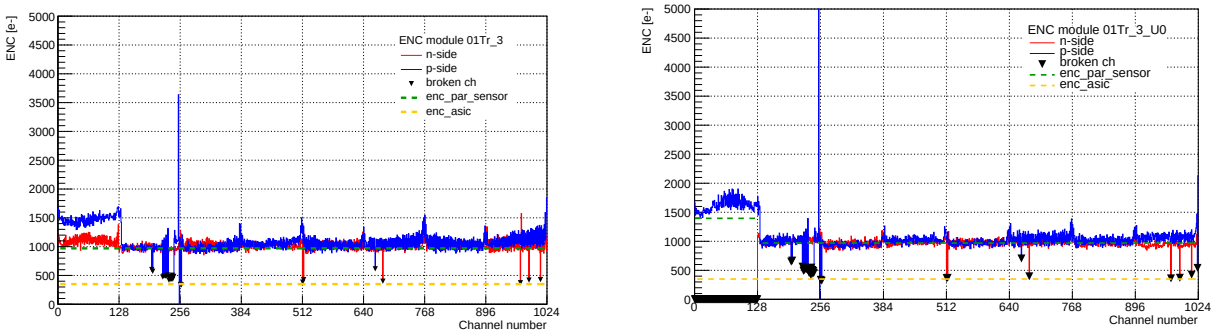
(b) *S-curves for a calibrated channel (left side). Linearity of the ADC after calibration (right).*

Figure C.2: *ADC s-curves and linearity, for the 31 discriminators in one channel, before (a) and after (b) calibration procedures.*

Appendix D

Noise comparison for module 01Tr_3 in different setups

Figure D.1 shows the equivalent noise charge (ENC) average values across all channels for the module 01Tr_3. The average system noise is around 1000 e- for the two plots independently of the setup. There is an ASIC in the p-side not working properly due to communication problems for the module mounted in the ladder. The odd-even difference, related to the routing and stretching of the microcables during the measurements in the test box, almost disappears when the modules are mounted on a carbon fiber ladder, as in the final detector setup.



(a) *Noise levels for module 01Tr_3 in the test box.* (b) *Noise levels for module 01Tr_3 in the ladder.*

Figure D.1: *Average noise levels comparison across the 1024 channels for module 01Tr_3 in two different setups: the test box and the carbon fiber ladder.*

List of Acronyms

A	
ADC	Analog-to-Digital Converter
AFCK	AMC FMC carrier Kintex
AFE	Analog Front-end
ALICE	A Large Ion Collider Experiment
APPA	Atomic Physics, Plasma and Applications
ASIC	Application Specific Integrated Circuit
B	
BM@N	Baryonic Matter at Nuclotron
C	
CBM	Compressed Baryonic Matter
CMOS	Complementary MOS
CRI	Common Readout Interface
D	
DAC	Digital-to-Analog Converter
DAQ	Data Acquisition System
DCS	Detector Control System
DPB	Data Processing Board
E	
ENC	Equivalent Noise Charge
EoS	Equation of State
ESD	Electrostatic Discharge

F	
FAIR	Facility for Antiprotons and Ions Research
FEB	Front-end Board
FEE	Front-end Electronics
FIFO	First In First Out. Electronic circuits for buffering and flow control
FLES	First Level Event Selector
FPGA	Field Programmable Gate Array
G	
GBT	Gigabit Transceiver
GEM	Gas Electron-Multiplier
GSI	Gesellschaft für Schwerionenforschung GmbH
H	
HADES	High Acceptance Di-Electron Spectrometer
I	
IC	Integrated Circuit
IPBus	IP-based protocol for controlling hardware devices
J	
JINR	Joint Institute for Nuclear Research
L	
LDO	Low Dropout regulator
LHC	Large Hadron Collider
LHCb	Large Hadron Collider beauty
LSB	Least Significant Bit
LVDS	Low Voltage Digital Signal
M	
MAPMT	Multi Anode Photomultiplier
MAPS	Monolithic Active Pixels
mCBM	mini CBM experiment
MIP	Minimum Ionizing Particles
MOS	Metal Oxide Semiconductor
MPD	Multi-Purpose Detector
MPV	Most Probable Value
MRPC	Multi-gap Resistive Plate Chambers
mSTS	mini STS
MUCH	Muon Chambers
MVD	Micro Vertex Detector
MWPC	Multi-Wire Proportional Chambers

N	
NA61/SHINE	North Area 61/The SPS Heavy Ion and Neutrino Experiment
NICA	Nuclotron-based Ion Collider fAcility
NIEL	Non-Ionizing Energy Loss
NuSTAR	Nuclear STructure, Astrophysics and Reactions
P	
PANDA	anti-Proton ANihilation at DArmstadt
PCB	Printed Circuit Board
POB	Power Board
PSD	Particle Spectator Detector
Q	
QCD	Quantum Chromodynamics
QGP	Quark Gluon Plasma
R	
RHIC	Relativistic Heavy Ion Collider
RICH	Ring Imaging Cherenkov Detector
ROB	Readout Board
RPC	Resistive Plate Chambers
S	
SCA	Slow Control ASIC
SEU	Single Event Upset
SIS	Schwerionensynchrotron
SNR	Signal-to-Noise Ratio
SPS	Super Proton Synchrotron
STS	Silicon Tracking System
STS-XYTER	STS, X,Y coordinate, Time and Energy Resolution ASIC
T	
TAB	Tape Automated Bonded
TFC	Timing and Fast Control
Thr2_glb	Absolute Threshold of the FAST discriminator
TID	Total Ionizing Dose
ToF	Time of Flight
TRD	Transition Radiation Detector

U

UrQMD Ultra-relativistic Quantum Molecular Dynamics

V

VRef_P Positive Reference Voltage of the ADC

VRef_N Negative Reference Voltage of the ADC

VRef_T Absolute Threshold for the ADC

VTemp Reference PAD for monitoring the temperature of the ASIC

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- *Readout of a prototype CBM-STS silicon sensor module with STS-XYTERv2 ASIC.* D. Emschermann et al. Photonics Applications in Astronomy, Communications, Industry, and High-Energy Physics Experiments, Wilga 2018; 1080849 (2018) https://doi.org/10.1117/12.2501936

Journals

- *The powering concept of the Silicon Tracking System for CBM@FAIR.* P. Koczon et al. Topical Workshop on Electronics for Particle Physics TWEPP2019. Santiago de Compostela, Spain, 2019; DOI: 10.22323/1.370.0063.
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