

# Status of Picosecond Measurements

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The lack of understanding of the odd behaviour of TOT and signal width raised the question if TDC is inverted or not.

DIRICH threshold program told “TDC inverted”  
... but it was not

Later the TDC was inverted on the command line (Startup.sh)

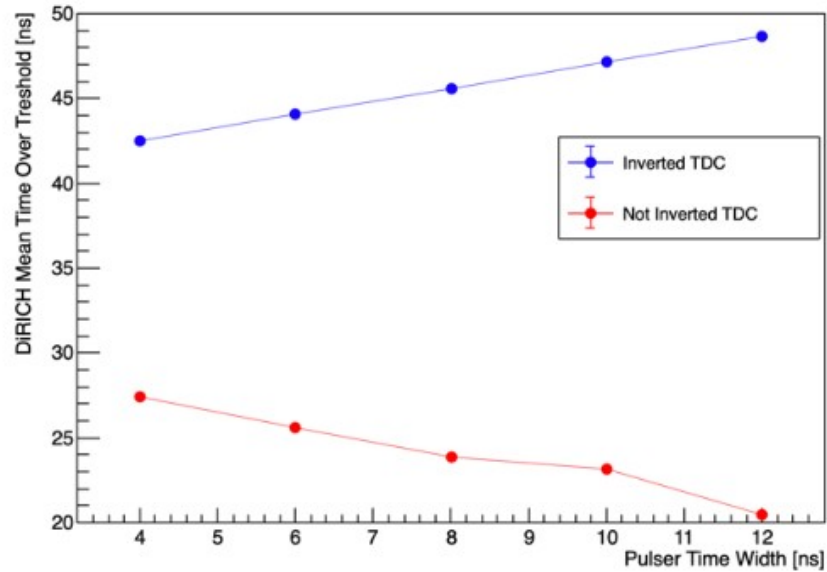


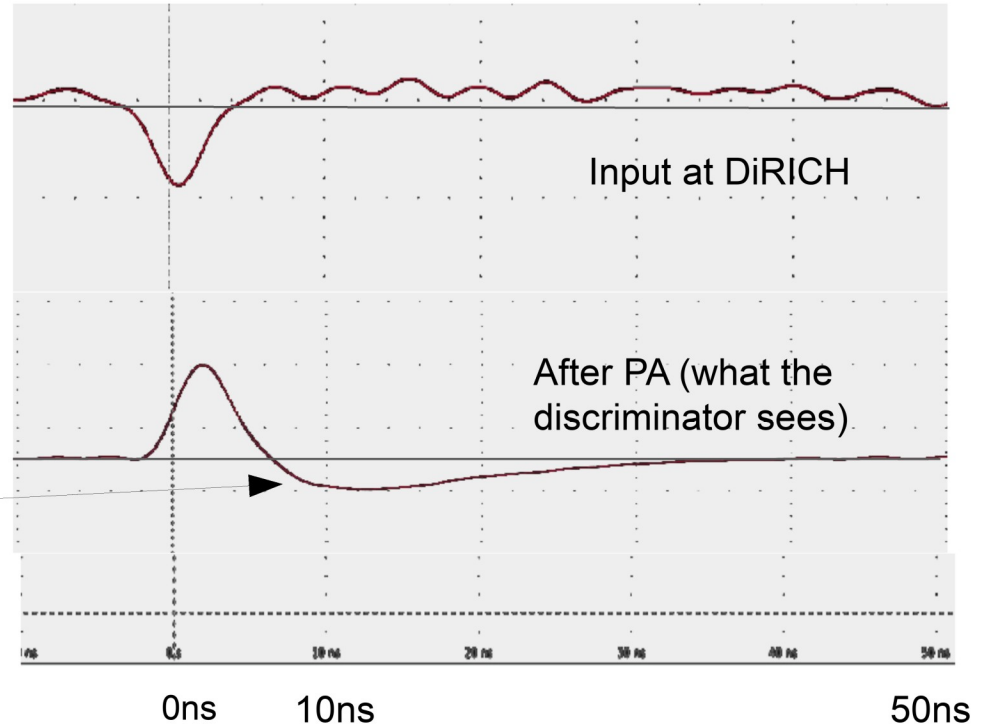
Fig. 7: Plot of measured pulse width ( $ToT$ ) vs pulse generator set width for negative signals and positive threshold. As clearly shown, with inverted TDC for longer signals the measured  $ToT$  increases as expected.

Same plot with red and blue swapped for negative thresholds → but overshoot is measured

## EE-Department, Scope measurement

# TDC Inversion Issue

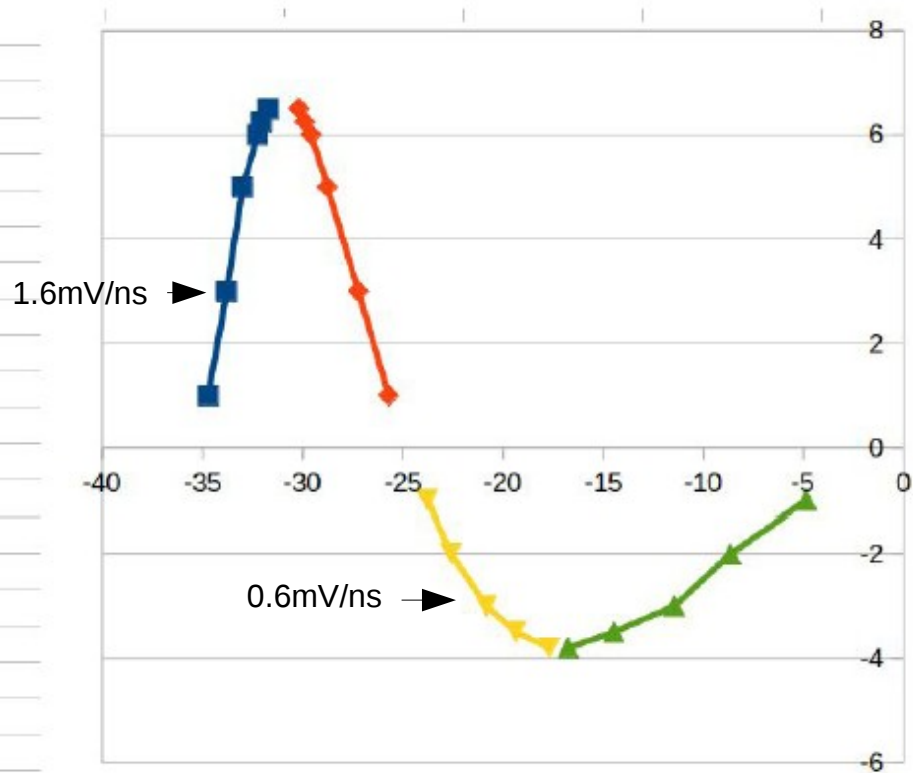
- The HADESthreshscan\_v1 tool incorrectly reported an inverted TDC.
- Due to this, the ToT of the overshoot was being measured instead of the actual peak.



Courtesy: Manuel Reyes

# Scan with pocket pulser

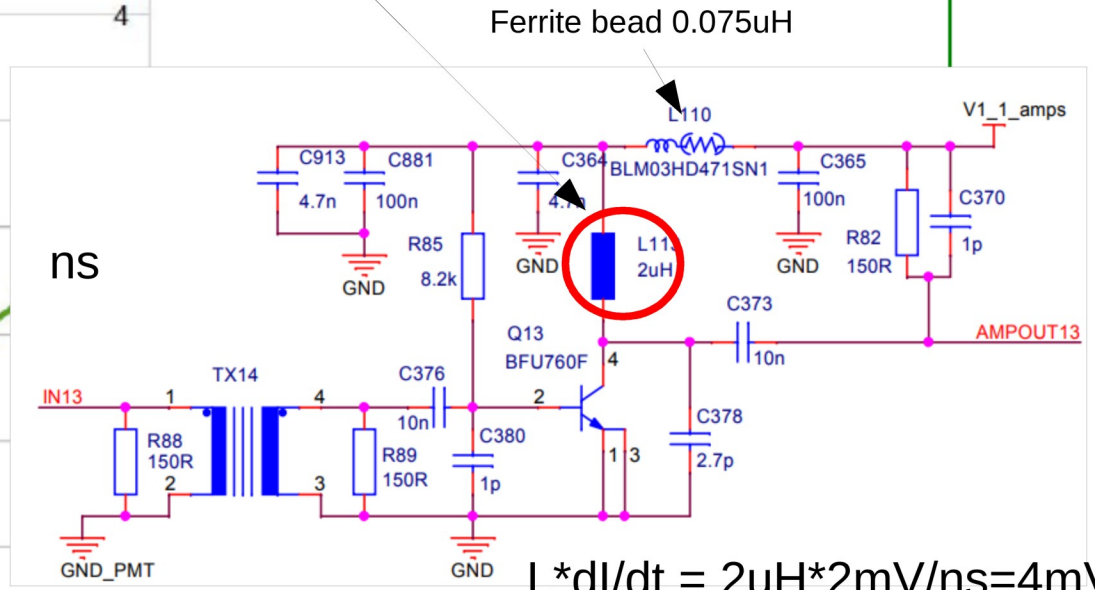
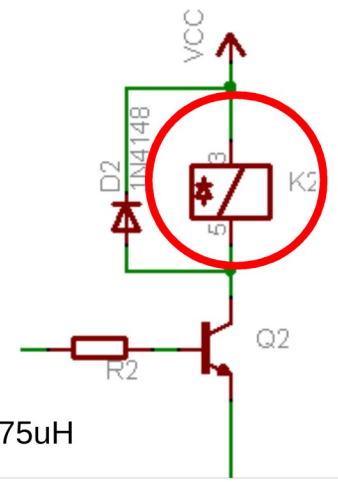
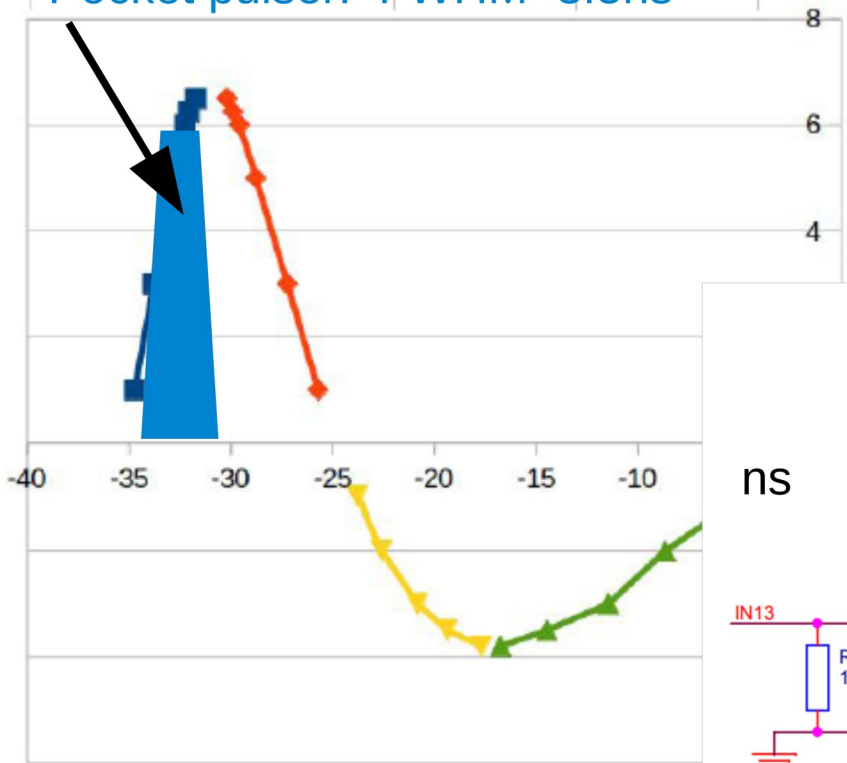
Threshold	Leading	Trailing corrected	Trailing
3	-27.18	-33.76	2.47
1	-34.72	-25.7	10.53
3	-33.79	-27.228	9.002
5	-32.99	-28.761	7.469
6	-32.24	-29.569	6.661
6.25	-32.06	-29.885	6.345
6.5	-31.71	-30.177	6.053
7		0 counts	
-1	-23.78	-4.85	31.38
-2	-22.58	-8.64	27.59
-3	-20.83	-11.44	24.79
-3.5	-19.36	-14.45	21.78
-3.8	-17.69	-16.74	19.49
-5		0 counts	



Overshoot: 2.7 times worse t.-precision

Overshoot produced by inductance in collector branch of amplifier  
 → better defined trailing edge of discriminator signal

Pocket pulser: FWHM=3.5ns

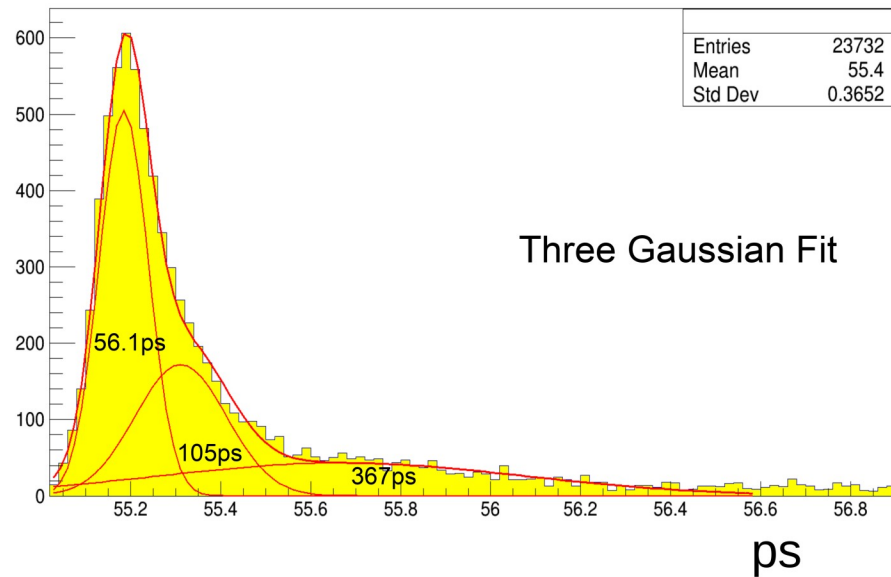
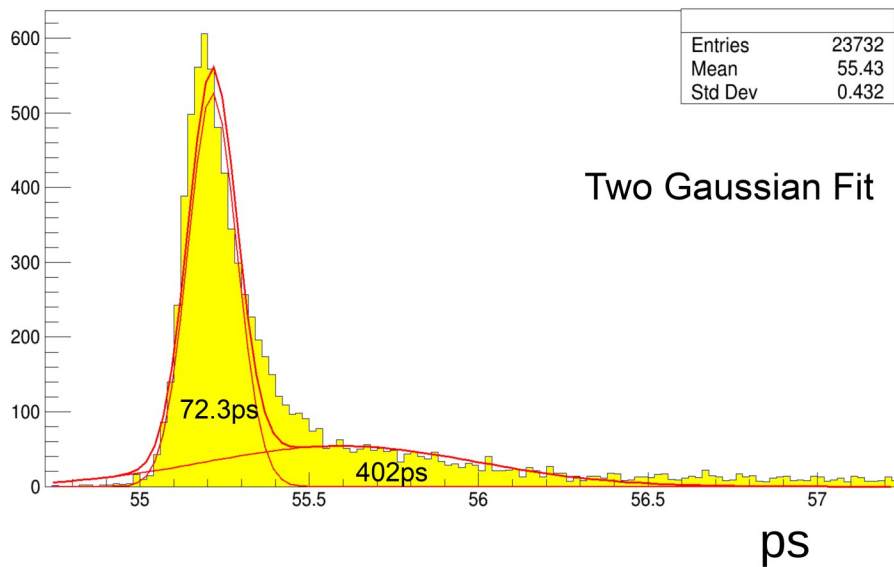


Ferrite bead 0.075uH

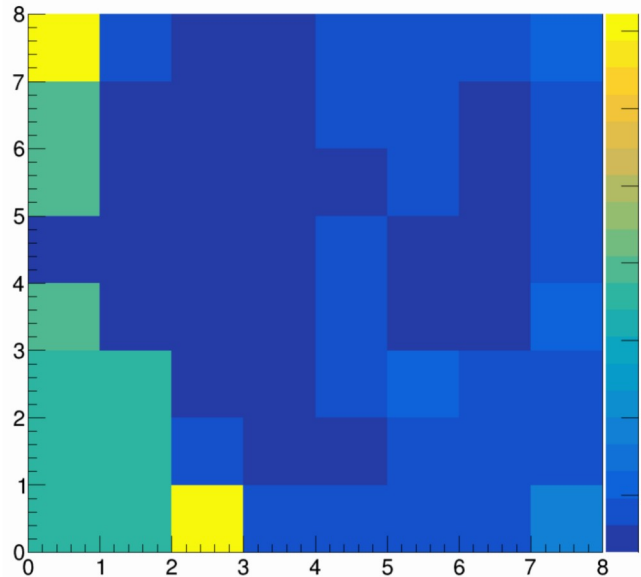
$$L \cdot di/dt = 2\mu\text{H} \cdot 2\text{mV}/\text{ns} = 4\text{mV}$$

# Gaussian Fit

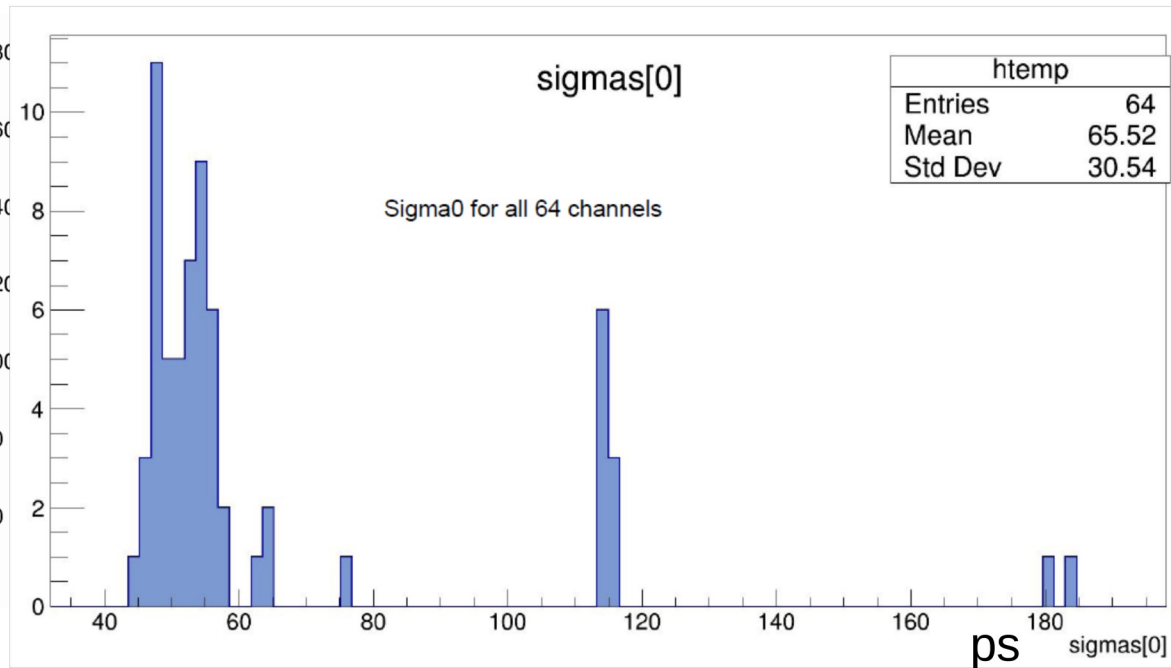
- Detector: Photonis XP85012
- Is there a third Gaussian component?



# Corrected timing precision

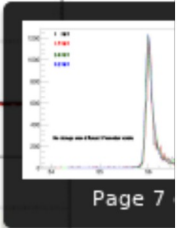
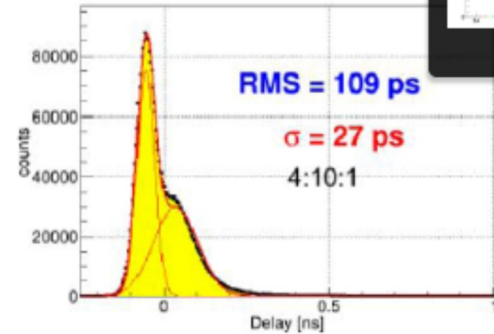
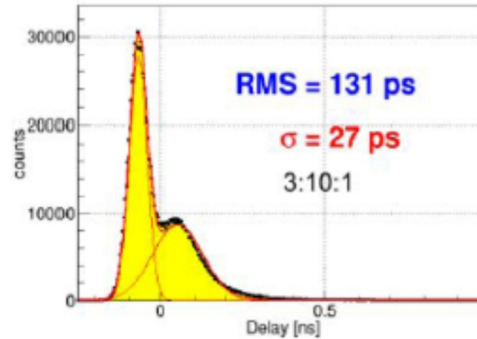
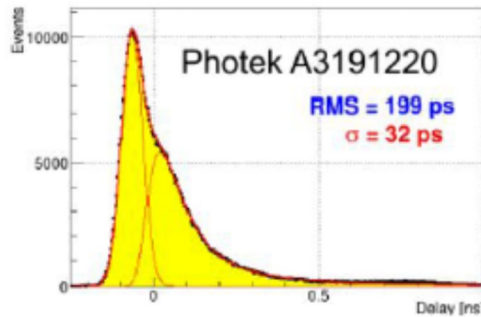
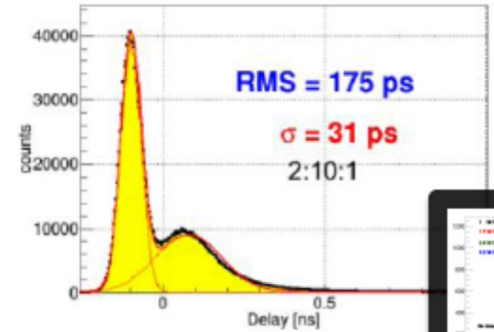
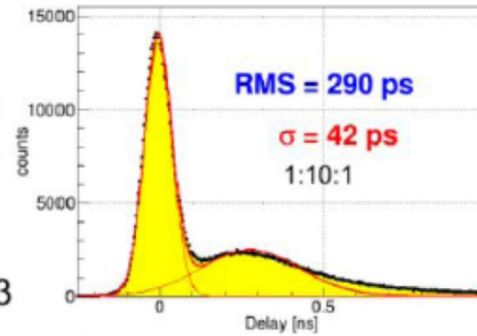


**Spatial representation of the timing precision**  
(Mean: 65.52ps)



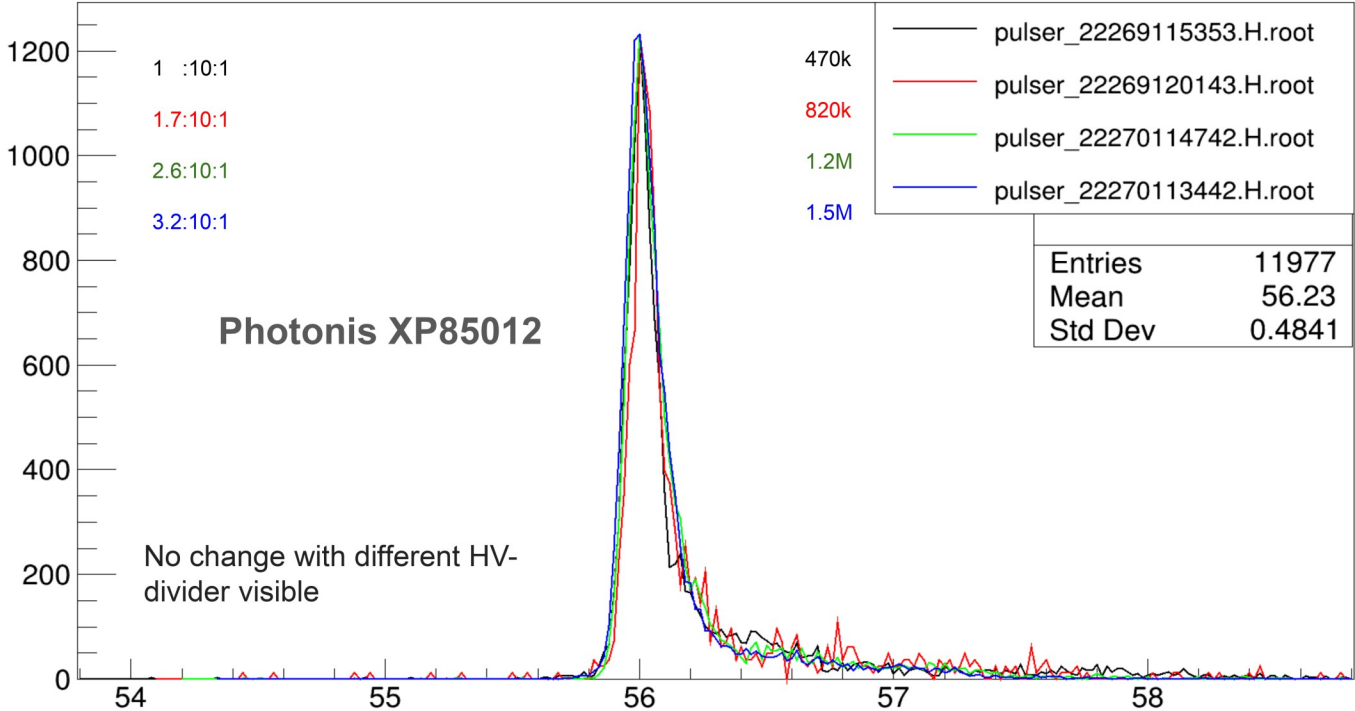
- Higher CE of Photonis comes with a price: more collected recoil electrons → worse time resolution (especially RMS!)
- Solution: increase of HV between PC and MCPin → shift of recoil peak into the main peak → better TTS ( $\sigma$ ) and RMS (-0.5...2 ns)
- RMS timing improves by a factor 2 – 3

Photonis 9002193 with different voltage dividers, from 1:10:1 (PC-MCPin:MCPin-MCPout:MCPout-Anode) to 4:10:1





# Modifying HV-divider ratio



Bug of DIRICH threshold program tells about a inverted DIRICH, while it is not inverted.  
(Inverting has to be done within the startup script)

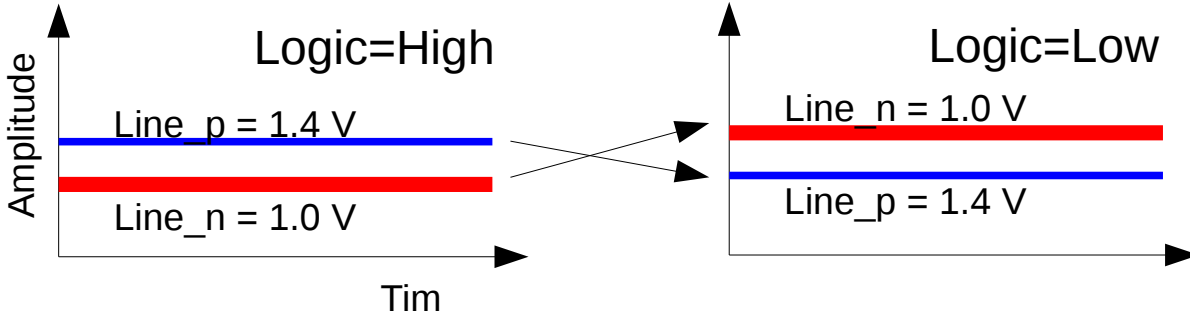
We now measure consistent timing precision compared to the results in Erlangen.

The old PHOTONIS tubes (XP850012) show no reduction of the recoiling photoelectrons with higher voltage between PC and CP.

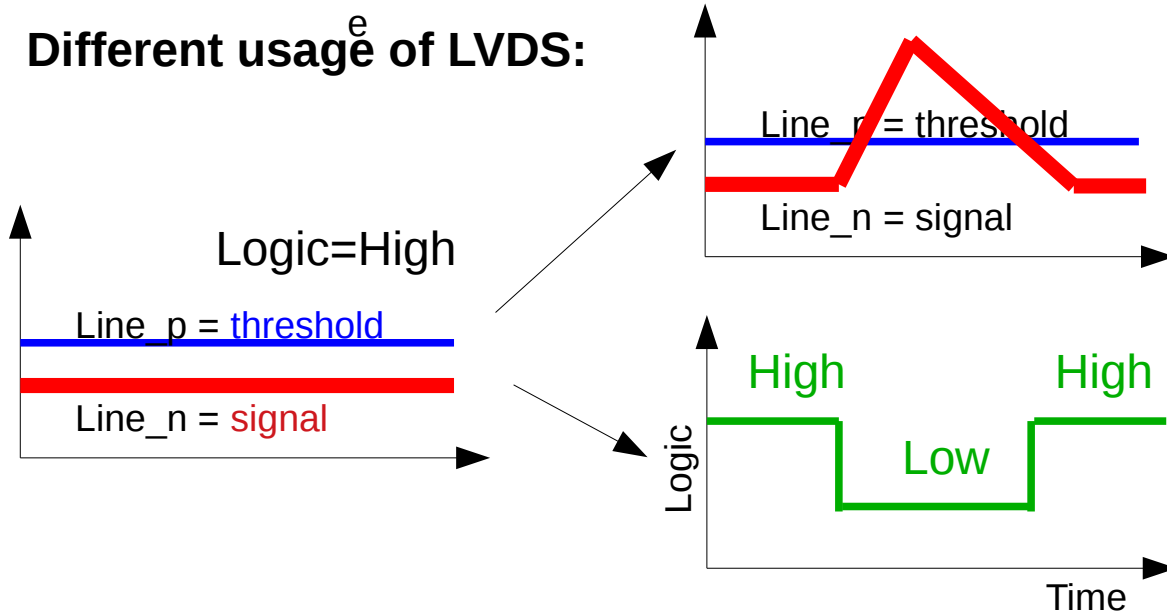
Backup slides

# Discriminator with LVDS

## Low Voltage Differential Signaling (LVDS)



## Different usage of LVDS:

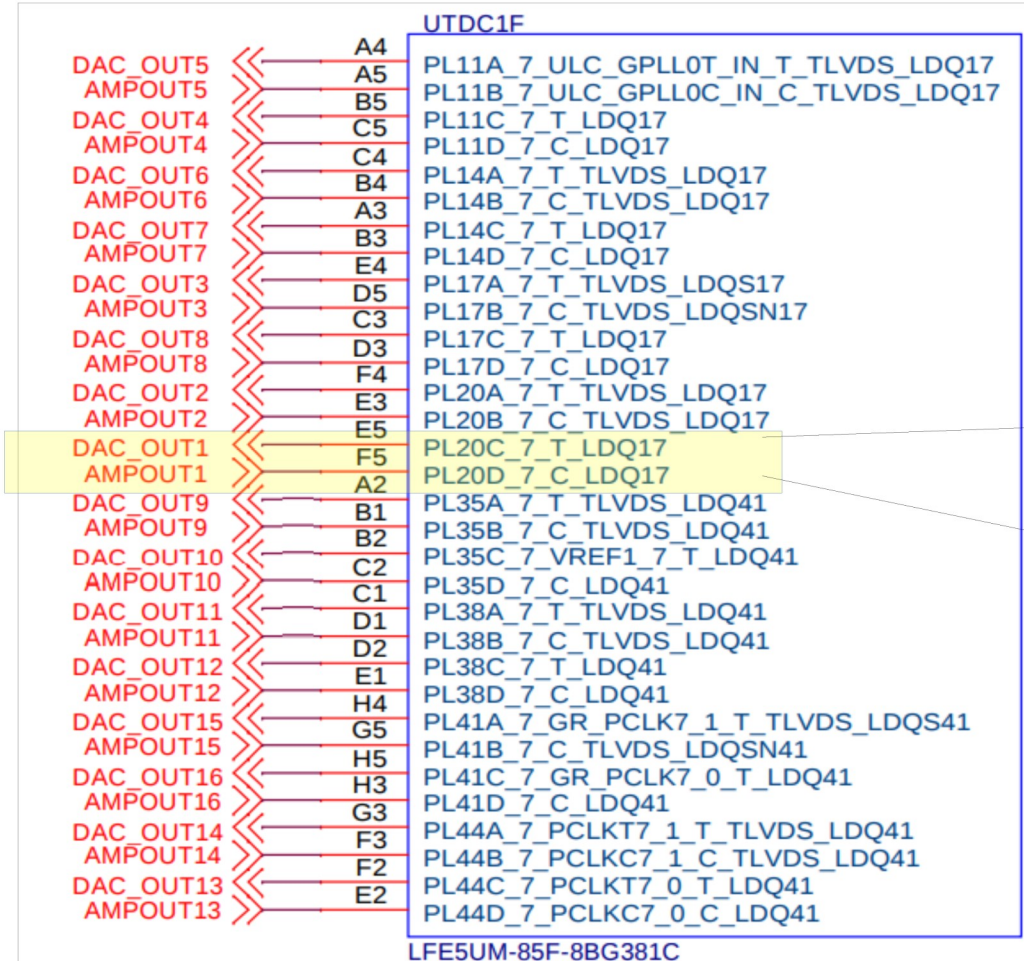


## FPGA (DiRICH2)

UTDCIF	
DAC_OUT5	A4
AMP_OUT5	A5
DAC_OUT4	B5
AMP_OUT4	C5
DAC_OUT6	B4
AMP_OUT6	A3
DAC_OUT7	B3
AMP_OUT7	E4
DAC_OUT3	D5
AMP_OUT3	C3
DAC_OUT8	D3
AMP_OUT8	F4
DAC_OUT2	E3
AMP_OUT2	E5
DAC_OUT1	F5
AMP_OUT1	F5
DAC_OUT9	A2
AMP_OUT9	B2
DAC_OUT10	C2
AMP_OUT10	C1
DAC_OUT11	D2
AMP_OUT11	D1
DAC_OUT12	E2
AMP_OUT12	H4
DAC_OUT15	G5
AMP_OUT15	H5
DAC_OUT16	H3
AMP_OUT16	H3
DAC_OUT14	G3
AMP_OUT14	F2
DAC_OUT13	F2
AMP_OUT13	E2

```
PL11A_7_ULC_GPLL0T_IN_T_TLVDS_LDQ17
PL11B_7_ULC_GPLL0C_IN_C_TLVDS_LDQ17
PL11C_7_T_LDQ17
PL11D_7_C_LDQ17
PL14A_7_T_TLVDS_LDQ17
PL14B_7_C_TLVDS_LDQ17
PL14C_7_T_LDQ17
PL14D_7_C_LDQ17
PL17A_7_T_TLVDS_LDQS17
PL17B_7_C_TLVDS_LDQS17
PL17C_7_T_LDQ17
PL17D_7_C_LDQ17
PL20A_7_T_TLVDS_LDQ17
PL20B_7_C_TLVDS_LDQ17
PL20C_7_T_LDQ17
PL20D_7_C_LDQ17
PL35A_7_T_TLVDS_LDQ41
PL35B_7_C_TLVDS_LDQ41
PL35C_7_VREF1_7_T_LDQ41
PL35D_7_C_LDQ41
PL38A_7_T_TLVDS_LDQ41
PL38B_7_C_TLVDS_LDQ41
PL38C_7_T_LDQ41
PL38D_7_C_LDQ41
PL41A_7_GR_PCLK7_1_T_TLVDS_LDQS41
PL41B_7_C_TLVDS_LDQS41
PL41C_7_GR_PCLK7_0_T_LDQ41
PL41D_7_C_LDQ41
PL44A_7_PCLKT7_1_T_TLVDS_LDQ41
PL44B_7_PCLKC7_1_C_TLVDS_LDQ41
PL44C_7_PCLKT7_0_T_LDQ41
PL44D_7_PCLKC7_0_C_LDQ41
```

LFESUM-85F-8BG381C

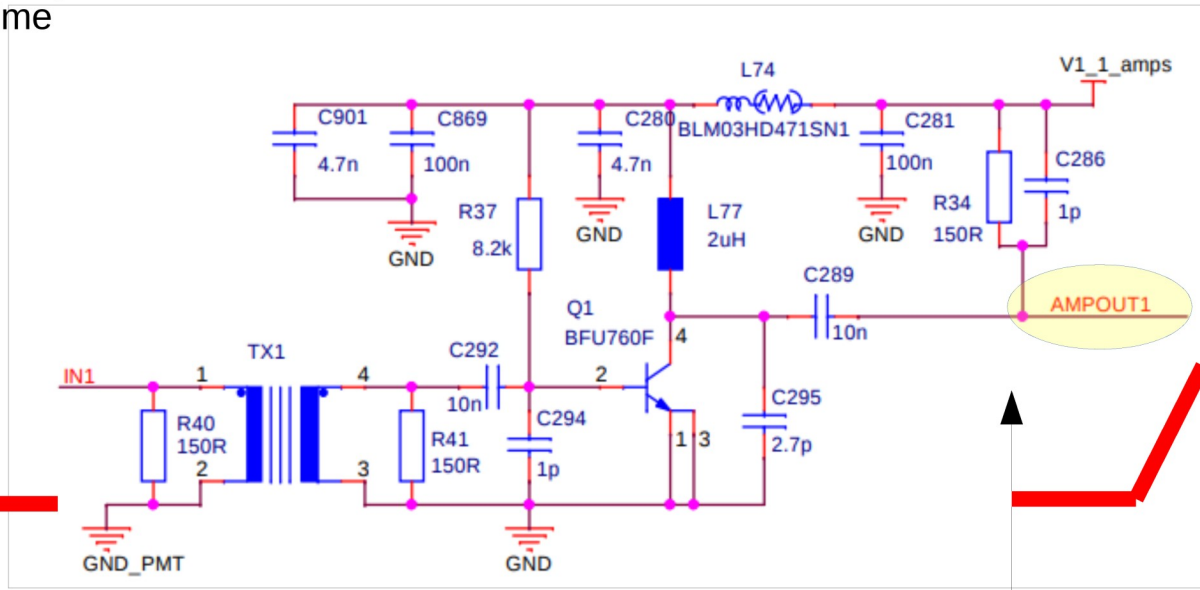
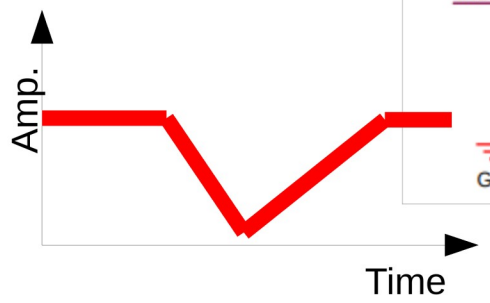
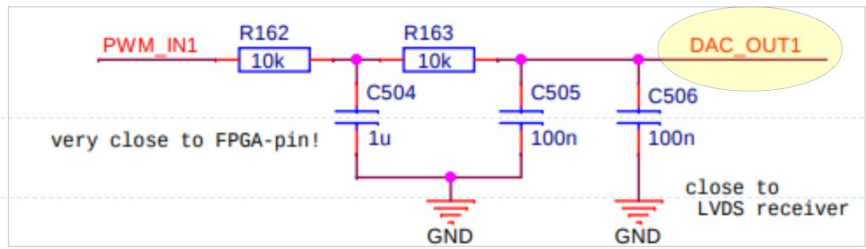
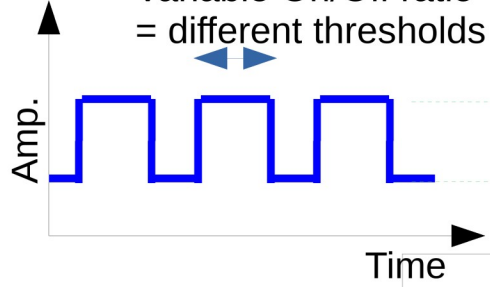


FPGA

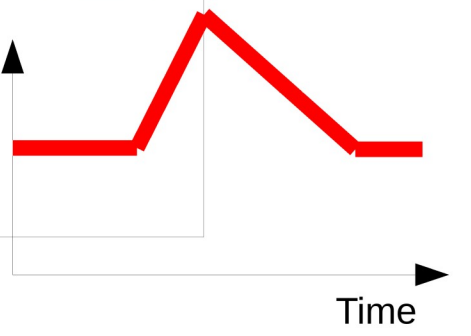
“T” for threshold

“C” for channel

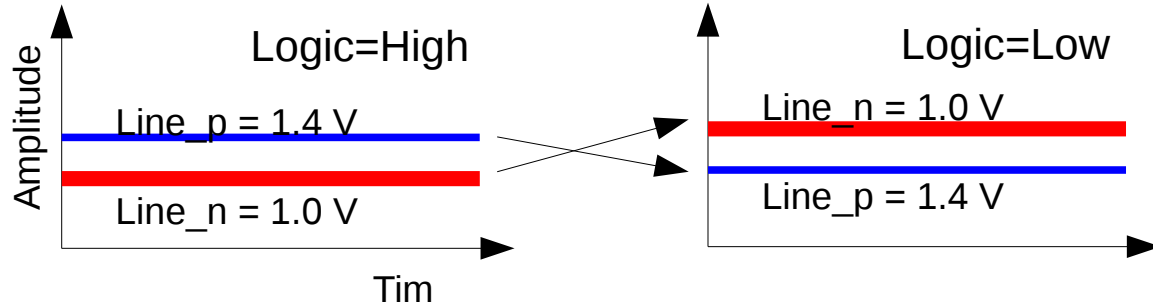
Variable On/Off ratio  
= different thresholds



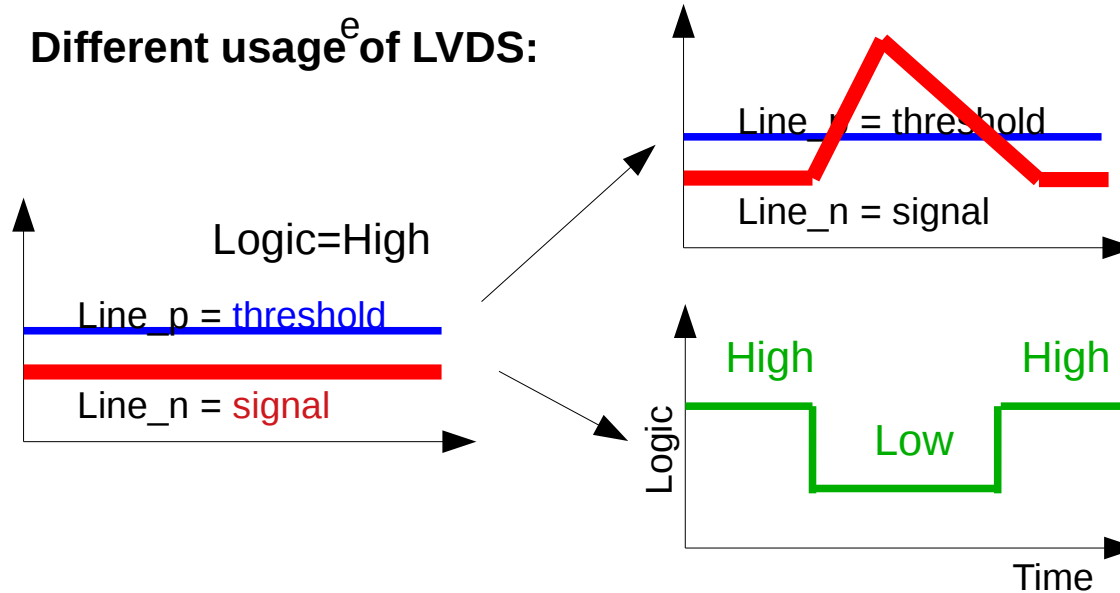
Common emitter inverts signal



## Low Voltage Differential Signaling (LVDS)



## Different usage<sup>e</sup> of LVDS:



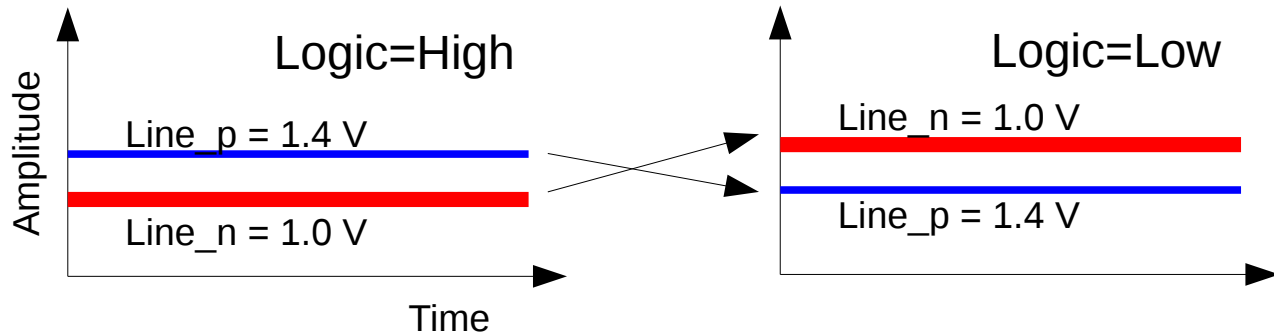
## FPGA (DiRICH2)

UTDC1F	
DAC_OUT5	A4
AMP_OUT5	A5
DAC_OUT4	B5
AMP_OUT4	C5
DAC_OUT6	C4
AMP_OUT6	B4
DAC_OUT7	A3
AMP_OUT7	E4
DAC_OUT3	D5
AMP_OUT3	C3
DAC_OUT8	D3
AMP_OUT8	F4
DAC_OUT2	E3
AMP_OUT2	E5
DAC_OUT1	F5
AMP_OUT1	A2
DAC_OUT9	B1
AMP_OUT9	B2
DAC_OUT10	C2
AMP_OUT10	C1
DAC_OUT11	D1
AMP_OUT11	D2
DAC_OUT12	E1
AMP_OUT12	H4
DAC_OUT15	G5
AMP_OUT15	H5
DAC_OUT16	H3
AMP_OUT16	G3
DAC_OUT14	F3
AMP_OUT14	F2
DAC_OUT13	E2
AMP_OUT13	E2

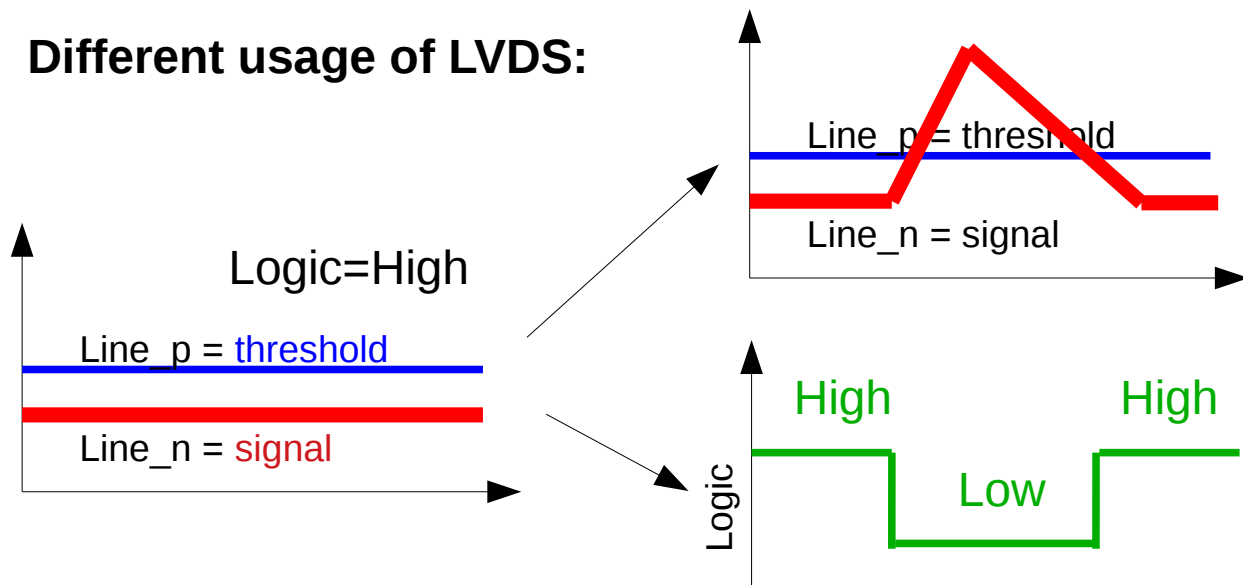
  

PL11A_7_ULC_GPLL0T_IN_T_TLVDS_LDQ17
PL11B_7_ULC_GPLL0C_IN_C_TLVDS_LDQ17
PL11C_7_T_LDQ17
PL11D_7_C_LDQ17
PL14A_7_T_TLVDS_LDQ17
PL14B_7_C_TLVDS_LDQ17
PL14C_7_T_LDQ17
PL14D_7_C_LDQ17
PL17A_7_T_TLVDS_LDQS17
PL17B_7_C_TLVDS_LDQSN17
PL17C_7_T_LDQ17
PL17D_7_C_LDQ17
PL20A_7_T_TLVDS_LDQ17
PL20B_7_C_TLVDS_LDQ17
PL20C_7_T_LDQ17
PL20D_7_C_LDQ17
PL35A_7_T_TLVDS_LDQ41
PL35B_7_C_TLVDS_LDQ41
PL35C_7_VREF1_7_T_LDQ41
PL35D_7_C_LDQ41
PL38A_7_T_TLVDS_LDQ41
PL38B_7_C_TLVDS_LDQ41
PL38C_7_T_LDQ41
PL38D_7_C_LDQ41
PL41A_7_GR_PCLK7_1_T_TLVDS_LDQS41
PL41B_7_C_TLVDS_LDQSN41
PL41C_7_GR_PCLK7_0_T_LDQ41
PL41D_7_C_LDQ41
PL44A_7_PCLK7_1_T_TLVDS_LDQ41
PL44B_7_PCLK7_1_C_TLVDS_LDQ41
PL44C_7_PCLK7_0_T_LDQ41
PL44D_7_PCLK7_0_C_LDQ41

## Low Voltage Differential Signaling (LVDS)



## Different usage of LVDS:



## FPGA (Di

Signal	Pin	Function
UTDC1F		
DAC_OUT5	A4	PL11A_7_ULC_GPLL0T_IN
AMPOUT5	A5	PL11B_7_ULC_GPLL0C_IN
DAC_OUT4	B5	PL11C_7_T_LDQ17
AMPOUT4	C5	PL11D_7_C_LDQ17
DAC_OUT6	B4	PL14A_7_T_TLVDS_LDQ17
AMPOUT6	C4	PL14B_7_C_TLVDS_LDQ17
DAC_OUT7	A3	PL14C_7_T_LDQ17
AMPOUT7	B3	PL14D_7_C_LDQ17
DAC_OUT3	D5	PL17A_7_T_TLVDS_LDQS
AMPOUT3	C3	PL17B_7_C_TLVDS_LDQS
DAC_OUT8	D3	PL17C_7_T_LDQ17
AMPOUT8	F4	PL17D_7_C_LDQ17
DAC_OUT2	E3	PL20A_7_T_TLVDS_LDQ17
AMPOUT2	E5	PL20B_7_C_TLVDS_LDQ17
DAC_OUT1	F5	PL20C_7_T_LDQ17
AMPOUT1	F3	PL20D_7_C_LDQ17
DAC_OUT9	A2	PL35A_7_T_TLVDS_LDQ41
AMPOUT9	B1	PL35B_7_C_TLVDS_LDQ41
DAC_OUT10	B2	PL35C_7_VREF1_7_T_LDC
AMPOUT10	C1	PL35D_7_C_LDQ41
DAC_OUT11	D1	PL38A_7_T_TLVDS_LDQ41
AMPOUT11	D2	PL38B_7_C_TLVDS_LDQ41
DAC_OUT12	E1	PL38C_7_T_LDQ41
AMPOUT12	E2	PL38D_7_C_LDQ41
DAC_OUT15	H4	PL41A_7_GR_PCLK7_1_T
AMPOUT15	G5	PL41B_7_C_TLVDS_LDQS
DAC_OUT16	H5	PL41C_7_GR_PCLK7_0_T
AMPOUT16	H3	PL41D_7_C_LDQ41
DAC_OUT14	F3	PL44A_7_PCLKT7_1_T
AMPOUT14	F2	PL44B_7_PCLKT7_1_C
DAC_OUT13	E2	PL44C_7_PCLKT7_0_T
AMPOUT13	E1	PL44D_7_PCLKT7_0_C