Status of Picosecond Measurements

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The lack of understanding of the odd behaviour of TOT and signal width raised the question if TDC is inverted or not.

DIRICH threshold program told “TDC inverted”
… but it was not

Later the TDC was inverted on the command line (Startup.sh)

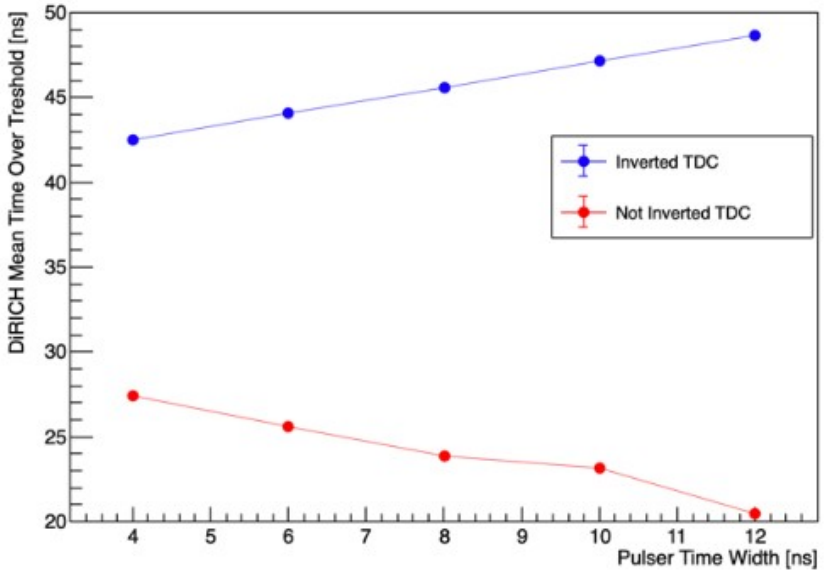
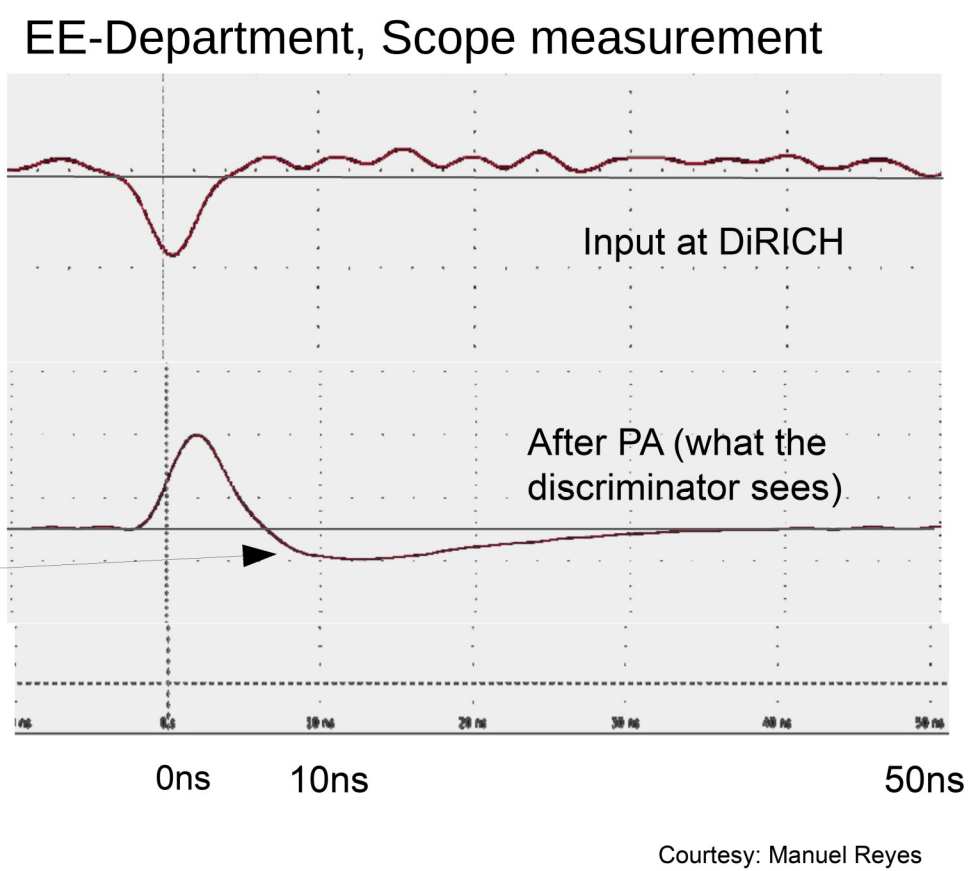


Fig. 7: *Plot of measured pulse width (ToT) vs pulse generator set width for negative signals and positive threshold. As clearly shown, with inverted TDC for longer signals the measured ToT increases as expected.*

Same plot with red and blue swapped for negative thresholds → but overshoot is measured

TDC Inversion Issue

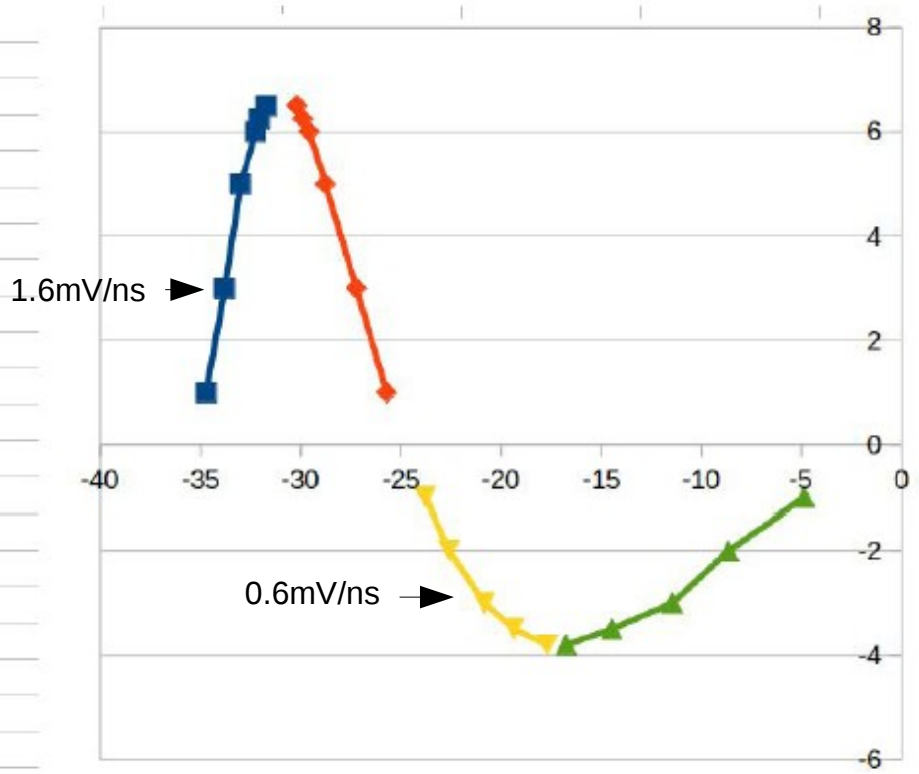
- The HADESthreshscan_v1 tool incorrectly reported an inverted TDC.
- Due to this, the ToT of the overshoot was being measured instead of the actual peak.



Courtesy: Manuel Reyes

Scan with pocket pulser

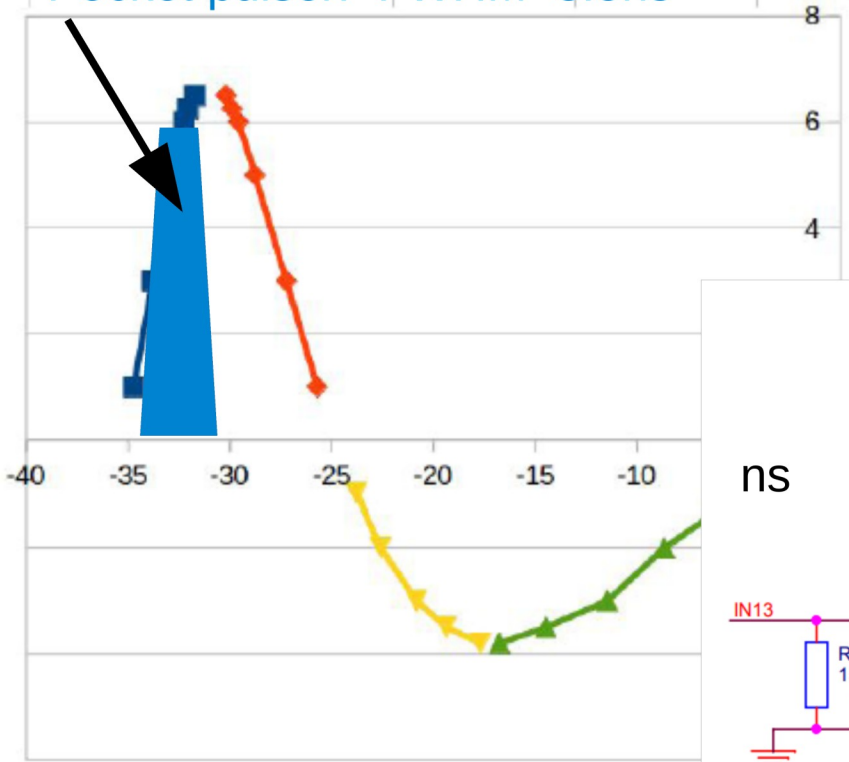
Threshold	Leading	Trailing corrected		Trailing
3	-27.18	-33.76	ninv, +i	2.47
1	-34.72	-25.7		10.53
3	-33.79	-27.228		9.002
5	-32.99	-28.761		7.469
6	-32.24	-29.569		6.661
6.25	-32.06	-29.885		6.345
6.5	-31.71	-30.177		6.053
7			0 counts	
-1	-23.78	-4.85		31.38
-2	-22.58	-8.64		27.59
-3	-20.83	-11.44		24.79
-3.5	-19.36	-14.45		21.78
-3.8	-17.69	-16.74		19.49
-5			0 counts	

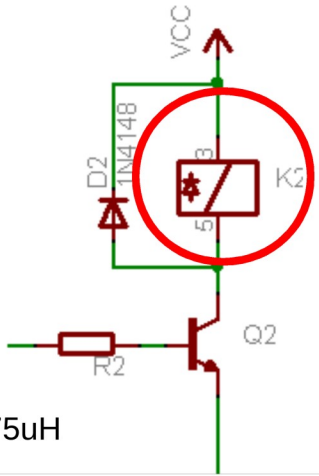


Overshoot: 2.7 times worse t.-precision

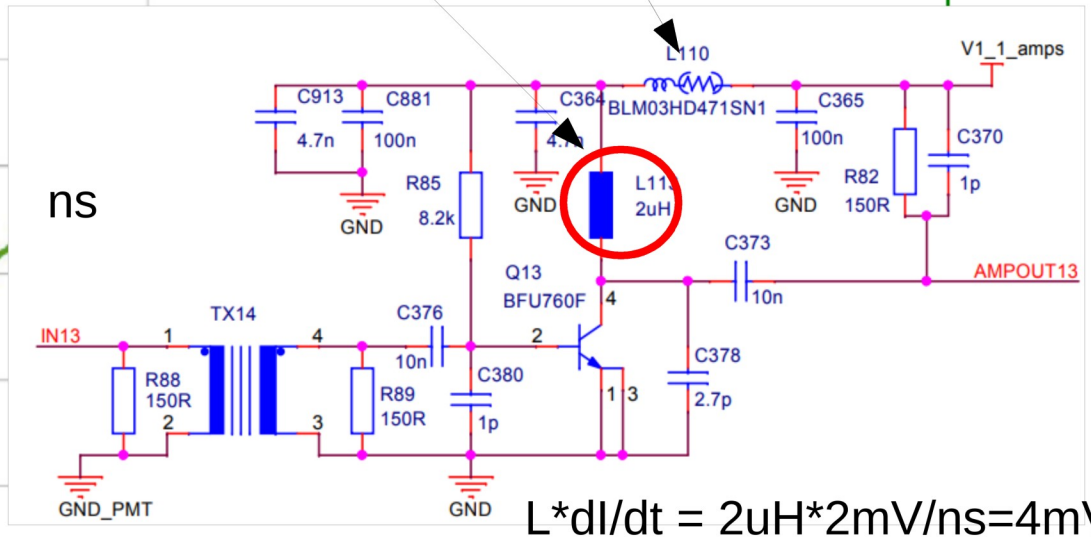
Overshoot produced by inductance in collector branch of amplifier
→ better defined trailing edge of discriminator signal

Pocket pulser: FWHM=3.5ns





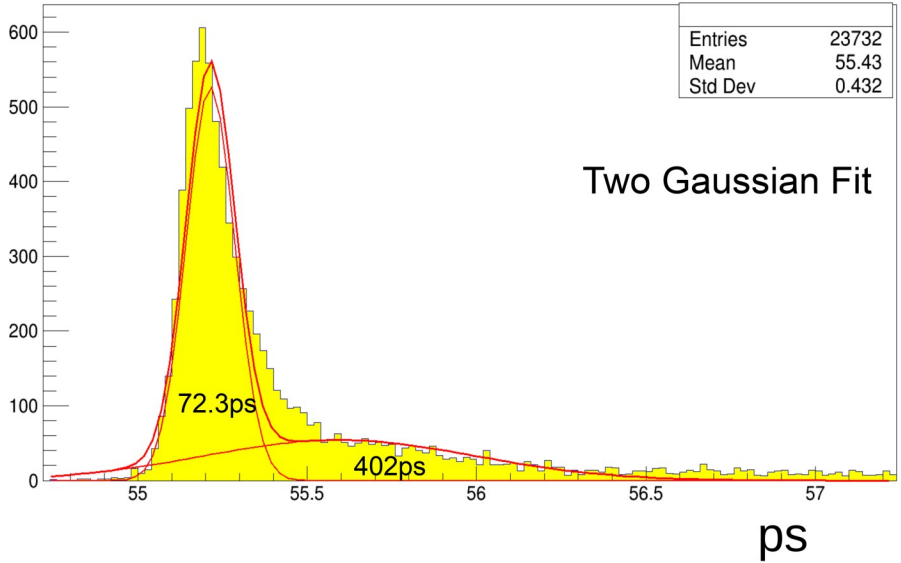
Ferrite bead 0.075uH

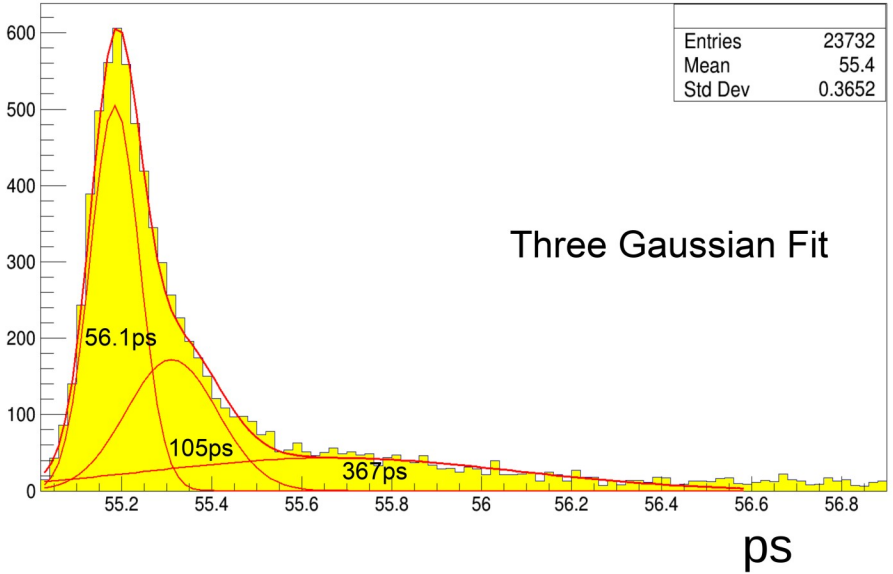


L*dI/dt = 2uH*2mV/ns=4mV

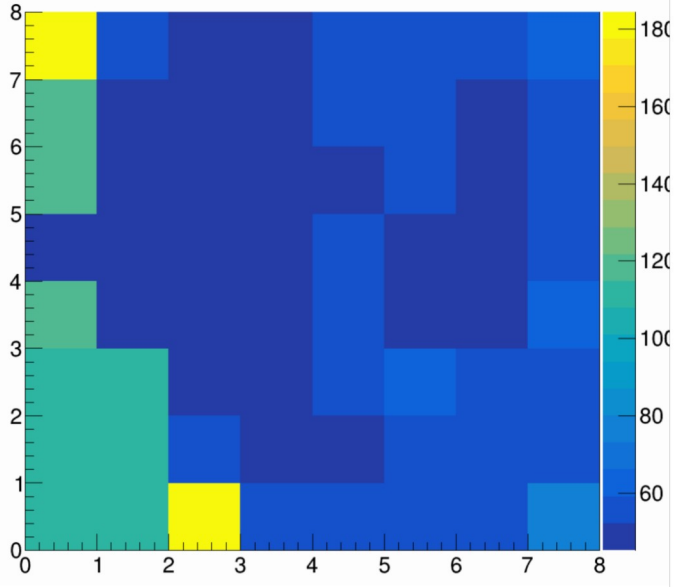
Gaussian Fit

- **Detector: Photonis XP85012**
- **Is there a third Gaussian component?**

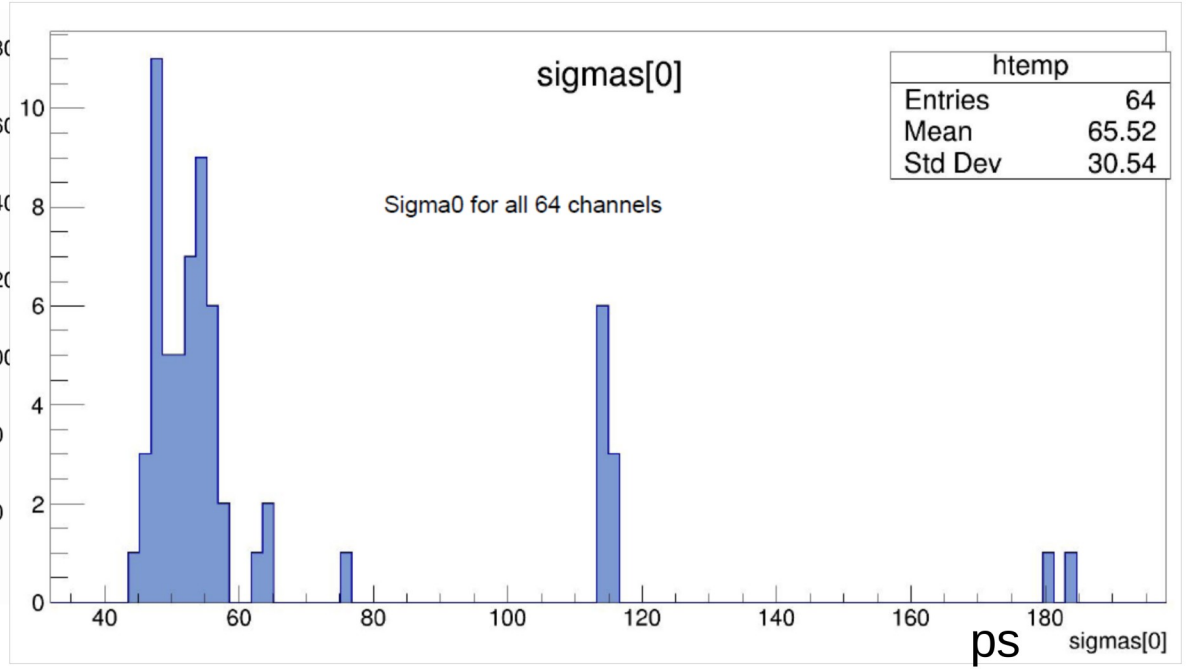




Corrected timing precision



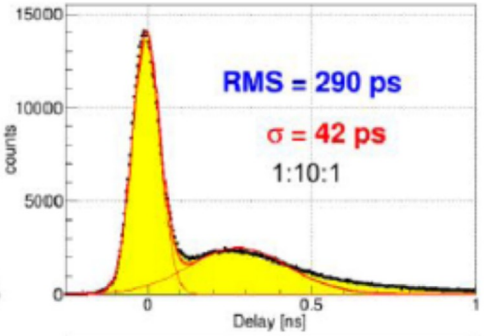
Spatial representation of the timing precision
(Mean: 65.52ps)

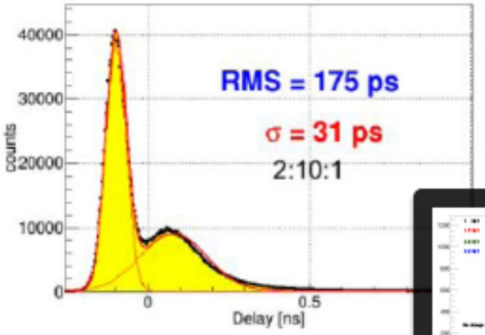


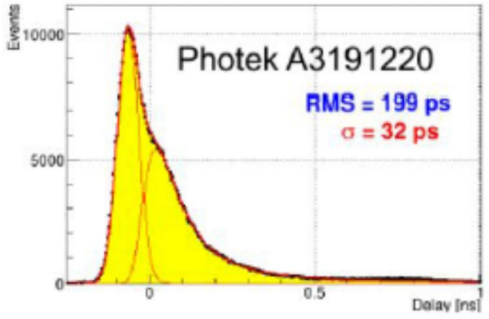
Time resolution

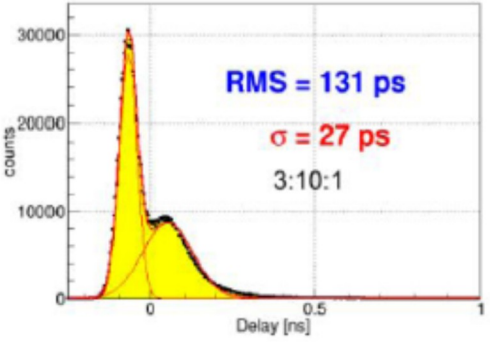
- Higher CE of Photonis comes with a price: more collected recoil electrons → worse time resolution (especially RMS!)
- Solution: increase of HV between PC and MCPin → shift of recoil peak into the main peak → better TTS (σ) and RMS (-0.5…2 ns)
- RMS timing improves by a factor 2 – 3

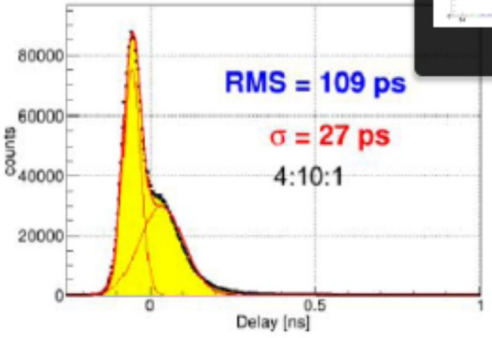
Photonis 9002193 with different voltage dividers, from 1:10:1 (PC-MCPin:MCPin-MCPout:MCPout-Anode) to 4:10:1

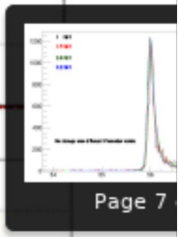












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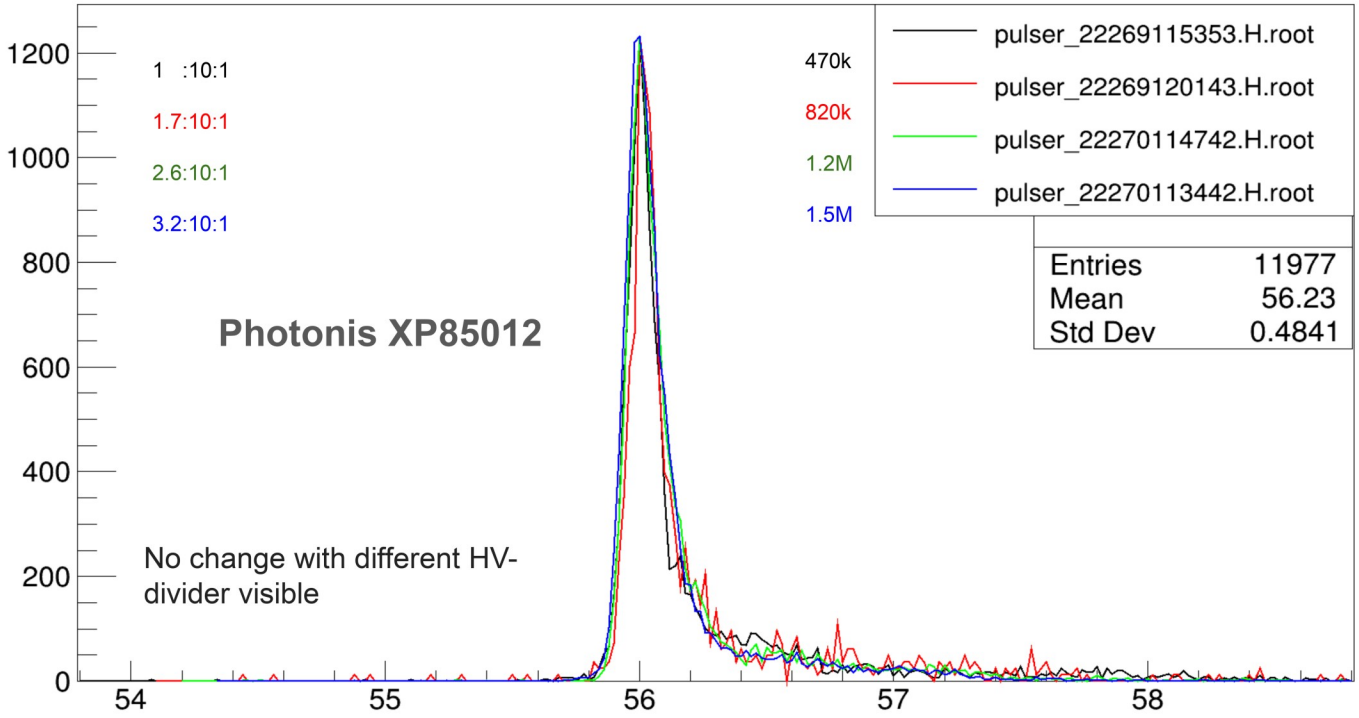
XP85112

Results from Erlangen

Modifying HV-divider ratio



Bug of DIRICH threshold program tells about a inverted DIRICH, while it is not inverted.
(Inverting has to be done within the startup script)

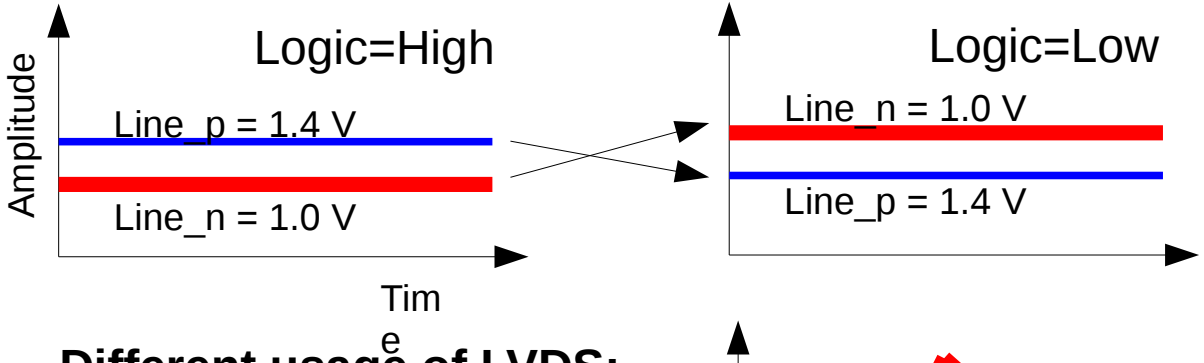
We now measure consistent timing precision
compared to the results in Erlangen.

The old PHOTONIS tubes (XP850012) show no reduction of the recoiling photoelectrons with higher voltage between PC and CP.

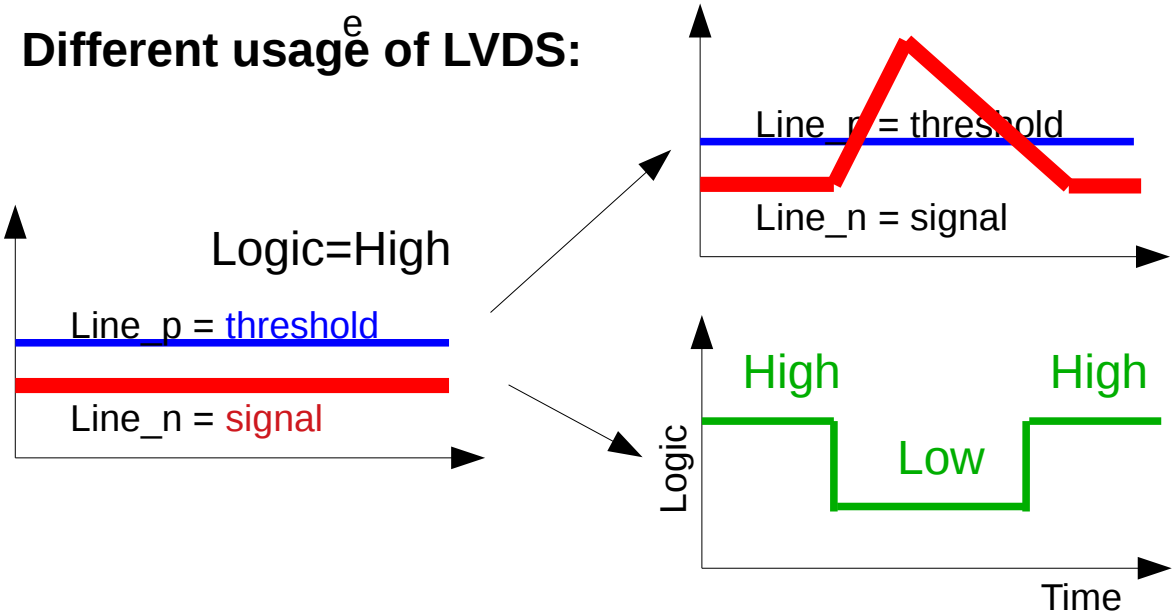
Backup slides

Discriminator with LVDS

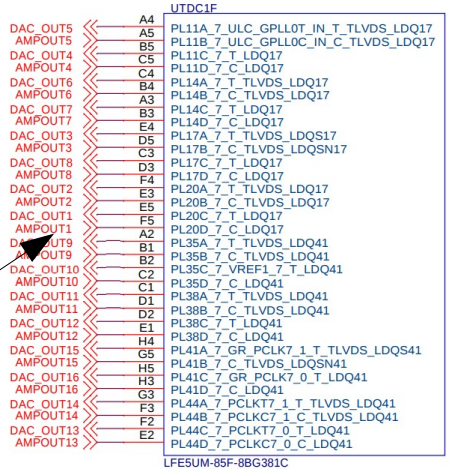
Low Voltage Differential Signaling (LVDS)

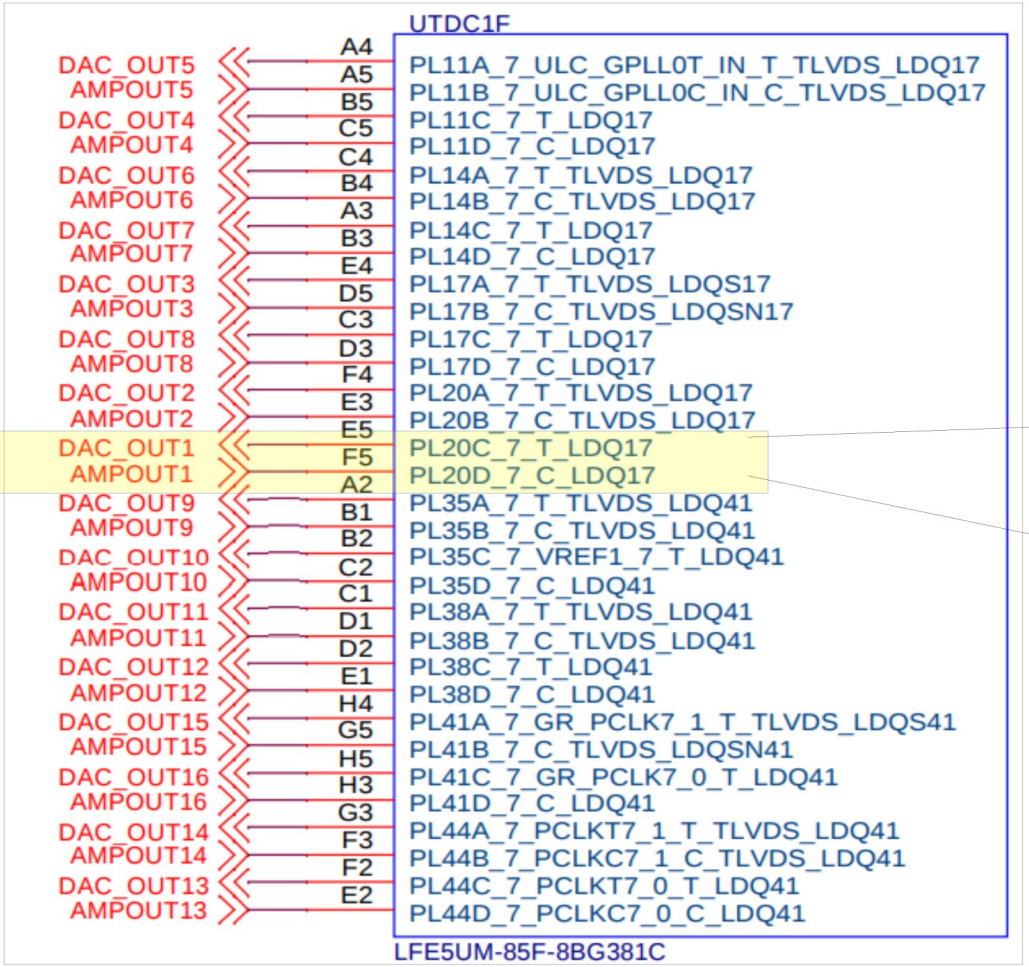


Different usage of LVDS:



FPGA (DiRICH2)



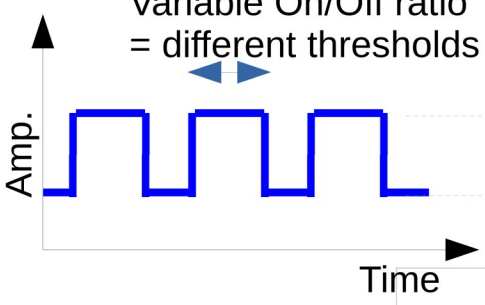


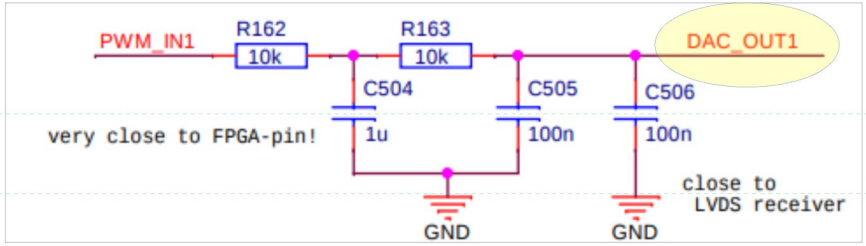
FPGA

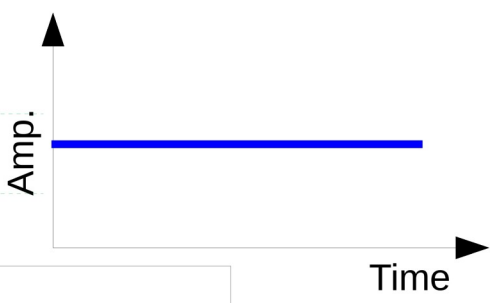
“T” for threshold

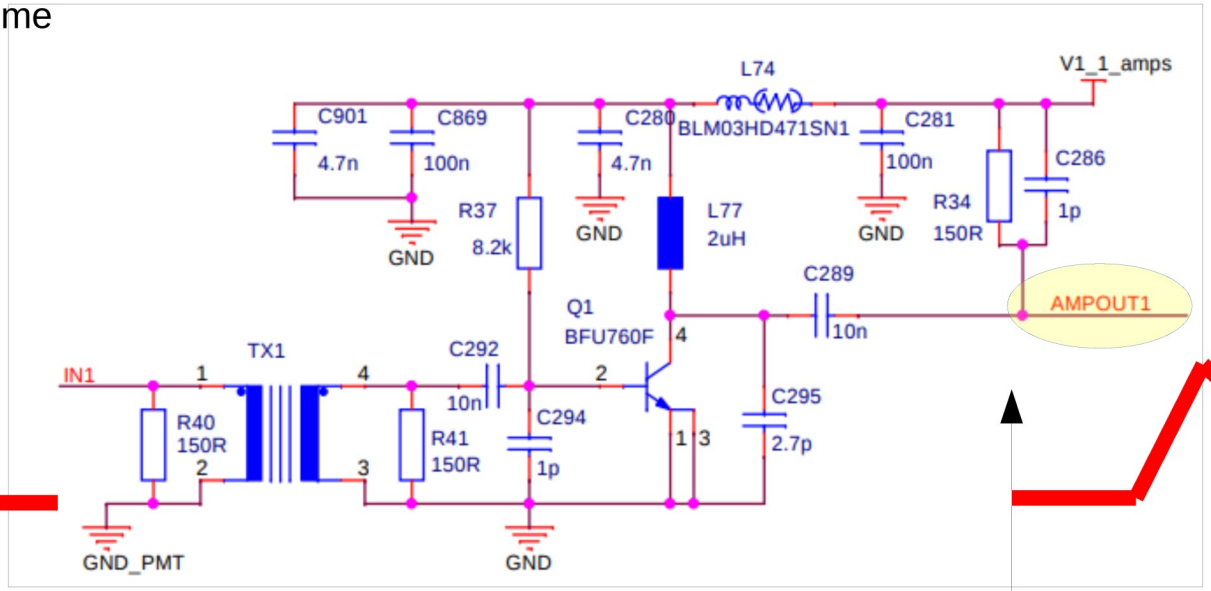
“C” for channel

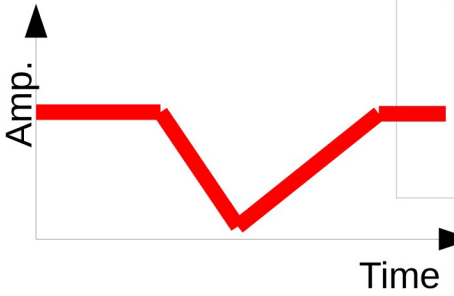
Variable On/Off ratio
= different thresholds



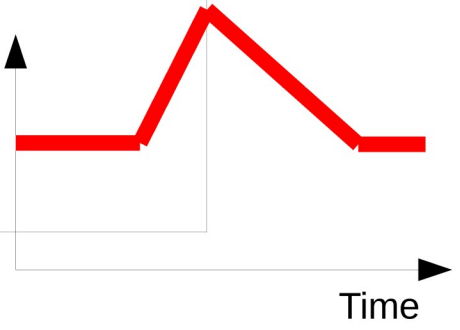






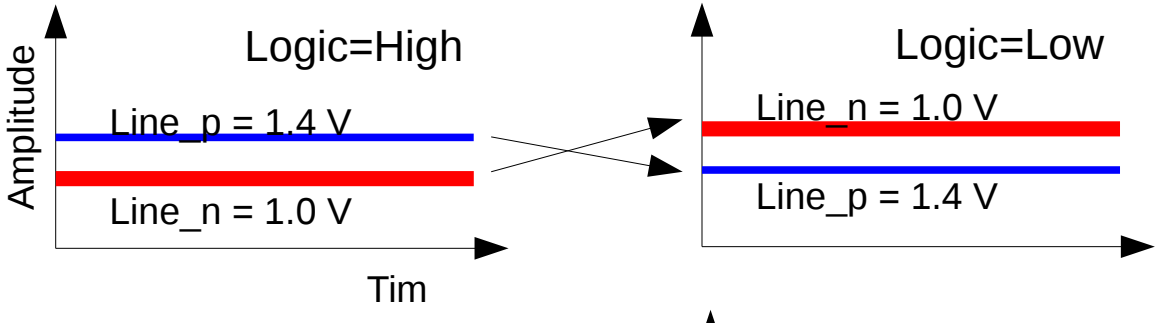


Common emitter inverts signal

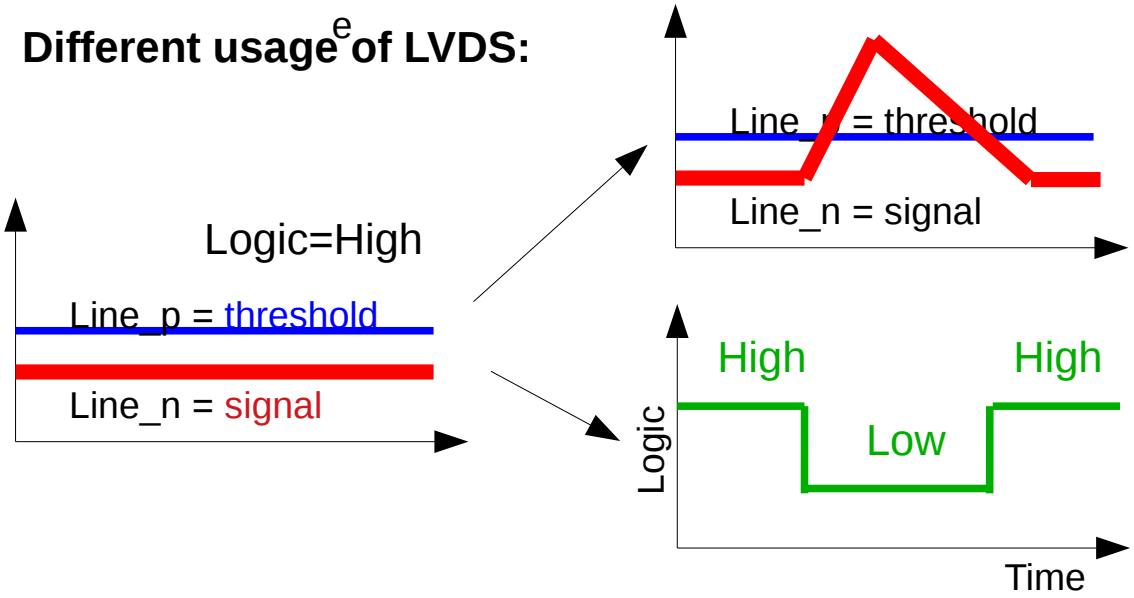


Discriminator with LVDS

Low Voltage Differential Signaling (LVDS)



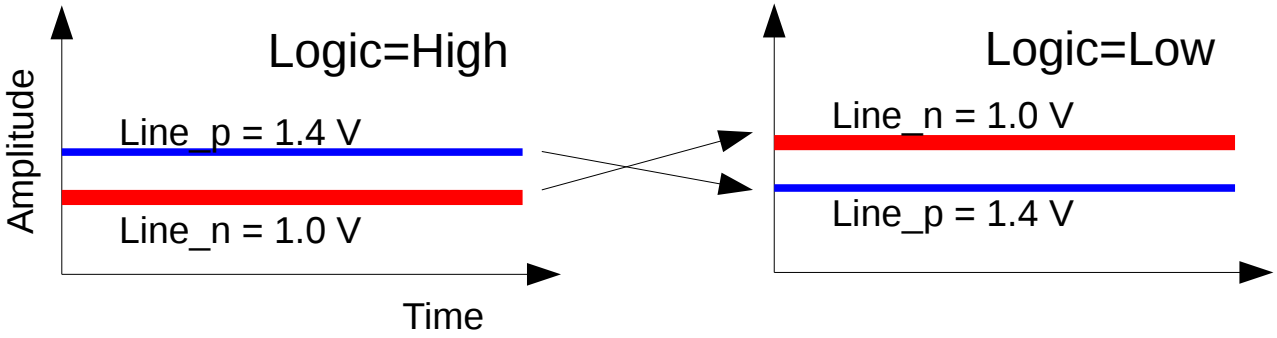
Different usage of LVDS:



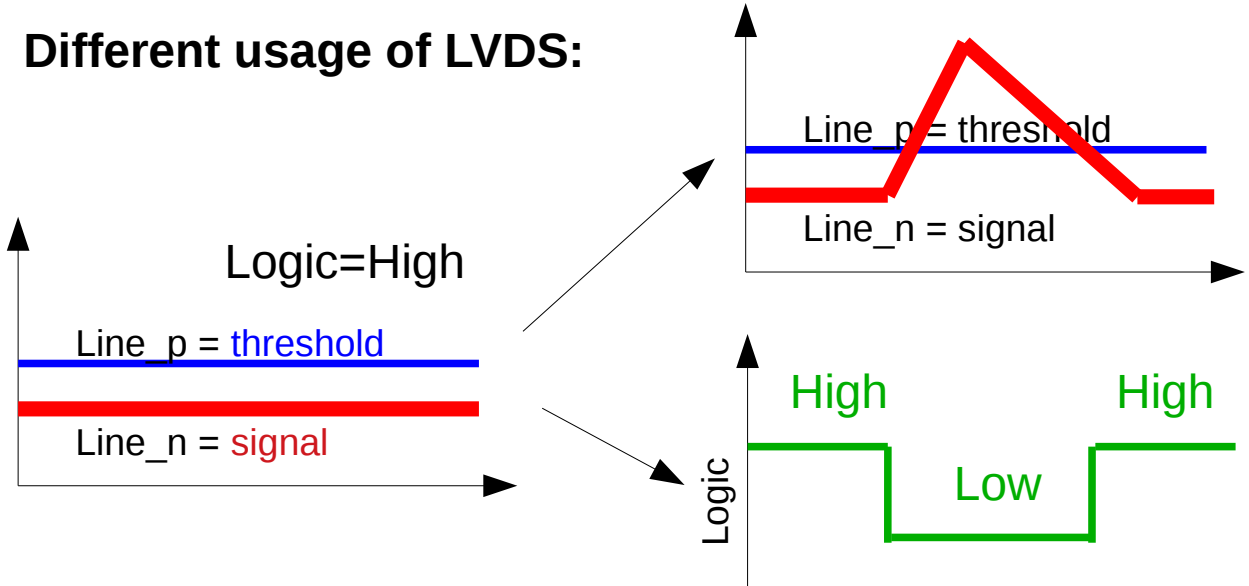
FPGA (DiRICH2)

Discriminator with L

Low Voltage Differential Signaling (LVDS)



Different usage of LVDS:



FPGA (Di