News from GSI ASIC-Design

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GET4++

Motivation

- The GET4 ASIC is a 4 channel event driven TDC with a single channel time precision $\leq 20\,\text{ps}$
  - Based on a closed *Delay Locked Loop* (DLL)
  - Designed for CBM ToF
  - Successfully applied at CBM Tof@STAR and Mini-CBM
- Question: Can the time precision be improved in the current technology
- Idea: Evaluation of a modified time interpolation architecture

$\Rightarrow$ Design of a Test-ASIC to evaluate an improved architecture

$\Rightarrow$ GET4++

GET4++

Concept

- Target technology: UMC 180 nm CMOS
- New time interpolation core architecture with 15.625 ps binning.
- 128 Time bins $\Rightarrow$ $T_{cyc} = 2\,\text{ns}$ resp. $f_{Clk} = 500\,\text{MHz}$.
- On Chip linearity correction
- Scalable Channel architecture, test-chip with four channels
- Readout compatible to Transient recorder ASICs ATR16 & CTR16

GET4++

Concept

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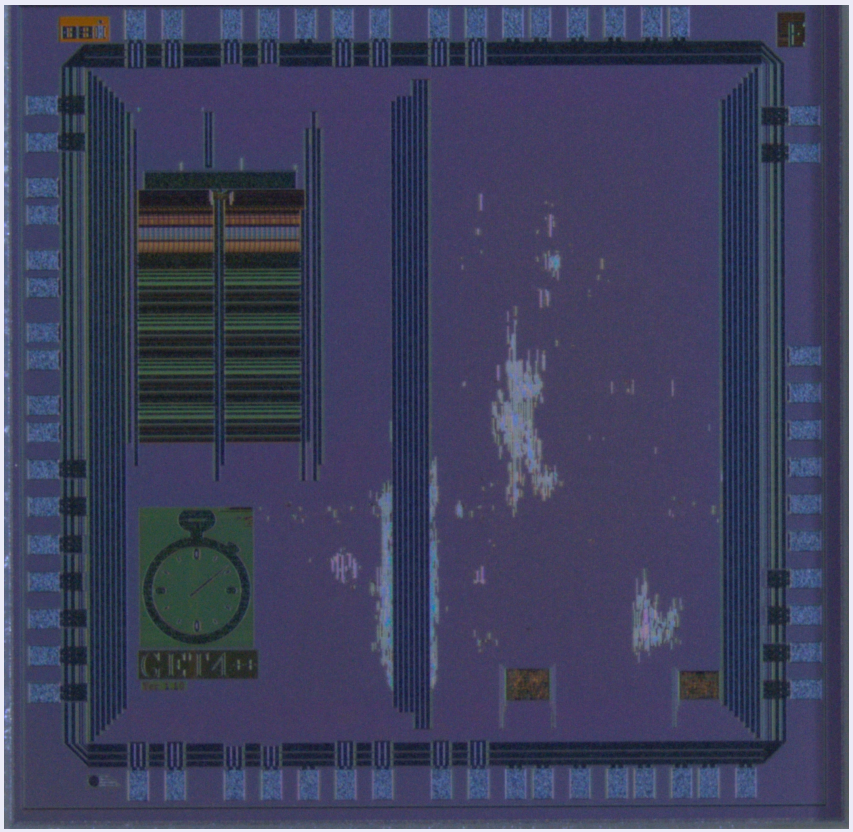

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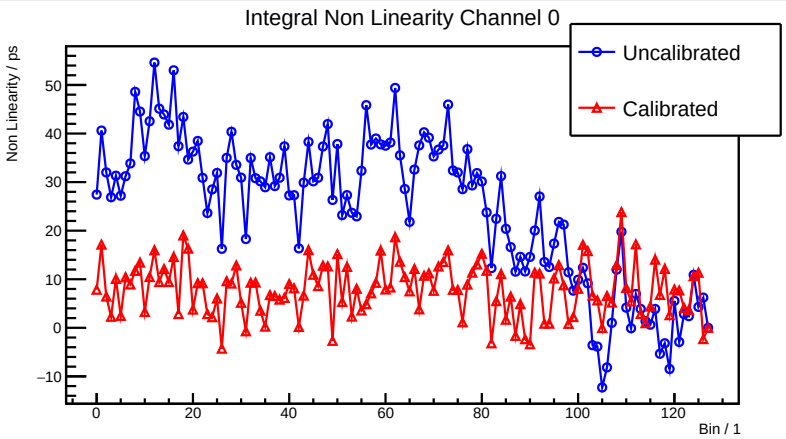
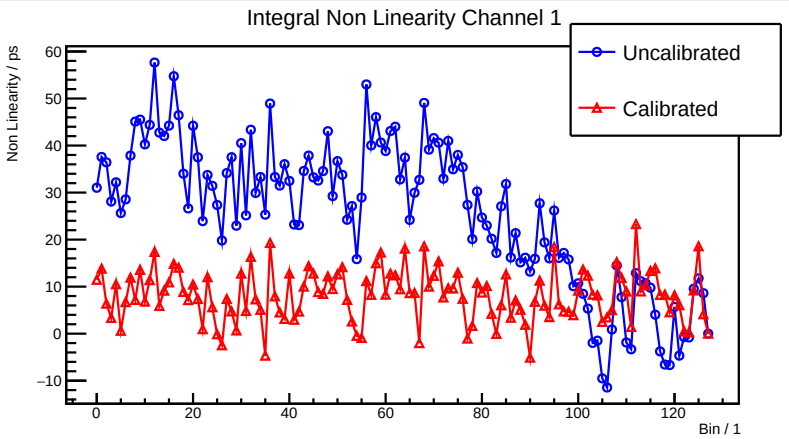
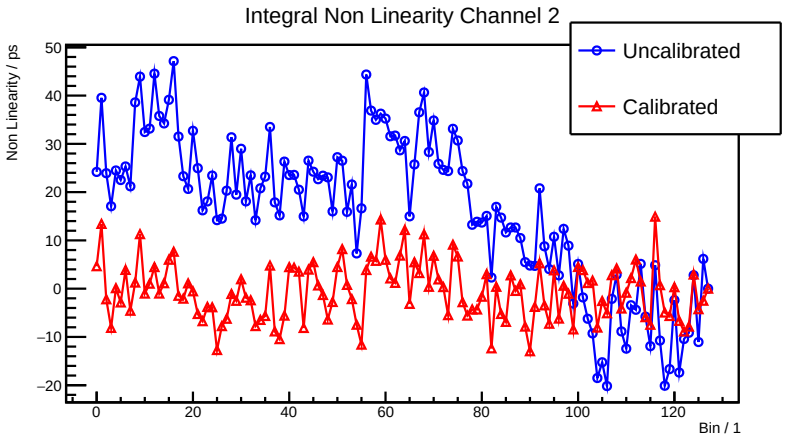
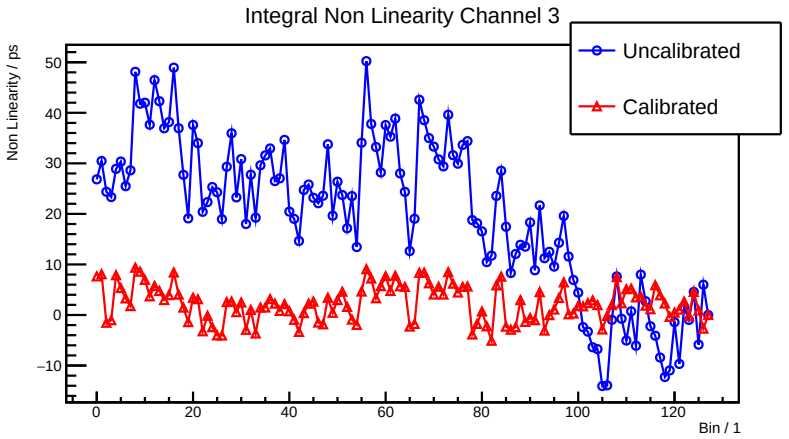
Results

Integral Non-Linearity





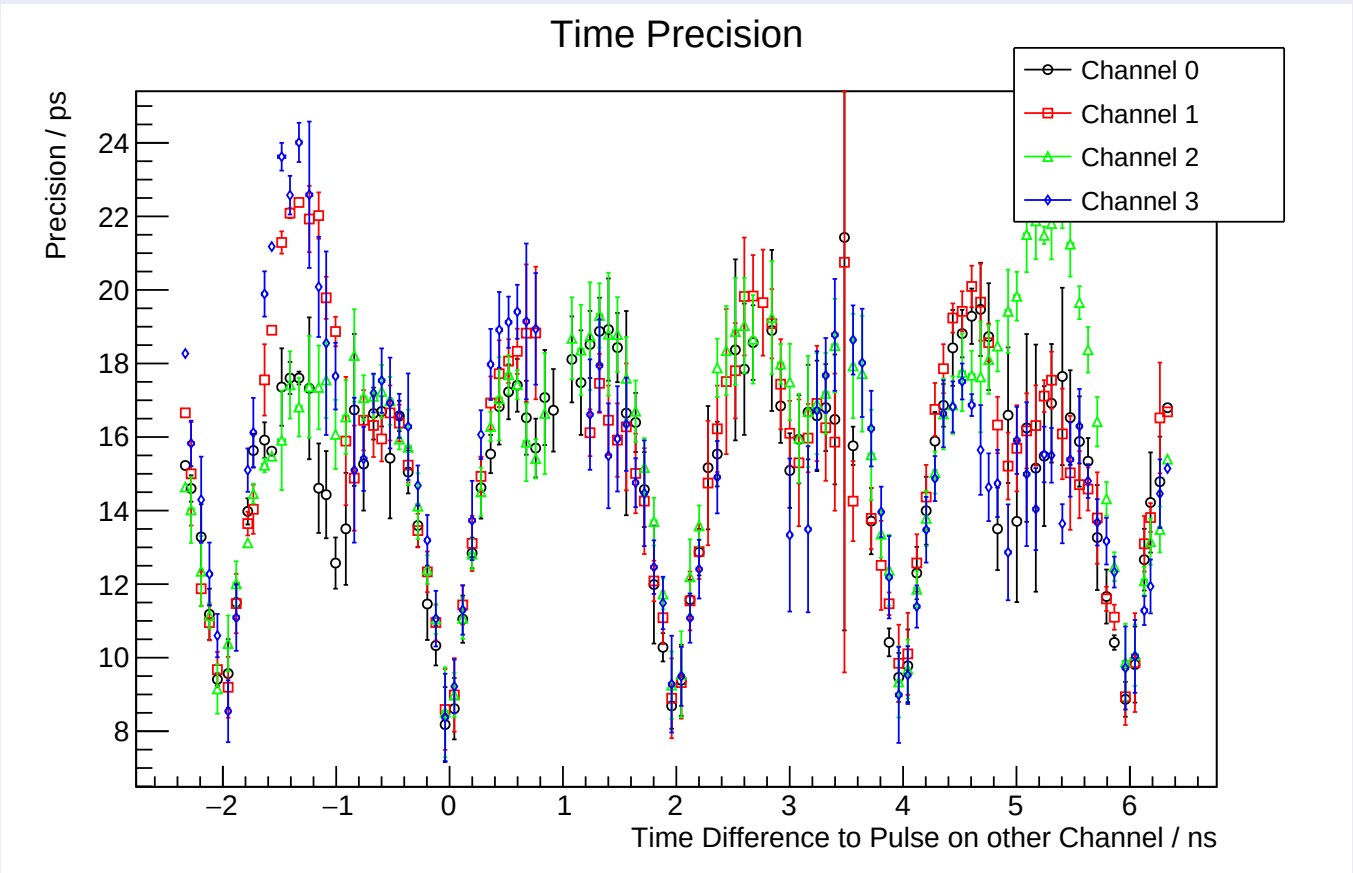




GET4++

Results

Single Channel Time Precision (Uncorrected)



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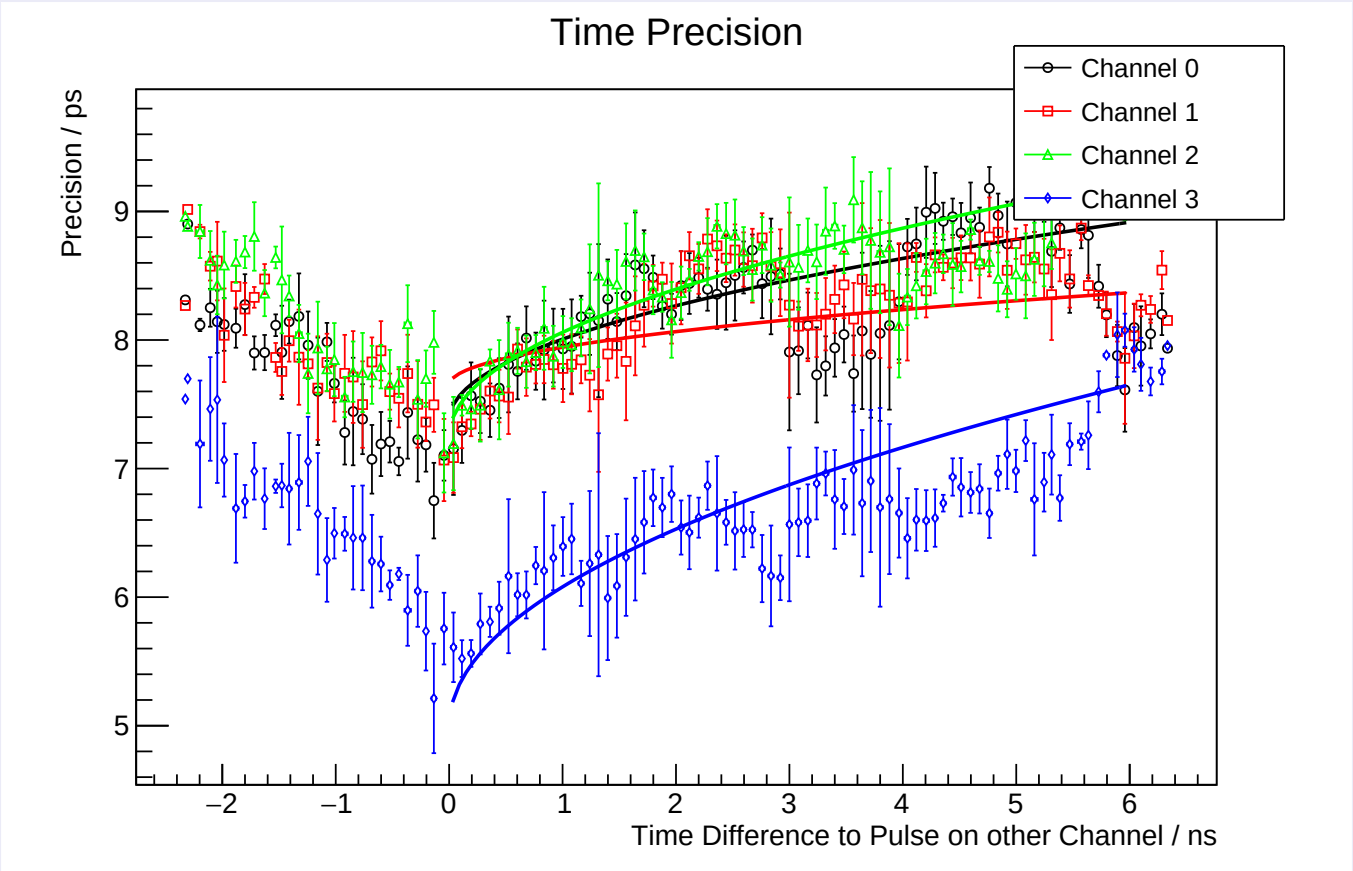
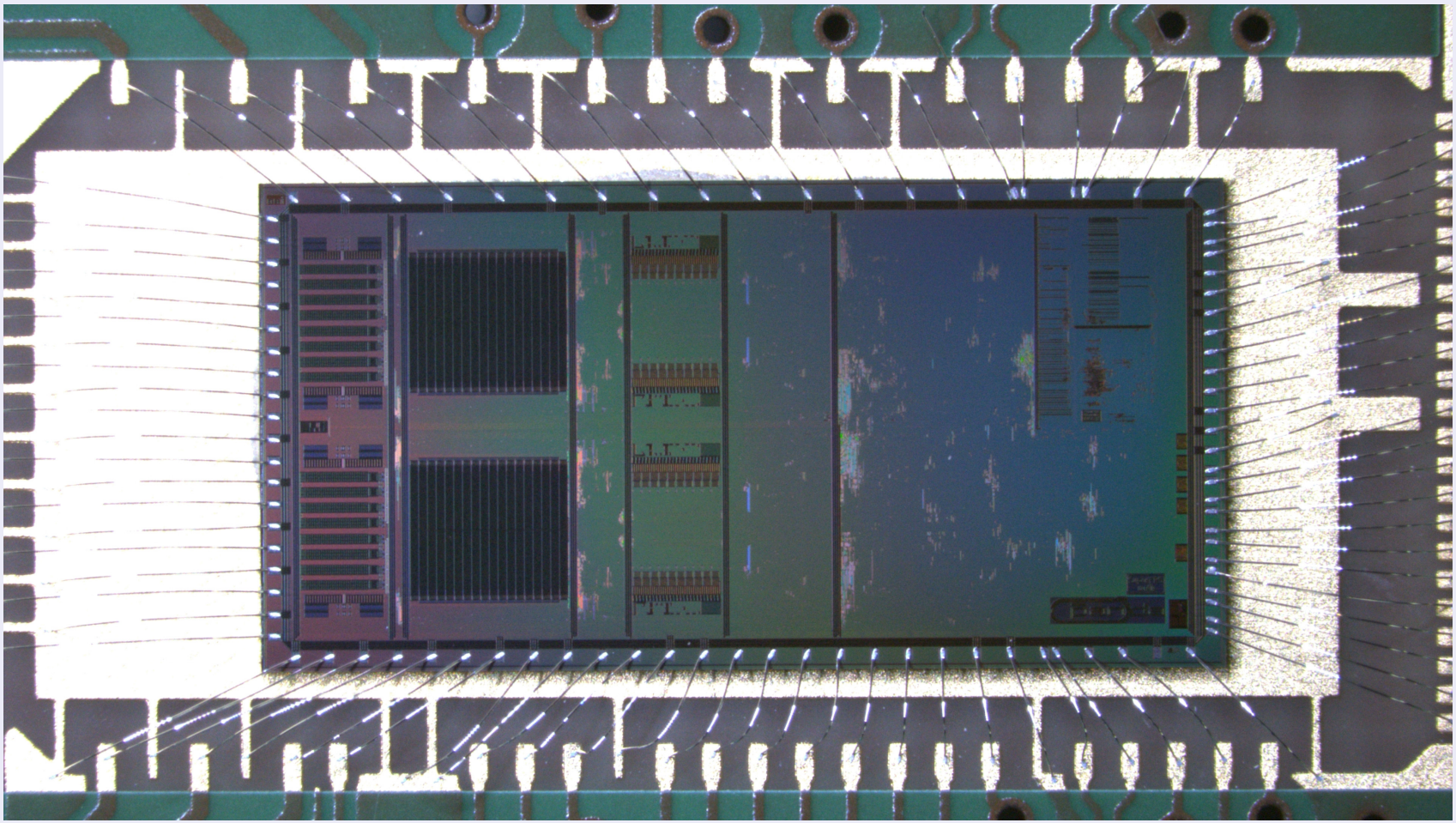
Results

Single Channel Time Precision (Corrected)



CTR16

CTR16 Tests and Measurements



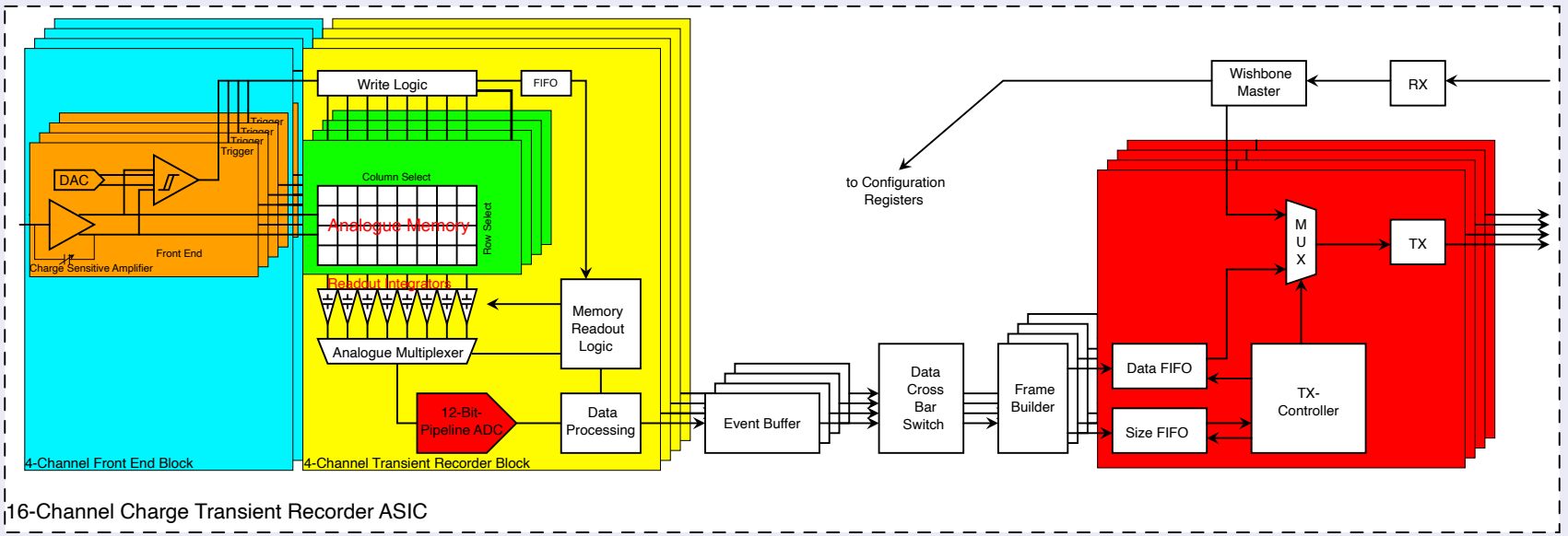
CTR16

Reminder:Transient Recorder with Charge Sensitive Frontend CTR16

- One branch of a family of analogue transient recorder[FDW22] Another ASIC with same backend: ATR16
- Integrated Front end: Charge sensitive amplifier with large dynamic range[WFD22]
- Possible applications: PANDA GEM-Tracker, SFRS GEM-TPC
- Designed in UMC 180 nm technology
- Produced in Fall 2021

CTR16

CTR16 Block Diagram



CTR16

CTR16 Tests and Measurement Status

- Tests and Measurements started in 2023
- Going from Frontend to Backend
- Already tested:
  - Baseline reference DACs
  - Threshold Scans
  - Automatic Threshold Calibration
  - Baseline Tracking with Drift Compensation
  - First Acquisitions of Baseline Traces
- Next Steps
  - Calibration of Analogue Chain, Memory cells
  - Measurement of charge pulses

Summary

- GET4++
  - With GET4++ a new TDC core is available with time precision $\leq 10\,\text{ps}$
  - Core could be combined with dedicated front ends
- CTR16
  - Tests and Measurements started
  - Tests done up to now very promising
  - Characterisation of Analogue Performance will coming soon

References

Flemming, H., Deppe, H. and Wieczorek, P.: *A family of transient recorder ASICs for detector readout*. Journal of Instrumentation, *vol. 17*(2022)(07), p. C07002
URL https://doi.org/10.1088/1748-0221/17/07/c07002

Wieczorek, P., Flemming, H. and Deppe, H.: *Low Noise Amplifier With Adaptive Gain Setting (AWAGS) ASIC*. Journal of Instrumentation, *vol. 17*(2022)(07), p. C06010
URL https://iopscience.iop.org/article/10.1088/1748-0221/17/06/C06010