Work development in Torino

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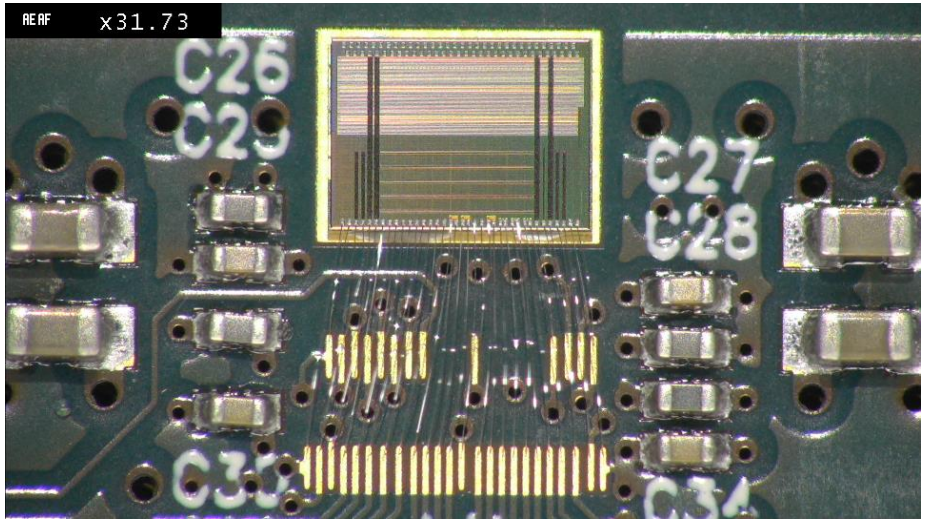
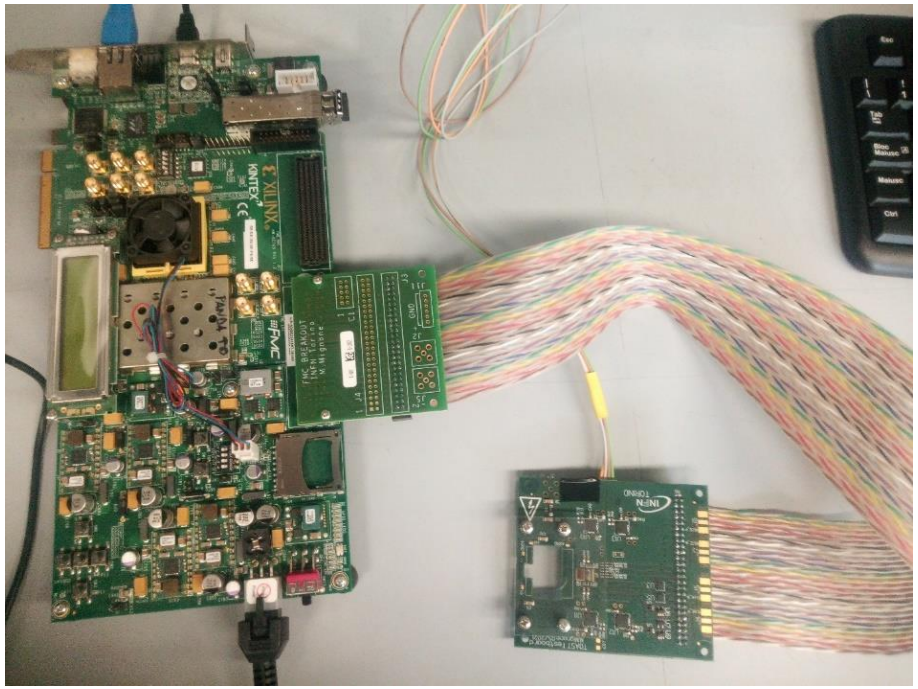
ToASt test boards





All the 6 test boards available in Torino have been equipped with all the needed components.

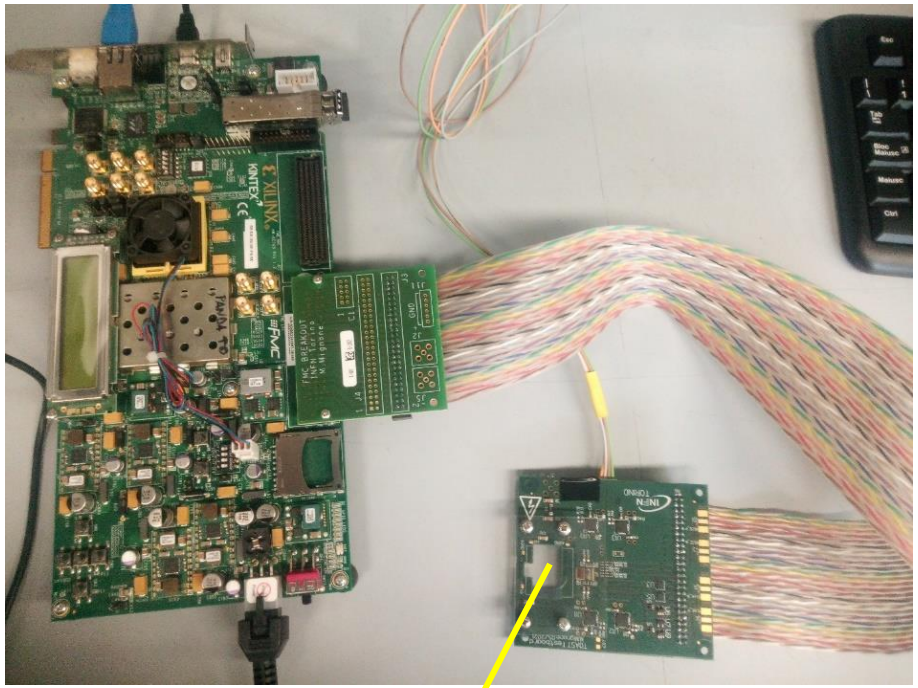
All boards were equipped with the SN74AUP1T34DCKR components de-soldered from old cards of CMS

The purchase order done for these specific components in 2021 was cancelled by the vendor.

5 test boards are equipped with working chips (one among them was sent to KIT, a second one was used for the SEU test, the third one is now equipped with a small sensor from FBK)

The 6th test board is equipped with a chip with some channels not working, to be investigated (to do!)

ToASt + sensor

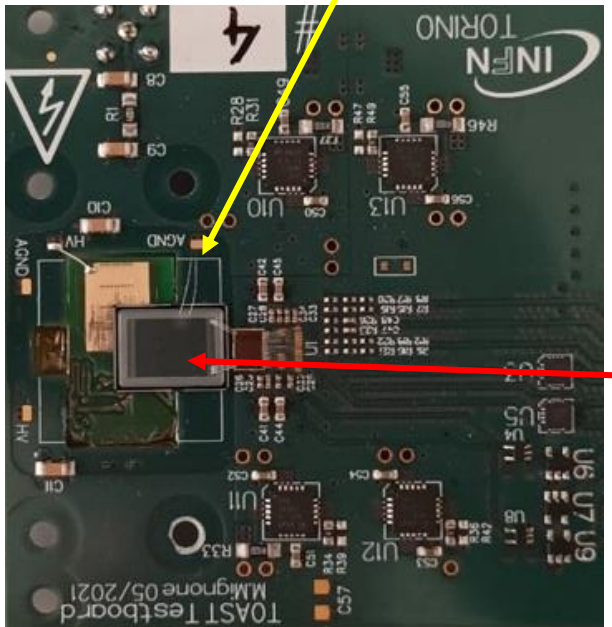


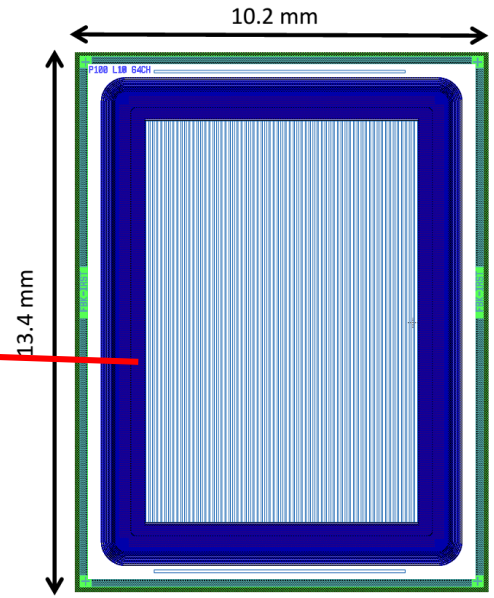
The sensor (from FBK) is small compared to the hole left on the test board and a temporary support holds it in place

Additional noise ?

The test with the sensor is in stand-by

The acquisition of a sensor signal is not yet implemented in the DAQ program





ToASt + sensor

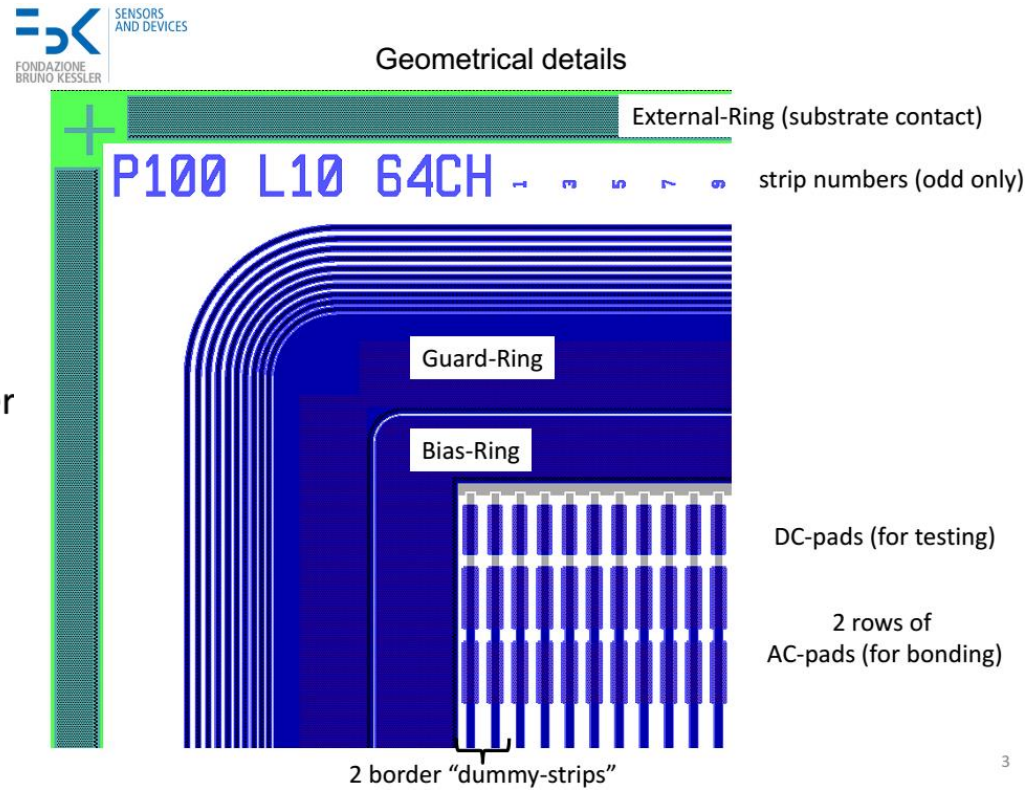
p+/n silicon strip detector (single-side)

Metal ohmic contact at the back-side

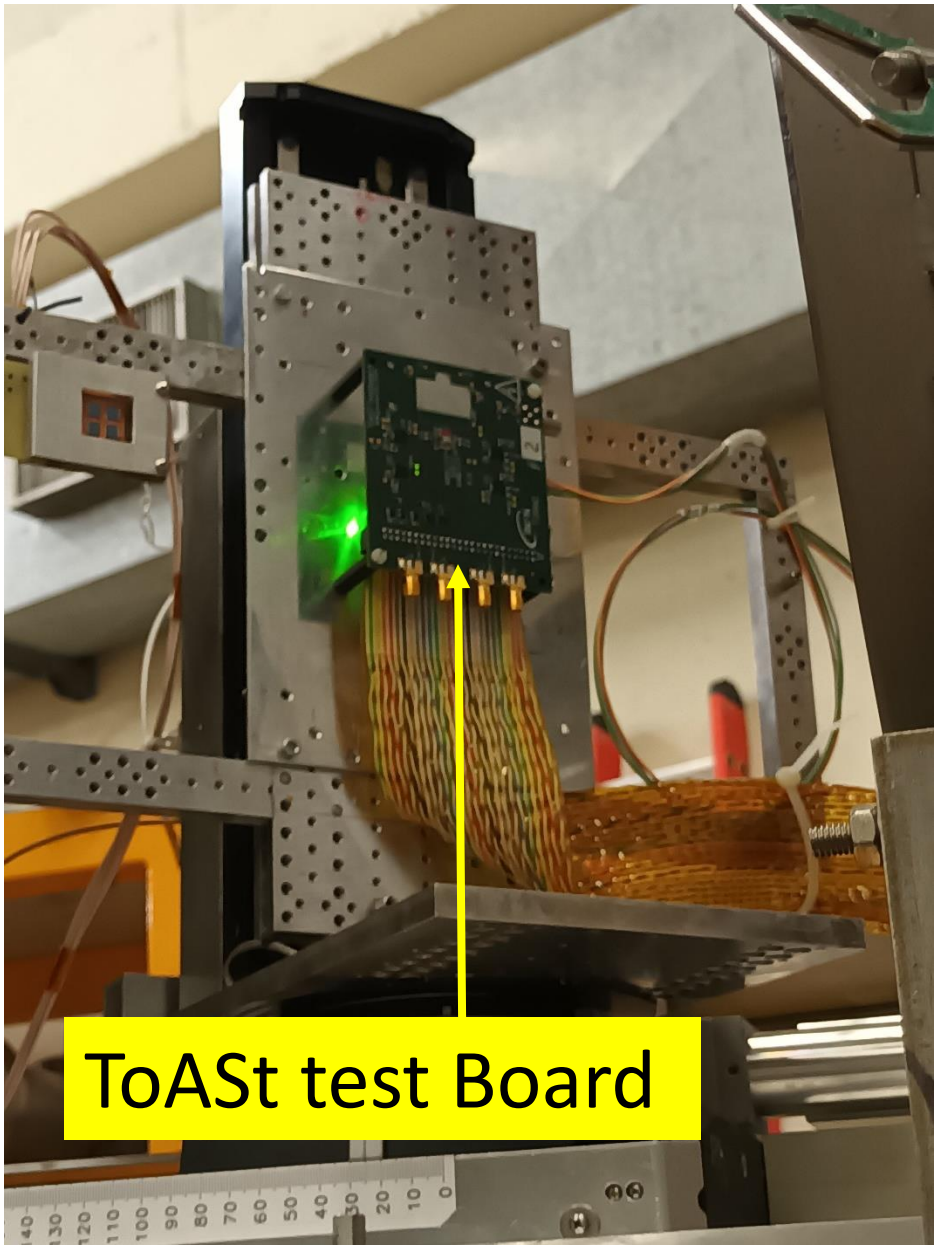
Strip Length = 10 mm
Strip pitch = 100 µm
# of strips = 64 (+ 2 dummy-strips at each border
Punch-through biasing (Bias-Ring)
AC coupling

Guard-ring + multi-rings termination structure

Substrate thickness = 300 µm
Full depletion voltage (expected): <40V



SEU test at SIRAD (INFN-LNL)



Results of the SEU test

1728 bits in the configuration registers

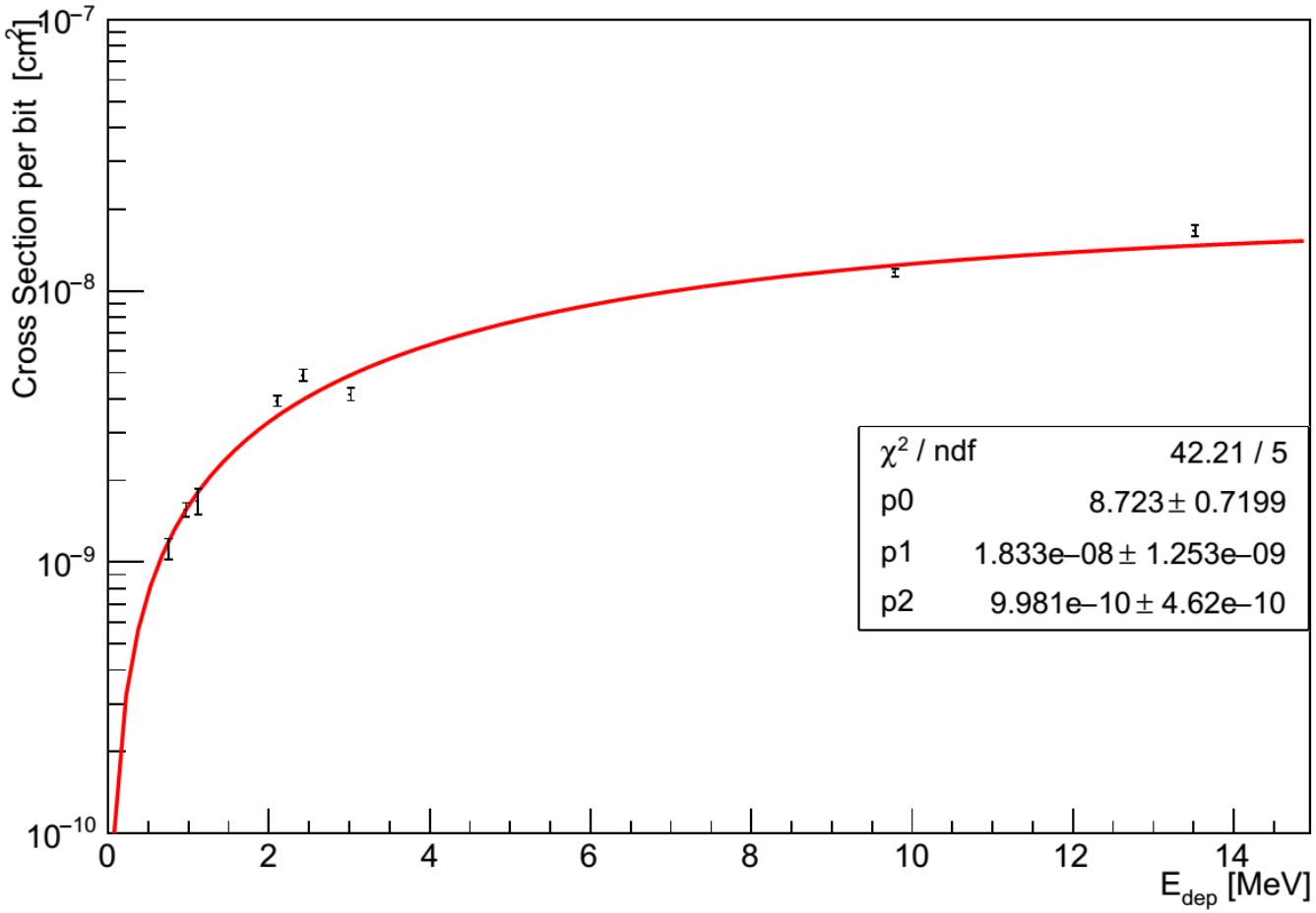
(16 GCR + 64x2 CCR) with TMR protection

Configuration with 0, 1 balance

Only 1 -> 0 type bit flips were observed → ???

SEU cross section: $9.20 \pm 0.17 \cdot 10^{15} cm^2/bit$

→ 0.06 upset/(chip·h) @ 10^6 hit/cm²·s



Results of the SEU test

Explanation of the 1 -> 0 type bit flips

The automatic synthesis process that must optimize the circuit and then also the ‘TMR parts ’ would not have worked correctly on these last parts.

The load signal is triplicated in the pre-synthesis, it is not in the post-synthesis

The problem concerns all the configuration registers

A SET on the load signal at the clock edge causes zeros to be loaded into the register may be the explanation of bit flips in only one direction.

Future

Submission of a second prototype requires still to answer to many questions:

- Why the yield is about 50 %? A debugging activity is needed on the chips not working correctly. Now we have one test board equipped with a chip candidate to be investigated
- A systematic study of the analogue part has to be done
- Study of ToASt behavior under X ray irradiation should be done (a test is foreseen within 2022)
- Study of the chip + sensor in the lab is needed. Sensors should be available
- Study of chip performances at high rate with a test beam should be done
- Connection to the strip readout architecture and test should be done to verify the interface between ToASt and MDC

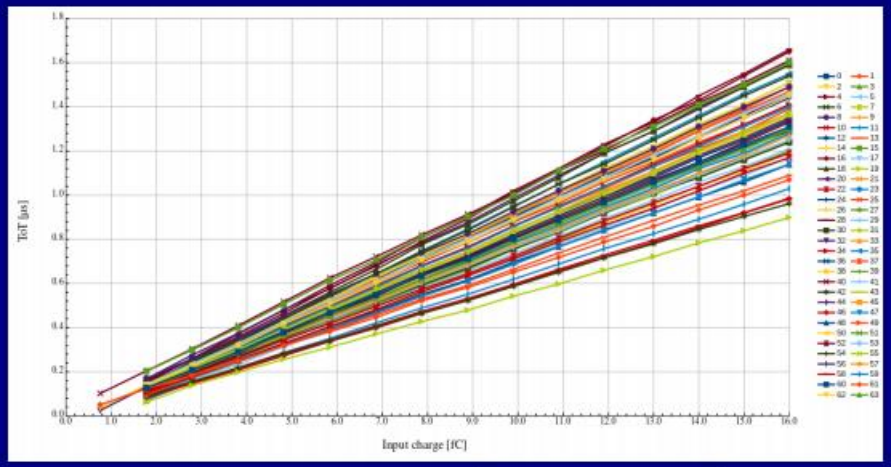
Spares

Specifications

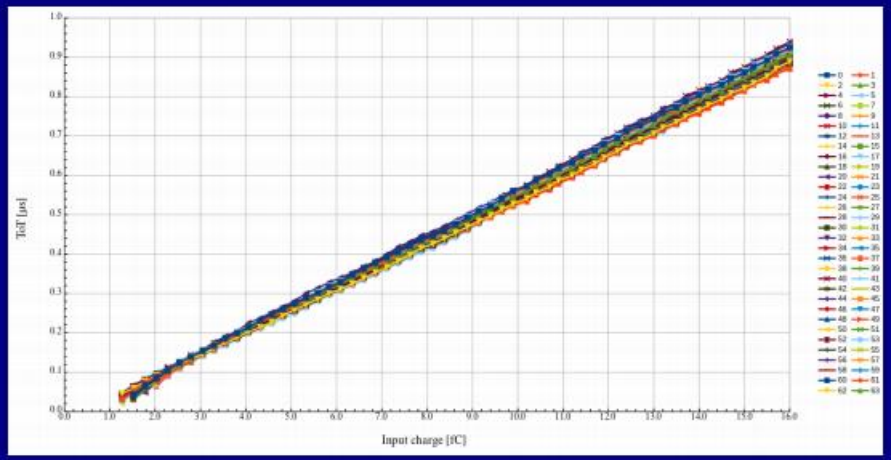
Specification	Min	Max	Unit
Input capacitance	2	17	pF
Max rate per strip		40	kHz
Input charge	1	40	fC
Noise		1500	e^-
Preamp peaking time	50	$\geq$ 100	ns
Channels per chip	64		
Reference clock		160	MHz
Charge resolution	8		bits
Time resolution (pk-pk)		6.25	ns
Time resolution (r.m.s.)		1.8	ns
Power consumption		256	mW
Chip dimensions	4.5 $\times$ 3.5		mm^2
Pads position	On two sides only		

Measurement - transfer function

Before calibration

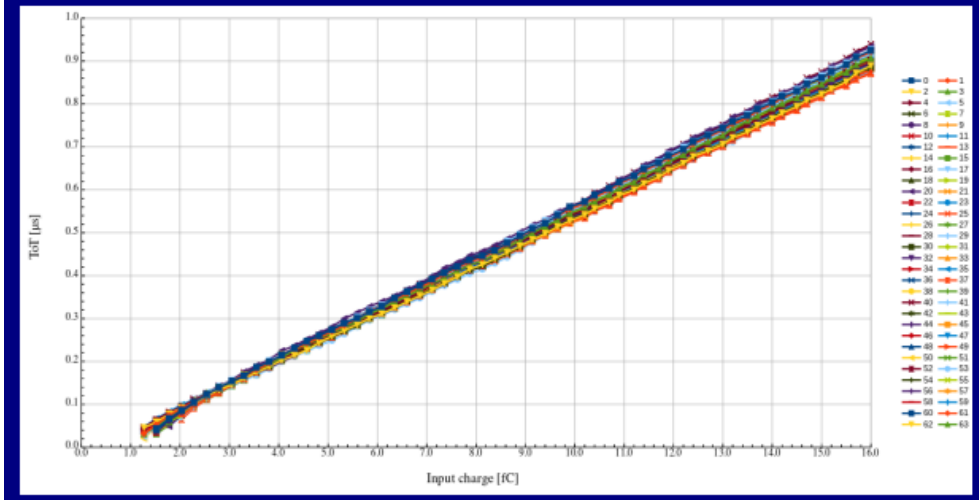


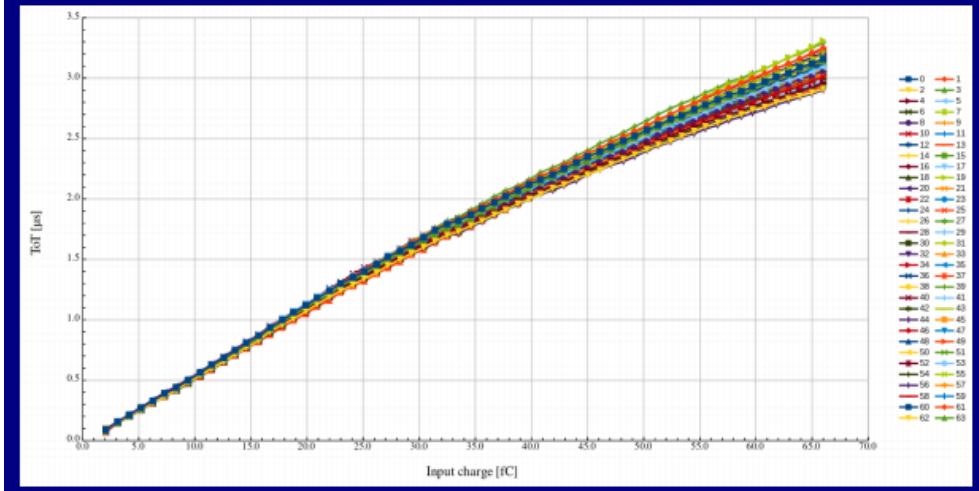
After calibration (gain & offset)



- No smoke at power-on
- Configuration interface ok
- Data transmission ok
- All 64 channels respond correctly to test pulse
- Fairly large gain spread
  - *Expected : depends on a very small current*
  - Channel level gain calibration implemented - gain spread reduce from 12% to 1.7%
  - Channel level offset calibration implemented - offset spread reduced from 30% to 5.8%
- Power consumption : 180 mW @1.2 V

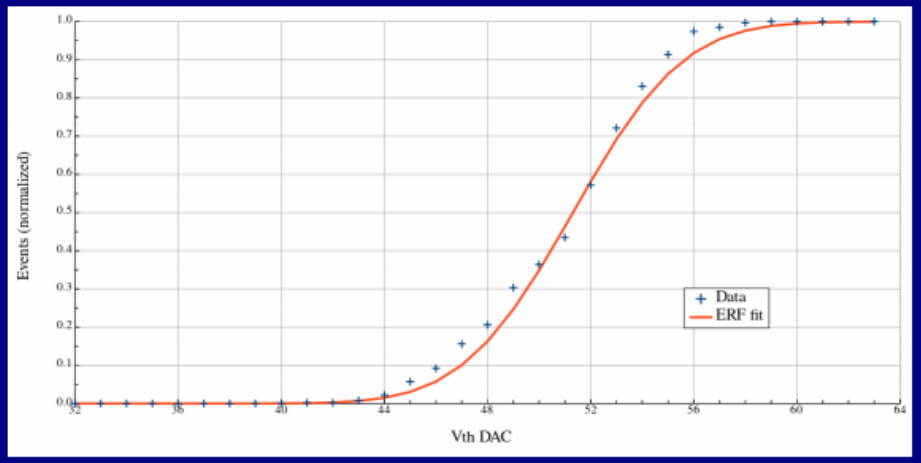
Measurement - test pulse ranges

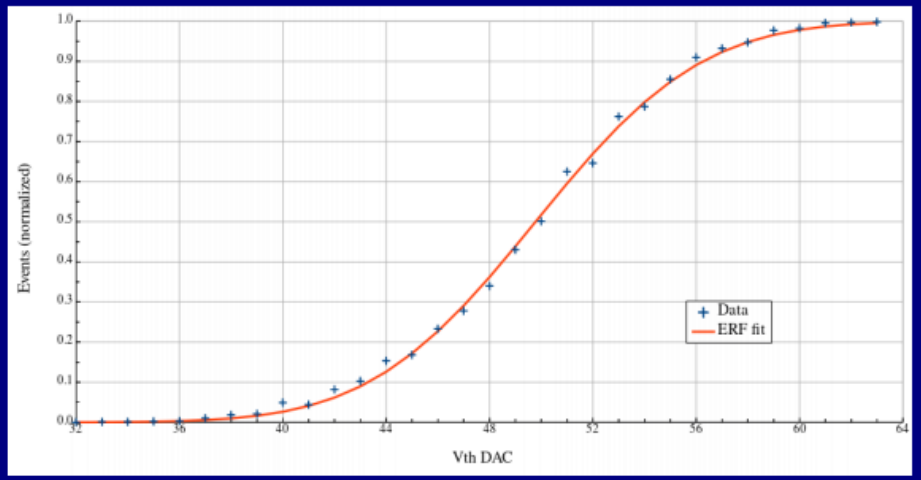




- Test pulse input with internally programmable amplitude via 6+1 bit internal DAC.
- Two test pulse ranges *(the +1 bit)* :
  - Normal range : up to 16 fC, step 0.25 fC
  - Extended range : up to 66 fC, step 1.03 fC
- Non linearity (rms) $<0.64\%$ in the $2 \div 16$ fC range

Measurement - noise





- S-curve obtained with channel threshold scan
  - Test pulse resolution and global threshold resolution too coarse
  - Baseline resolution gives similar results but with fewer points
- Conversion from DAC codes to input charge from simulations
- No input capacitance
- Average noise : 0.034 fC (211 e^-)
- Maximum noise : 0.05 fC (312 e^-)