Galileo Readout Electronics

For the AGATA Upgrade

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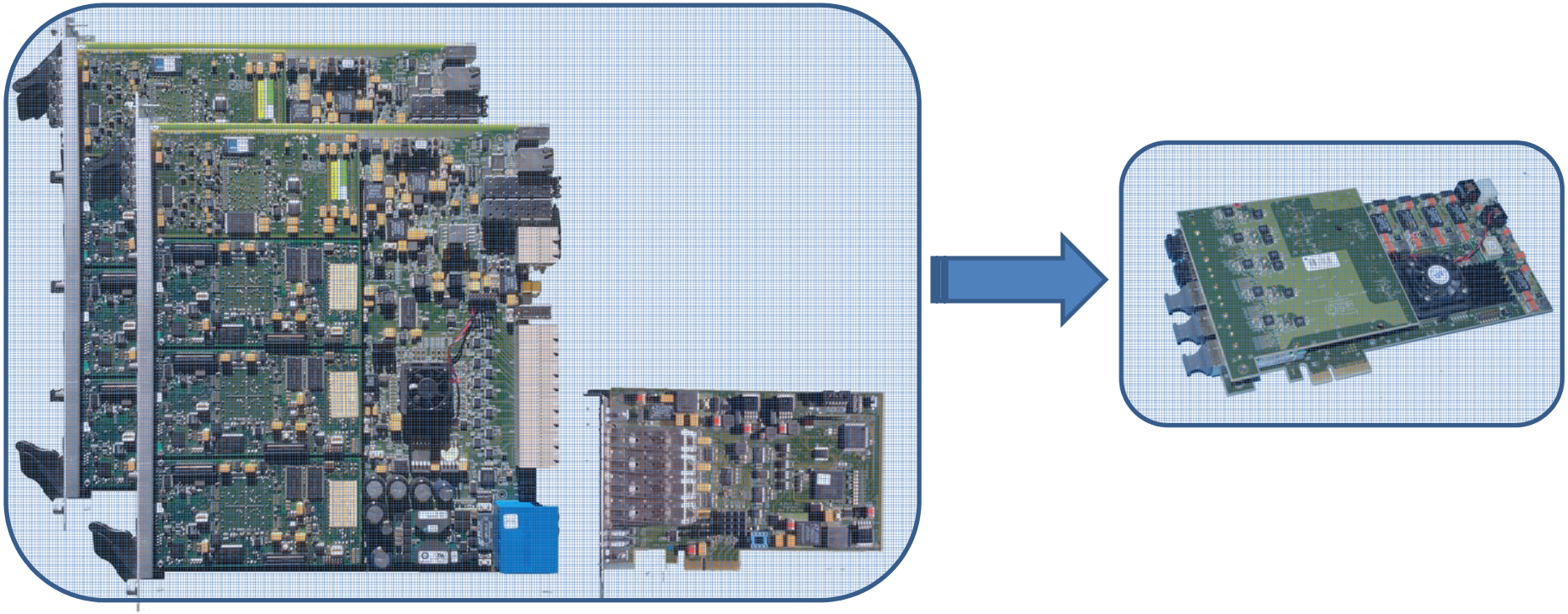
The Target

- Instrument Galileo with a readout that is AGATA 100% compatible
  - Use the new readout as un upgrade to AGATA FEE
- Exploit state of the art technology to
  - Reduce costs
  - Improve ease of operation

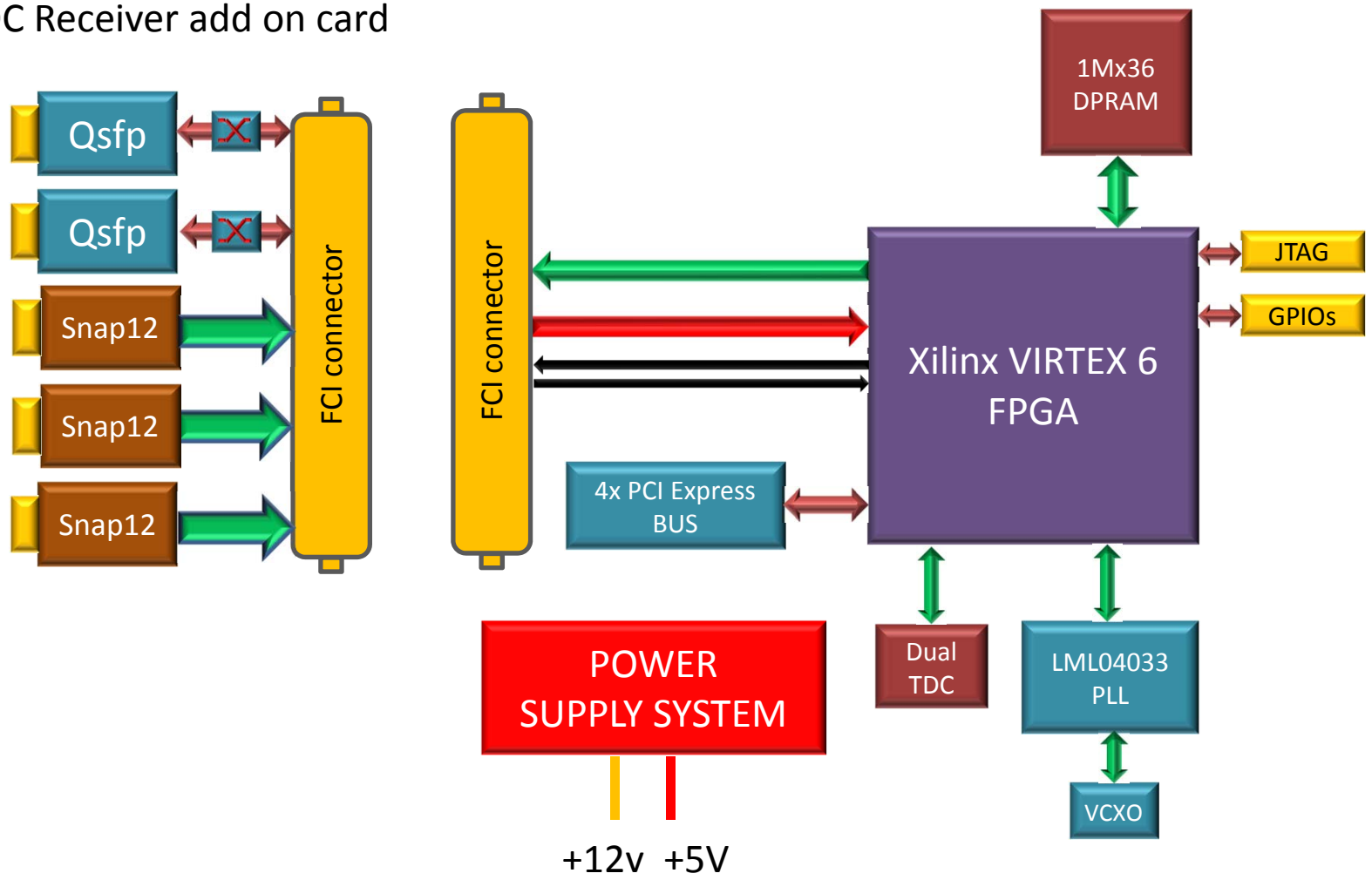
The approach

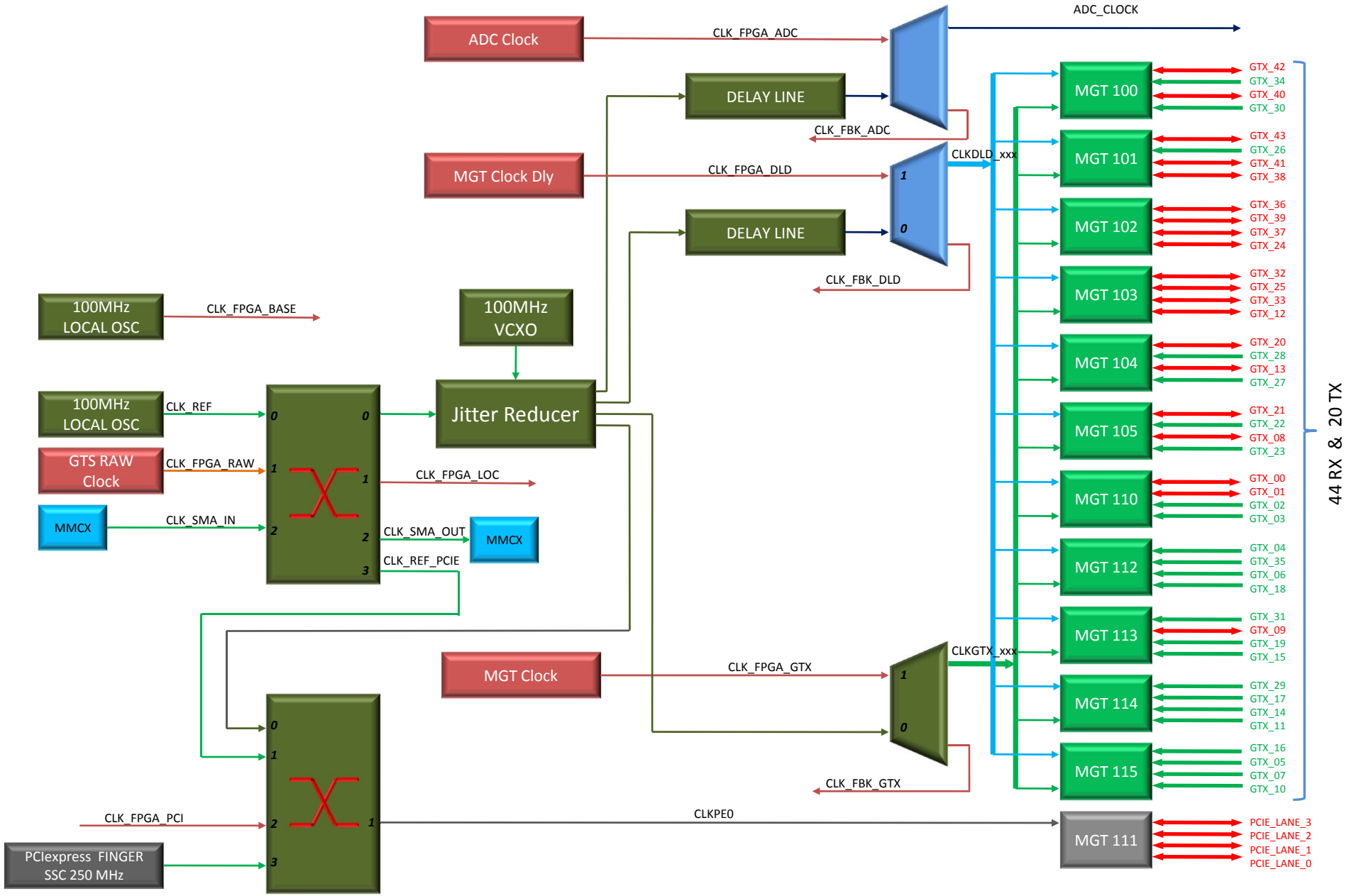
- Squeeze the readout of one crystal in a PC form factor add-on card
  - Reuse PSA servers infrastructure (box, motherboard, PS)
    - Save crate, PS, cooling and area costs



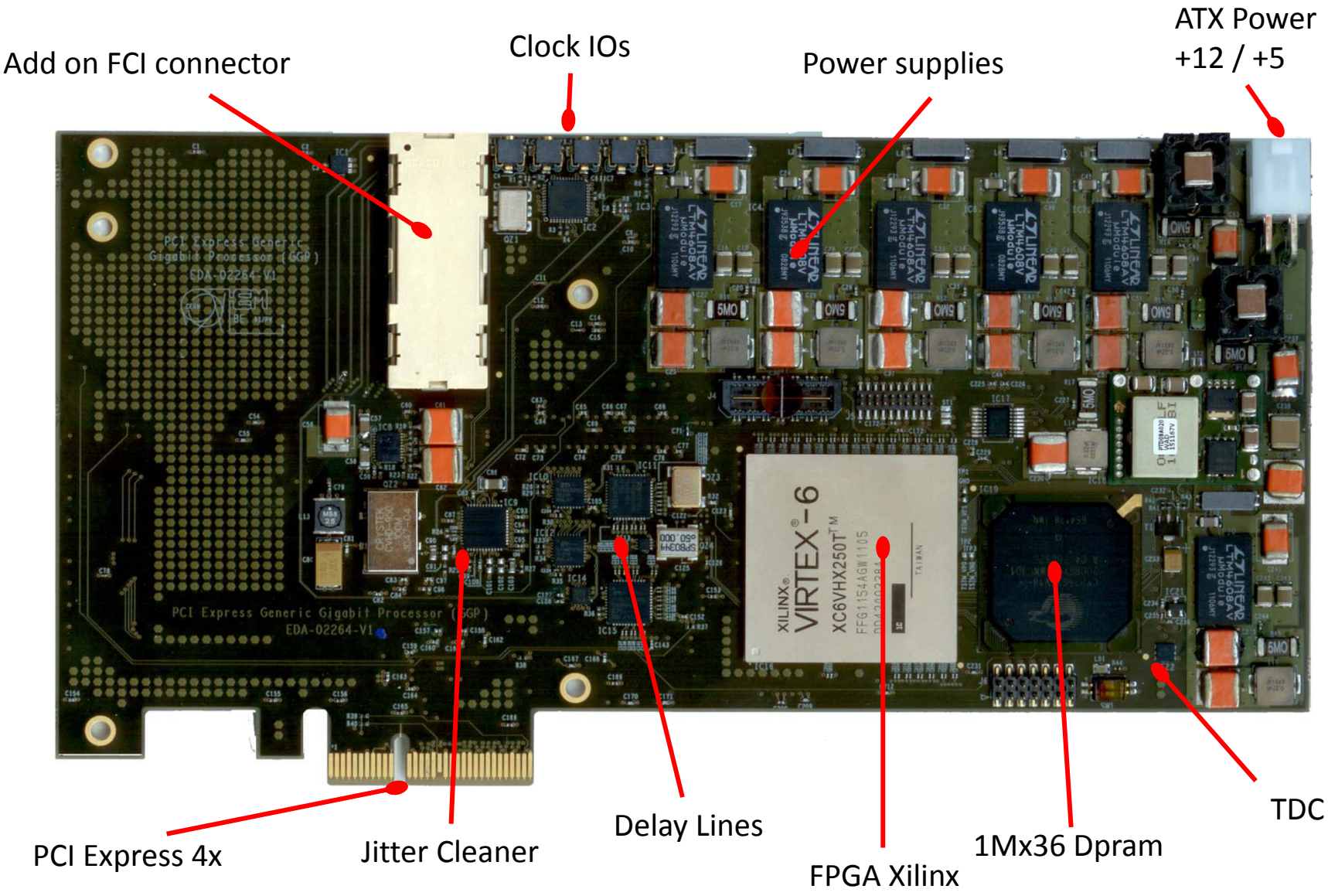
Hardware block diagram

Main card simplified block diagram
+ ADC Receiver add on card

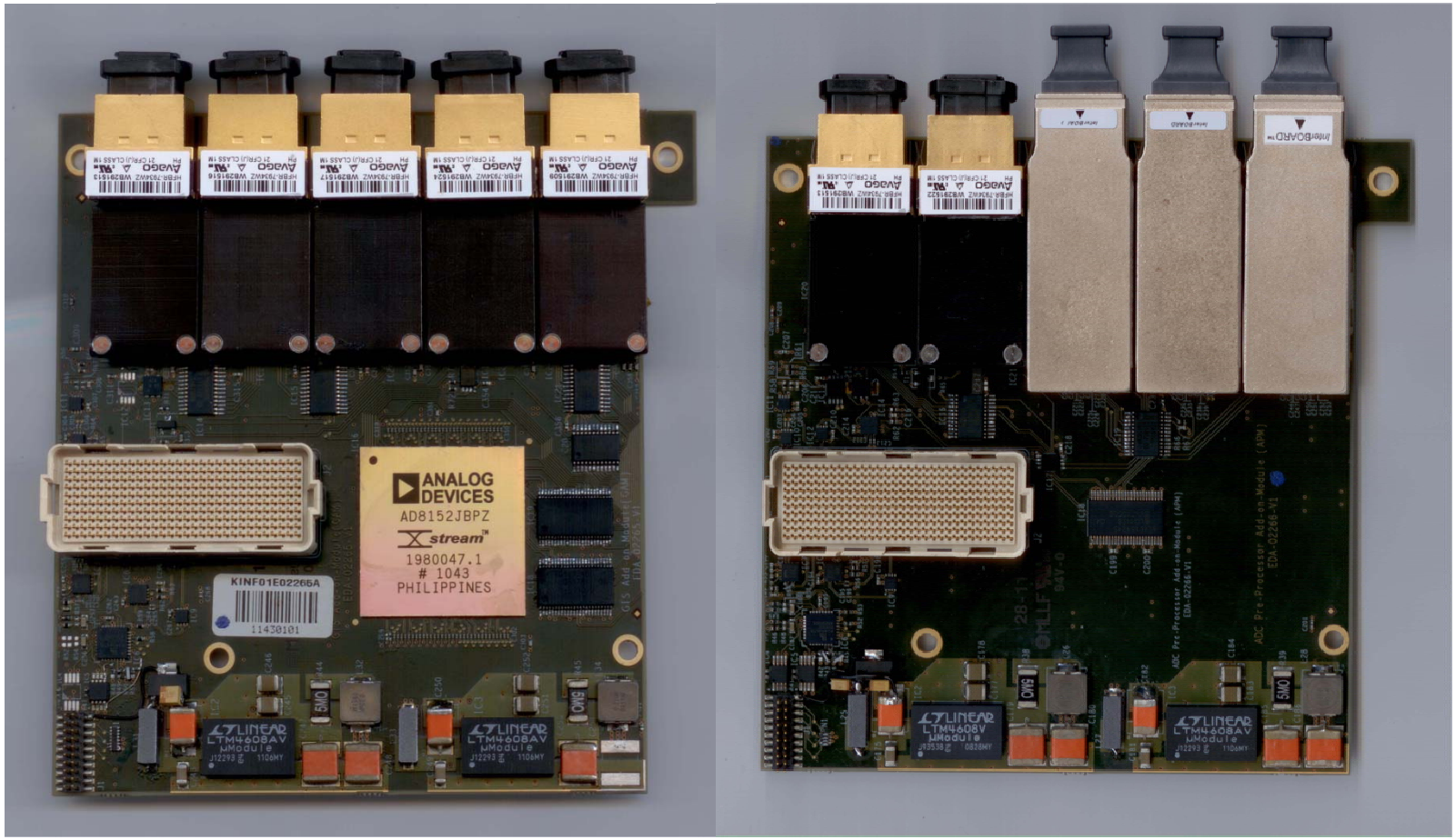



ADC Clock
CLK_FPGA_ADC
ADC_CLOCK
DELAY LINE
CLK_FBK_ADC
MGT Clock Dly
CLK_FPGA_DLD
CLKDLD_xxx
DELAY LINE
CLK_FBK_DLD
100MHz LOCAL OSC
CLK_FPGA_BASE
100MHz VCXO
100MHz LOCAL OSC
CLK_REF
GTS RAW Clock
CLK_FPGA_RAW
MMCX
CLK_SMA_IN
Jitter Reducer
CLK_FPGA_LOC
CLK_SMA_OUT
MMCX
CLK_REF_PCIE
MGT Clock
CLK_FPGA_GTX
CLKGTX_xxx
CLK_FBK_GTX
CLK_FPGA_PCI
PCIexpress FINGER SSC 250 MHz
CLKPE0
MGT 100
MGT 101
MGT 102
MGT 103
MGT 104
MGT 105
MGT 110
MGT 112
MGT 113
MGT 114
MGT 115
MGT 111
GTX_42 GTX_34 GTX_40 GTX_30
GTX_43 GTX_26 GTX_41 GTX_38
GTX_36 GTX_39 GTX_37 GTX_24
GTX_32 GTX_25 GTX_33 GTX_12
GTX_20 GTX_28 GTX_13 GTX_27
GTX_21 GTX_22 GTX_08 GTX_23
GTX_00 GTX_01 GTX_02 GTX_03
GTX_04 GTX_35 GTX_06 GTX_18
GTX_31 GTX_09 GTX_19 GTX_15
GTX_29 GTX_17 GTX_14 GTX_11
GTX_16 GTX_05 GTX_07 GTX_10
PCIE_LANE_3 PCIE_LANE_2 PCIE_LANE_1 PCIE_LANE_0
44 RX & 20 TX

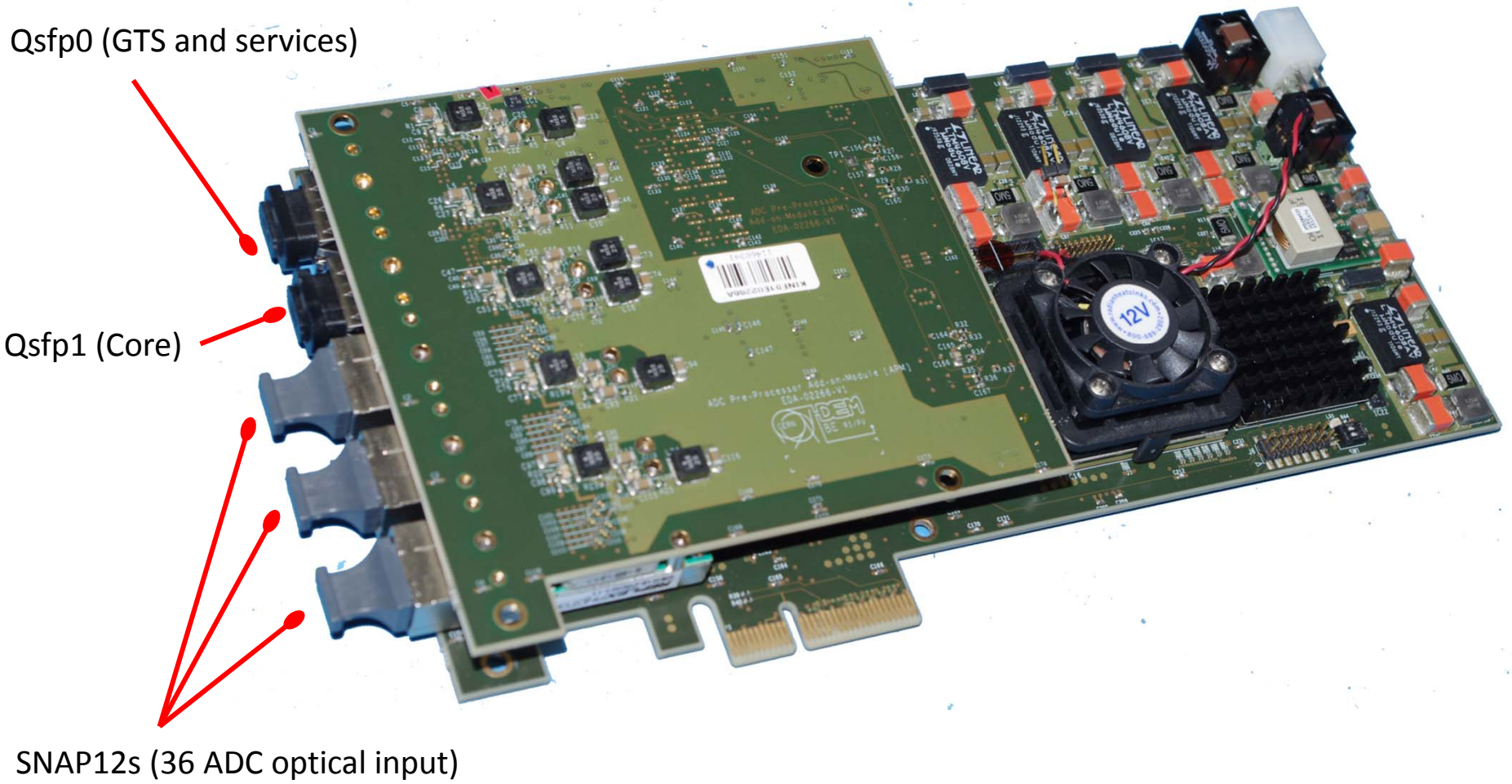
Main card


Add on FCI connector
Clock IOs
Power supplies
ATX Power
+12 / +5
PCI Express 4x
Jitter Cleaner
Delay Lines
FPGA Xilinx
1Mx36 Dpram
TDC
PCI Express Generic Gigabit Processor (GGP)
EDA-02264-V1
XILINX
VIRTEX-6
XC6VHX250T

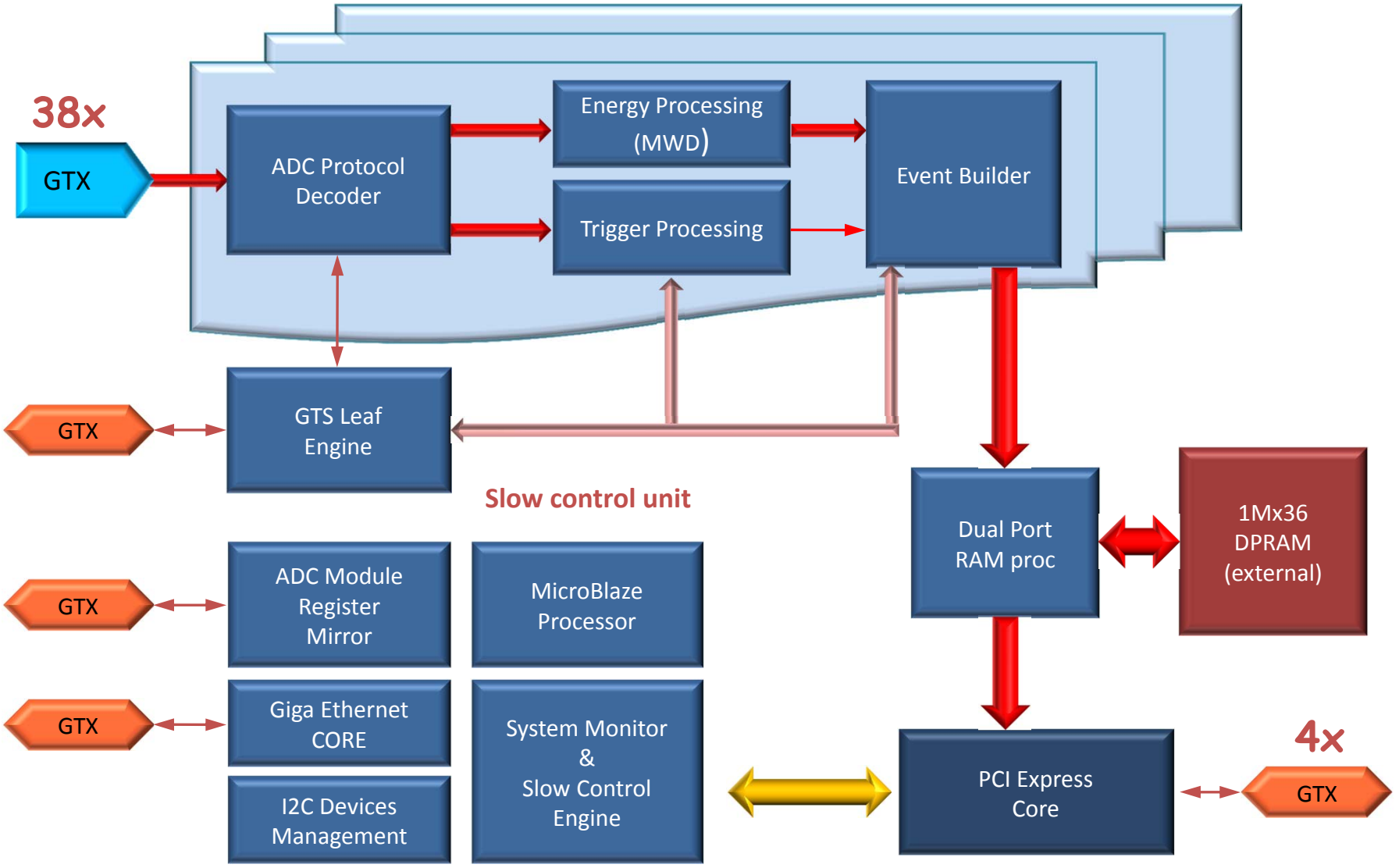
Plug-in mezzanines



The assembly



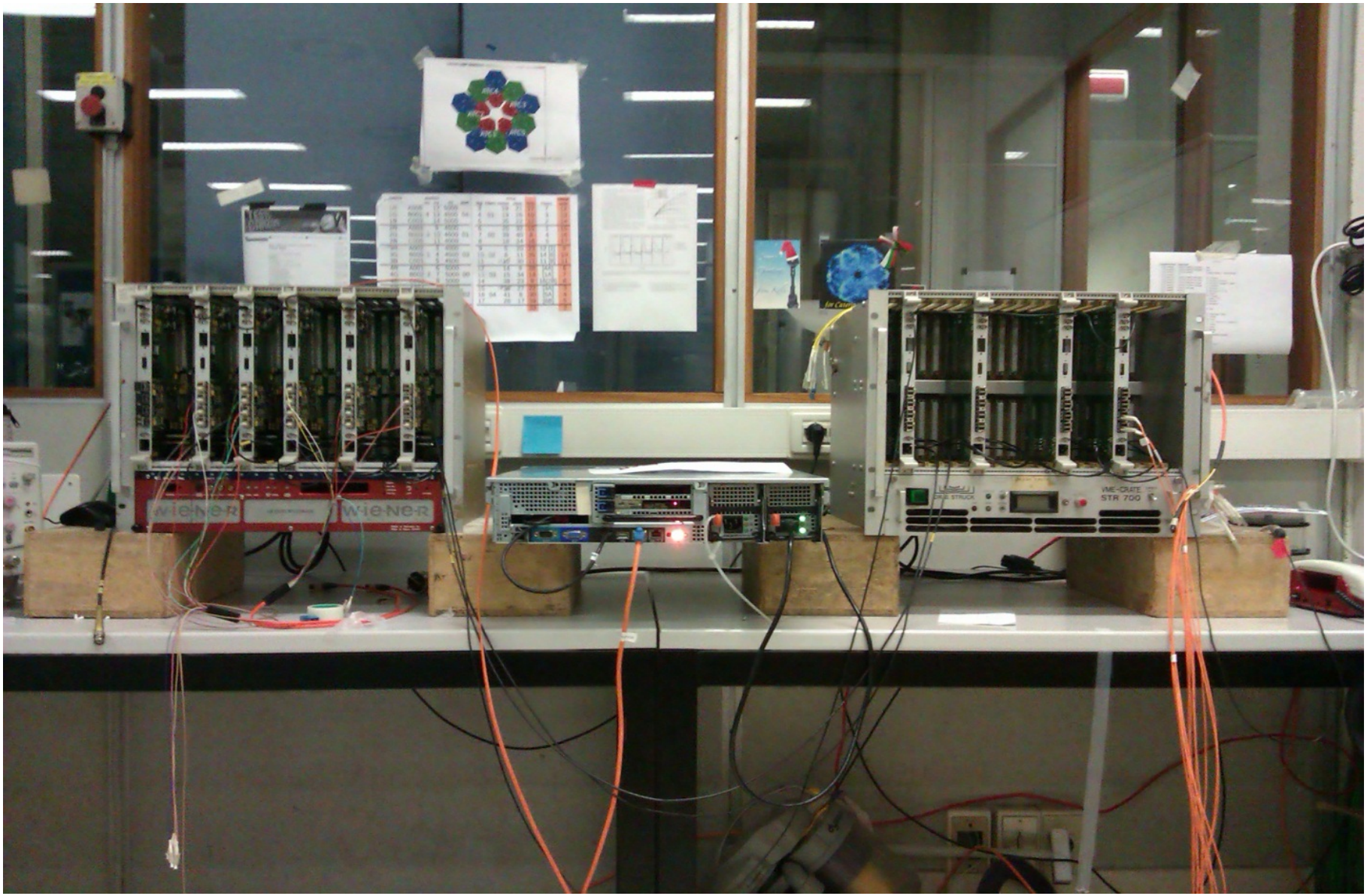
Firmware


38x
GTX
ADC Protocol Decoder
Energy Processing (MWD)
Trigger Processing
Event Builder
GTX
GTS Leaf Engine
Slow control unit
Dual Port RAM proc
1Mx36 DPRAM (external)
GTX
ADC Module Register Mirror
MicroBlaze Processor
GTX
Giga Ethernet CORE
I2C Devices Management
System Monitor & Slow Control Engine
PCI Express Core
4x
GTX

Relevant Features

Form factor	**Add-on card 111.5 x 200 mm**
Host Interface	**Pci Express Gen 2 – 4x**
Supply Voltages	**+12V; +5V**
Power Consumption	**< 70W at full AGATA configuration**
Optical Channels	**(36 + 7) in – 5 out at max 3.125 Gb/s**
FPGA	**Xilinx XC6VHX250T-FF1154**
RAM	**True dual port 1Mx36**
TDC	**2 channels @ 50ps rms resolution**
GTS support	**1 GTS Leaf channel**
Clock filter	**National LMK-04033**
Local / recovered clock frequency	**100 MHz**
External clock I/O	**5 -- MMCX connectors**
Target cost (for volume production)	**6 KEuro + VAT**

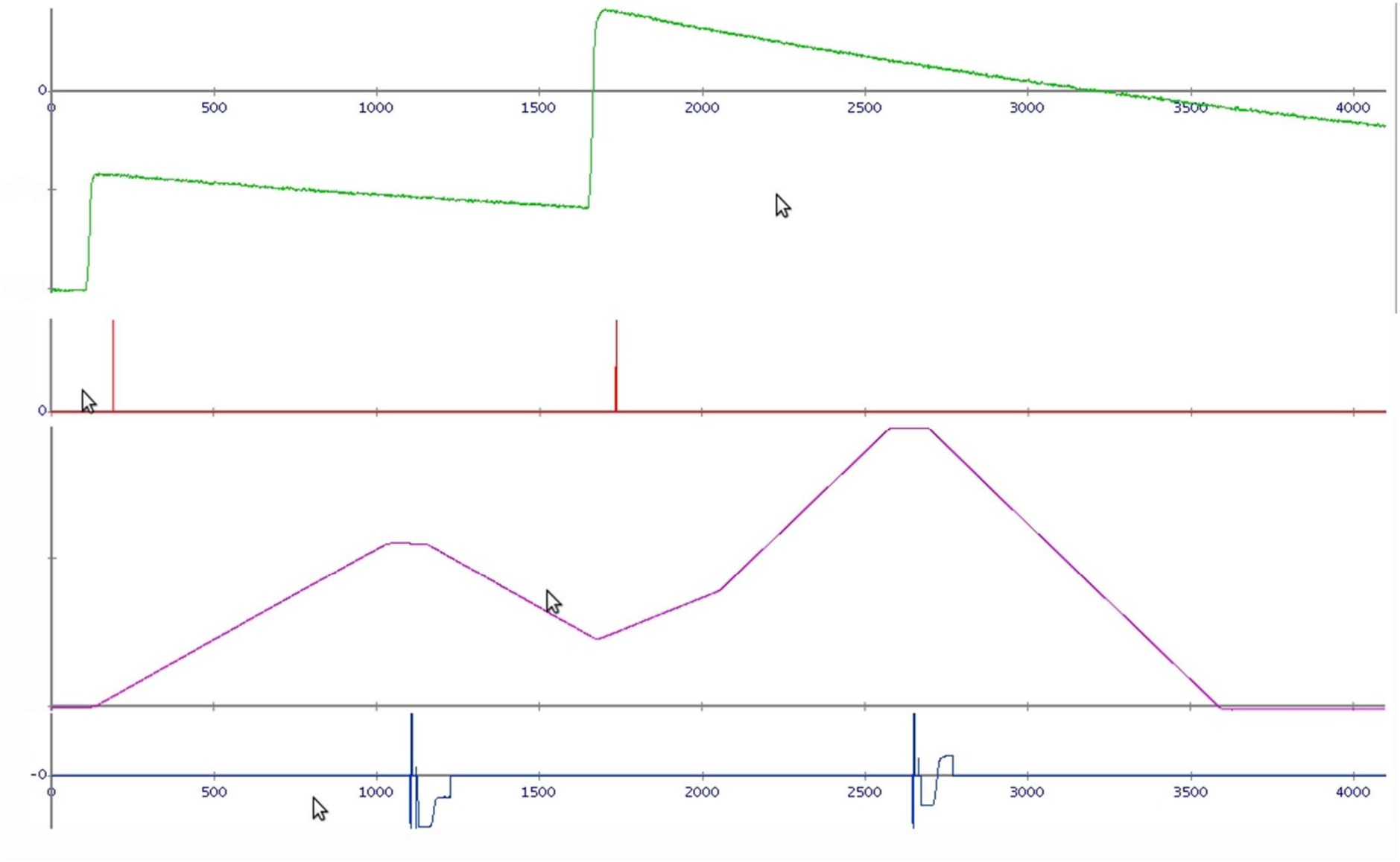
BER Tester



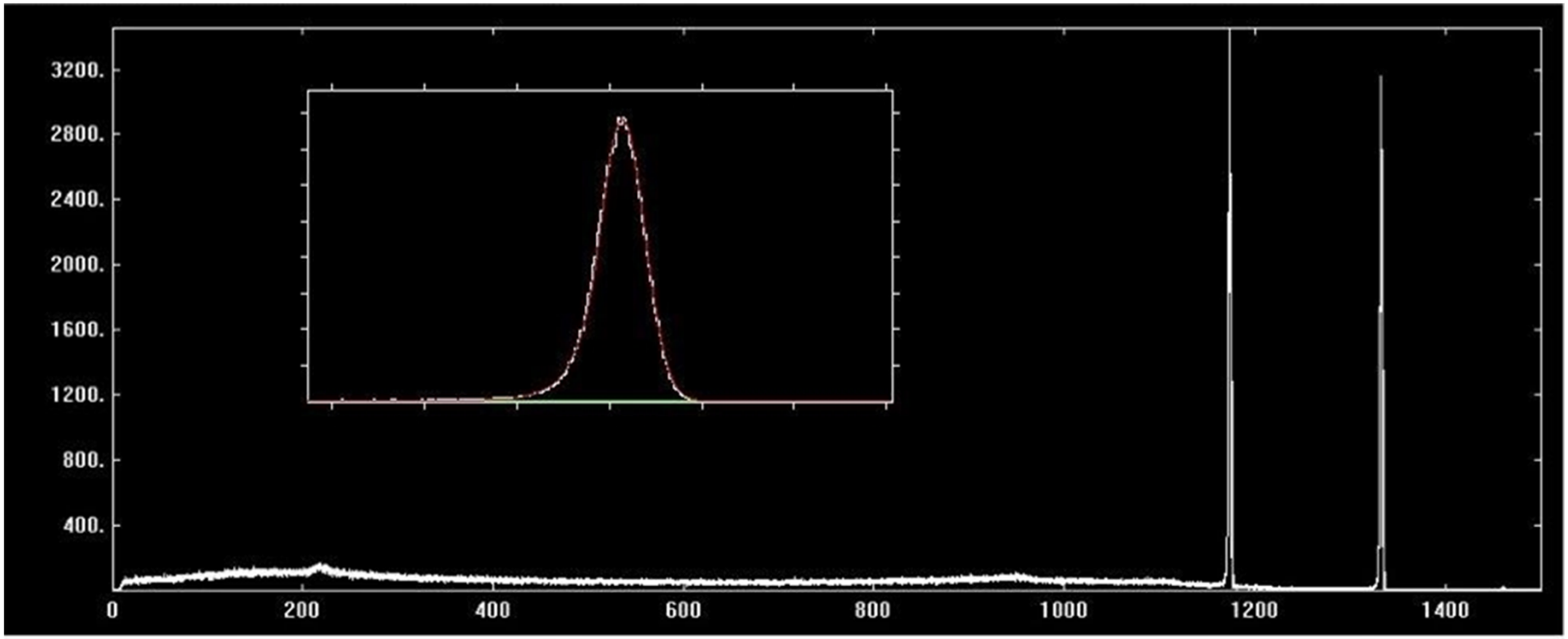
Tests

- Basic connectivity
- Signal integrity
- PCIe host interfacing
- Power distribution, integrity and consumption
- Ventilation and cooling
- Compatibility with AGATA digitizers
- Dual-port RAM interfacing (ongoing)
- GTS support
- BER on all high speed lanes

Tests : processing example



Tests with ^{60}Co source




```
25  spec__1-32768-UI__ener.spec    0  UI    1    (D:\zData\testACQ\101117\spec__1-32768-UI__ener.spec)
26  GFit         2.215     0.00000   0.00169       2.260     1.823 &      1.73    24.358    24.397    49.720
    0       86471.737   14352.762    24.397    1332.532     2.265 |    516.37    0.0516    0.0958    0.0048    0.0089
```

Status

- HW:
  - Almost completely qualified
  - Card ready for pre-production in one month
  - GTS “flavour” not tested yet
- FW:
  - Ver. 1.0 almost ready for online deployment
    - GTS alignment support missing
    - The same FW has been used for hardware qualification
    - Will be qualified with present and new digitizers
- SW:
  - Integration with DAQ : TBD
- Slow Control :
  - TDB
- Run Control :
  - TBD

Impact on present AGATA readout & Issues

- The card is 100% compatible with present digitizers
- The present Linux driver for the ATCA readout has been modified to drive the new card
  - The card can be fully fitted to AGATA DAQ software
- The GTS tree software must be updated
- The present slow control and run control must be adapted for the new card
- All startup, reset, monitor procedures must be updated
- Integration and commissioning requires 6-8 months work whose manpower is missing
- Maintenance : ?

Conclusions

- A brand new FEE is alive and kicking
- Although HW is working fine still a lot to do on the SW side for integration
- Manpower is THE urgent issue to address
- Still unclear (to me) how, who and when to do the integration, commissioning, maintenance, training, …