Signal Processing and Digitization of the Analog Front-End Data

Peter Wieczorek

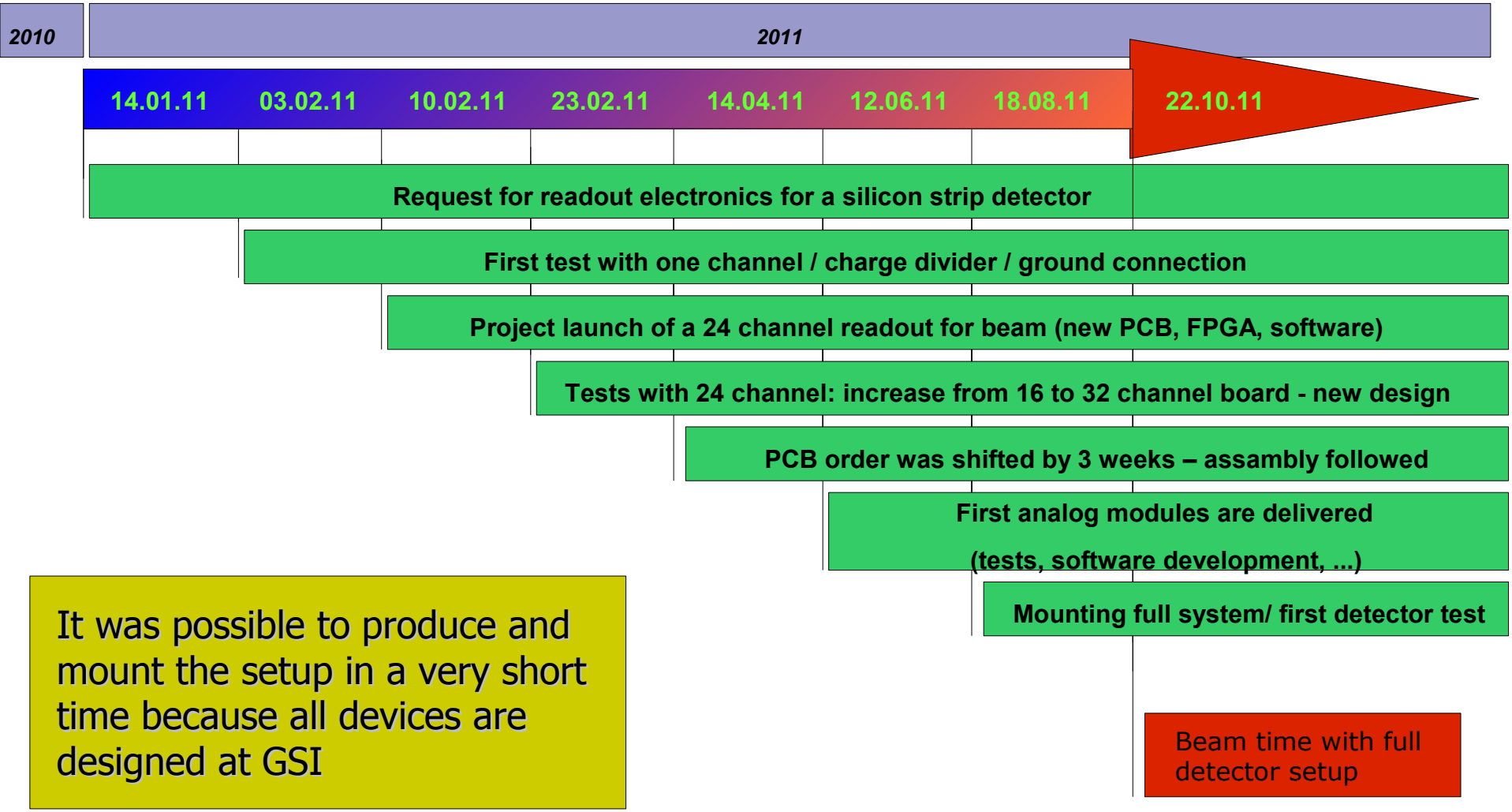
GSI Experiment Electronics

ASIC Design

Overview

- Time schedule of the electronics development
- Electronic setup
  - Analog readout
  - Digitization of the analog data
  - Data processing in FPGA – overview
  - Programming (APFEL ASIC and ADC CM - voltage)
- First measured results with detector
- Summary

Project History



It was possible to produce and mount the setup in a very short time because all devices are designed at GSI

Beam time with full detector setup

Working Group (Electronics)

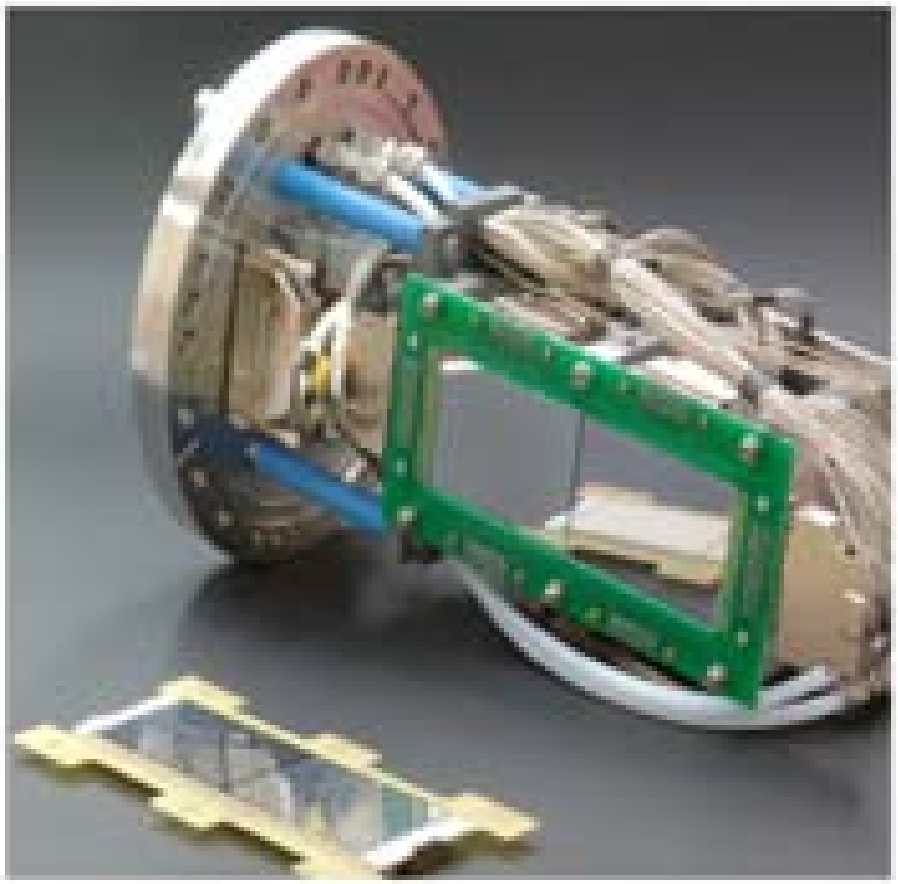
- **Hardware:**
  - Hoffmann, Jan – (EE)
  - Wieczorek, Peter – (EE)
  - Löchner, Sven – (EE)
  - Deppe, Harald – (EE)
  - Flemming, Holger – (EE)
  - May, Gerhard – (EE)
  - Skott, Peter – (EE)
  - Zeitträger, Gabriele – (EE)
  - Dugan, Dragutin – (EE)
  - Schindler, Helga – (EE)
  - Voltz, Sabine – (EE)
  - Simons, Carmen (Detector Lab)
- **Software:**
  - Kurz, Nikolaus – (EE)
  - Minami, Shizu – (EE)
  - Linev, Sergey – (EE)
  - Adamczewski-Musch, Jörn – (EE)
  - Rusanov, Ivan – (EE)
  - Ott, Wolfgang – (EE)

TASCA Experiment

Search for new elements: 115 to 120
Main detector: Silicon strip detector
In total: 320 strips
(320 readout channels)

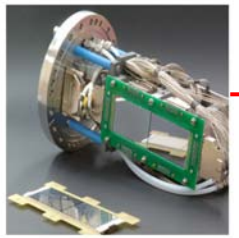
Requirements

Detector:	Silicon strip
Energy range:	0.5 MeV – 200 MeV
Input charge:	9.6 fC – 3.8 pC
Required resolution:	25 keV
Detector cap.:	80 pF
Operation temp.:	RT
Number of channels:	320



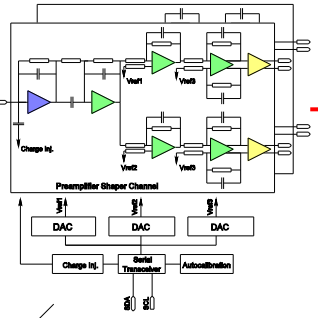
TASCA – Electronic – Setup

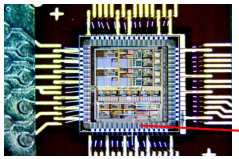
Detector



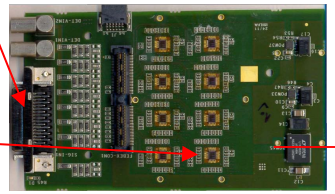
Silicon strip detector
In total: 320 strips

ASIC preamplifier



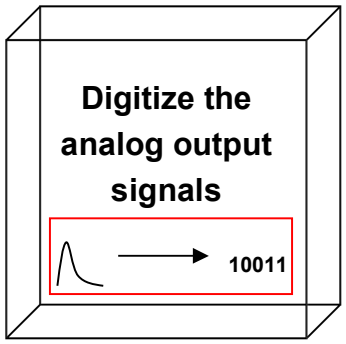


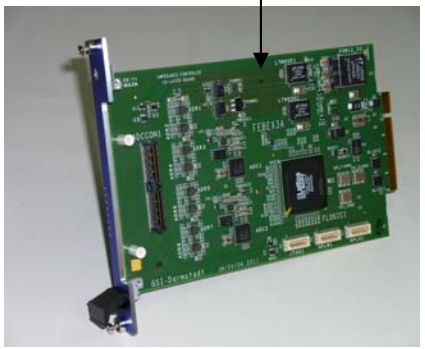
Charge sensitive preamplifier ASIC



8 ASICs per PCB
40 PCBs

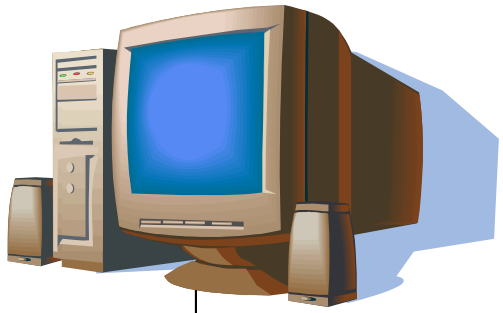
Digitizer board (FEBEX) and trigger logic





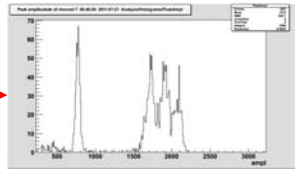
40 FEBEX PCBs

DAQ system and analysis



Connection to the Data Acquisition MBS and GO4 analysis

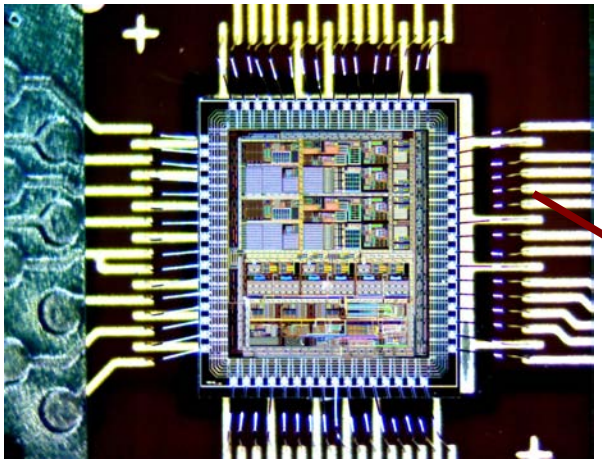
One PCI PCB



Spectra analysis with GO4

Analog Readout

Analog Readout Board for TASCA

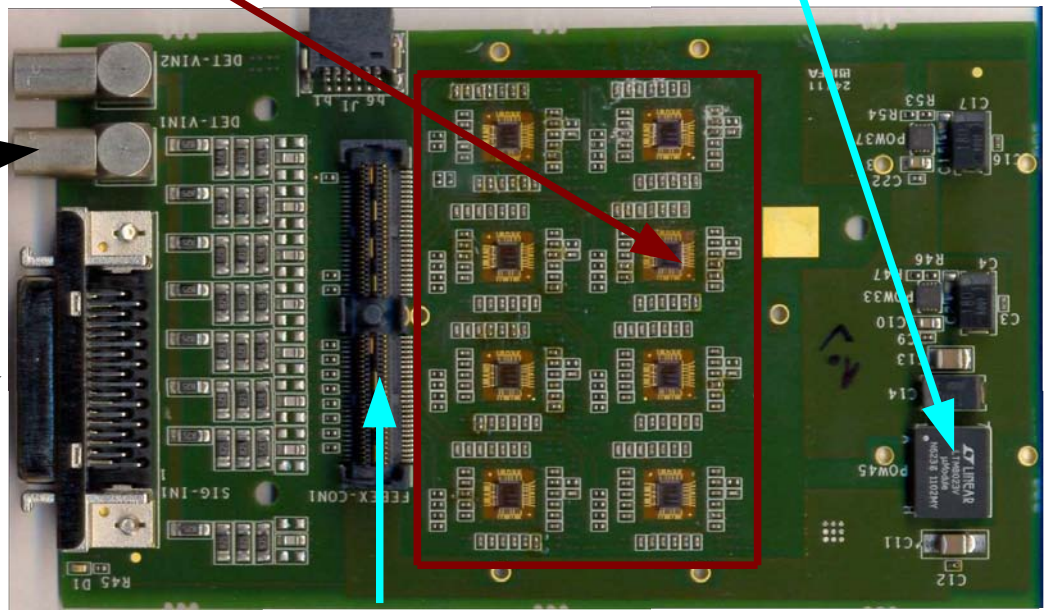


8 charge sensitive preamplifier ASIC

Power regulator (3.3 V)

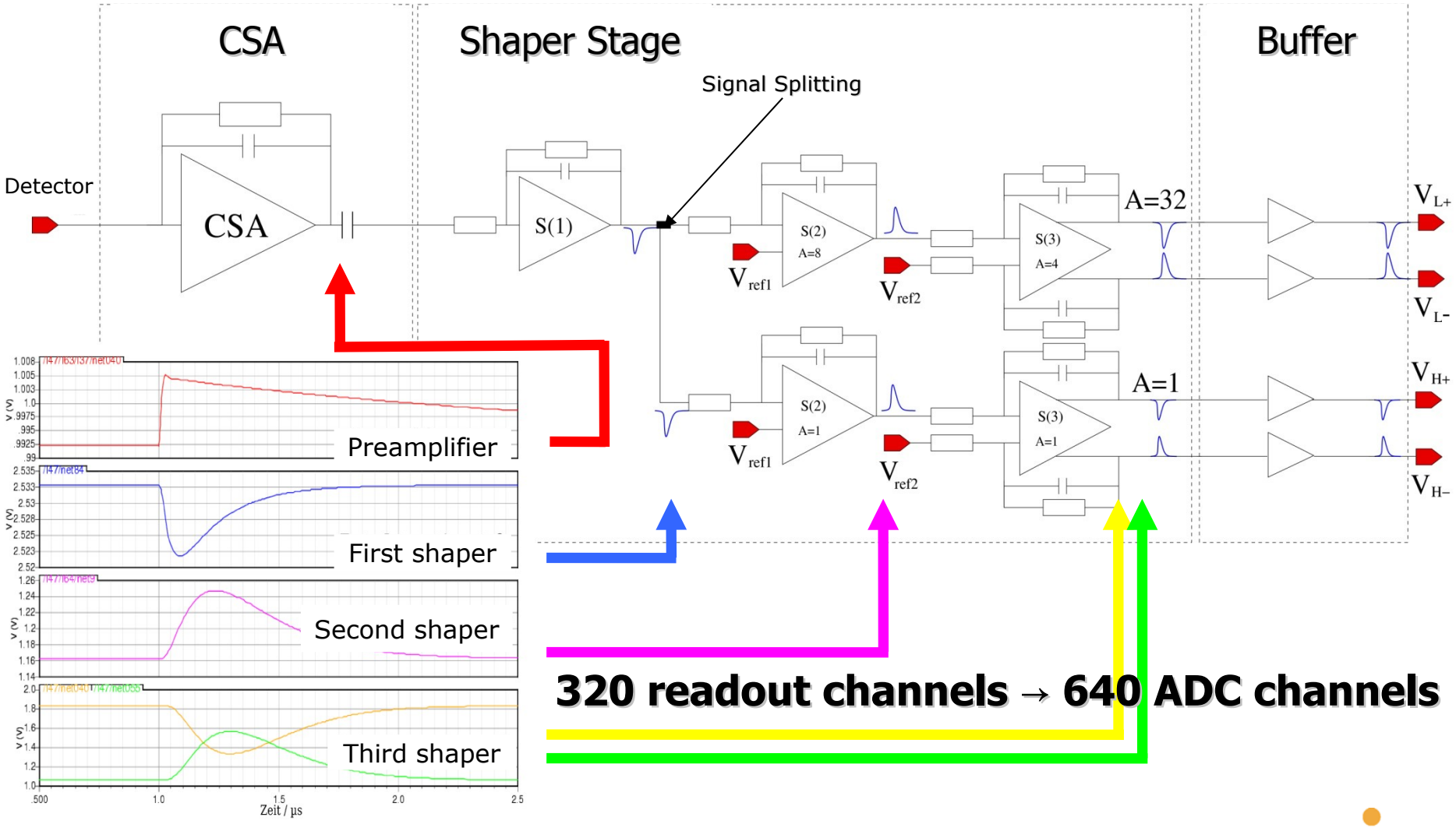
HV input

Detector connection



ADC connection

Readout Channel



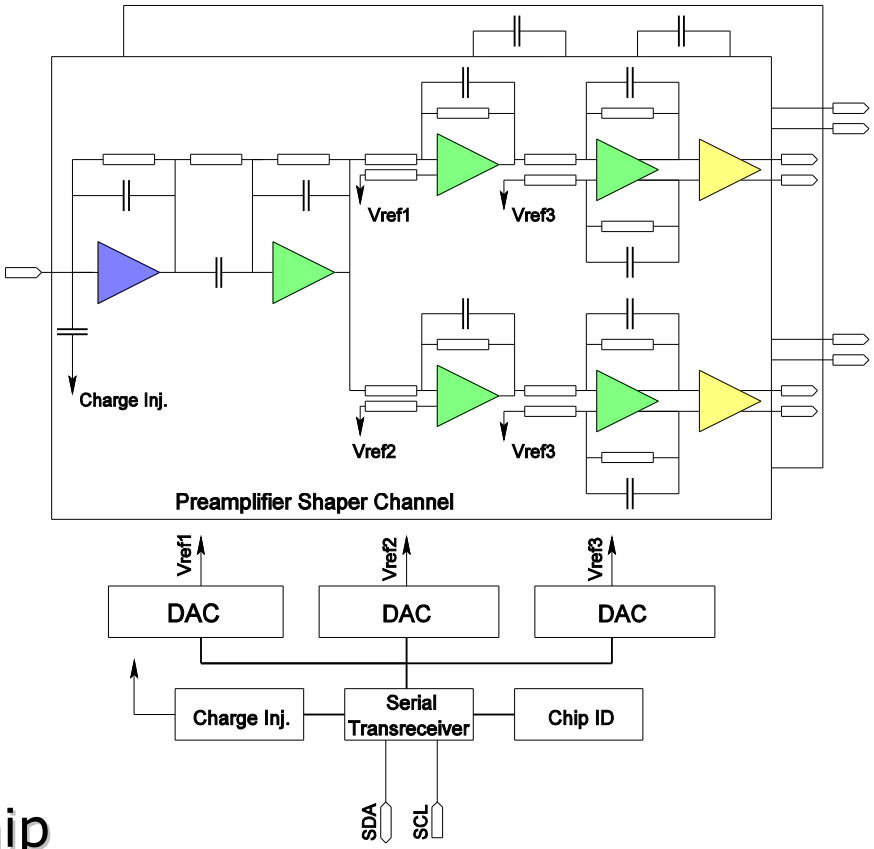
Chip Overview

Analog Readout

- Each channel consists of
  - Charge sensitive amplifier
  - Third order shaper stage
  - Differential output
  - 2 different paths (amp.: 1 & 32)

Digital Part (controlled with FPGA)

- Serial interface for
  - Trigger of the autocalibration
  - Optional charge injection
  - Read and write of DAC settings
- Chip ID on chip



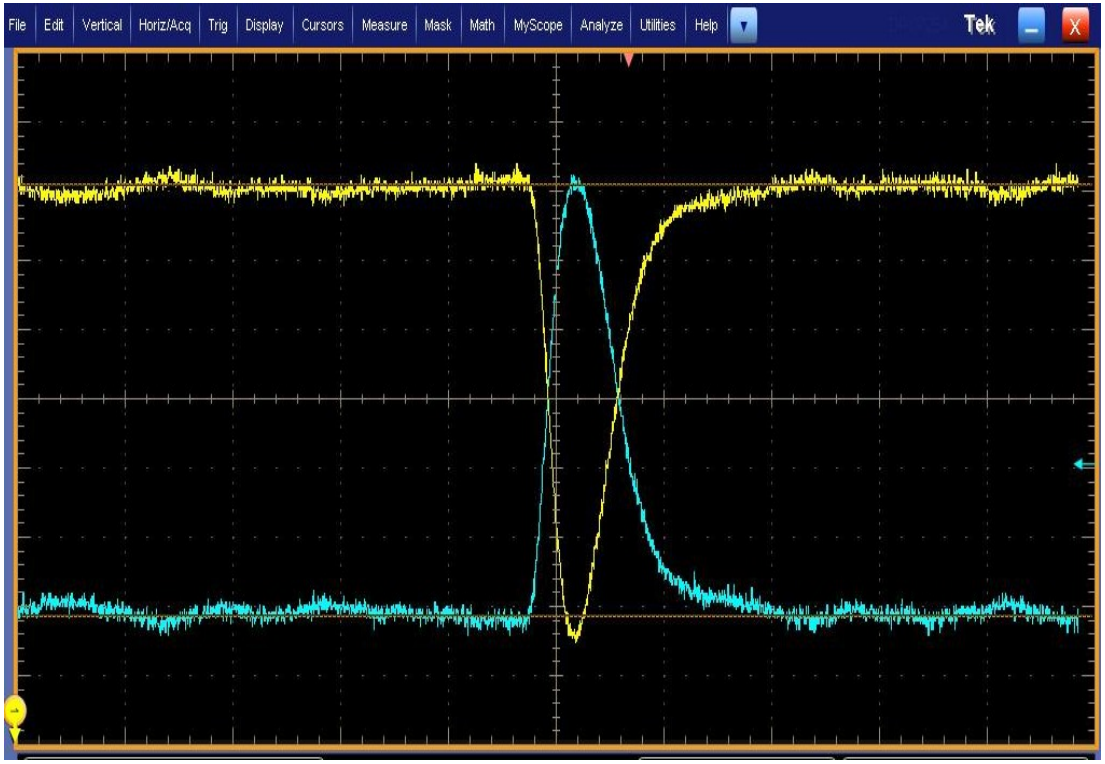
2 equivalent analog channels per chip

Results of Characterisation

	Results @ T=-25°C	
Gain path 1:	10.20±0.03	mV/fC
Gain path 2:	0.322±0.017	mV/fC
Rise time:	127±3	ns
ENC(C_{det} = 280pF):	0.67	fC
Max. input charge:	6.89	pC
Dynamic range:	>10000	1
Power:	56.4±0.2	mW/channel

Measured Analog Signal

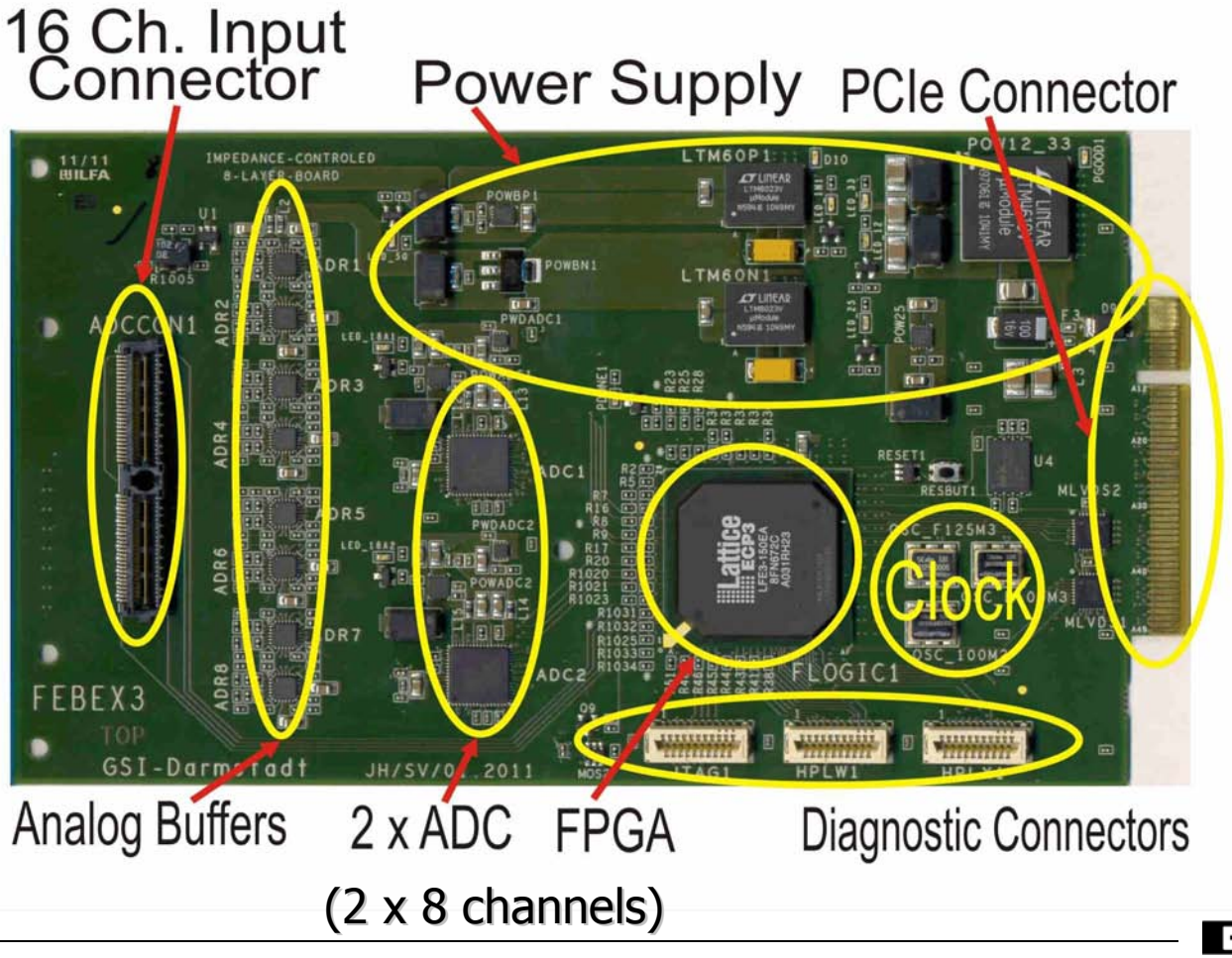
- **Differential output signal**
- **Peaking time: 250 ns**
- **Pulse width: 1 µs**



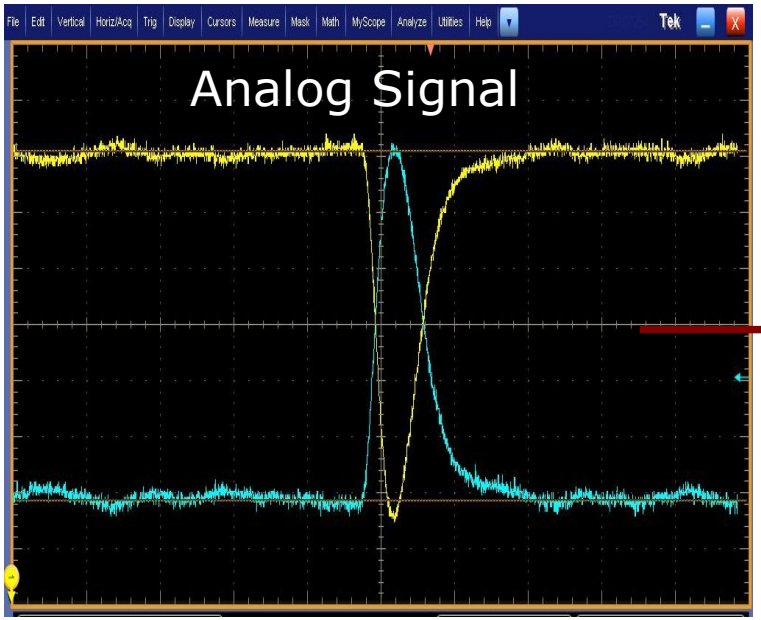
Digitization of the Analog Data

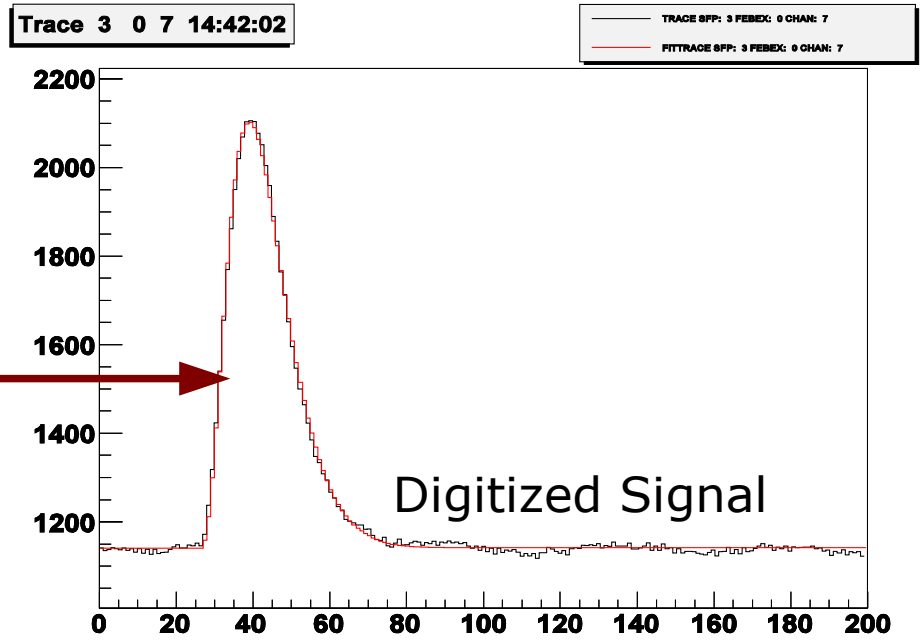
Digitizer Board – FEBEX

- **Designer: Jan Hoffmann**



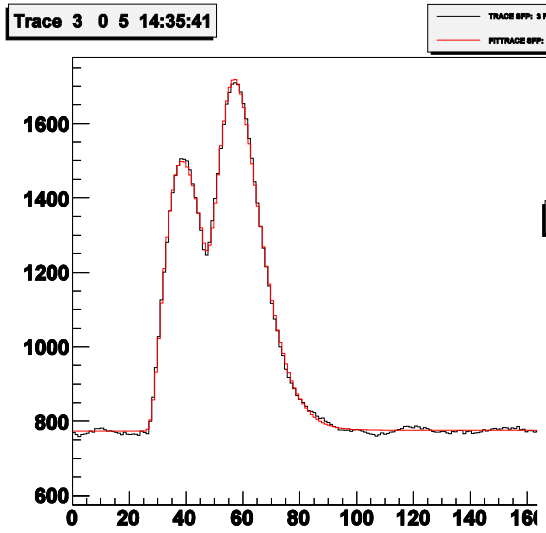
Analog to Digital



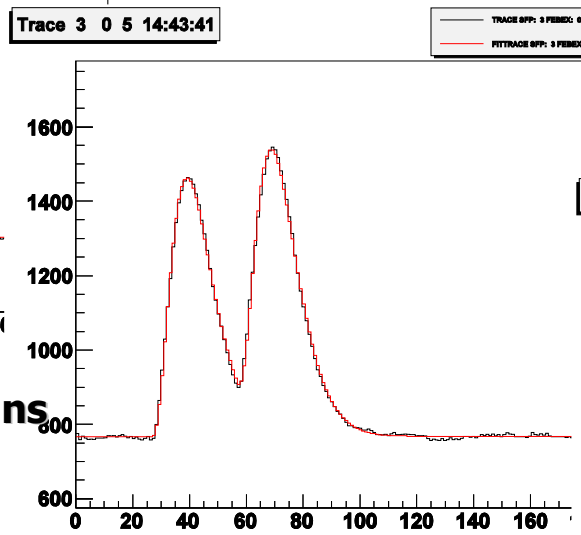


The FEBEX board read out the analog, differential signals, substract the values and send the trace to the MBS

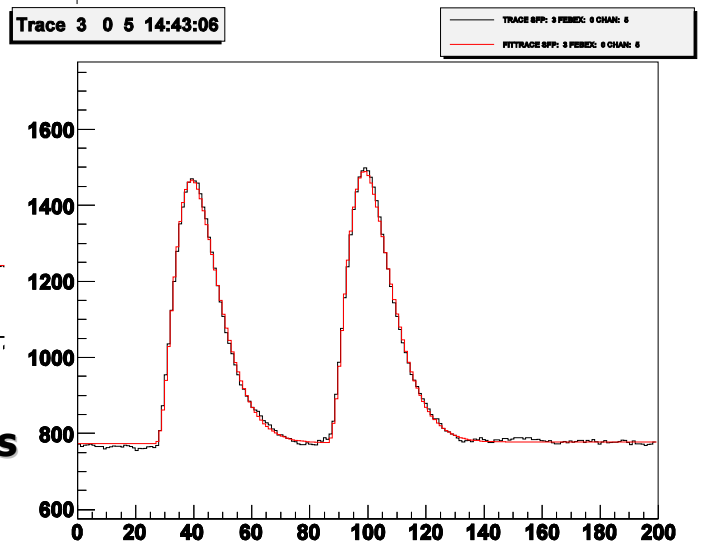
Multi Pulse Fitting



Pulse difference: 350 ns



Pulse difference: 500 ns



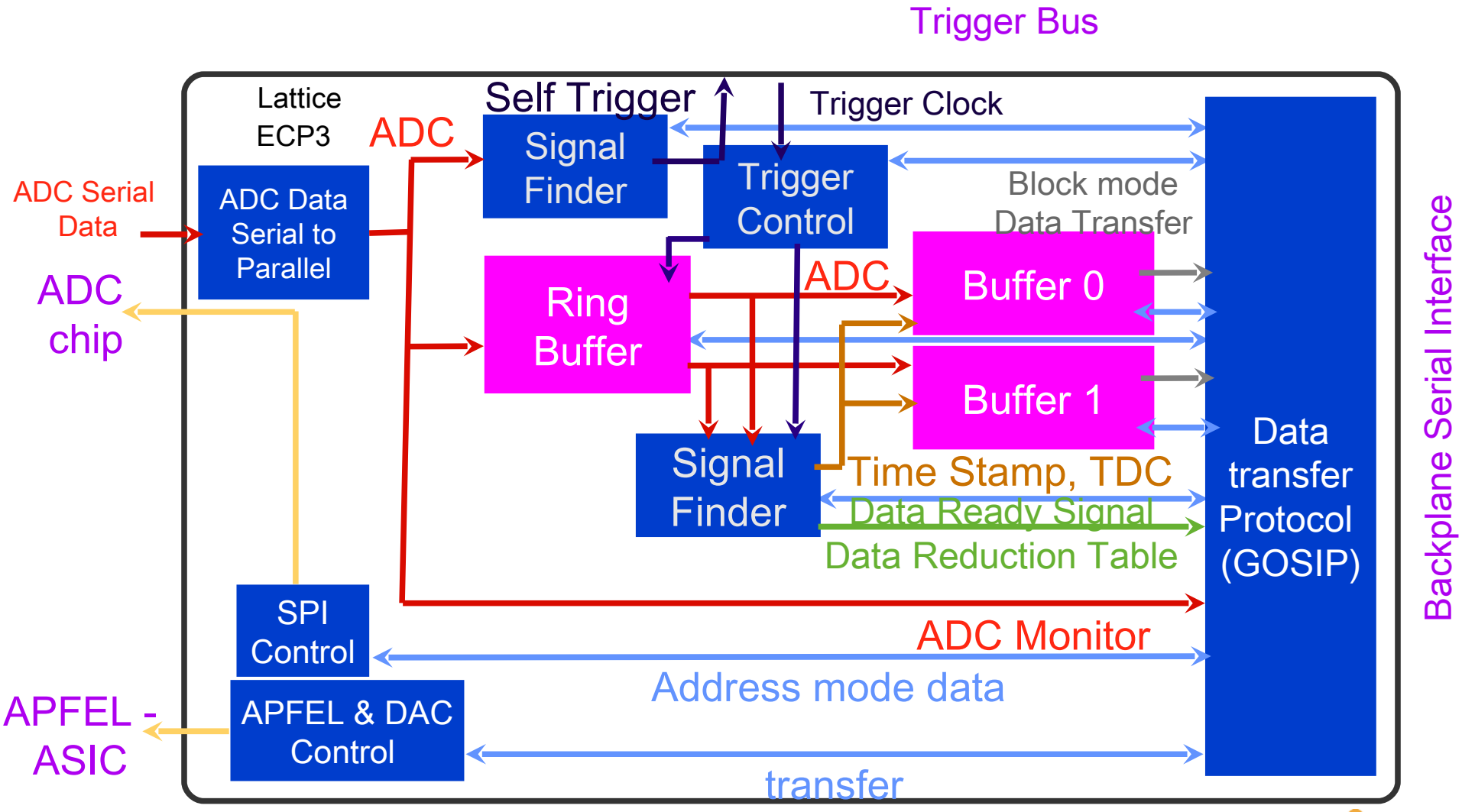
Pulse difference: 1000 ns

Go4 online - offline analysis

Data Processing in FPGA

Thanks to Shizu Minami

Overview of Data Processing in FPGA



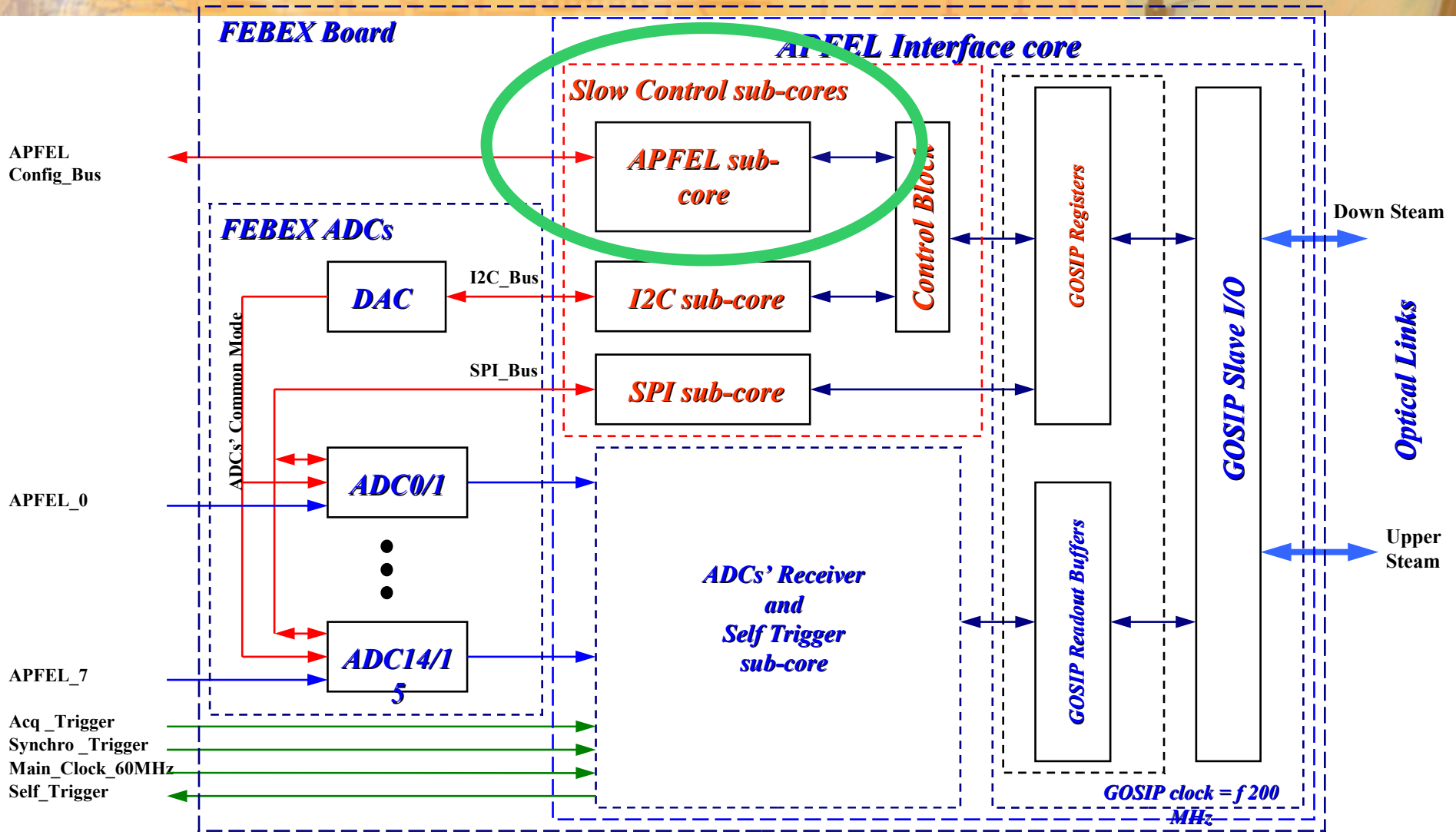
Data Processing in FPGA

- Data transfer protocol (GOSIP) - 2GBPS serial data transfer with 2 modes
  - Address mode - read/write access for slow control
  - Block mode - fast read access to readout buffers
- Ring buffer - temporally storage for ADC data before trigger signal
  - ADC data which comes max. 34 µs before trigger are able to be kept for next processing
- Readout buffer (Buffer0/Buffer1)
  - Double buffer to minimize deadtime
  - 4096 32-bit words/ch - max. 8192 samples ≈ 136µs
- Signal finder with 2 methods
  - 3 step -consecutive 3 samples need to be higher than previous one by specified threshold
  - Average - average of 8 samples for signal need to be higher than average of 16 samples for baseline by specified threshold - with 4 sampling frequency modes - 60, 30, 15 and 7.5 MHz
- Data reduction
  - ADC channel with which no signal is found by Signal Finder can be skipped by Block mode data transfer

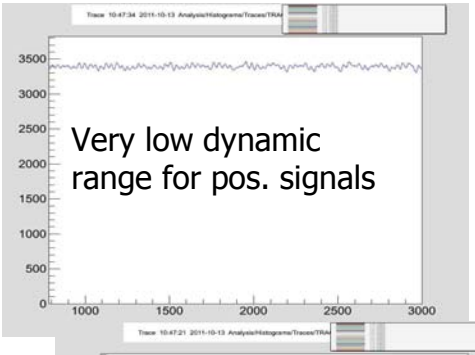
APFEL DAC Programming with FPGA

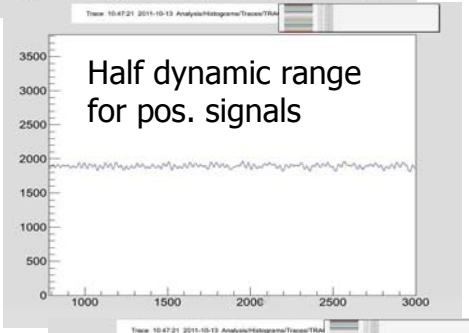
Thanks to Ivan Rusanov

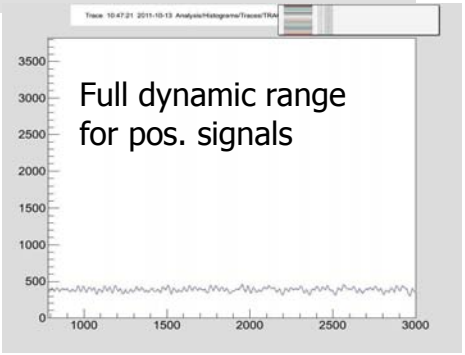
APFEL Interface: Slow Control



APFEL Programming







- To use the ASIC in the temperature range T= – 30 °C to + 30 °C programming of the ASICs at the current temperature is needed to cover the full dynamic range

- The programming also allows to shift the DC level to use the full ADC range
  - Ivan developed an I²C interface on FPGA
  - Slow control to read and write APFEL ASIC values

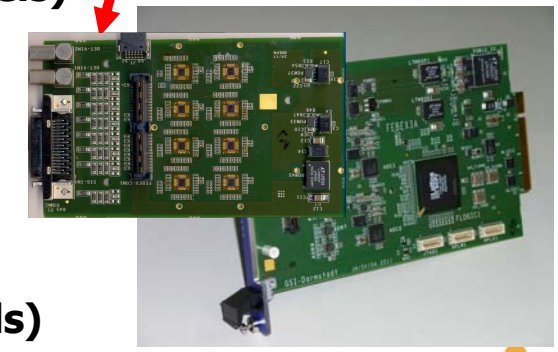
- A setup program developed by Nick allows
  - Set an autocalibration for all channels in serial (320 ASICs)
  - Shift the baseline for an optimal ADC range for all channels chip by chip

System Measurements

System Overview

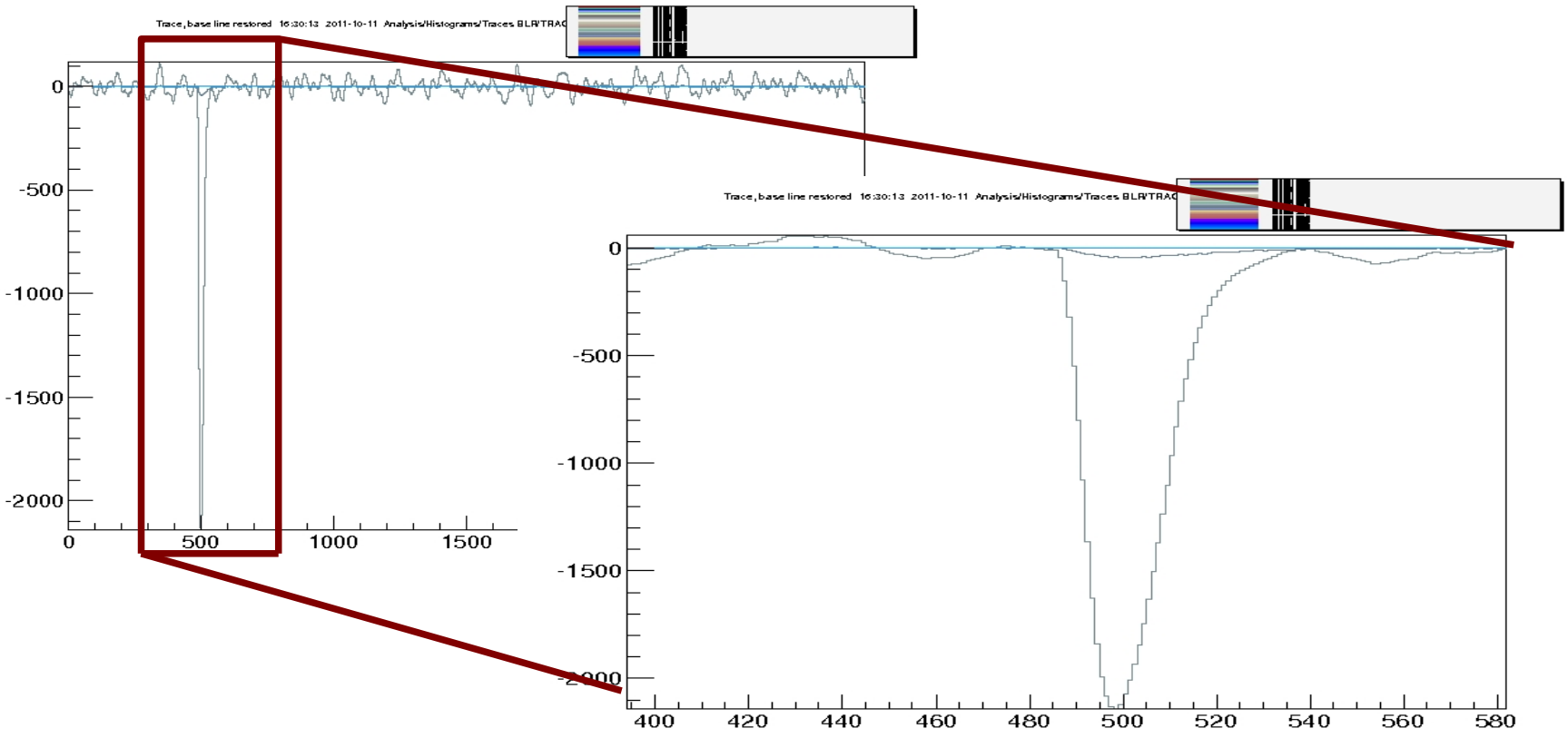
- Full system
  (640 ADC channels)

- Part of the system
  (160 ADC channels)



- Readout card
  (16 ADC channels)

Measured Trace with α – Source



Measured with a small detector of 64 strips

Summary

- During 10 months a full readout setup was developed and tested for the TASCA experiment

Thanks to all who were/are involved in this project

Next step:

- Mount the readout setup with the new detector which will arrive end of October