The 120 and 119 MBS Data Acquisition Systems at TASCA

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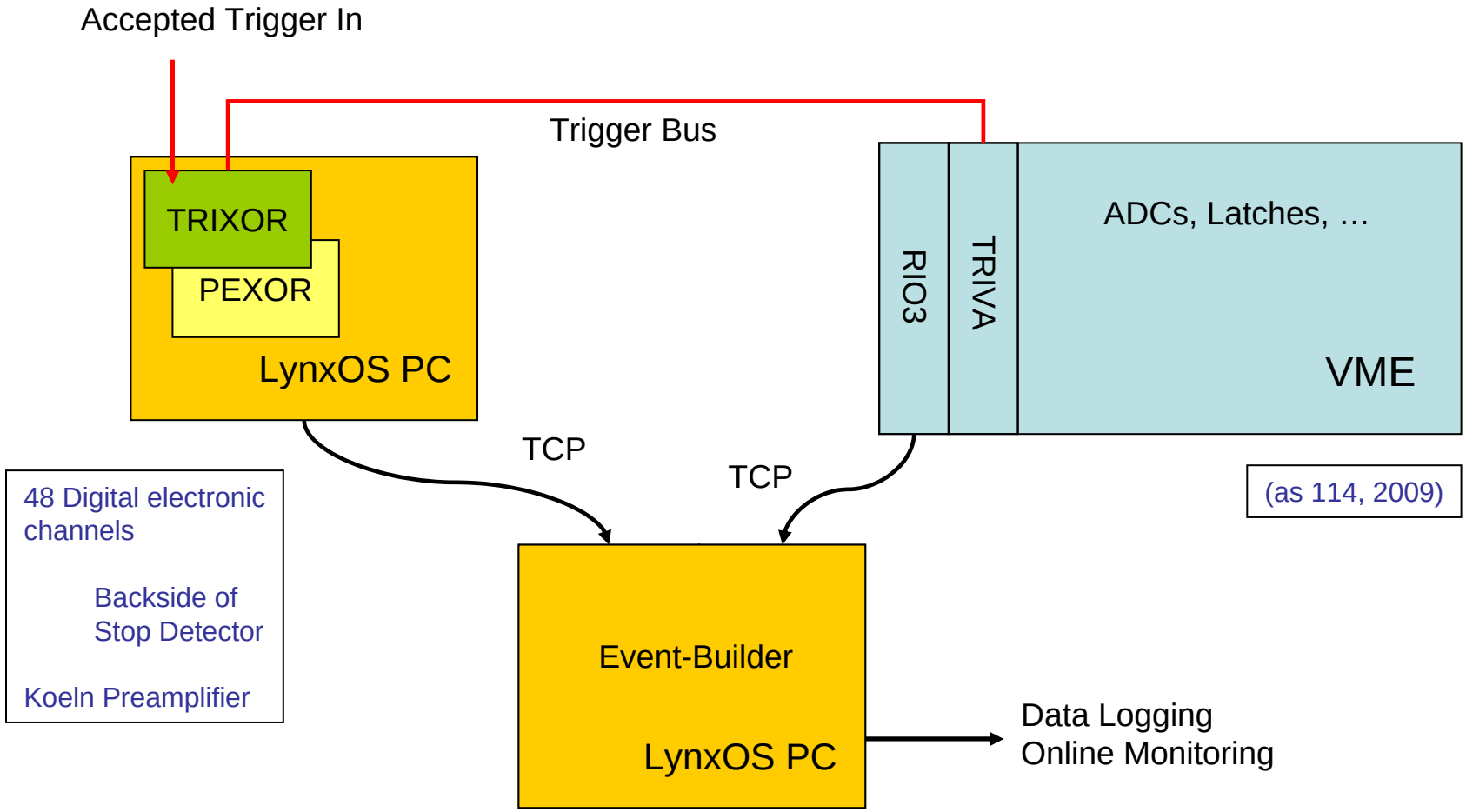
Most members of EE

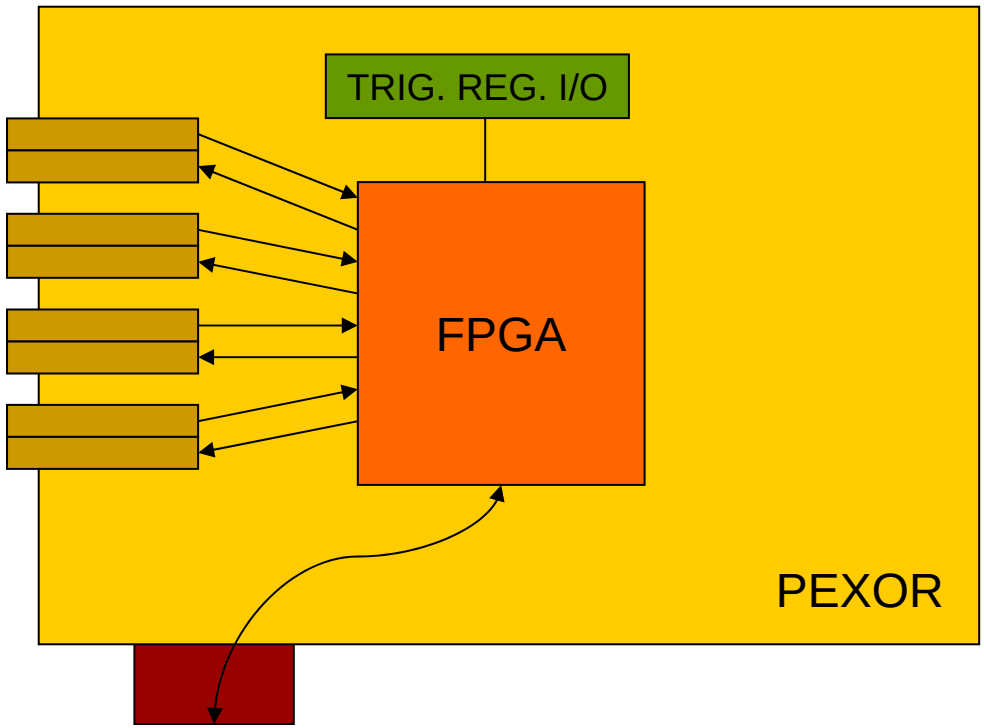
120 MBS DAQ 2011



PEXOR: Front End Data Collector

4 SFP Fiber pairs
each 2.5 Gbit/s to
connect 4 x 256
front end boards
at maximum

after 10/8 coding:
200 MB/s payload speed
per SFP



4 Lane PCI Express
> 600 MB/s FPGA -> PC DRAM payload speed

PEXOR


GSI-Darmstadt
JH/SV/II.2009
TNS
PEXOR3
JTAG1
SFP1
HPLA2
HPLA1
AUXFL1
RESET1
DIS1
VTT2
SFP2
SFP3
SFP4
11
LTM1A
LTM33
VTT1
RCLK100
RCLK125
PEXCON1
AUX_POW1
POW_25

TRIXOR

TRIXOR: - Identical functionality as TRIVA3/5/7

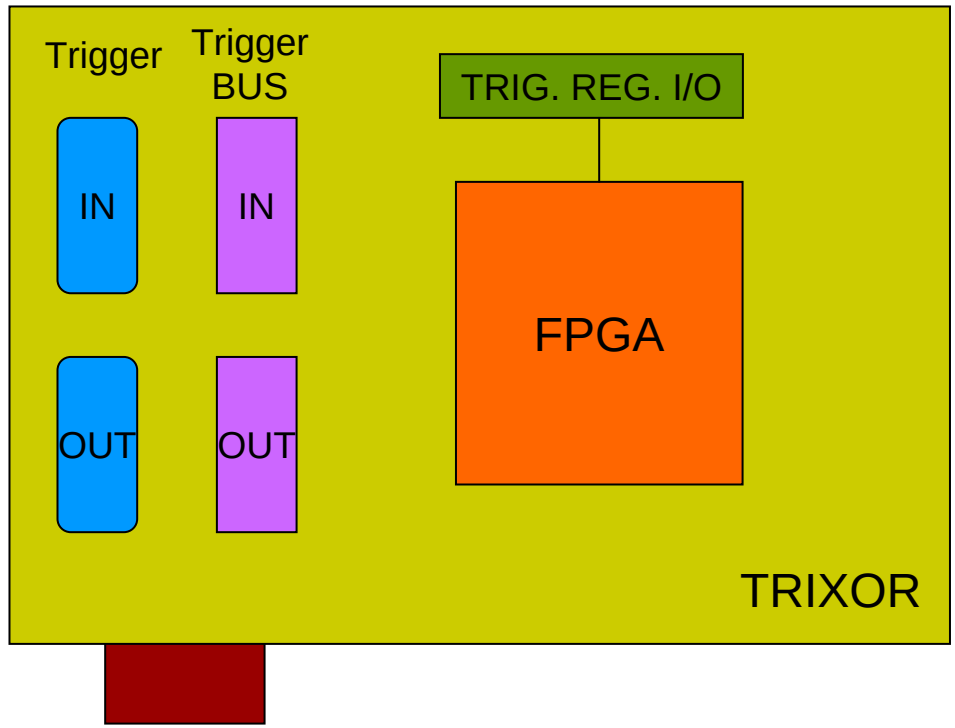
- Can be plugged in PCI Express or PCI slots. Takes only power.

- Works as master (trigger from input) and slave (trigger from trigger bus).

- Several TRIXOR and TRIVA can be inter-connected via the trigger bus to compose synchronous bigger MBS systems.

- Communication with the TRIXOR via PEXOR and the Trigger Register I/O connector.

- Accepted trigger send a signal via the Trigger I/O connector to the PEXOR, which is then transformed into a PCI Express interrupt to notify the PC readout processor.



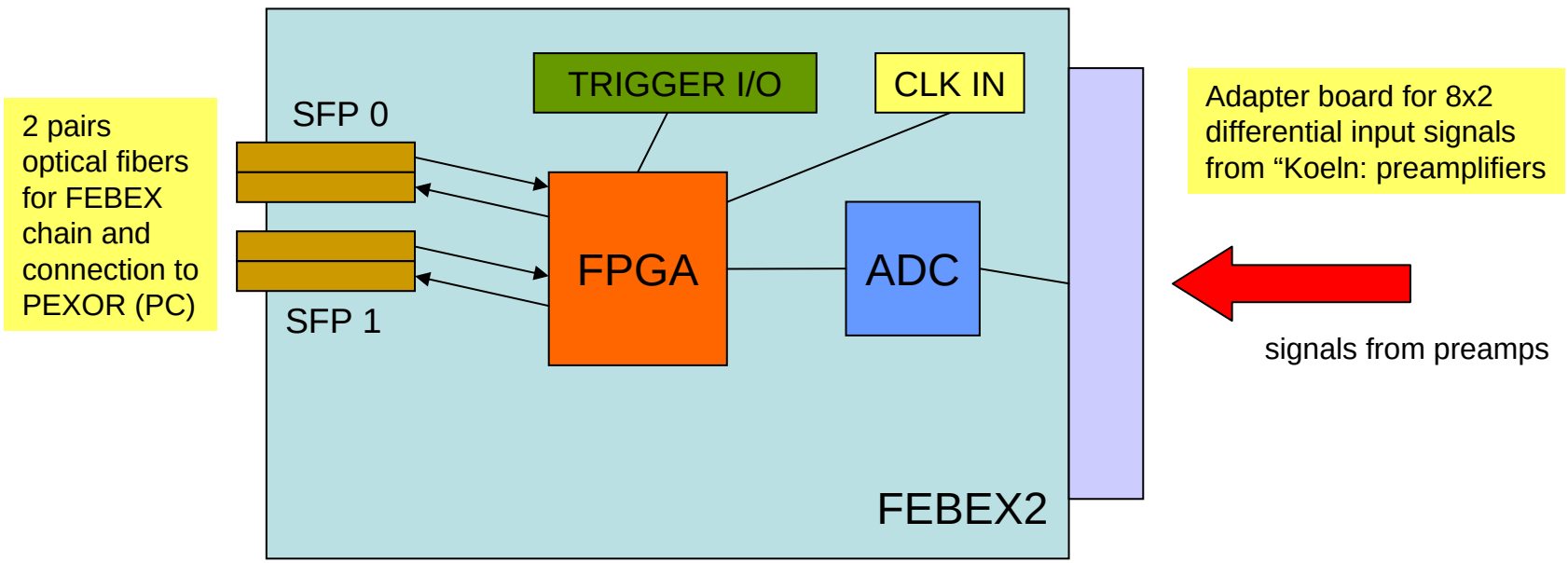
TRIXOR


TRIXORFP1
ECLOUT1
TRB1
TO_FRONT
ANC1
GT
SD
MT
CL
HPLW_1
LOGIC_1
JTAG1
TO_PC1
X-FRONT1
TRIXORPCIE1
AUX_POW1
F2

PEXOR-TRIXOR-FEBEX Test Setup (FEBEX not shown)

FEBEX2: Pipeline ADC Front End Board

8 Channel pipeline ADC
60 MHz, 12 bit, -1V - +1V differential inputs



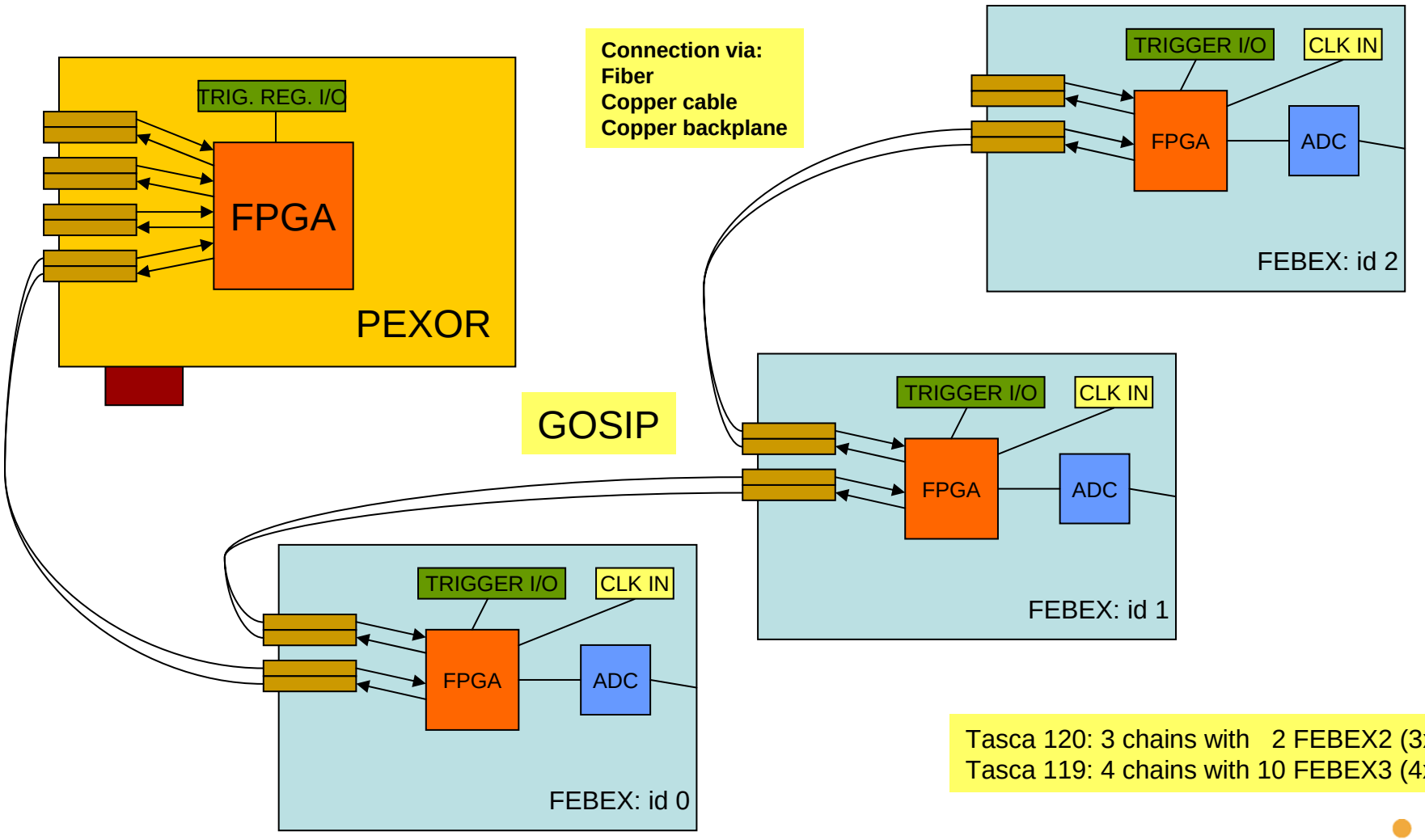
Purpose: Provide fast “digital electronics”.
Filter “continuous” data streams from ADCs with respect to trigger windows.

120: 6 FEBEX boards (48 channels)

FEBEX2


FEBEX2
8-LAYER-BOARD
IMPEDANCE-CONTROLED
LINEAR
LTM4619V
µModule

PEXOR-FEBEX2 Connections

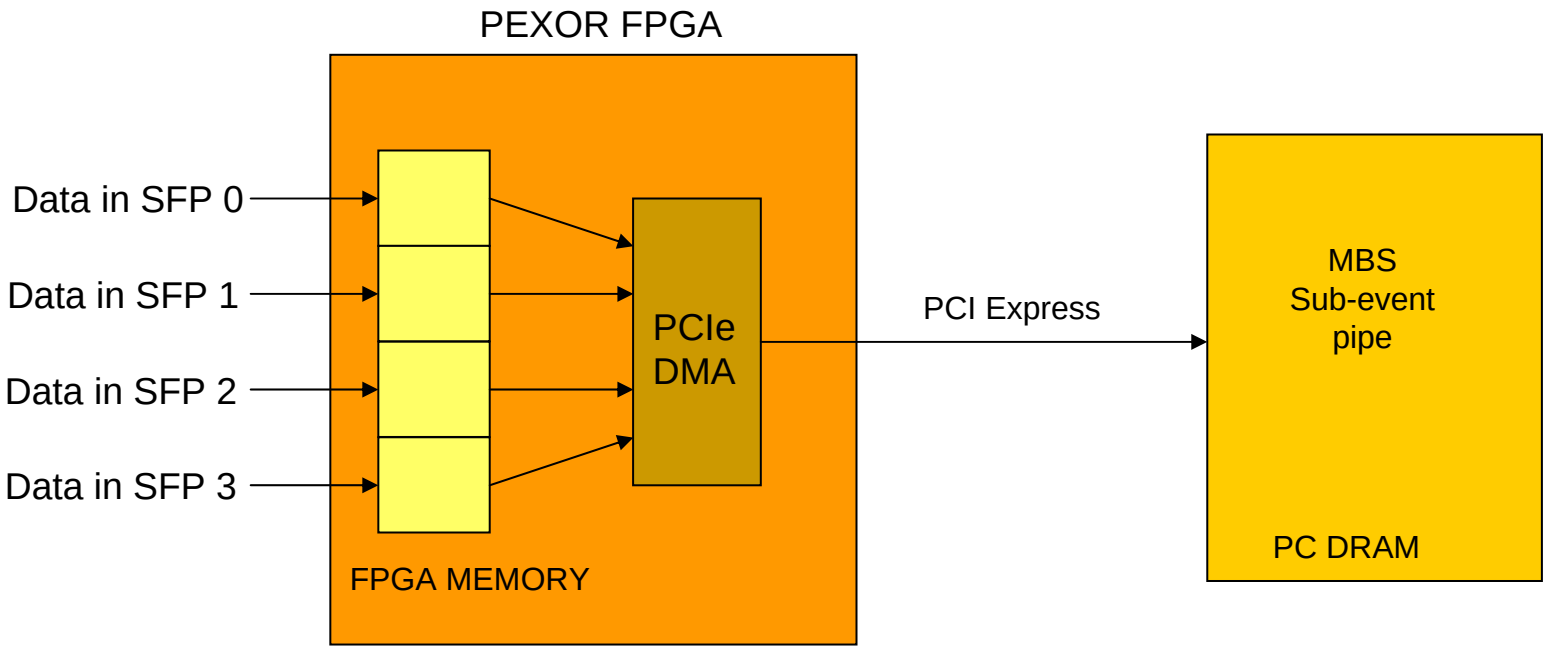


Tasca 120: 3 chains with 2 FEBEX2 (3x2)
Tasca 119: 4 chains with 10 FEBEX3 (4x10)

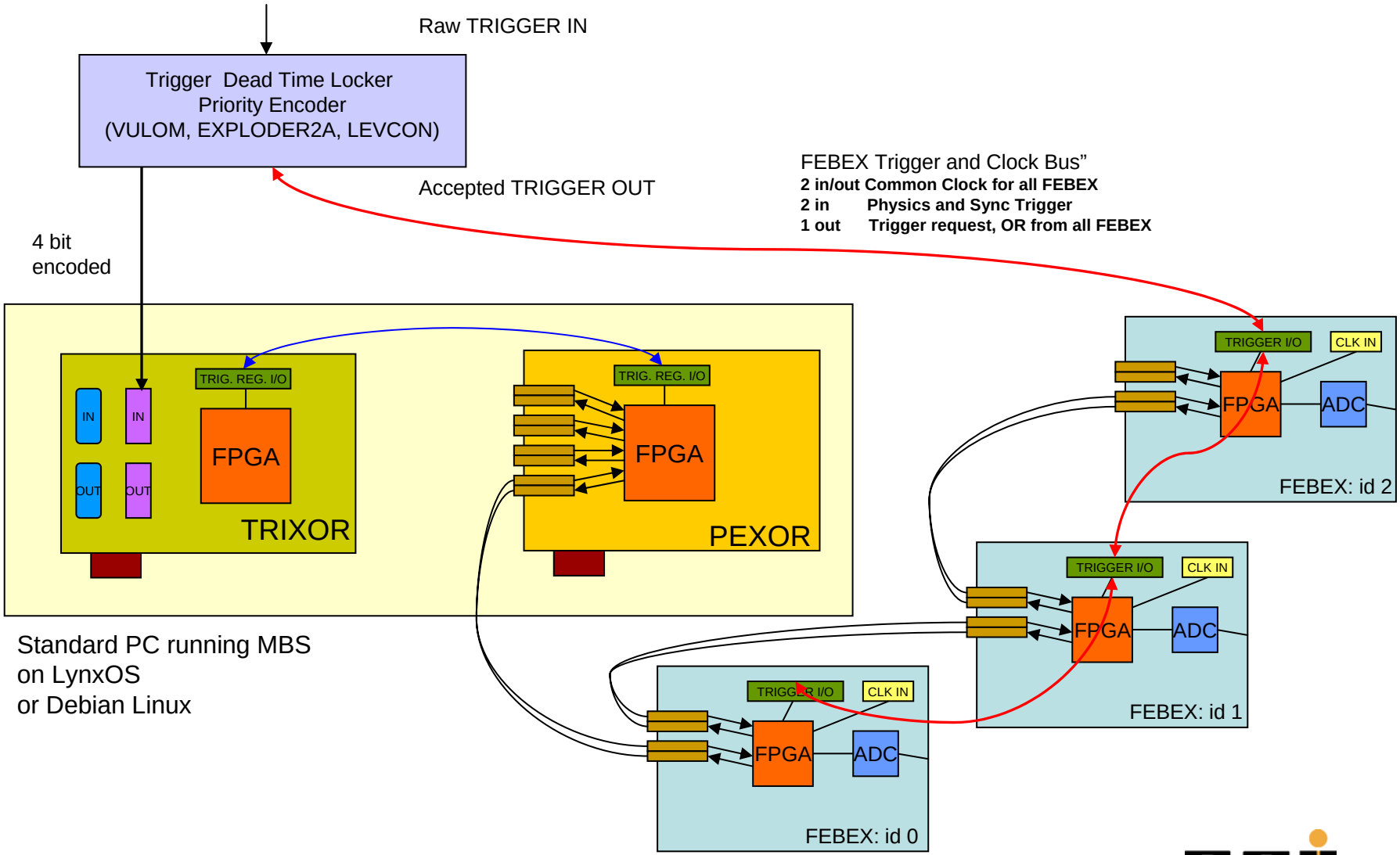
Fast Token Data Transfer Options
PEXOR -> PC DRAM / MBS

1) Parallel token data sending on for all connected front-end chains. Sequential DMA, initiated from MBS user readout function, from PEXOR to PC DRAM. Used for “small” data sizes.

2) Sequential token data sending for all connected front-end chains. Sequential DMA, automatically initiated by PEXOR FPGA from PEXOR to PC DRAM. Used for “big” data sizes. Limit is PC DRAM not PEXOR memory.



Standalone MBS Setup



FEBEX2 Features

- 60 MHz, 12 bit, +- 1 V input signals
- ADC input circular buffer (per channel)
- Double signal trace buffer (per channel)

- I/O: IN (2): Physics trigger, sync. trigger
  - IN: Common clock (for hit timing)
  - OUT: Common clock (dedicated FEBEX as clock master, external clock master)
  - OUT: Trigger request from hit finder. OR from all channels (see below and next slide)

- Two hit finder (or self trigger) algorithms (3 step, trapezoidal filter)
- Dead time clear before readout (double trace buffer!)

- Data Output: Complete trace in trigger window and hit time (from common clock)

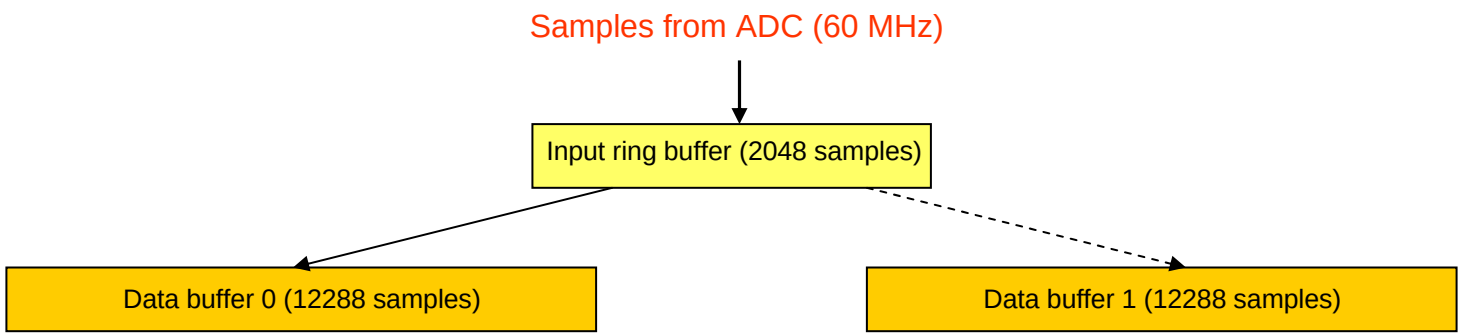
FEBEX2 Features (2), Setup Parameters

All features per channel:

	(120 Setup)
- Enable/Disable Channel	(enabled)
- Enable/Disable Self trigger (hit finder)	(enabled)
- Enable/Disable Data reduction	(enabled)
- Set positive or negative input signals	(negative)
- Even/Odd channel readout	(disabled)
- Set pre-trigger time (0 - 34 us, in nr. of ADC samples (1./60MHz := 16.7 ns)	(500 := 8.3 us)
- Set trace length (0 - 200 us, in nr. of ADC samples (1./60MHz := 16.7 ns)	(3000 := 50 us)
- Select Self trigger method:	
a) 3 step	(-)
b) trapezoidal filter, select one out of 4 different scanning frequencies 60 -, 30 -, 15 -, 7.5 MHz	(30 MHz)
- Self trigger Threshold (in ADC counts, 0.5 mV steps)	

FEBEX2 Signal Input Stage

FEBEX input stage implemented in FPGA for each ADC/Input channel:



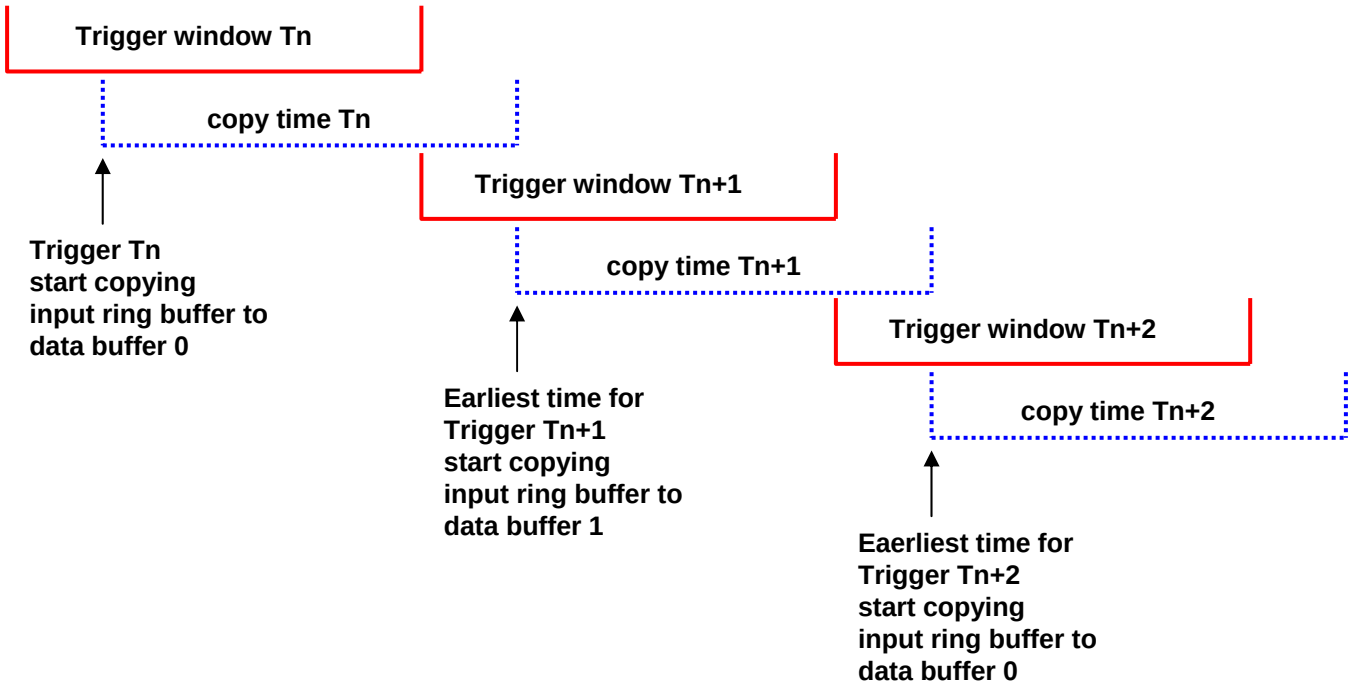
Input ring -, data buffer 0/1 for each ADC channel
Input ring buffer accepts ADC samples with the speed of the ADC without interruption
On occasion of a trigger, content of Input buffer is copied with the speed of the ADC in a toggling mode into one of the data buffers

Length of input ring buffer defines maximum pre trigger window: 60 MHz: 34 us

Length of data buffer defines the maximum trace length: 60 MHz: 200 us

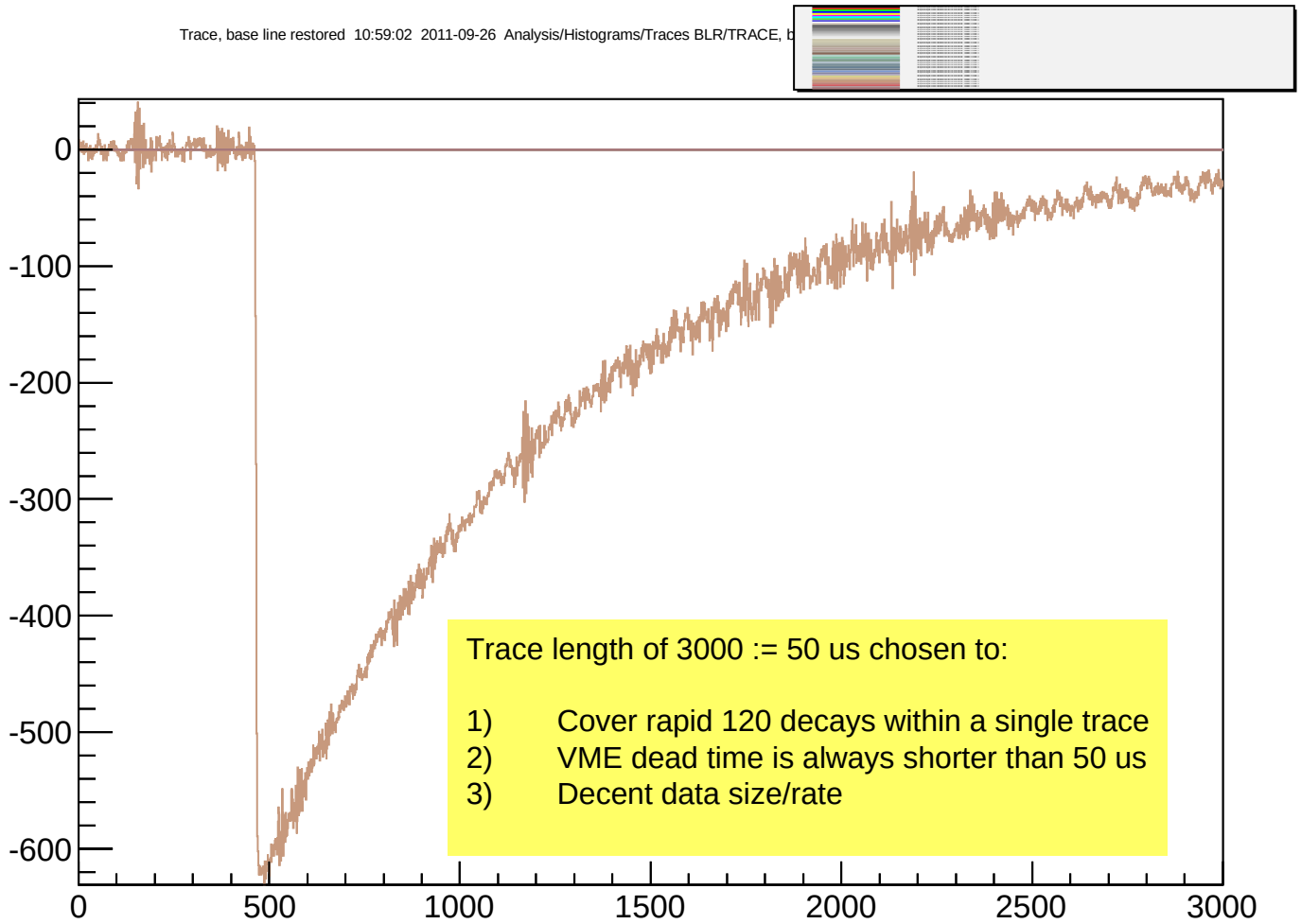
Double data buffer allows to accept next trigger/event BEFORE readout of actual trigger/event

Quasi Dead-Time free Data Acquisition with Trigger Windows

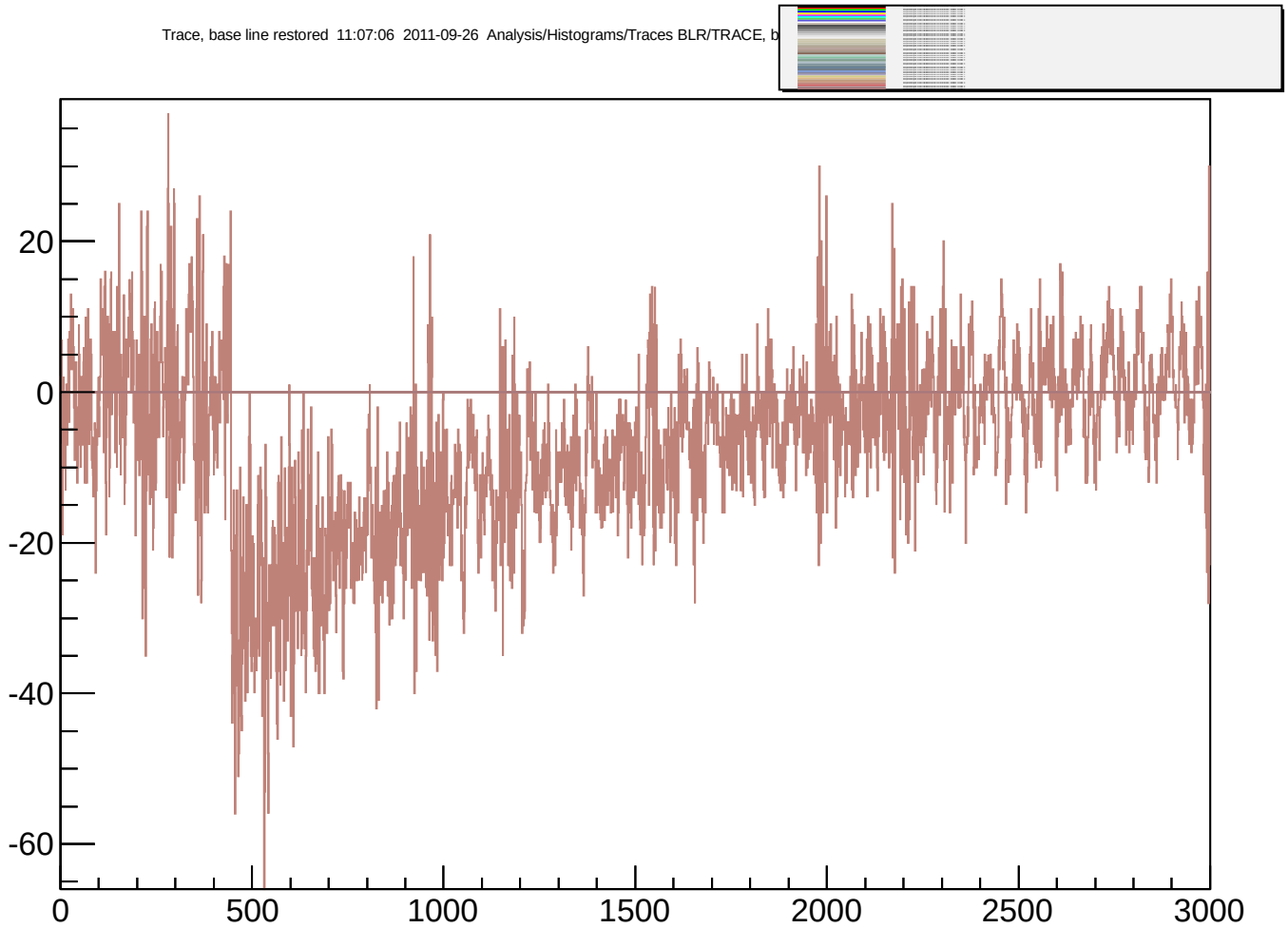


Note: - Trigger windows can be adjacent (no dead time)
- Avoid overlapping trigger windows by setting conversion time (minimum time between two triggers) to trigger window length
- Double data buffers 0/1 allow to realease the system dead time before actual readout of data from FEBEX to PEXOR.
- Very large data sizes (data rates > 200 MB/s) might delay dead time release in a sense, that adjacent trigger windows (dead time free) are not possible in all cases. In this case the system is not anymore dead time free. This situation is also present in so called “trigger less” systems, when data rates produced in the front-ends, exceeds the bandwidth of a transfer channel.

Example Trace (pulse height: ~ 300 mV)



Example Trace (pulse height: ~ 15 mV)

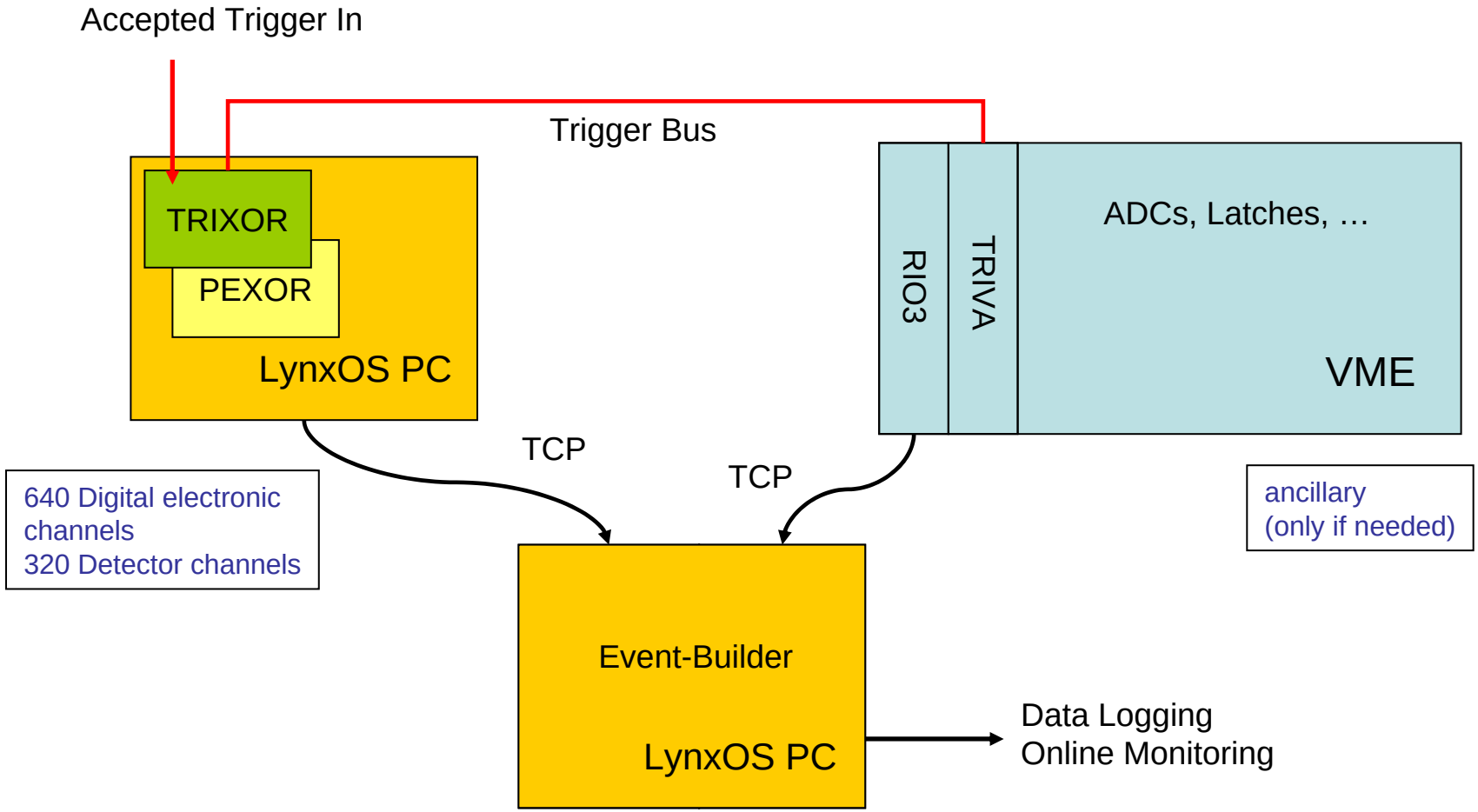


MBS Data Acquisition Summary 120

- Very stable running : 47 days gross running time
  1 VME bus (access) error after one wwek
  40 days gross running without restart
- 400-650 Hz sustained accepted trigger rate (1600 – 2600 Hz in duty cycle)
- 3.5-5 MB/s sustained data rate (14 – 20 MB/s in duty cycle, <= 10% of bandwidth).
- ~ 10 Terabyte of data stored
- 1.25 hits / signals / traces per trigger recorded (as expected)

- No 120 found (yet)

119 MBS DAQ 2012

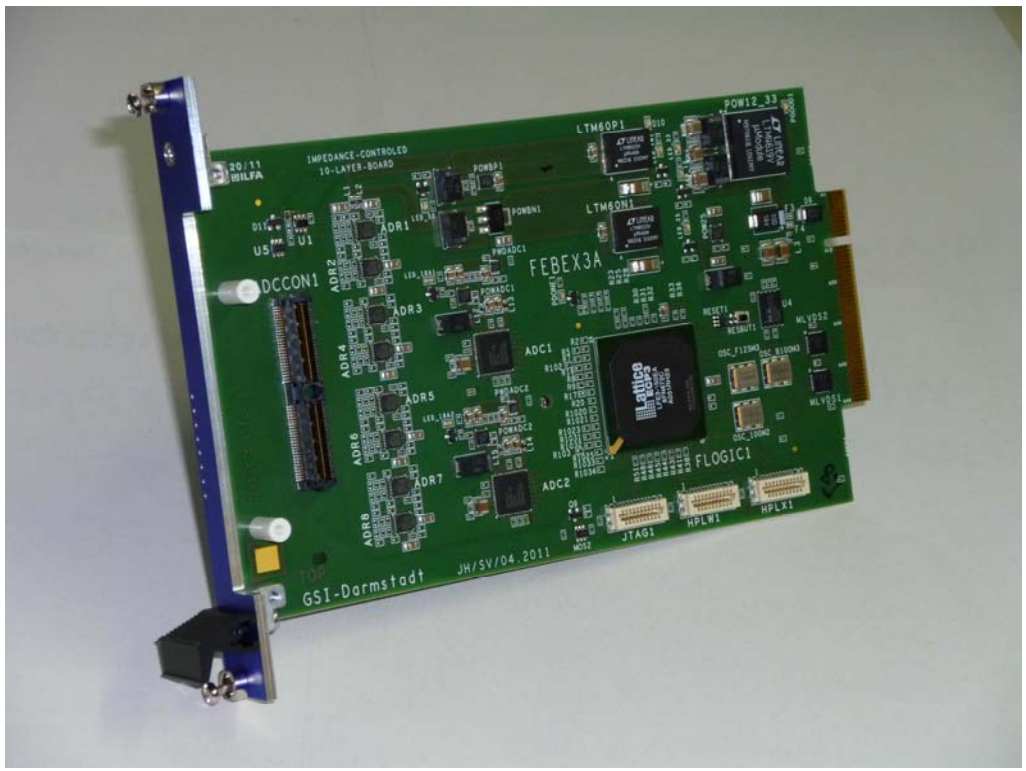


MBS Data Acquisition
Migration from 120 (2011) to 119 (2012)

Changes from 2011 to 2012:

- Use FEBEX3 with 16 channels. Crate based board. Data transport, trigger signals, clock, power via backplane.
- Replace Koeln preamplifier with APFEL preamplifier and shaper (next talk by Peter Wieczorek).
- Provide 640 digital channels for 320 detector channels (2 gains).
- Enable Even/Odd channel readout.
- Use 3 step hit finder instead of trapezoidal filter for internal trigger requests.
- VME sub-system can be used for ancillary signals/detectors.

FEBEX3, 640 Digital Channels



More details in next talk from Peter Wieczorek

Thank You