Update on High Voltage Board and additonal PCBs in FWEC cold volume

PANDA-Collaboration-Meeting 01.06.2022

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Topics

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- Update of radiation hardness simulation

  H*(10) [Sv/h] vs D(Si) [Gy/h]

- Tests of other part combination in HV part

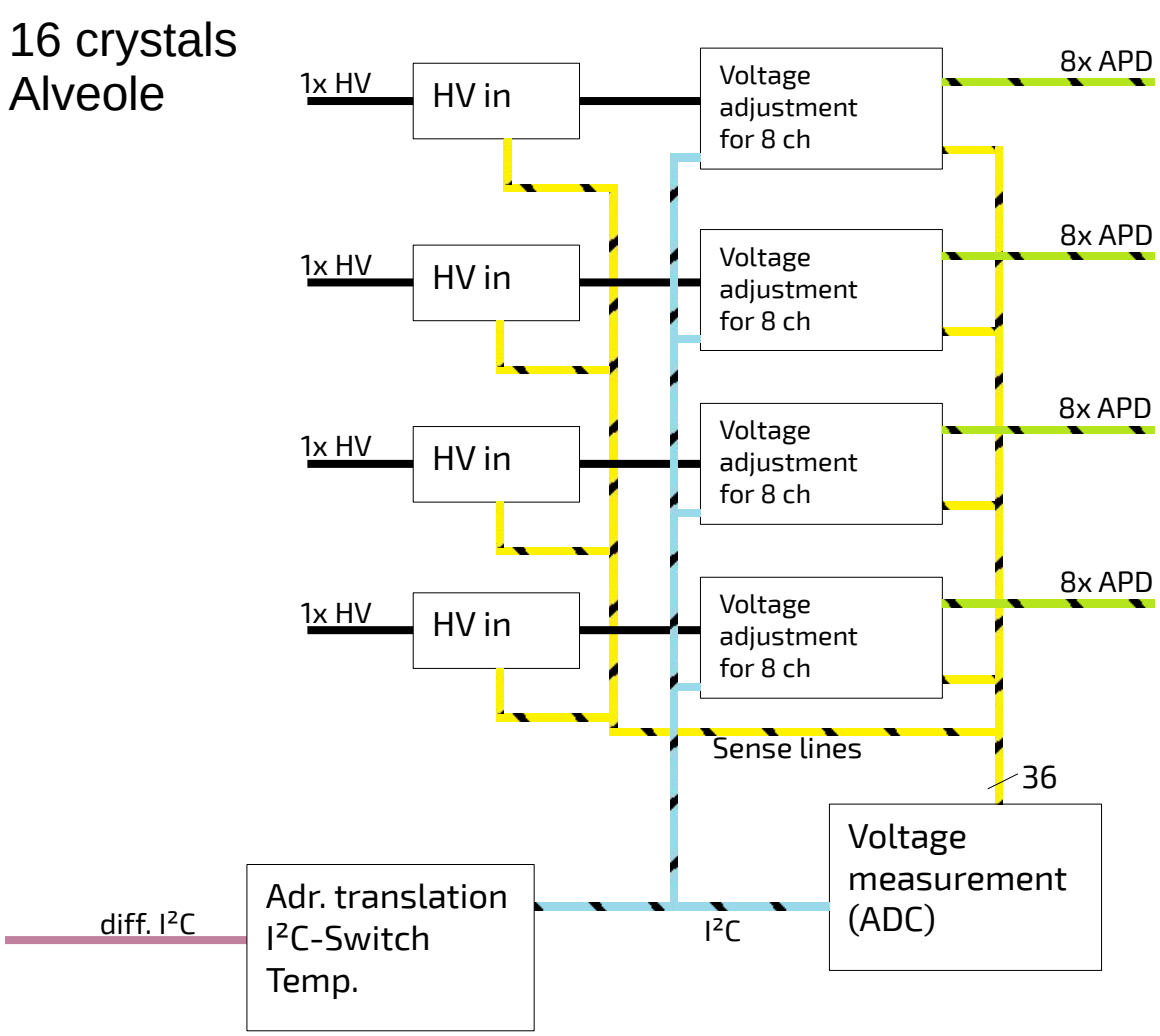
  Summary of rev. 7 and 8

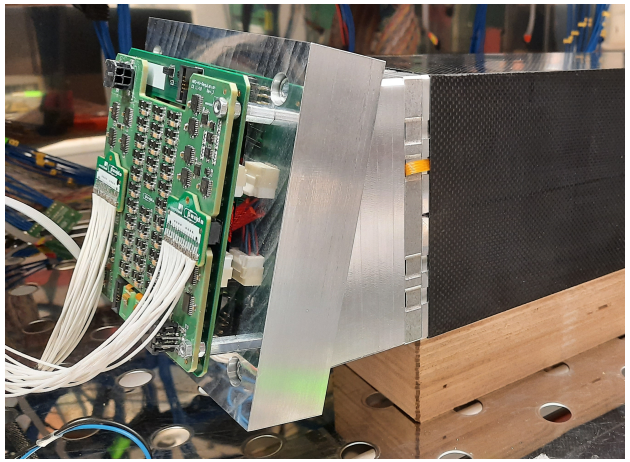
- Status HV-Adjustment boards

- Status of other PCBs in cold volume

HV-Adjustmentboard

16 crystals
Alveole

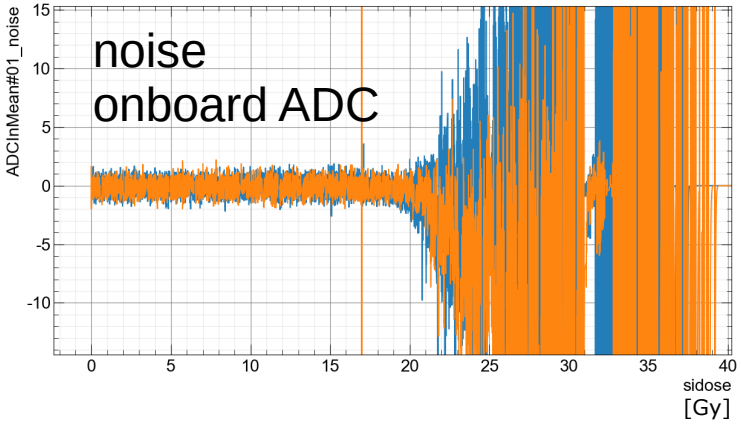


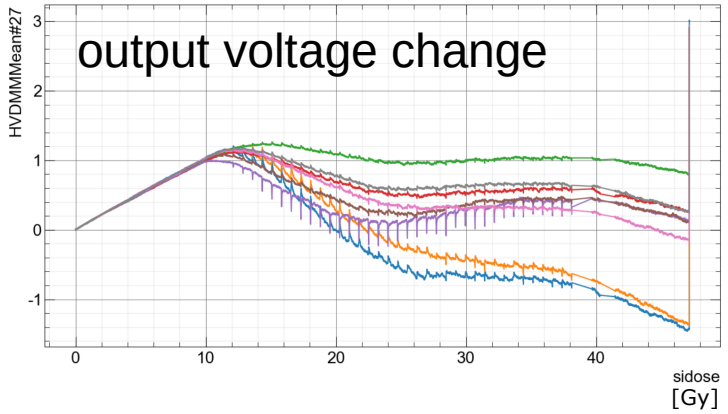


Recap of earlier Si dose simulation

Simulation of 1x1mm² Si chip in exp. setup give a lifetime dose of ~40Gy.

To determine dose at ^{60}Co irrad., using time, activity and simulated mean deposited energy per ^{60}Co photon:





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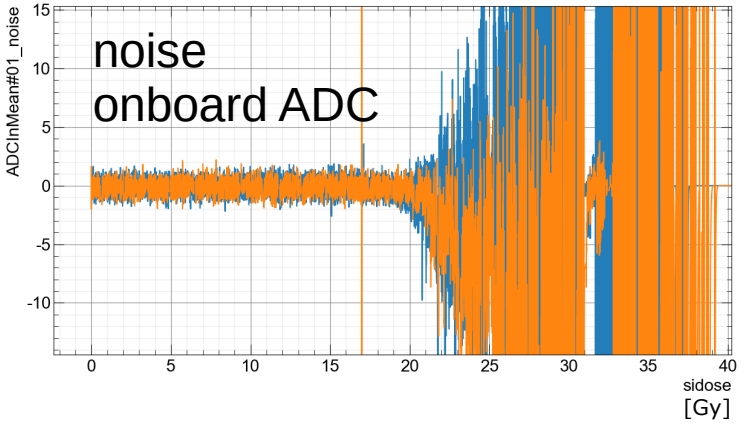

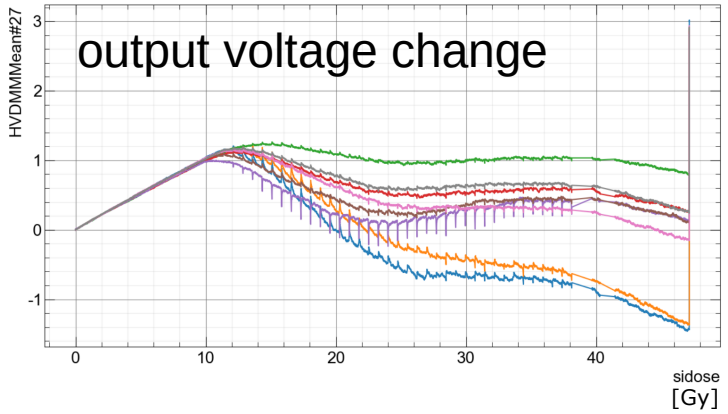

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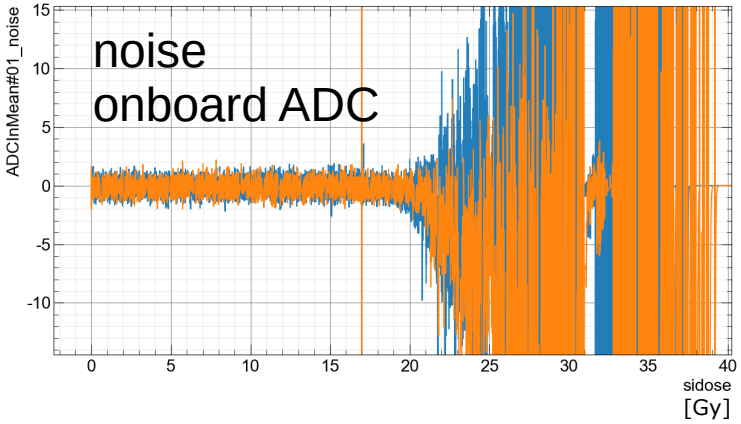

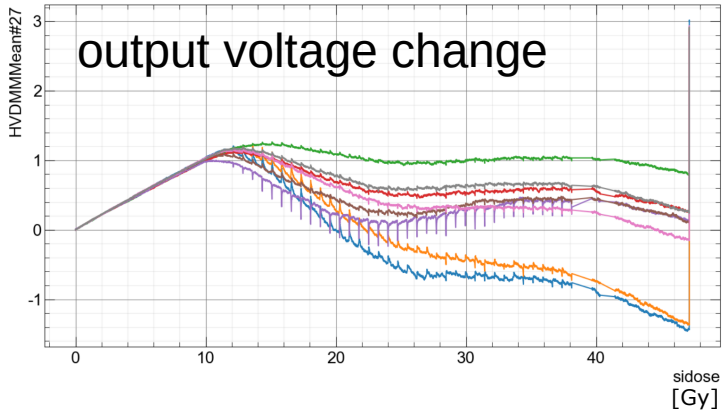

→ e.g. ADC only would only last half lifetime

But additional simulations show a strong dependence on package size and density

Results in a factor of up to 6 (approx. realistic packaging)

→ e.g. ADC would last ~3x lifetime

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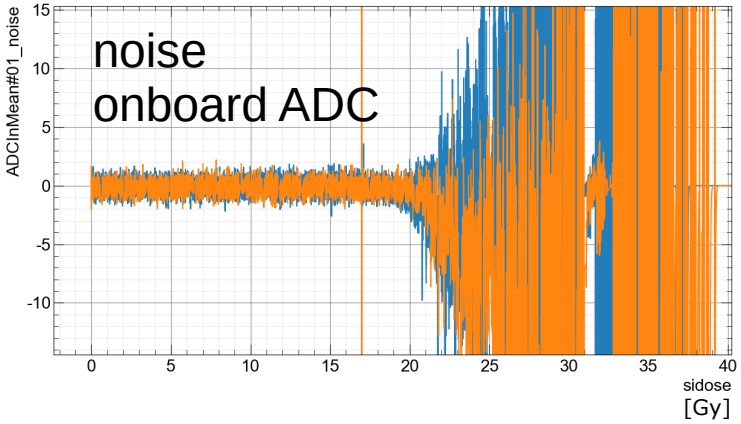

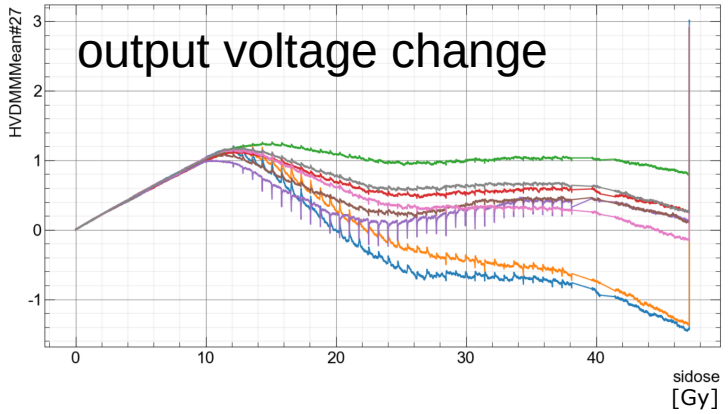

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But additi d density

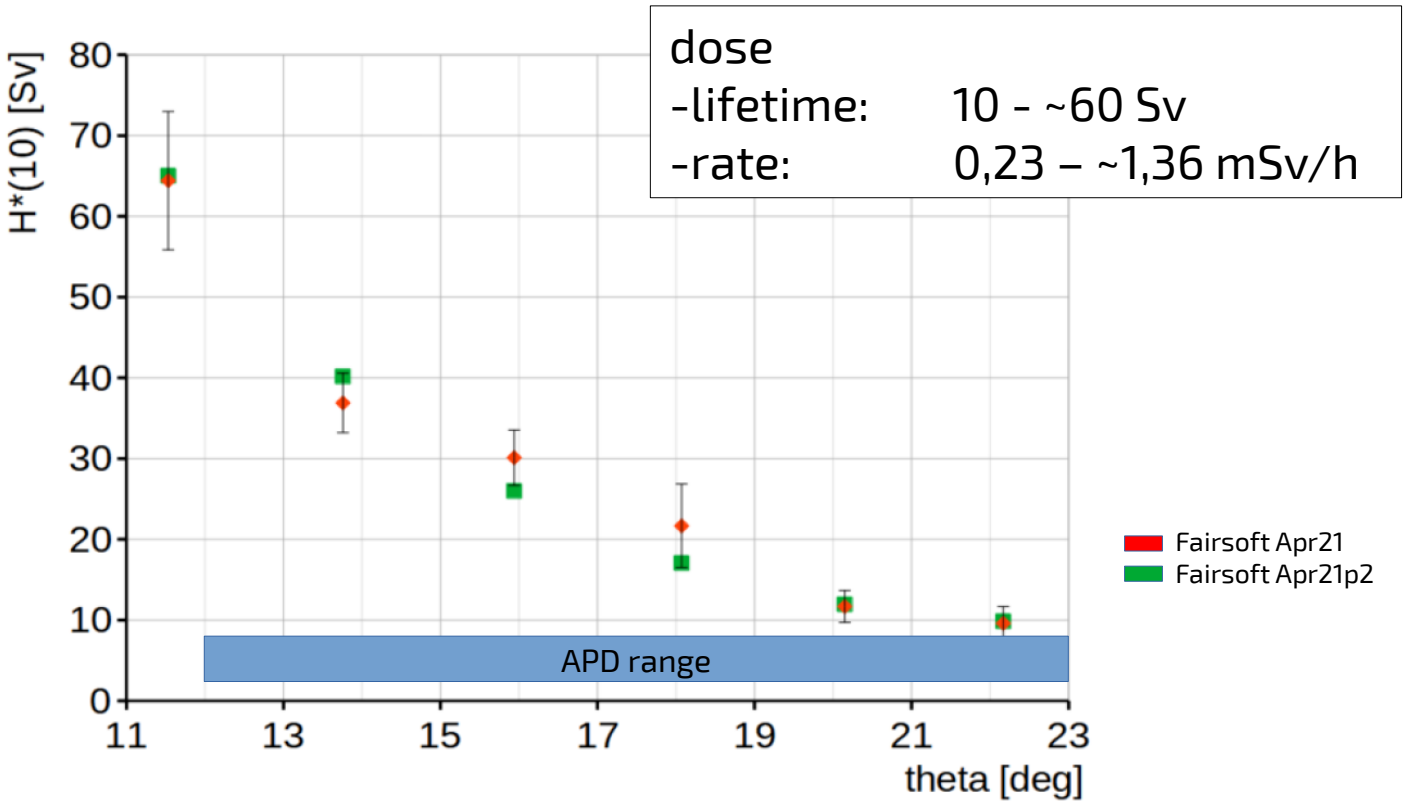
Results in

Redo simulation with different ansatz:

- Using H*(10) probe (ICRU phantom) in exp. monte carlo
- simulated dose corresponds to measuring device

Simulation H*(10) in exp. Setup

H*(10) dose at the position of high voltage boards for lumi $2 \cdot 10^{32}$, 10x half years, average luminosity (50%), 15GeV DPM, full detector setup:



→ 3x lifetime dose results to 180Sv, which would be compatible to factor of 6 in realistic chip packaging

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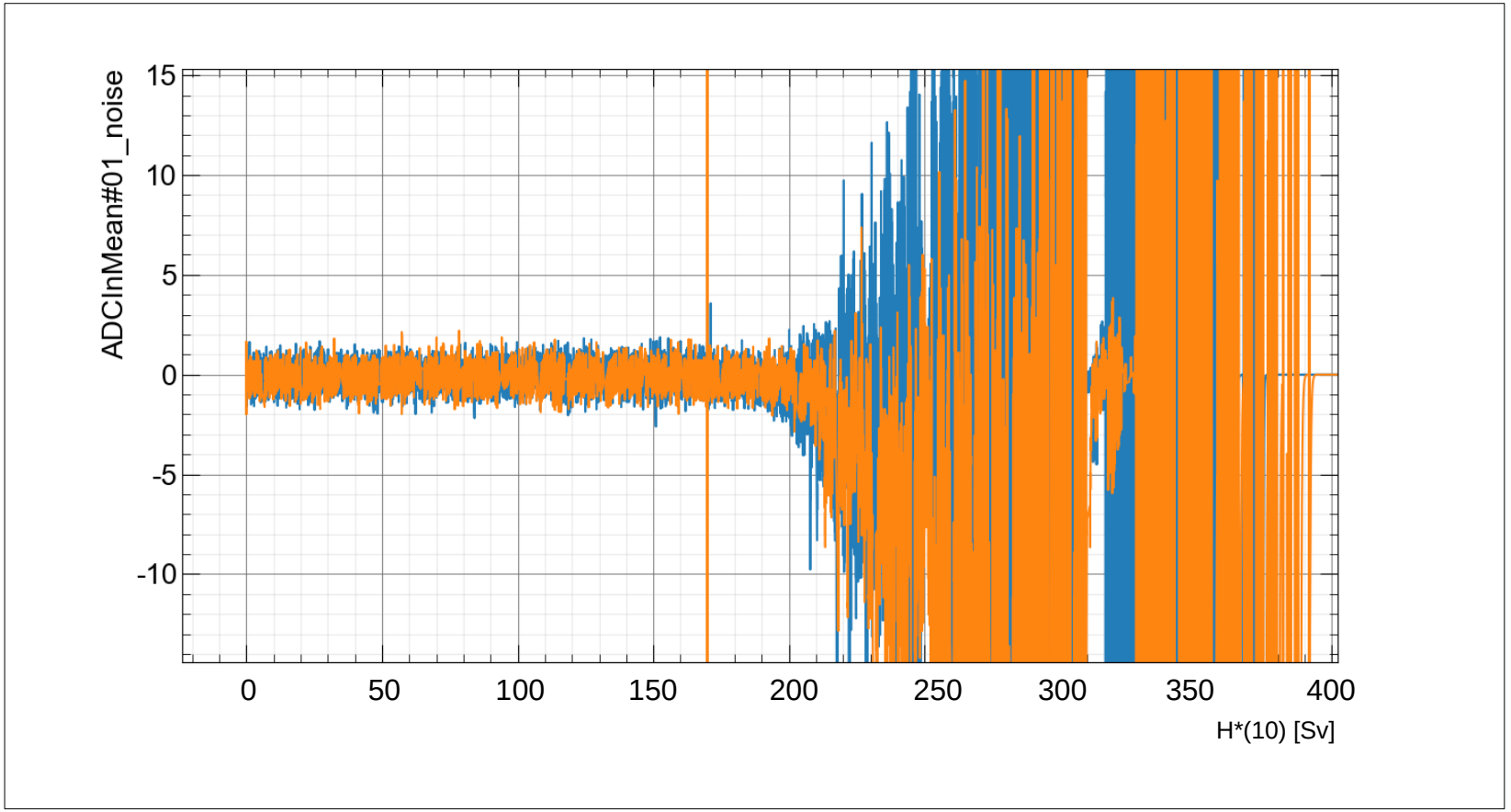

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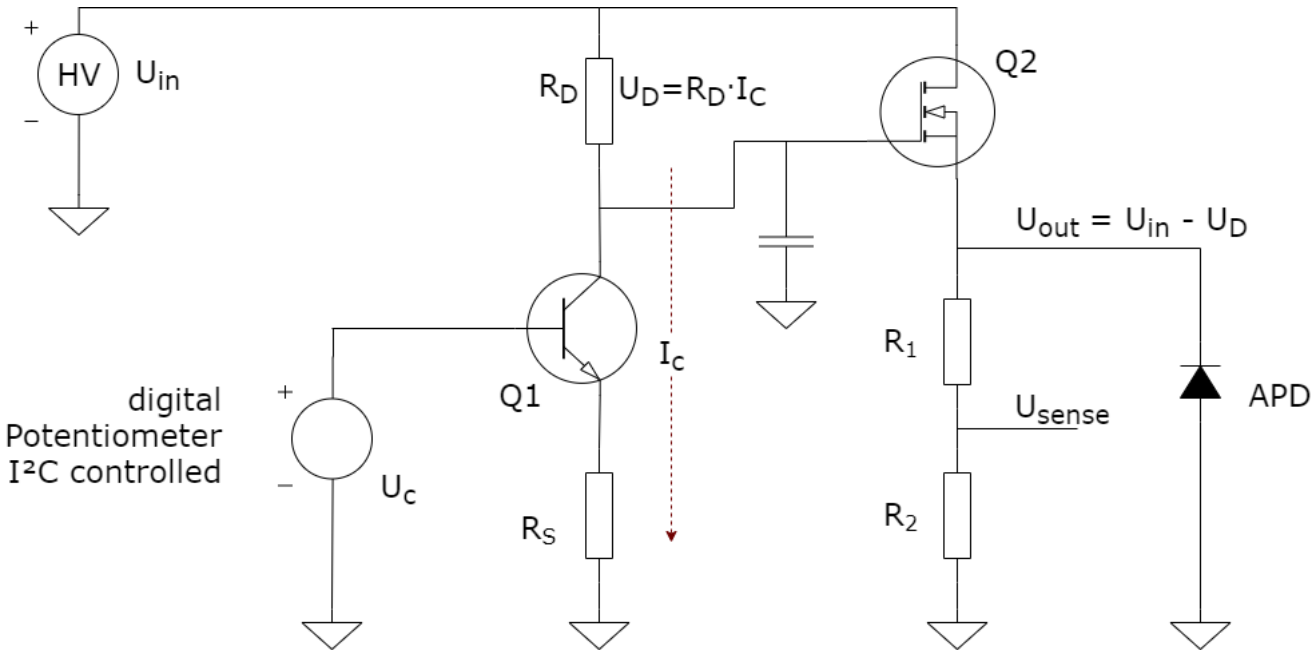
rev6/7 – Output drifts (APD bias)

U_{out} defines bias voltage for APD and total gain crystal (~8%/V at gain 200)



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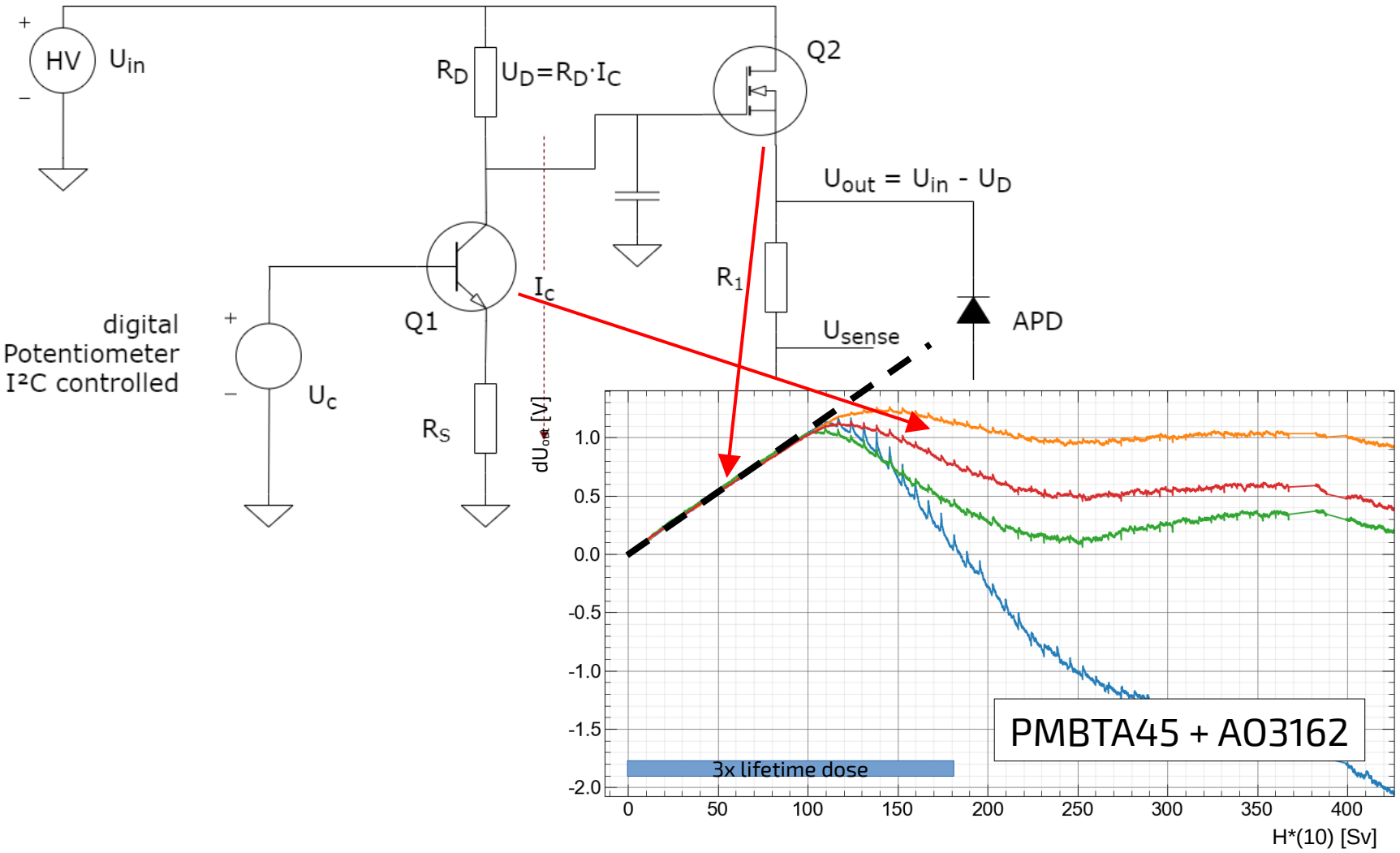

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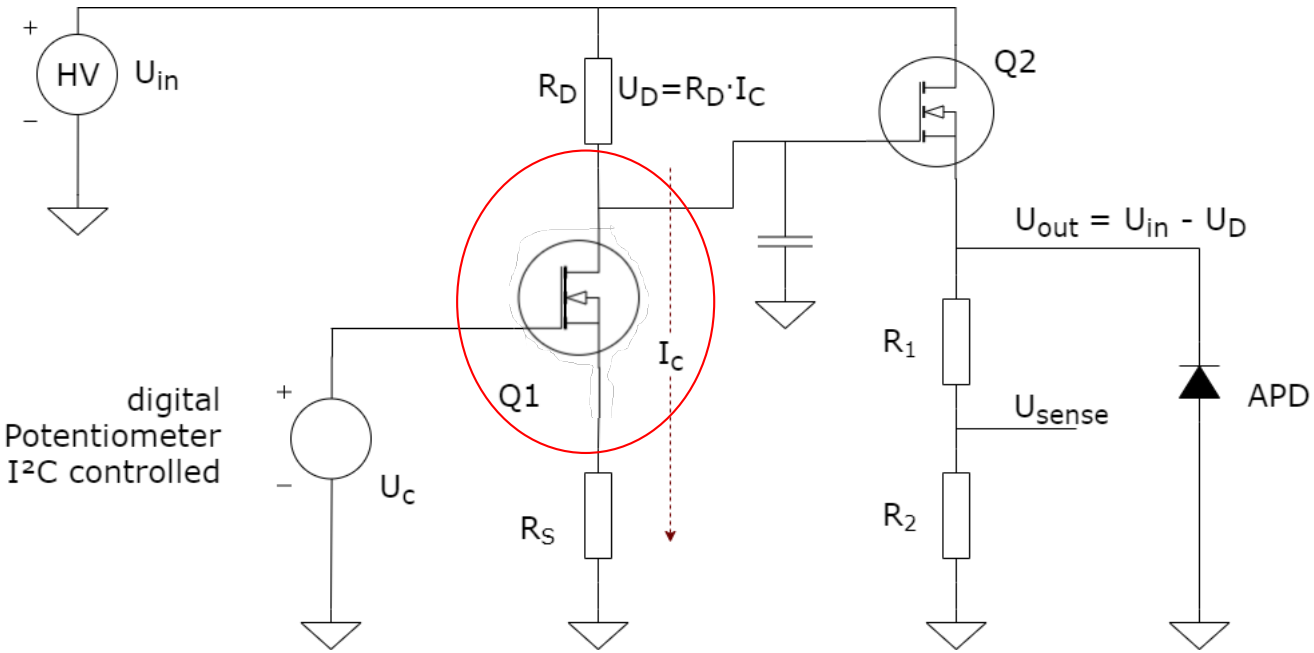
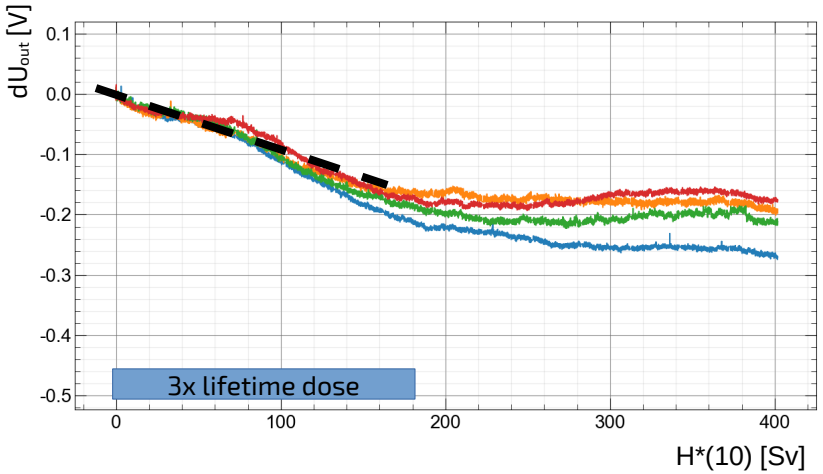


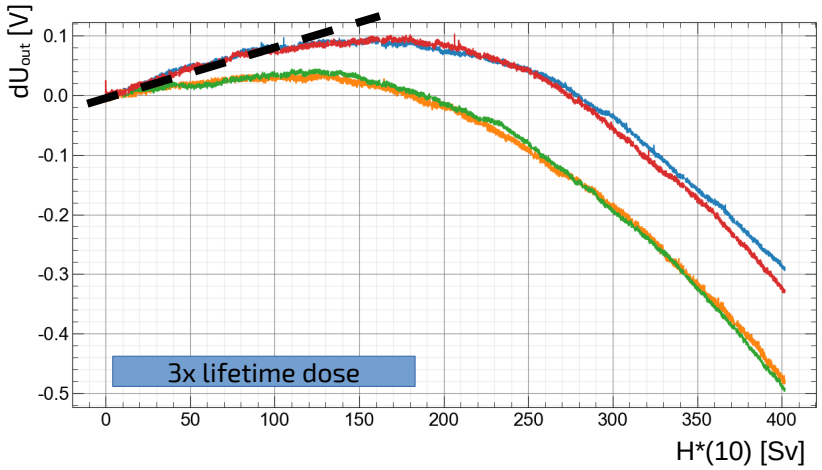
Final test to use a MOSFET as a current sink for creating Ic, because MOSFET has a well-behaved dose dependency.

Voltage drift rev8 during irrad.

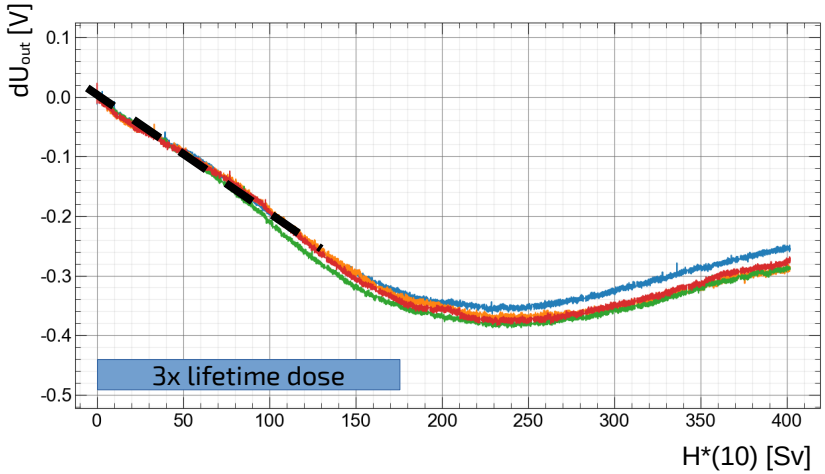
LND150K + AO3162



BSS126 + AO3162



LND150K + BSS127



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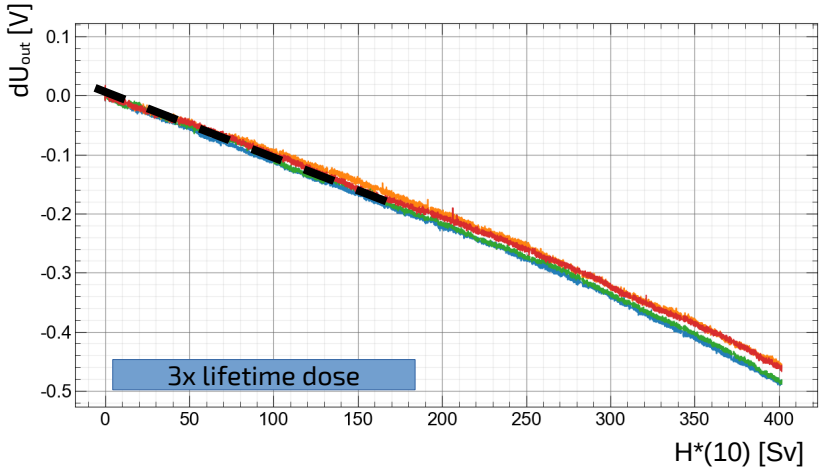
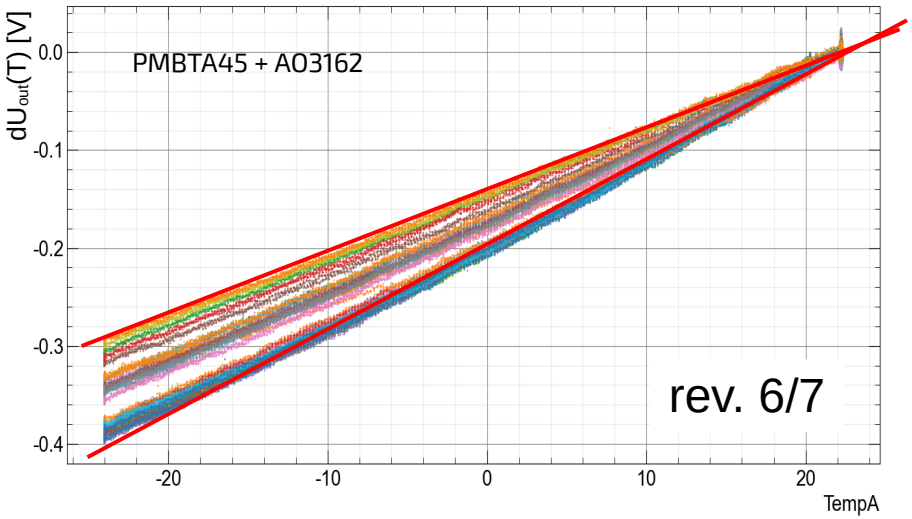
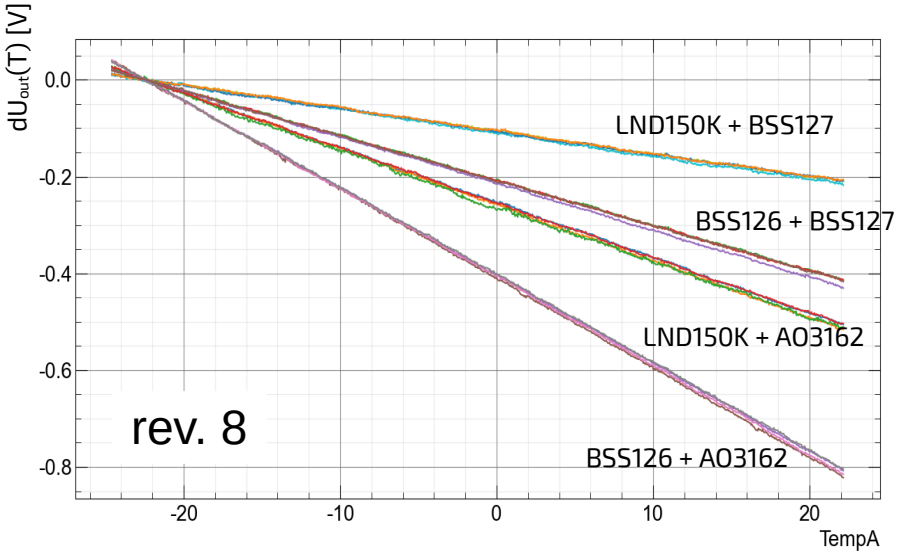


Temp. coefficient





rev6/7/8 - Features

Output voltage (APD bias):

	rev 8				rev 6/7
	LND150K+ AO3162	BSS126 + AO3162	LND150K + BSS127	BSS126 + BSS127	PMBTA45 + AO3162
Temp.-Coeff.	-11 mV/C	-18 mV/C	-4 mV/C	-9 mV/C	6-9 mV/C
Drift / dose (< 100Sv)	-1 mV/Sv	0.8 mV/Sv	-2 mV/Sv	-1 mV/Sv	10 mV/Sv
Drift 400Sv (min,max)	-0.3 – 0 V	-0.5 – 0.1 V	-0.4 – 0 V	-0.5 – 0 V	-1.8 – 1.3 V
Range	~17.7 V	~17.5 V	~12 V	~12 V	~20 V
P(8ch)@128	~43mW	~43mW	~43mW	~43mW	~33mW

chip-shortage:
LND150K first available 24-Oct-2022

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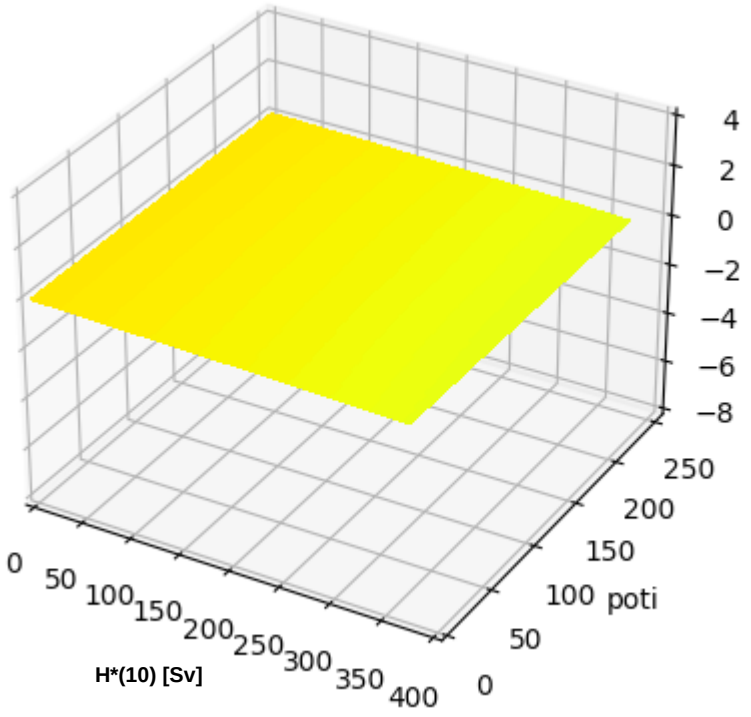
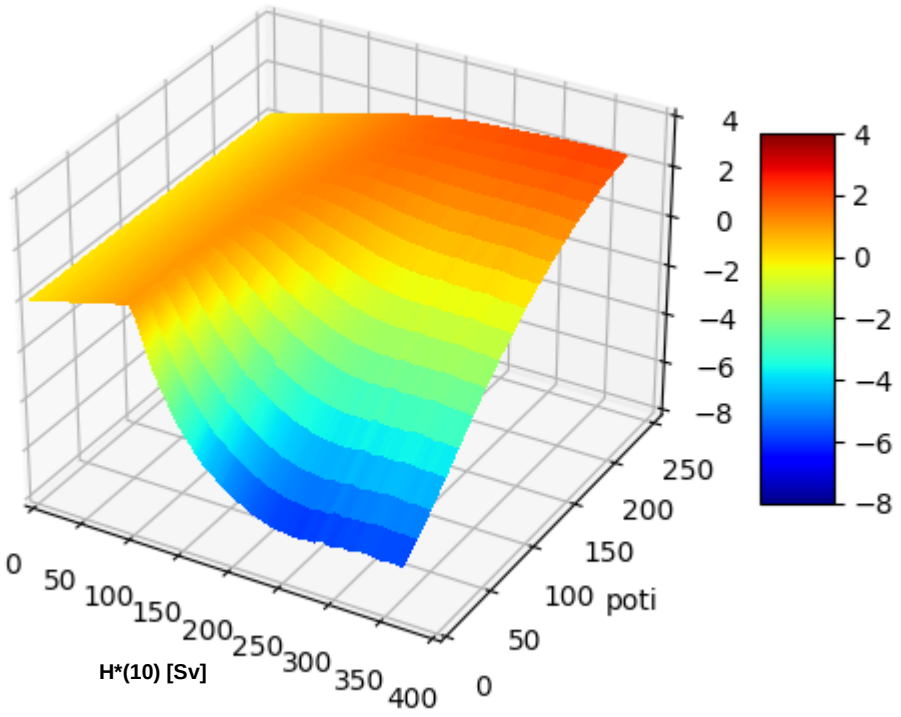
Voltage setting rev7 to rev8

rev8: MOSFET + MOSFET



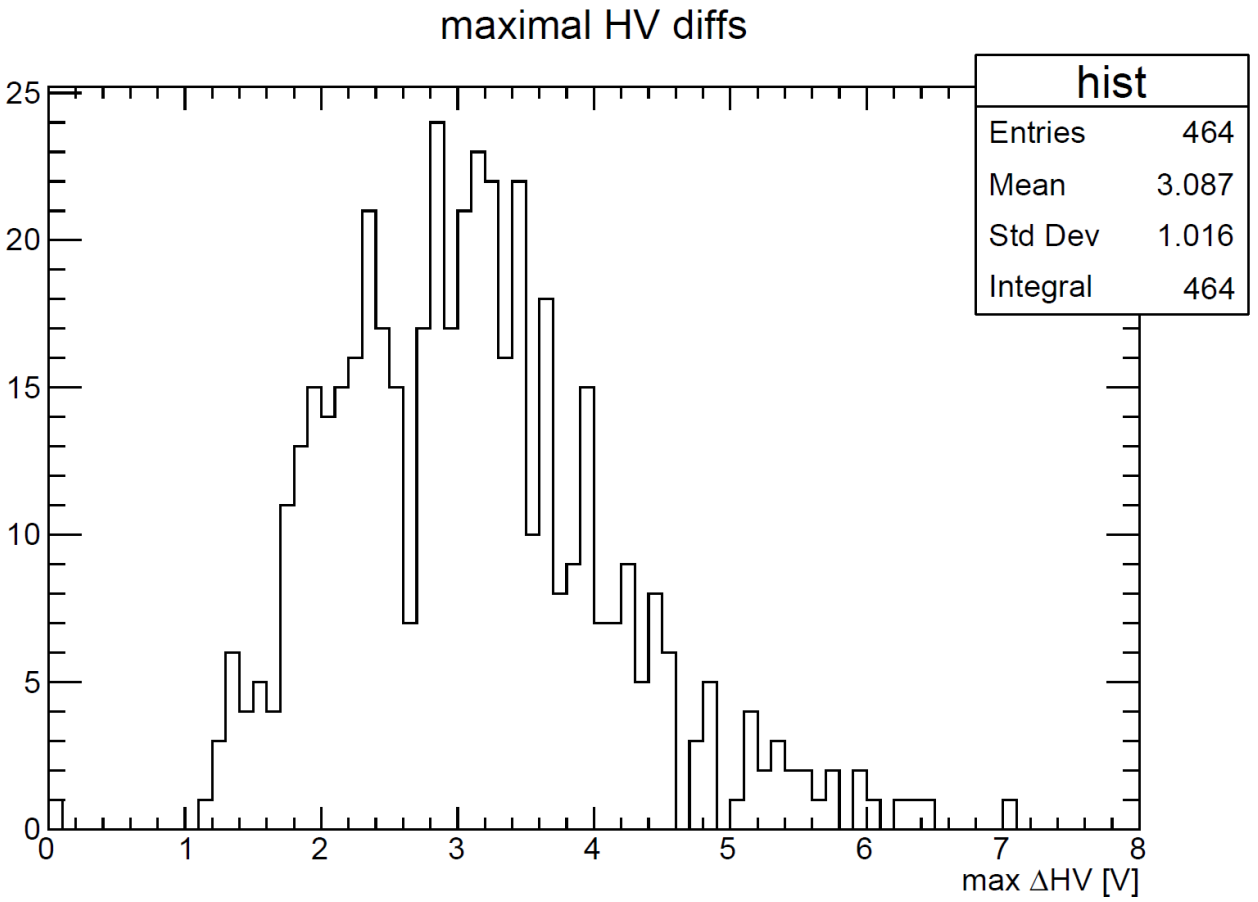
rev7: Transistor + MOSFET



Drift is one order lower and independet of potentiometer position!

Voltage adjustment

Maximal voltage difference on one HV-line of 117 APD-Alveoles measured so far:



Up to 7V adjustment is needed to get a common gain on one HV-line

Stability output/ADC

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HV-Board rev. 8 (lab. setup, temp. stabilized)

Drift ranges in comparison of revisions

	ADC (Voltage-Measurement)		Output (APD bias)	
Test duration	rev. 7	rev. 8	rev. 7	rev. 8
6d	0 – 20mV	0 – 30mV	-20 – 30mV	-10 – 10mV
14d		0 – 30mV		-30 – 10mV

Pros and Cons

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	rev7 Transistor + MOSFET	rev8 MOSFET + MOSFET
Drift range	1.1V @130Sv 0V @180Sv	-0.06V @60Sv -0.18V @180Sv
Power (0-255)	lower 64-120uA@360V 23-43mW/8ch	higher 96-140uA@370V 35-51mW/8ch
Drift under rad. Predictable	no, voltage can change drasticly	yes
Poti calibration	pol(3) not enough, residuum up to 80mV	linear, residuum < 10mV
ADC	unusable >200Sv	unusable >200Sv
Temp.-coeff.	pos. 6 – 9mV/C (lower I_s)	neg. -4 - -9mV/C (higher I_s)

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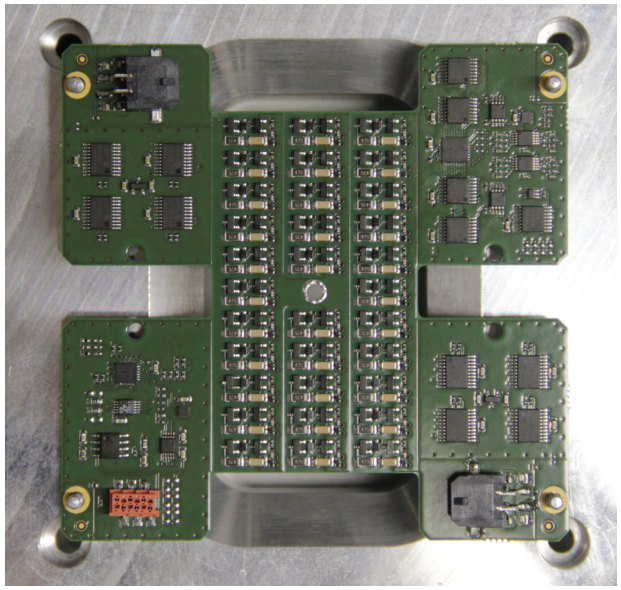
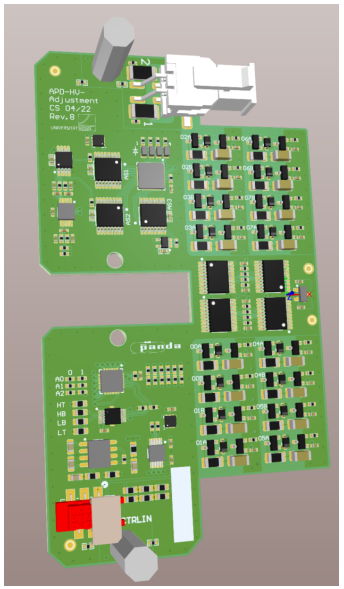
HV-Adjustment-Boards next steps

HV-Adjustment-Board (APD):

- All parts bought/available
- PCBs of 32ch/16ch design in production (delivery mid june)
- July series production (in-house):
  - assembly
  - testing
  - coating
  - calibration of ADCs/output voltage at -25°C

Time consumeing
several calibration points
for at least 4 temperatures

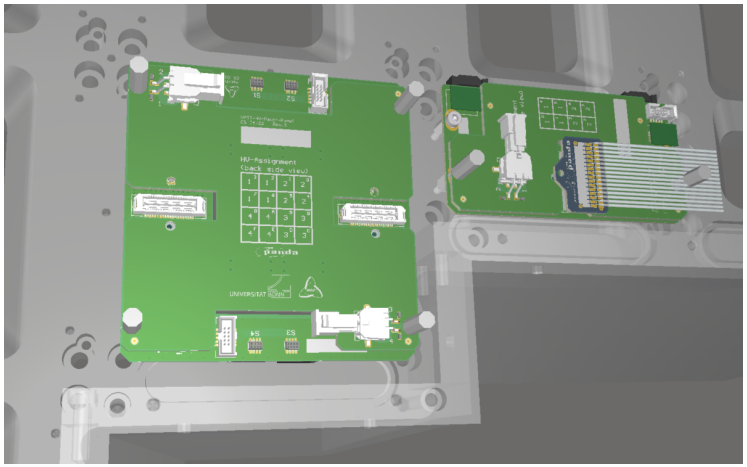




Other PCBs ...

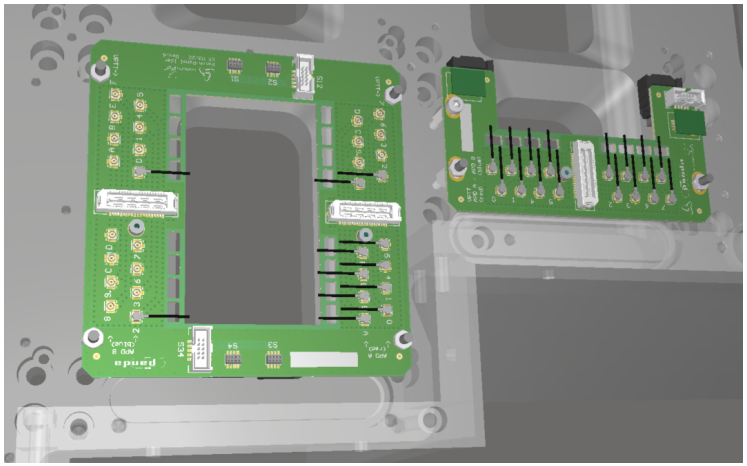
HV-Feedthrough boards (VPTT):

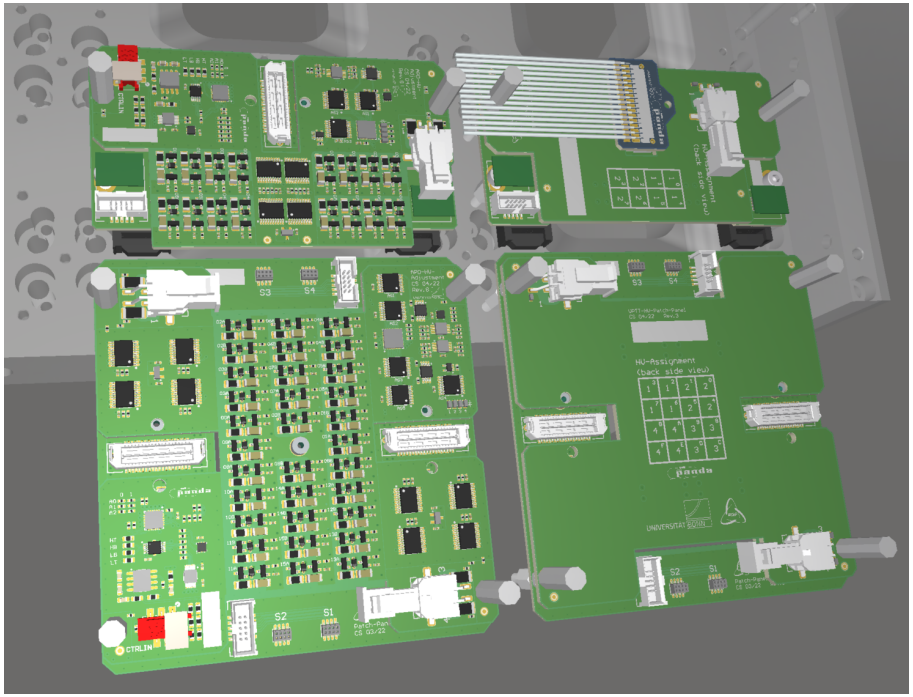
- Design ready, delivery expected begin of july.
- Assembly ~1 month



Patch-Panel boards (APD,VPTT):

- Design ready, delivery expected begin of july.
- Assembly 1-2 month





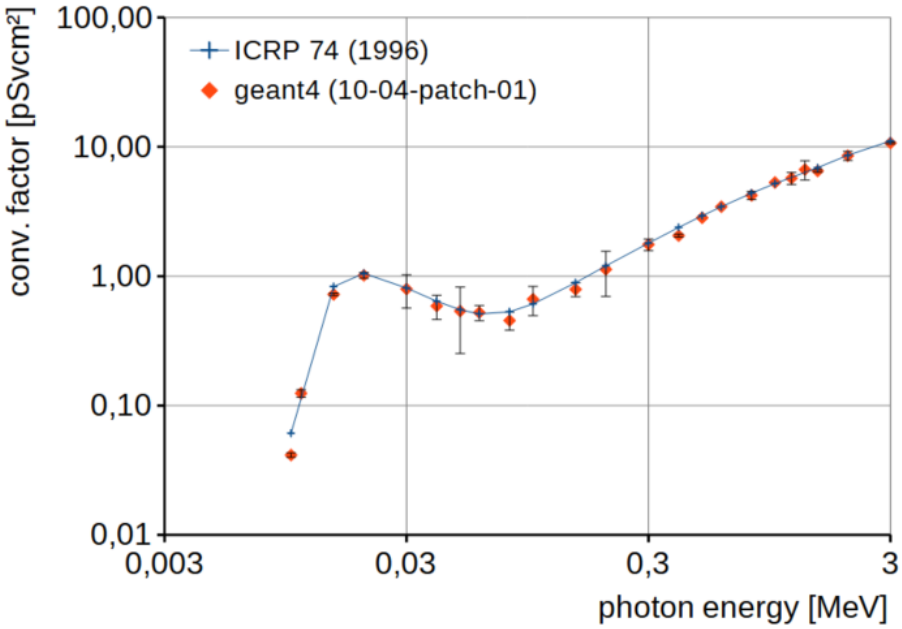
Thank you for your attention

Backup

Dose determination

Use PandaRoot (geant4) to determine dose in 200µm 1x1mm² Si:

- Used full PANDA detector setup in PandaRoot to determine dose at HV-board position
- Simulation of ^{60}Co photons were done to determine mean energy deposition per photon
- Simulation parameters verified by reproducing fluence coeff. for the conversion into H*(10) in the 0.5-3MeV energy range



Dose conversion Sv → Si(Gy)

Activity of ^{60}Co source :

- activity: 5.896 TBq calculated from start activity and $T_{1/2}$
- calculated from measured H*(10) dose e.g. 7.71Sv/h@46cm → 5.823 TBq (Rad Pro Calculator). Uncertainty ~ +/-15%

Simulation of ^{60}Co photons on 200µm Si :

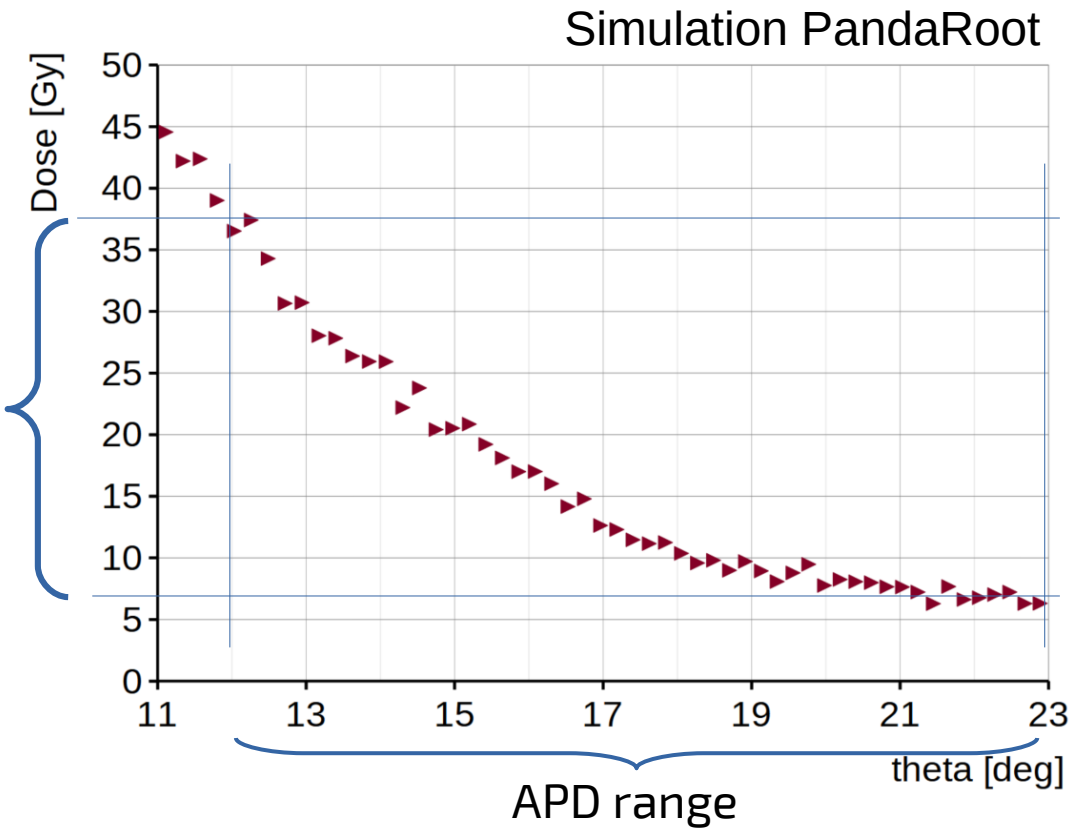
- Mean energy deposit in 200µm Si (1x1mm²) per photon: $\overline{E}_\gamma = 0.16*10^{-3}$ MeV
- Photon fluence through 1x1mm² : $\phi = 2.18*10^6$ Bq (@46cm) (point-like source assumed)
- Energy fluence: $\psi = 0.16*2.18*10^3$ MeV/s = $0.3488*10^3$ MeV/s
- With mass of Si: D = 0.43 Gy/h
- 2 photons (1.17 + 1.33MeV) → D = 0.86 Gy/h

Factor for converting H*(10) to dose in Si: 0.86 Gy/7.71 Sv = 0.104 Gy/Sv

Expected dose from experiment simulation

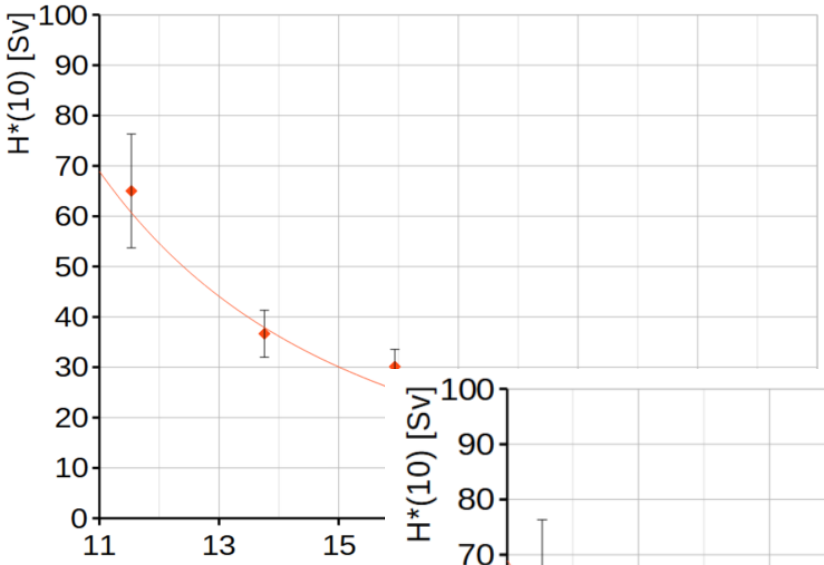
Dose for 200µm Si at the position of high voltage boards for lumi $2 \cdot 10^{32}$, 10x half years, average luminosity (50%), 15GeV DPM, full detector setup:

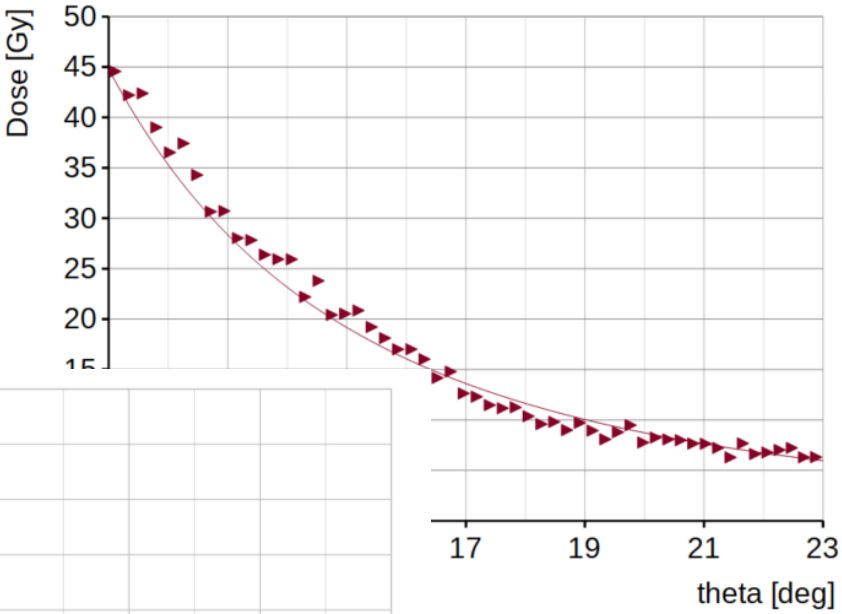
dose
-lifetime: 6 - 37 Gy
-rate: 0.3 – 1.75 mGy/h

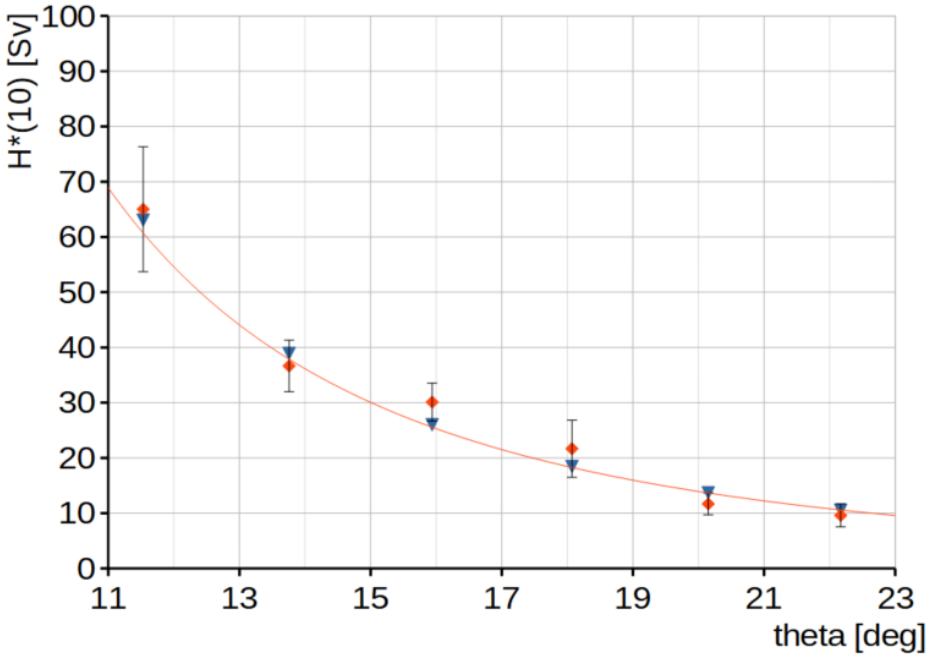


Simulation with 1x0.2mm Si ring for several radii

Compare to energy deposit







right with

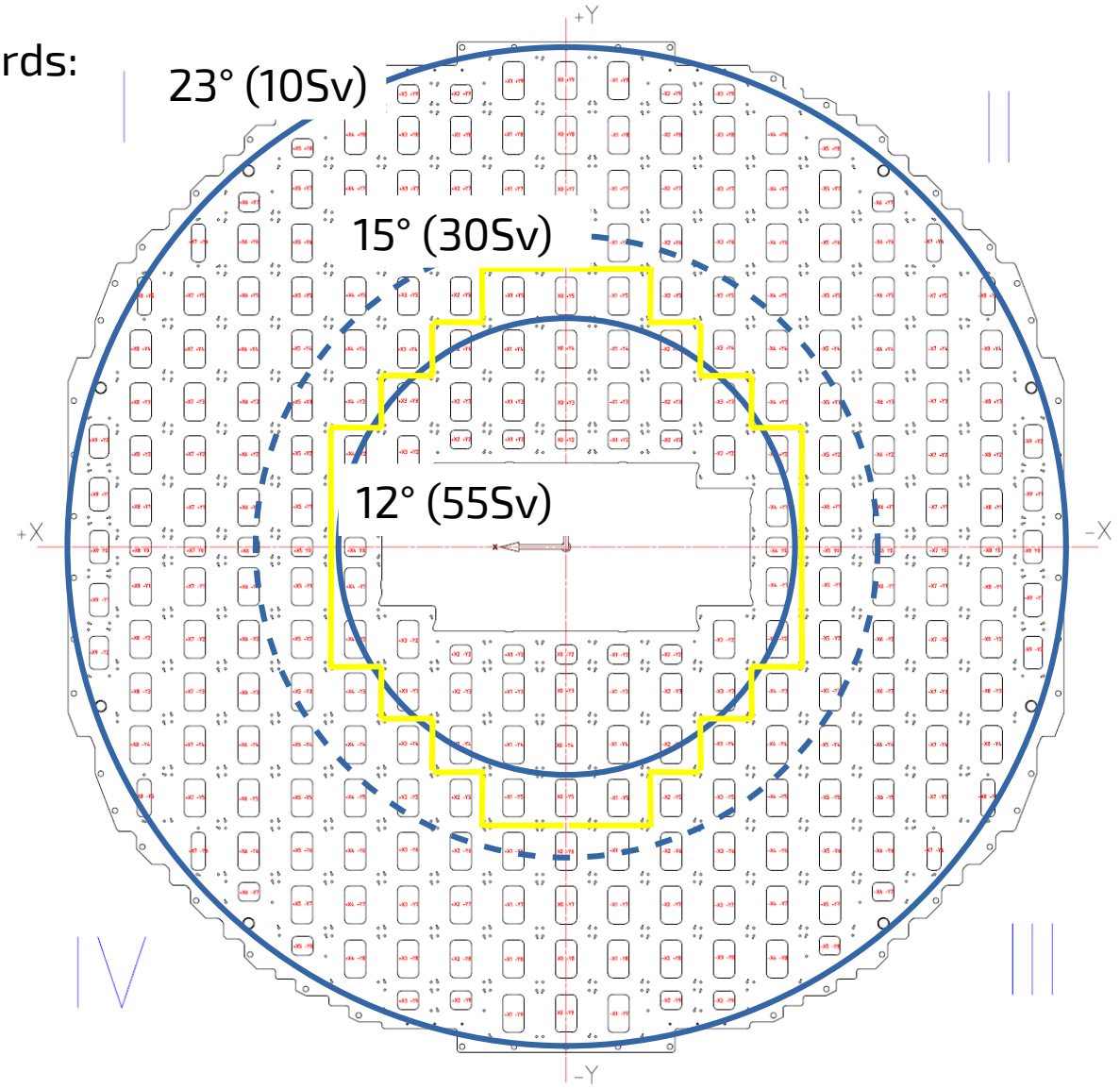
/(0,104*6)

Simulation shall give a handle bzw. ball park in what range to look.

HV-board positions

Min/max radii of HV-boards:
51.3cm (12°)
102.7cm (23°)

214 HV-boards total:
24 in 12°-15°
190 in 15°-23°

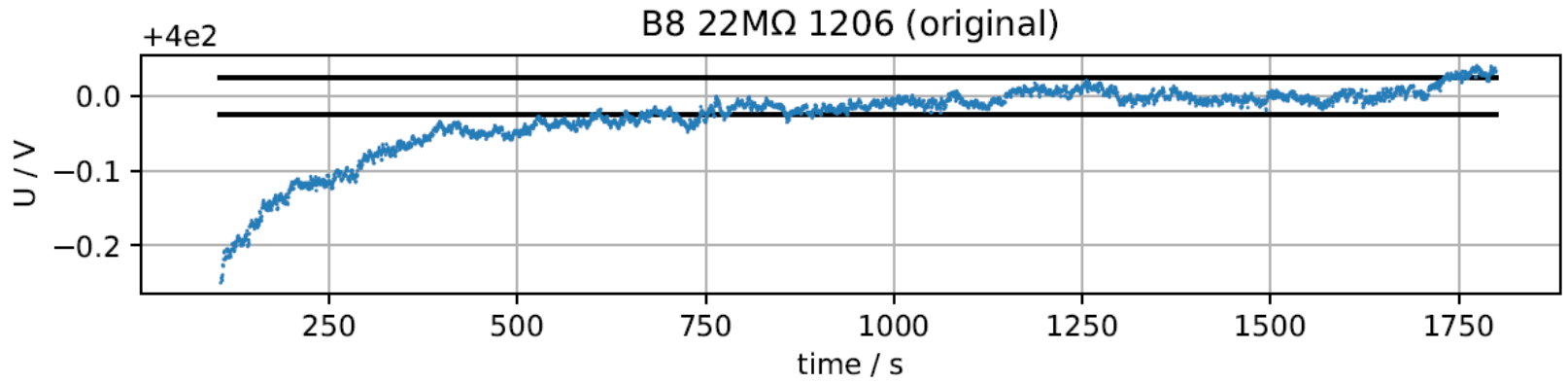


Sense voltage

Input/output high voltage up to 500V needs to be scaled down to 2V@ADC-input to be able to digitize it:

- For a measurement range of 500V → calibration factor is ~0,016V/ch
- To get accurate calibrated readings, the scaled down voltage (U_{sense}) needs to be stable quickly

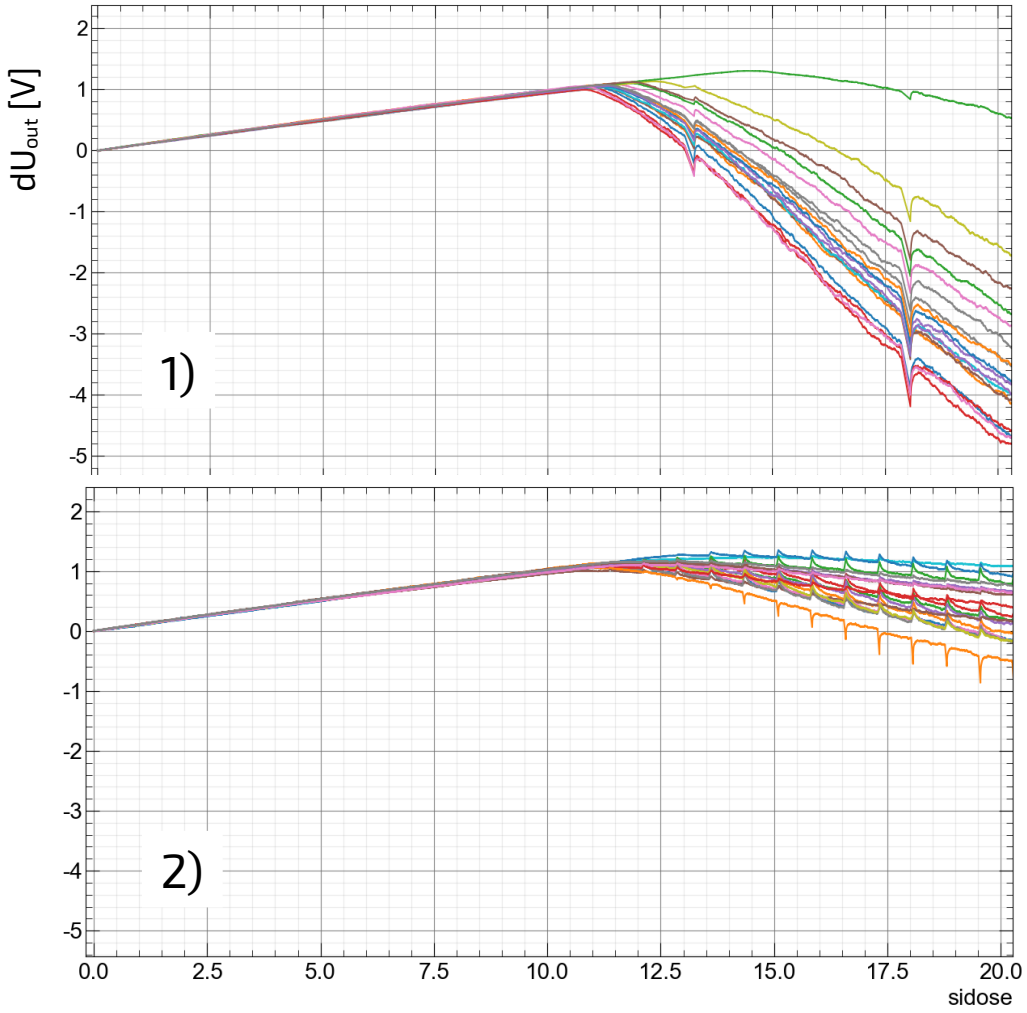
But used HV-resistor (22MOhm, 1206 size) shows slow dirft after switch on:



Effect reproduced in a separate setup in stabilized temp. environment.

Adjustment range

Test of different I_C settings and a fixed potentiometer position of 128:



$dU_{out} = U_{out}(t) - U_0$

Interval irradiation

„Simulation“ beamtimes by irradiate the board in parts with a pause in between: