# ToASt ASIC development status

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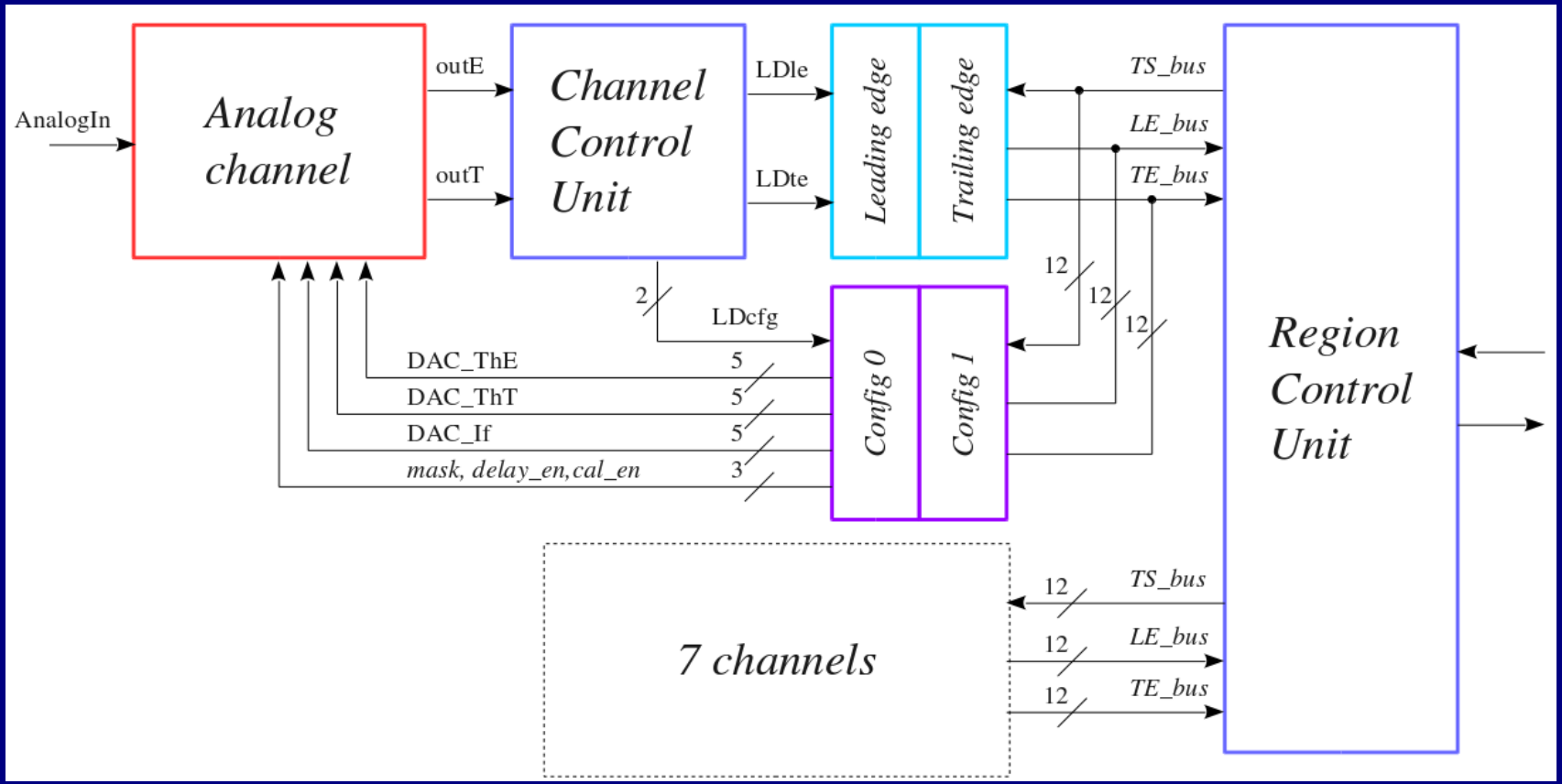
# Specifications

| **Specification** | Min | Max | Unit |
|---|---|---|---|
| Input capacitance | 2 | 17 | pF |
| Max rate per strip | | 40 | kHz |
| Input charge | 1 | 40 | fC |
| Noise | | 1500 | $e^-$ |
| Preamp peaking time | 50 | $\geq$ 100 | ns |
| Channels per chip | 64 | | |
| Reference clock | | 160 | MHz |
| Charge resolution | 8 | | bits |
| Time resolution (pk-pk) | | 6.25 | ns |
| Time resolution (r.m.s.) | | 1.8 | ns |
| Power consumption | | 256 | mW |
| Chip dimensions | 4.5 $\times$ 3.5 | | $mm^2$ |
| Pads position | On two sides only | | |

# ToASt main characteristics

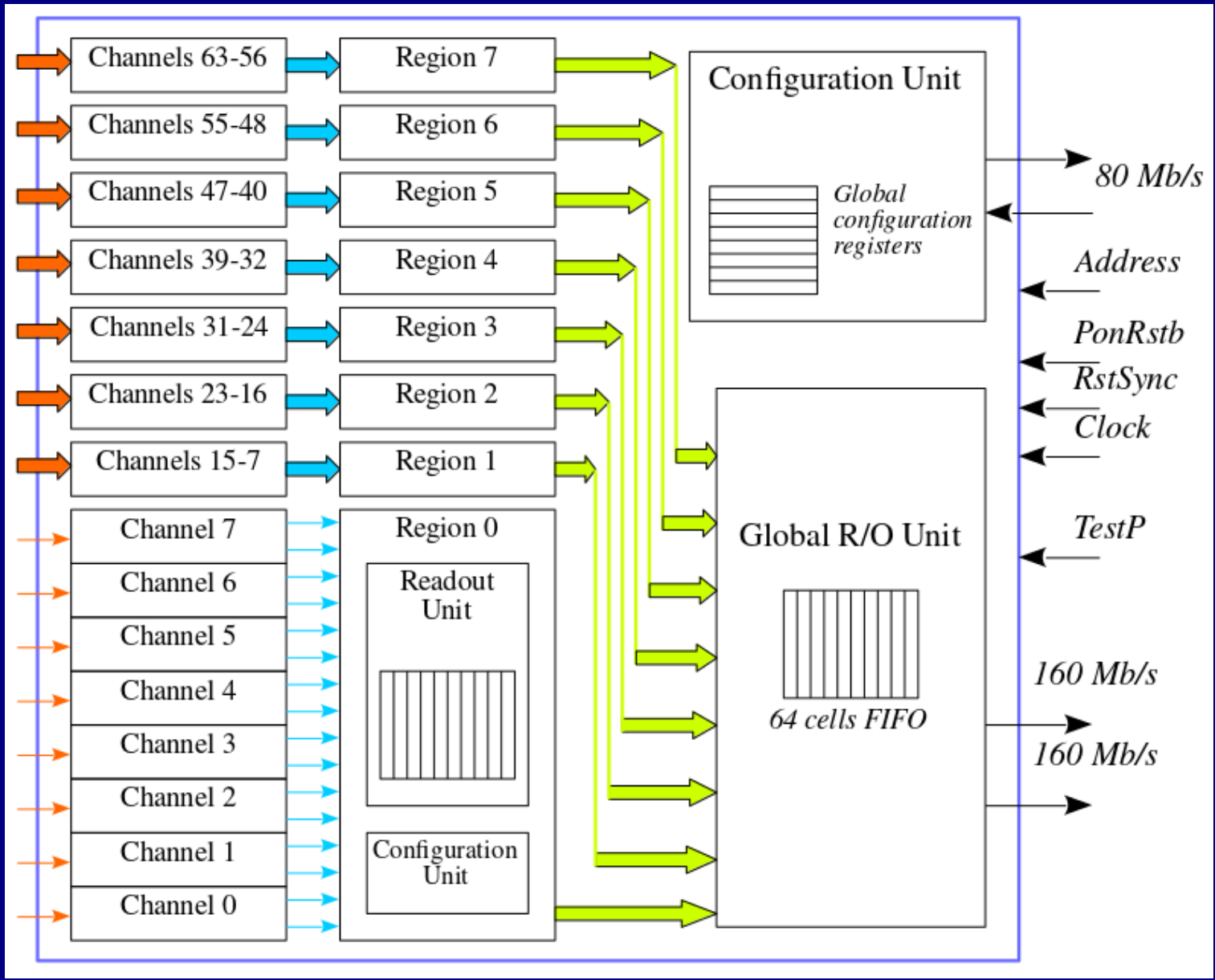
- 64 input channels
- Time of Arrival (ToA) and Time over Threshold (ToT) measurements
- Master clock frequency : 160 MHz
- Region : groups of 8 channels with local FIFO
- Second level FIFO buffering for the 8 regions
- Two output serial links at 160 Mb/s
- Serial configuration protocol at 80 Mb/s
- Full SEU protection via Triple Modular Redundancy
- CMOS 0.11 $\mu$m technology

# ToASt channel schematic




- Common time reference : 12 bits time stamp distributed to all channels
- Time stamp can be Gray-encoded
- LE and TE registers latch time stamp at comparator rising/falling edges

# ToASt architecture



# Output data format

- Data output in 32 bits words over 160 Mb/s serial links
- It can be configured to use 1 or 2 links
- Frame : rollover time for the time stamp counter, i.e. 25.6 $\mu$s at 160 MHz
- Data within a frame are packed within a frame header and a frame trailer
- Frame header contains chip id and frame number
- Frame trailers contains the number of valid samples and CRC

| Packet type | Header<br>*2 bits* | Data<br>*30 bits* |
|---|---|---|
| Data | 11 | Region[2:0] Channel[2:0] Le[11:0] Te[11:0] |
| Header | 10 | 10 ChipId[6:0] Reserved[12:0] FrameN[7:0] |
| Trailer | 01 | 01 DataCnt[11:0] CRC[15:0] |
| Sync | 00 | 00 1100 1100 1100 1100 1100 1100 1111 |

# Control unit

- Serial link at 1/2 of the master clock frequency
- Input : 16 bits command
- Output : 16 bits data
- Address :
  - $a_B$ : broadcast address
  - $a_6 a_5 a_4 a_3 a_2 a_1 a_0$ : chip address
- 16 12-bits Global Control Registers (GCR)
- 64×2 12-bits Channel Control Registers (CCR)

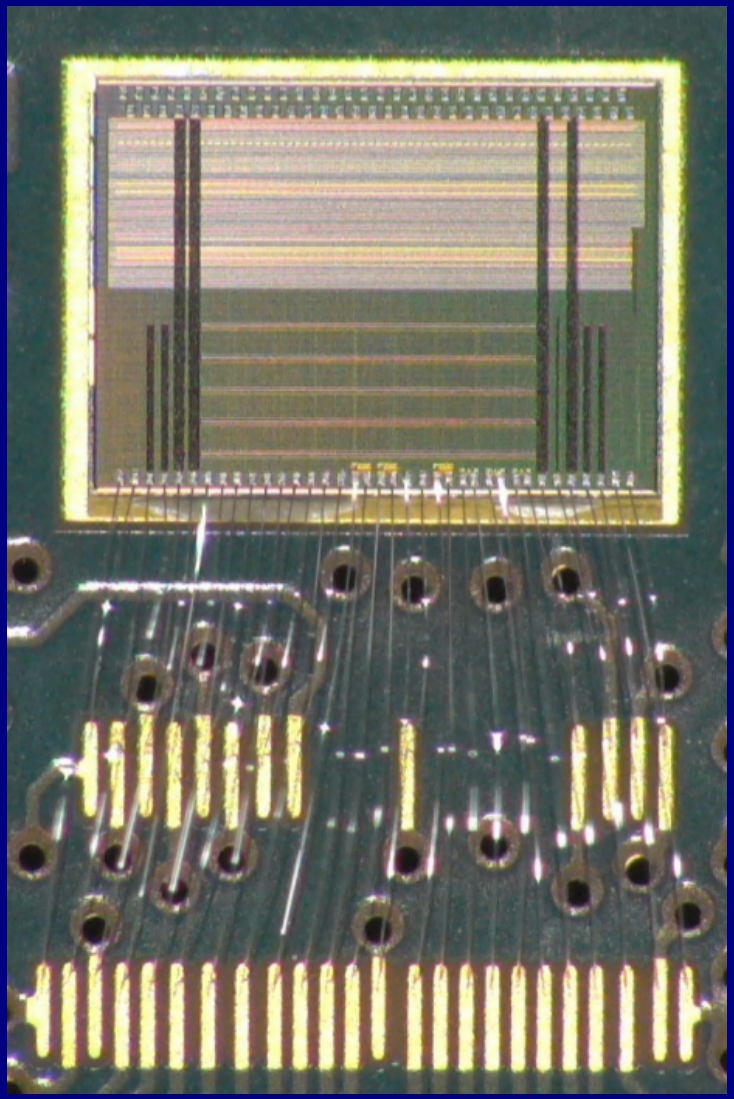
# Control data format

| **Function** | **Data**<br>4 bits | **Op code**<br>12 bits |
|---|---|---|
| Chip Select | 1101 | $01a_B a_6 a_5 a_4 a_3 a_2 a_1 a_0 00$ |
| Chip Deselect | 0000 | 00xx xxxx xxxx |
| Register select (channel) | 0100 | $0000 r_2 r_1 r_0 0 c_2 c_1 c_0 a_0$ |
| Register select (region) | 0100 | $0000 r_2 r_1 r_0 1 a_3 a_2 a_1 a_0$ |
| Register select (global) | 0100 | $00010 a_6 a_5 a_4 a_3 a_2 a_1 a_0$ |
| Register write | 0101 | $d_{11} d_{10} d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0$ |
| Register read | 0110 | 0000 0000 0000 |
| No operation | 1111 | 0000 0000 0000 |
| *Reserved for config output* | 1000 | $d_{11} d_{10} d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0$ |

# Reset management

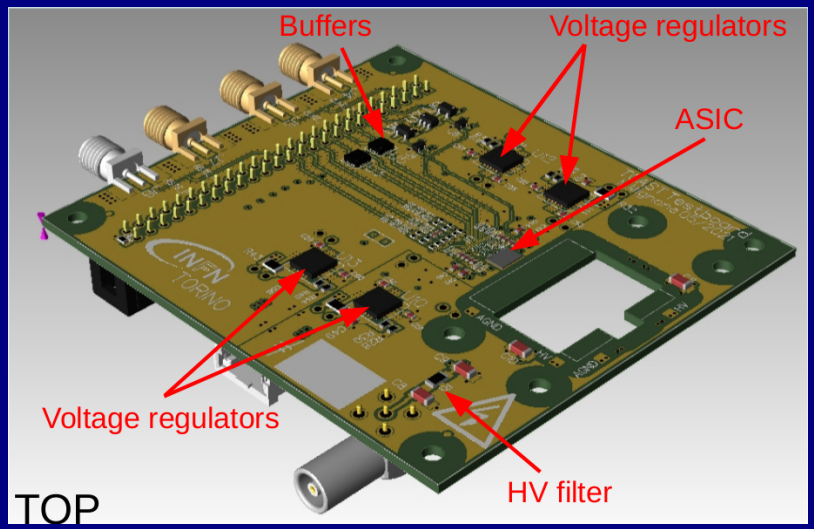
- Asynchronous power-on reset : for start-up only
- Synchronous, pulse lenght encoded reset :
  - 1 clock cycle reset pulse : ignored
  - 2 clock cycles reset pulse : time stamp counter and Tx units reset
  - 3 clock cycle reset pulse : ignored
  - n$\geq$4 clock cycles reset pulse : global reset

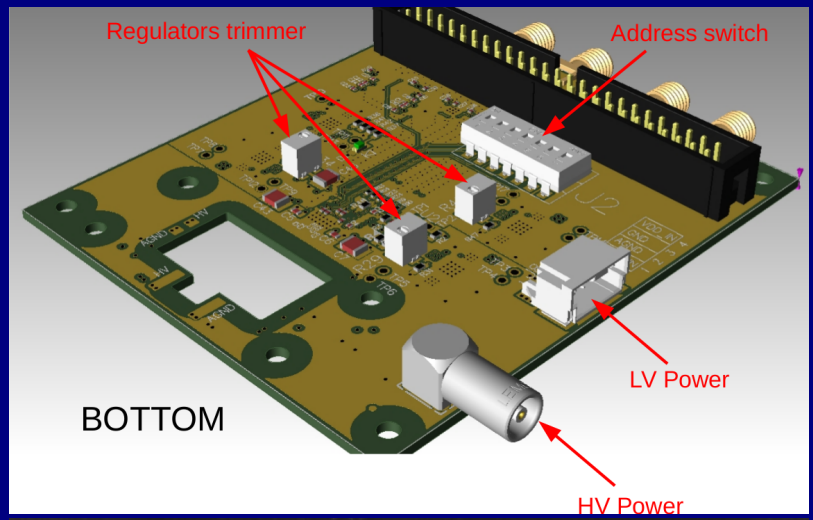
# ToASt prototype

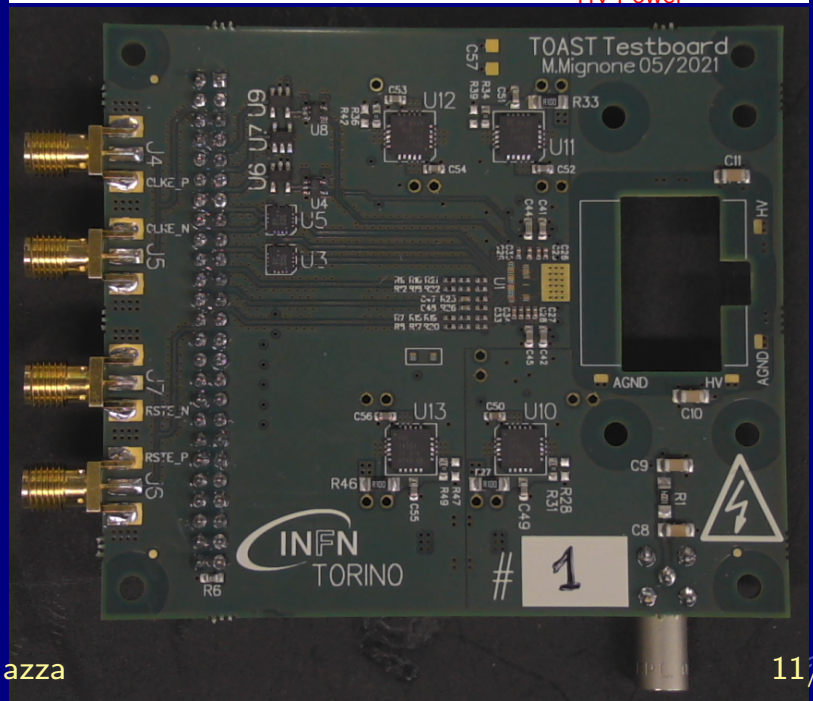


- CMOS UMC 0.11 $\mu$m technology
- Digital-on-top design flow
- Die size : $3.24 \times 4.41$ mm$^2$
- Left pads pitch (on two rows) : 63 $\mu$m
- Right pads pitch : 90 $\mu$m
- Three power domains : analog, digital, digital pads *(all supply voltages at 1.2 V)*
- One external analog reference ($V_{BG} = 600$ mV)
- SLVS driver/receivers
- Submitted on April $26^{th}$ 2021
- Received on October $15^{th}$ 2021

# Test PCB



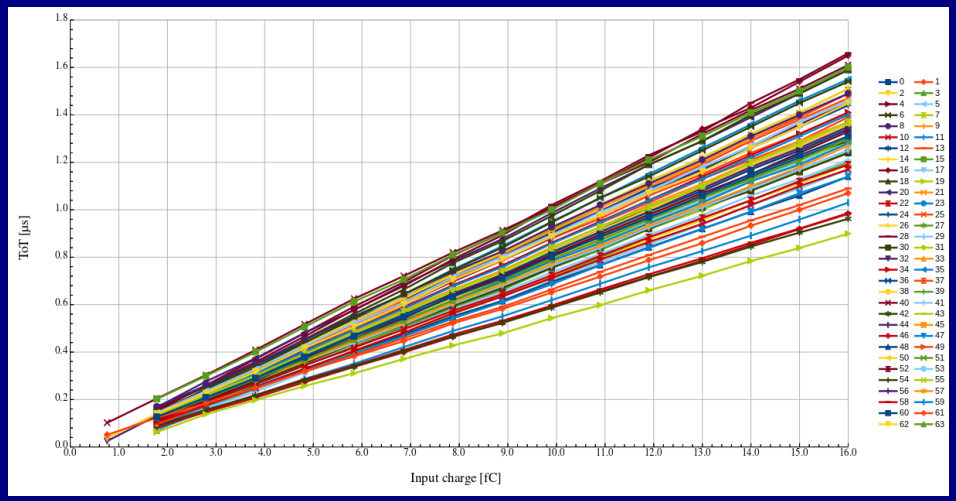



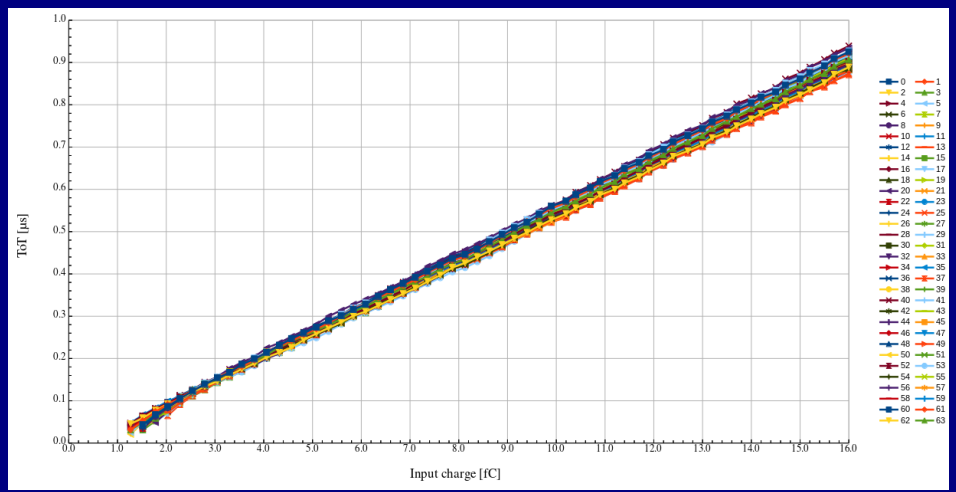

- Test setup based on a Xilinx Kintex 7 Evaluation Board
- Few external components (voltage regulators, SLVS to LVDS converters/drivers)
- Adjustable supply voltage
- Possibility to mount a detector

# Measurement - transfer function

Before calibration

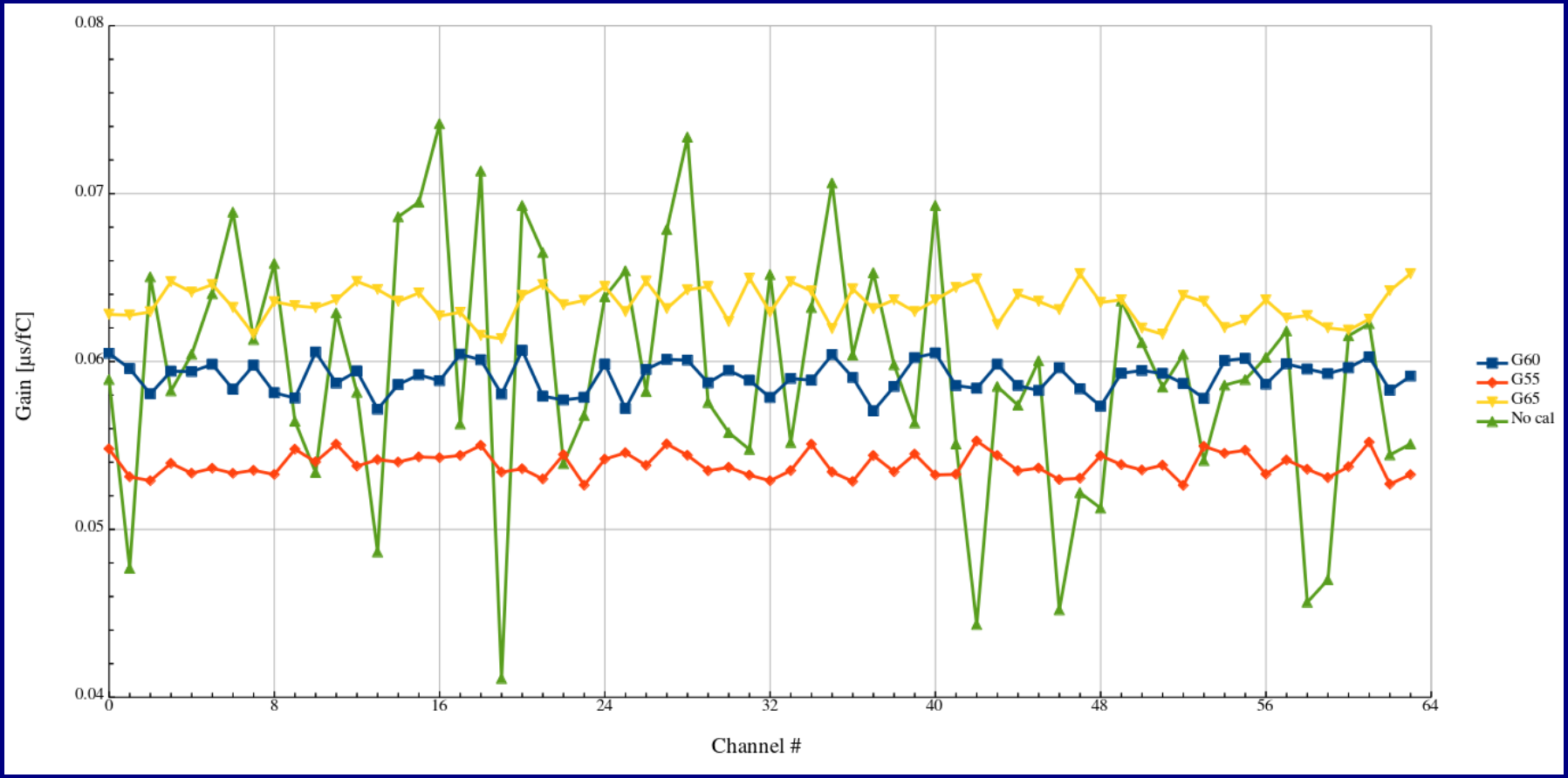



After calibration (gain & offset)



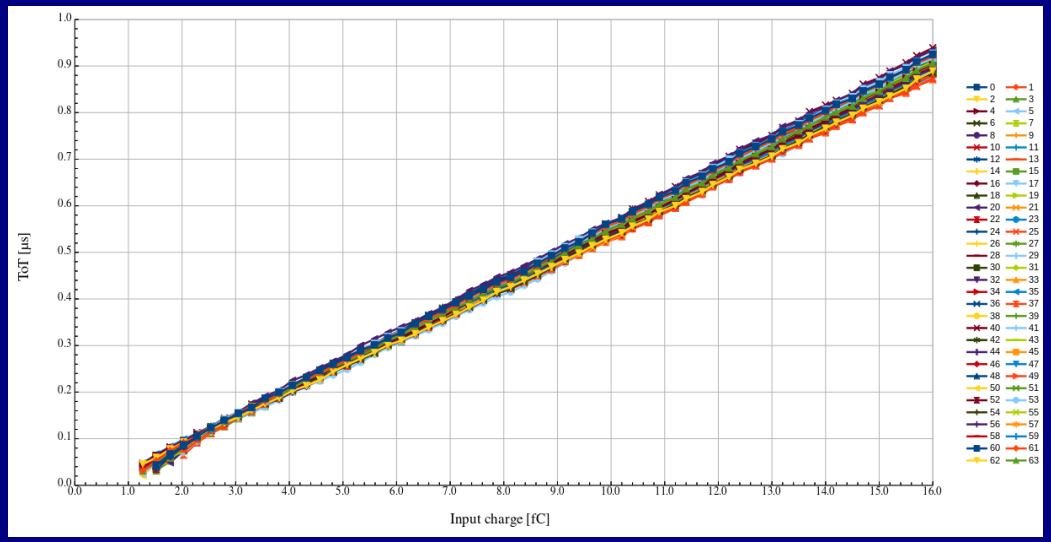

- No smoke at power-on
- Configuration interface ok
- Data transmission ok
- All 64 channels respond correctly to test pulse
- Fairly large gain spread
  - Expected : depends on a very small current
  - Channel level gain calibration implemented - gain spread reduce from 12% to 1.7%
  - Channel level offset calibration implemented - offset spread reduced from 30% to 5.8%
- Power consumption : 180 mW @1.2 V
  - Lower than expected $\rightarrow$ *to be understood*

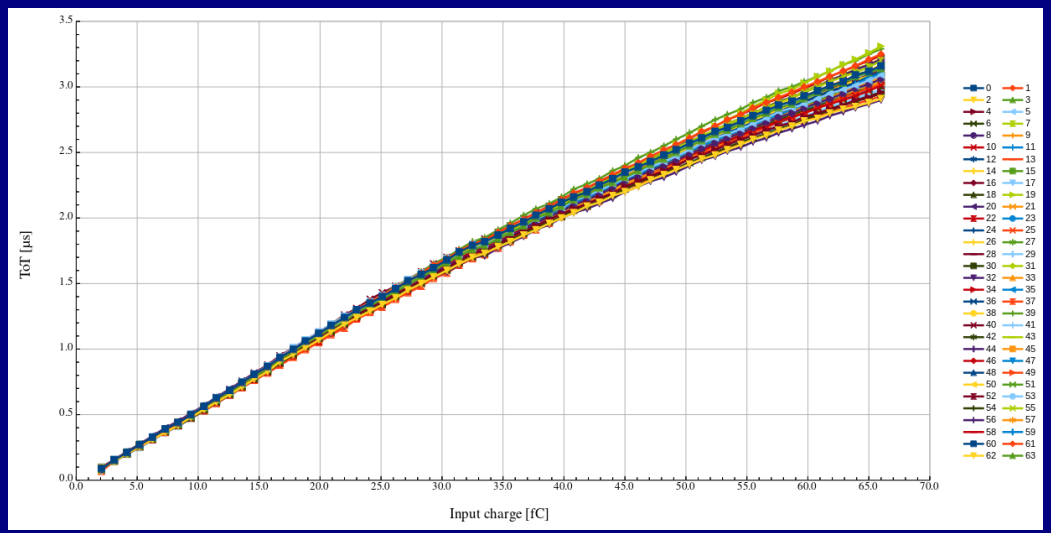
# Measurement - gain calibration




- Calibration procedure :
  - For each channel, measure the transfer curve for each channel ToT Ibias DAC value
  - Select a reference gain
  - For each channel, select the DAC value providing the closest gain

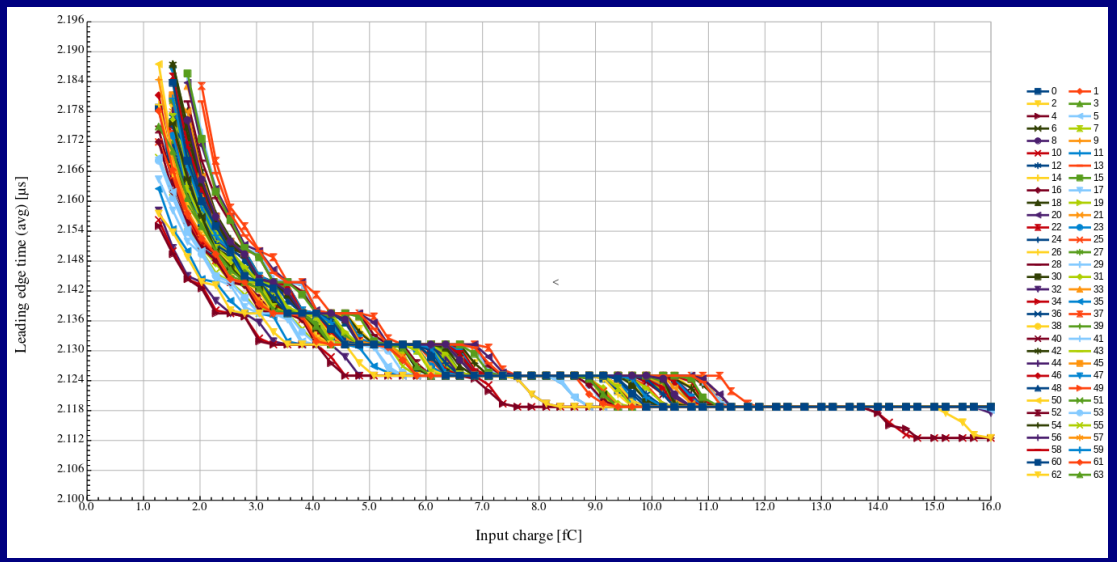
# Measurement - test pulse ranges

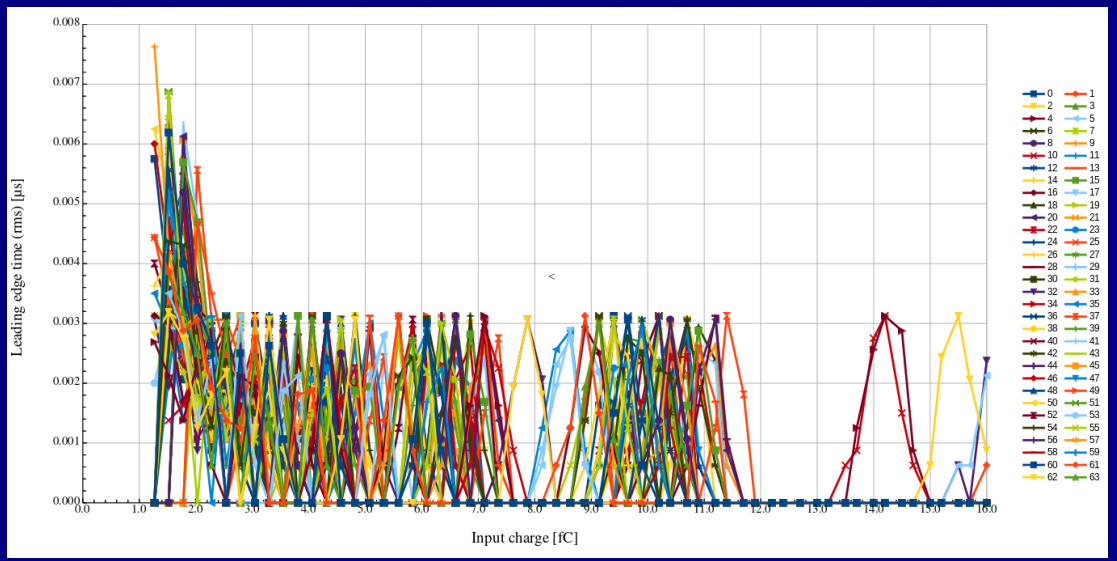



- Test pulse input with internally programmable amplitude via 6+1 bit internal DAC.
- Two test pulse ranges *(the +1 bit)* :
  - Normal range : up to 16 fC, step 0.25 fC
  - Extended range : up to 66 fC, step 1.03 fC
- Non linearity (rms) $<0.64\%$ in the $2 \div 16$ fC range

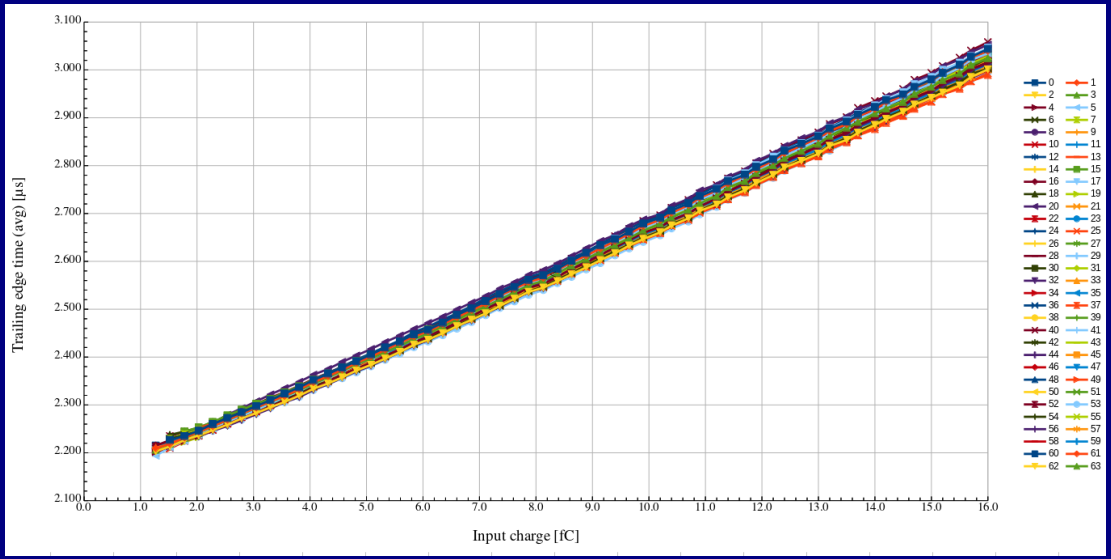
# Measurement - leading edge

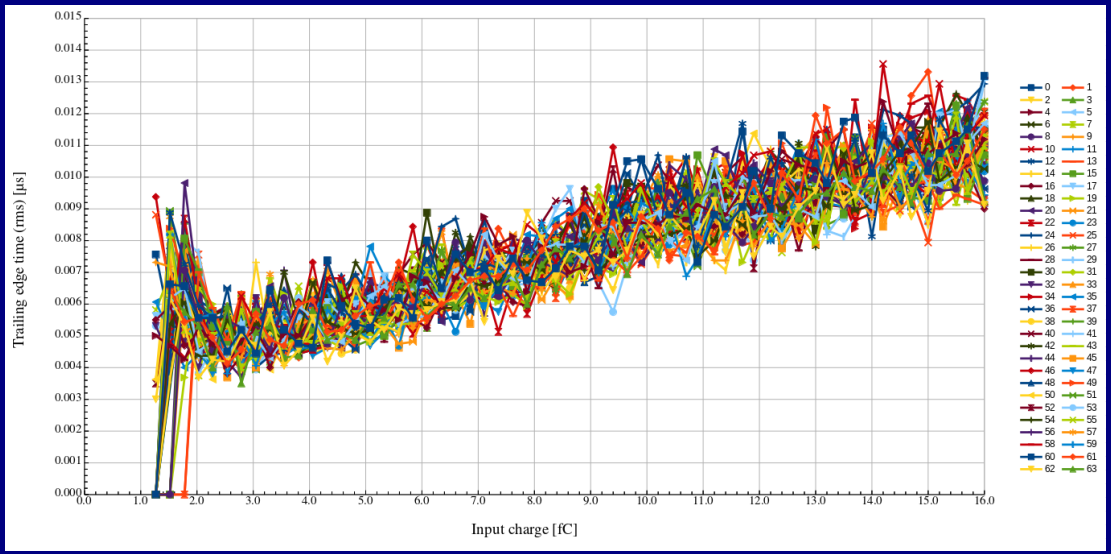



- Test : test pulses synchronous with reset
- Leading egde time
  - Average *(top)*
  - rms *(bottom)*
- Events per channel : 100
- Time bin : 6.25 ns

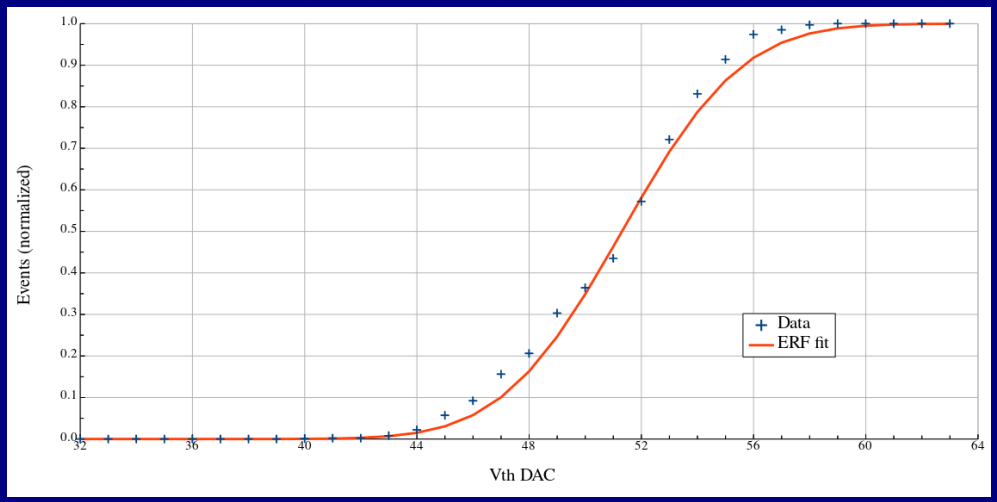
# Measurement - trailing edge

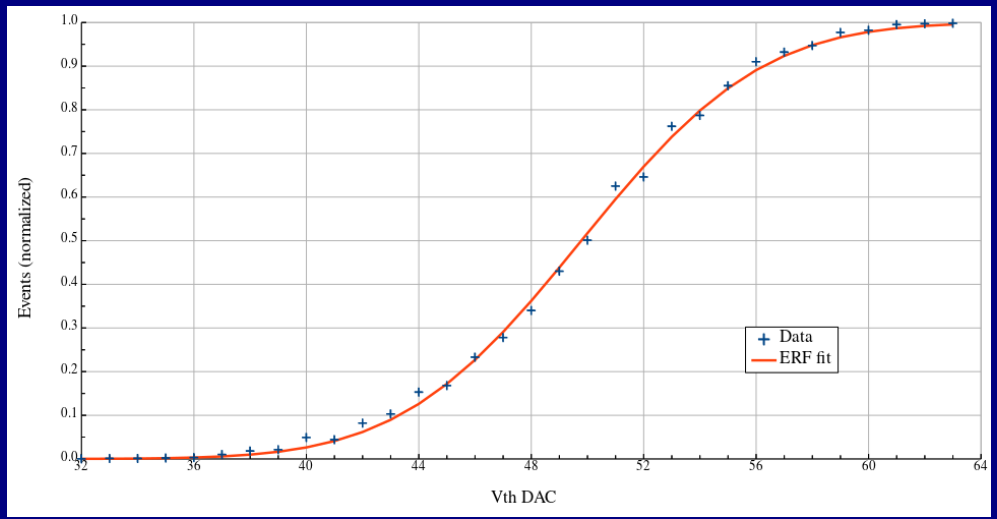



- Test : test pulses synchronous with reset
- Trailing egde time
  - Average *(top)*
  - rms *(bottom)*
- Events per channel : 100
- Time bin : 6.25 ns

# Measurement - noise




- S-curve obtained with channel threshold scan
  - Test pulse resolution and global threshold resolution too coarse
  - Baseline resolution gives similar results but with fewer points
- Conversion from DAC codes to input charge from simulations
- 10 channels analized so far, no input capacitance
- Average noise : 0.034 fC (211 $e^-$)
- Maximum noise : 0.05 fC (312 $e^-$)

# Test for Single Event Upset tolerance

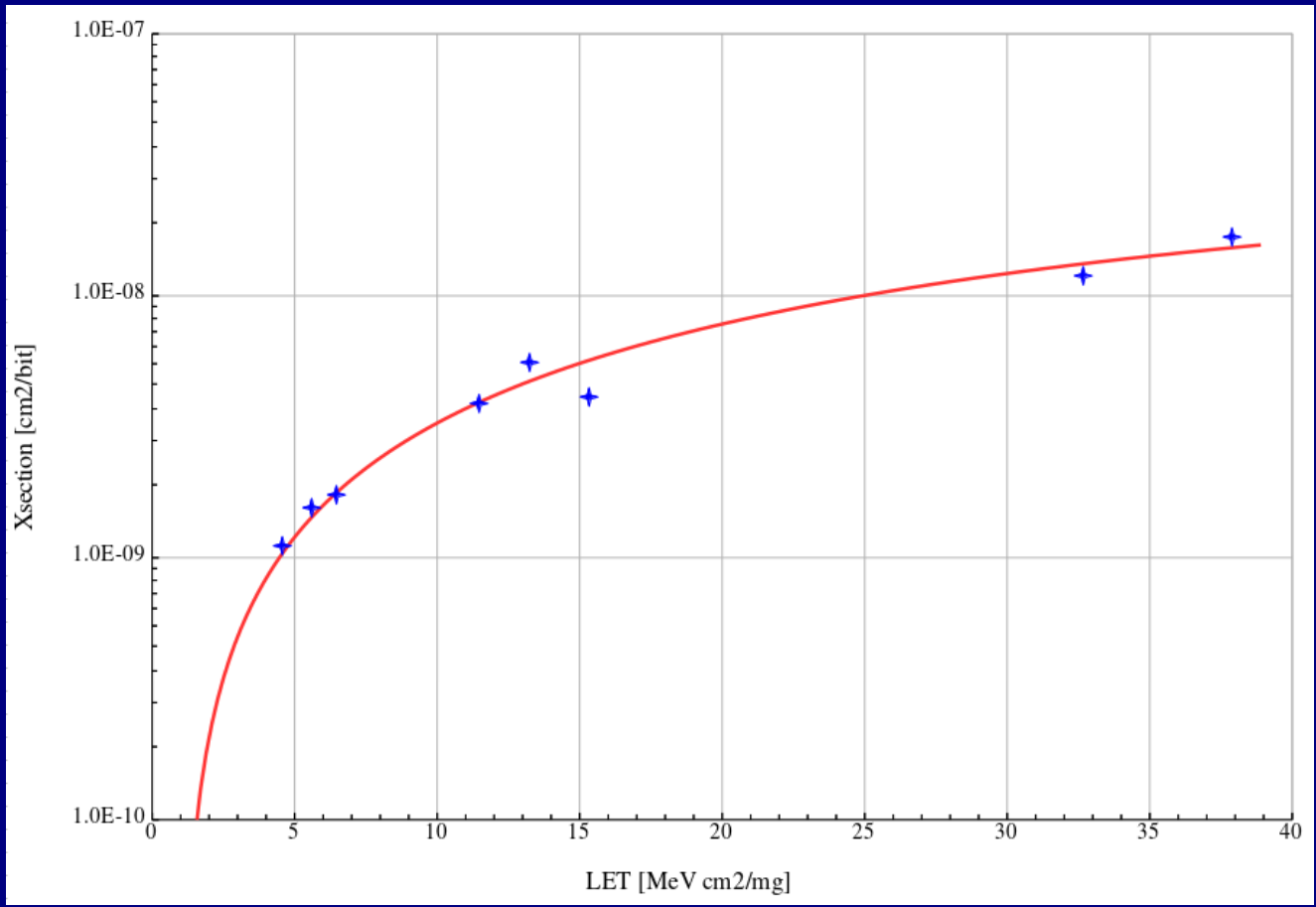
- Test at the SIRAD facility at LNL
  - May $23^{th}$-$24^{th}$ 2022
  - Beam time : 48 hours

| Ion | Angle | Energy $[MeV]$ | LET $[MeV \cdot cm^2/mg]$ | Fluence $[ions/cm^2]$ |
|---|---|---|---|---|
| O | 0° | 95.4 | 4.57 | $6.31 \cdot 10^7$ |
| F | 0° | 110.7 | 5.60 | $1.01 \cdot 10^8$ |
| F | 30° | 110.7 | 6.47 | $3.03 \cdot 10^7$ |
| Si | 0° | 141.6 | 11.47 | $6.80 \cdot 10^7$ |
| Si | 30° | 141.6 | 13.24 | $4.11 \cdot 10^7$ |
| Cl | 0° | 162.7 | 15.33 | $4.99 \cdot 10^7$ |
| Br | 0° | 218.9 | 32.67 | $4.39 \cdot 10^7$ |
| Ag | 0° | 247.0 | 37.89 | $1.52 \cdot 10^7$ |

Aim : estimate the SEU rate at LHC from ions cross section

*(reference : M.Huhtinen and F.Faccio, Computational method to estimate Single Event Upset rates in an accelerator environment, NIM A 450 (2000) pp 155-172)*

# Cross section - preliminary results




- Very preliminary results (*ophthalmic* fit)
- Estimated cross section for 200 MeV protons : $3\times10^{-15}$ cm$^2$
- Hadron flux $5\times10^6$ hadrons/(cm$^2\times$s) $\rightarrow$ $9.3\times10^{-2}$ errors/(h chip)
- *To be understood :* only 1$\rightarrow$0 errors observed

# Status

- Design submitted on April $26^{th}$ and received on October $15^{th}$ 2021
- Test ongoing :
  - Digital interface ok
  - Analog channels answers correctly to test pulse
  - Channel-level calibration required *(gain+offset)*
  - Good linearity
  - Low jitter on leading and trailing edge
  - Low noise - *(at least without detector)*
  - Power consumption 180 mW
- Test to be done :
  - Noise as a function of peaking time
  - Analogue bias optimization
  - Test with detector
  - SEU tests just completed, analysis ongoing
- Issues :
  - Yield - so far 50% : 6 out of 12 good dies

# Spare slides

# ToASt pinout

| Pin name | Direction | Description |
|---|---|---|
| in[63:0] | In | Analog inputs |
| PonRstb | In | Power on asynchronous reset |
| RstSync | Rx | Synchronous reset |
| ChipAddr[6:0] | In | Chip address |
| TestPulse | In | Digital test pulse |
| CfgRx | Rx | Configuration receiver |
| CfgTx | Tx | Configuration transmitter |
| TxOut_0 | Tx | Data serial output 0 |
| TxOut_1 | Tx | Data serial output 1 |
| $V_{BG}$ | In | Analog bandgap reference |
| $V_{DDA}$,$V_{SSA}$ | IO | Analog supply and ground |
| $V_{DDD}$,$V_{SSD}$ | IO | Digital supply and ground |
| $V_{DDE}$,$V_{SSE}$ | IO | Pads supply and ground |