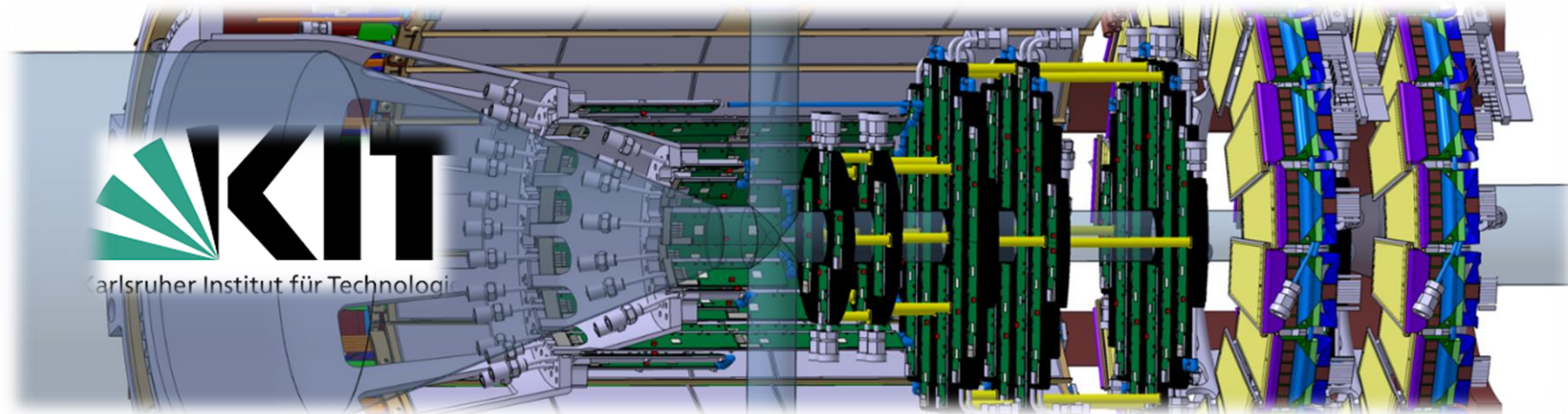


Status of DAQ development

Michele Caselle, Vladimir Sidorenko, Kai Lukas Unger, Olena Manzhura



Summary of the DAQ activities at KIT

Hardware, firmware and System-on-Chip

■ Hardware:

- Development of the Module Data Concentrator ASIC for the PANDA microstrip (UMC 110 nm) → *see MVD session (Caselle/Sidorenko's slide)*
- Development of the MVD Multiplexer Board (MMB) – AMC card
 - Similar design of the PANDA-DC (Pawel)

■ Firmware common infrastructure:

- Development of a ETH data link operating from few Gb/s up to 100 Gb/s
 - First implementation on UltraScale+ RFSoc ZCU216 (*by Olena*)
- Development of initial firmware for the PANDA-DC

PLL configuration of PANDA-DC card

Initial firmware, configuration of the on-board PLL at start-up

FPGA

100 MHz

100 MHz

CF_EMCL

Serial
Peripheral
Interface

RCV_CLK_p/n
PLL_CLK_SEL
PLL_SDIO
PLL_SCL
PLL_SCSN
PLL_STATUS_0
PLL_STATUS_1
PLL_RESETN
PLL_SYNC

100 MHz

PLL

CLKin0
PLL_CLK_SEL,
PLL_SDIO,
PLL_SCL,
PLL_SCSN,
PLL_STATUS_0,
PLL_STATUS_1,
PLL_RESETN,
PLL_SYNC

LMK04610

CLK 0
CLK 1
CLK 2
...

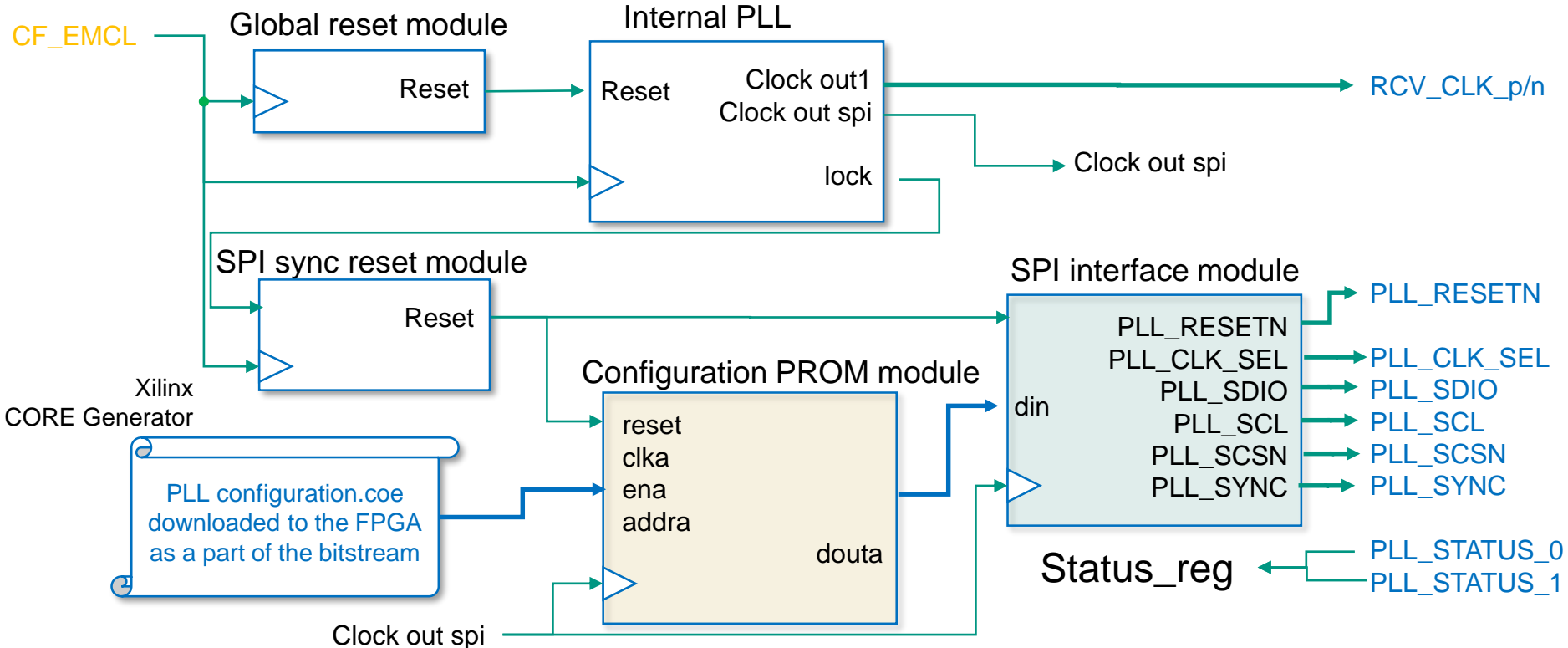
CLK 5

MGTREFCLK
FireFly
(100 /156.25 MHz)

- AMC card in stand-alone, only EMCL clock available
- Configuration of the on-board PLL, to be able to generates all necessaries clocks on AMC card

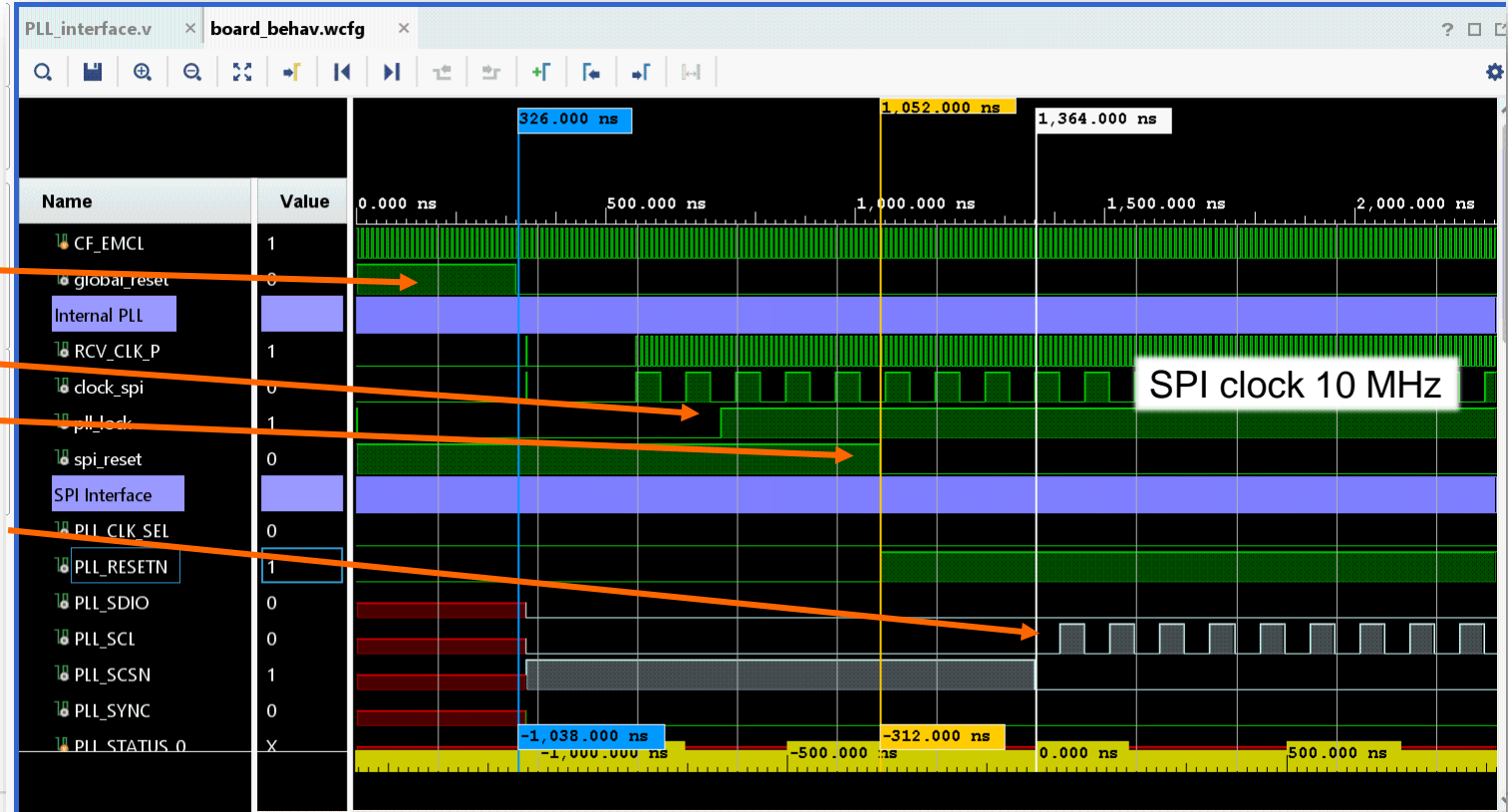
PLL configuration of PANDA-DC card

Firmware architecture



PLL configuration of PANDA-DC card

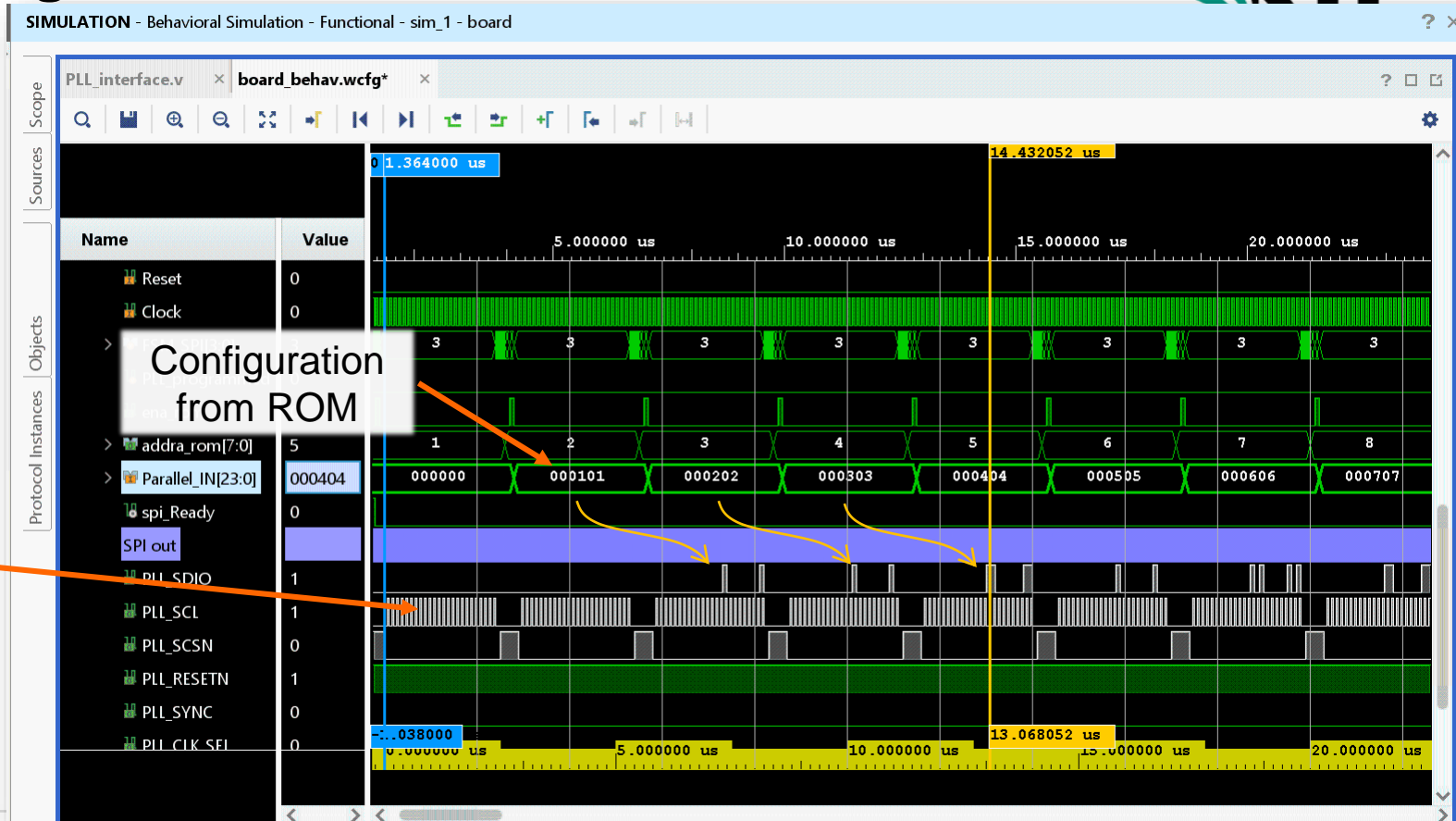
Simulation



Global reset
Int. PLL lock
Sync. reset
Start SPI programming

PLL configuration of PANDA-DC card

Simulation

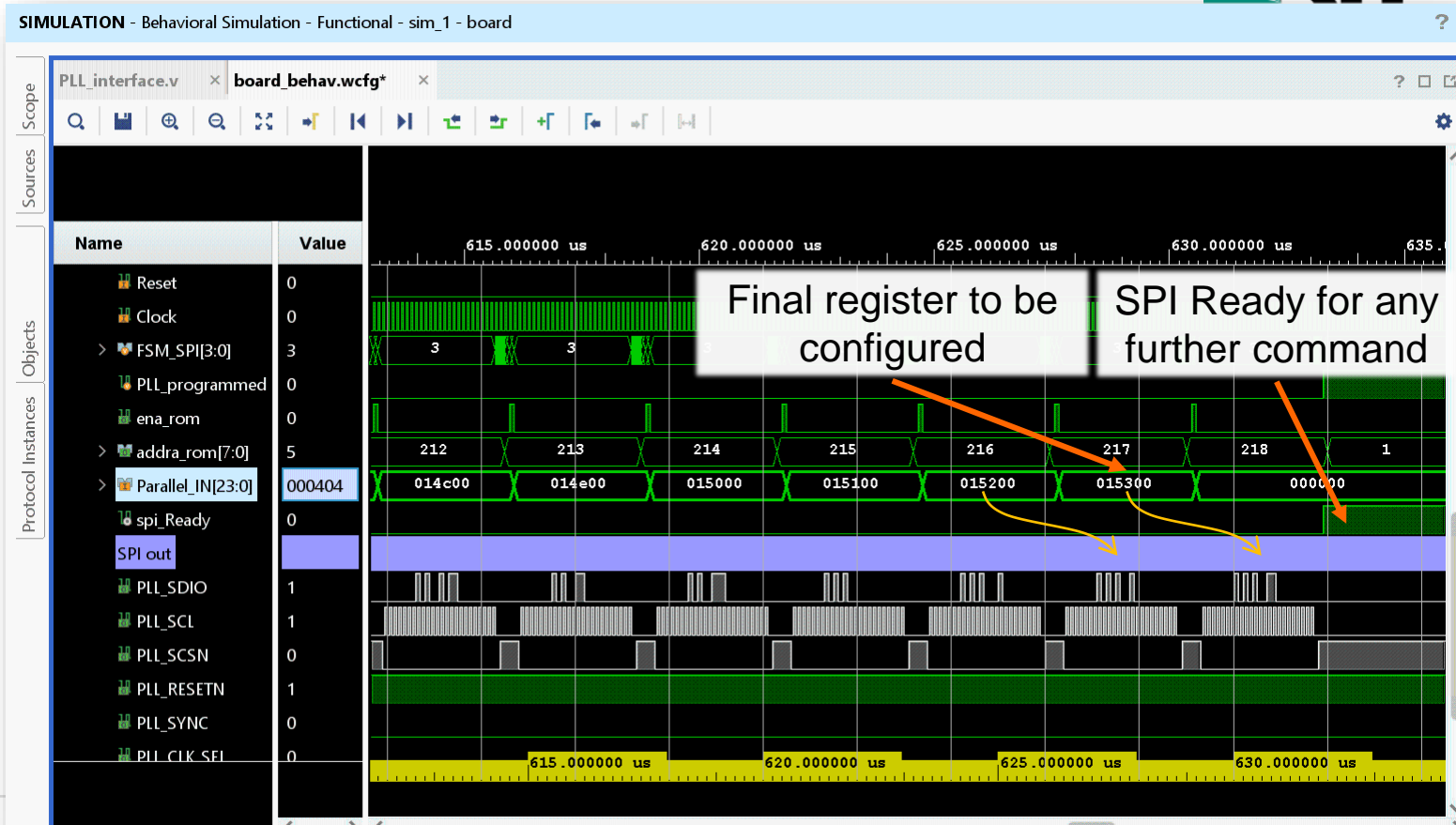


SPI signals to LMK04610

PLL configuration of PANDA-DC card



Simulation



PLL configuration of PANDA-DC card

FPGA implementation

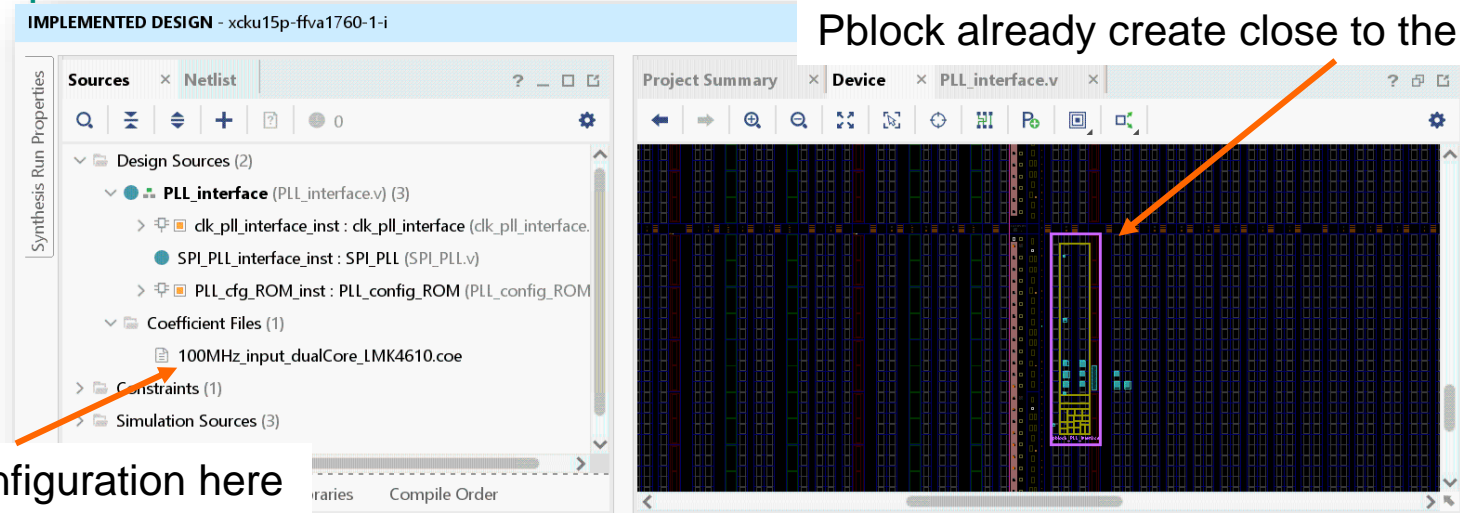
IMPLEMENTED DESIGN - xku15p-ffva1760-1-i

Sources x Netlist

- Design Sources (2)
 - PLL_interface (PLL_interface.v) (3)
 - clk_pll_interface_inst : clk_pll_interface (clk_pll_interface.v)
 - SPI_PLL_interface_inst : SPI_PLL (SPI_PLL.v)
 - PLL_cfg_ROM_inst : PLL_config_ROM (PLL_config_ROM.v)
 - Coefficient Files (1)
 - 100MHz_input_dualCore_LMK4610.coe
 - Constraints (1)
 - Simulation Sources (3)

Project Summary x Device x PLL_interface.v x

Pblock already create close to the SPI I/Os



For PLL configuration here

Tcl Console Messages Log Reports Design Runs Power DRC Methodology Timing x

Design Timing Summary

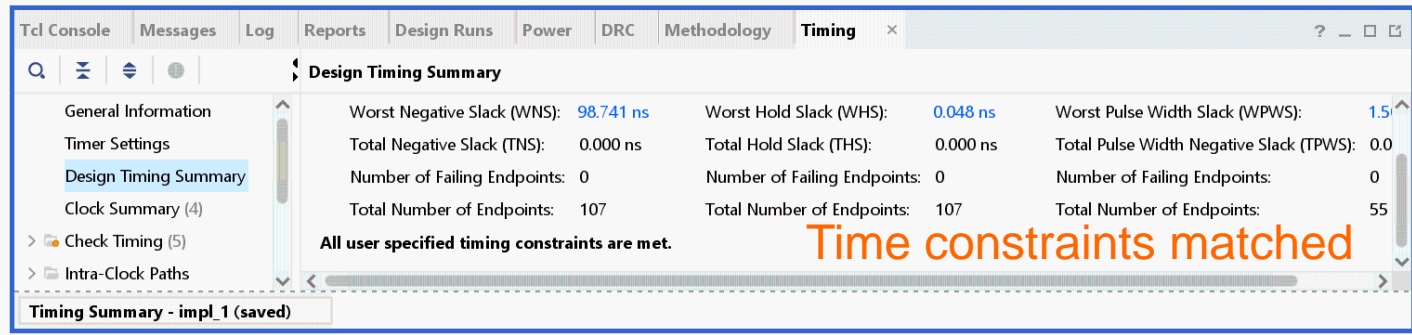
General Information	Worst Negative Slack (WNS): 98.741 ns	Worst Hold Slack (WHS): 0.048 ns	Worst Pulse Width Slack (WPWS): 1.5 ns
Timer Settings	Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.0 ns
Design Timing Summary	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Clock Summary (4)	Total Number of Endpoints: 107	Total Number of Endpoints: 107	Total Number of Endpoints: 55

Check Timing (5)
Intra-Clock Paths

All user specified timing constraints are met.

Timing Summary - impl_1 (saved)

Time constraints matched



What's next

- First version of the FPGA firmware ready to be tested
 - Constraint_file.xdc → already prepared for the AMC card (I/Os + FPGA definition)
 - Bitstream file generated

```
project Summary x Device x PLL_interface.v x pll_constraint.xdc x
D:/PANDA/AMC card/PLL_interface_PANDA_DC/PLL_interface_PANDA_DC.srcs/constrs_1/new/pll_constraint.xdc
Q [Icons] // ?
19 ## =====
20
21 create_clock -period 10.000 -name CF_EMCL [get_ports CF_EMCL]
22 set_property CLOCK_DEDICATED_ROUTE FALSE [get_nets IBUF_inst/O]
23 #set_input_delay -clock CF_EMCL -max 1.000 [get_ports {DI_1_p[*]}]
24 #set_input_delay -clock CF_EMCL -min 1.000 [get_ports {DI_1_p[*]}]
25
26 set_property PACKAGE_PIN AJ27 [get_ports CF_EMCL]
27
28 set_property PACKAGE_PIN AP27 [get_ports RCV_CLK_P]
29 set_property PACKAGE_PIN AR27 [get_ports RCV_CLK_N]
30
... set_property INSTURATED_INSTR [get_ports RCV_CLK_P]
```

EMCL clock not optimized as main FPGA clock
“Clock_dedicated_route” constraint needs to be applied

- Add dedicated clock in the next version
- How to test the firmware ?
- How to inform that all operations are successfully performed ?

backup

Development of the MVD Multiplexer Board (MMB)

AMC-card of the MVD off-detector electronics



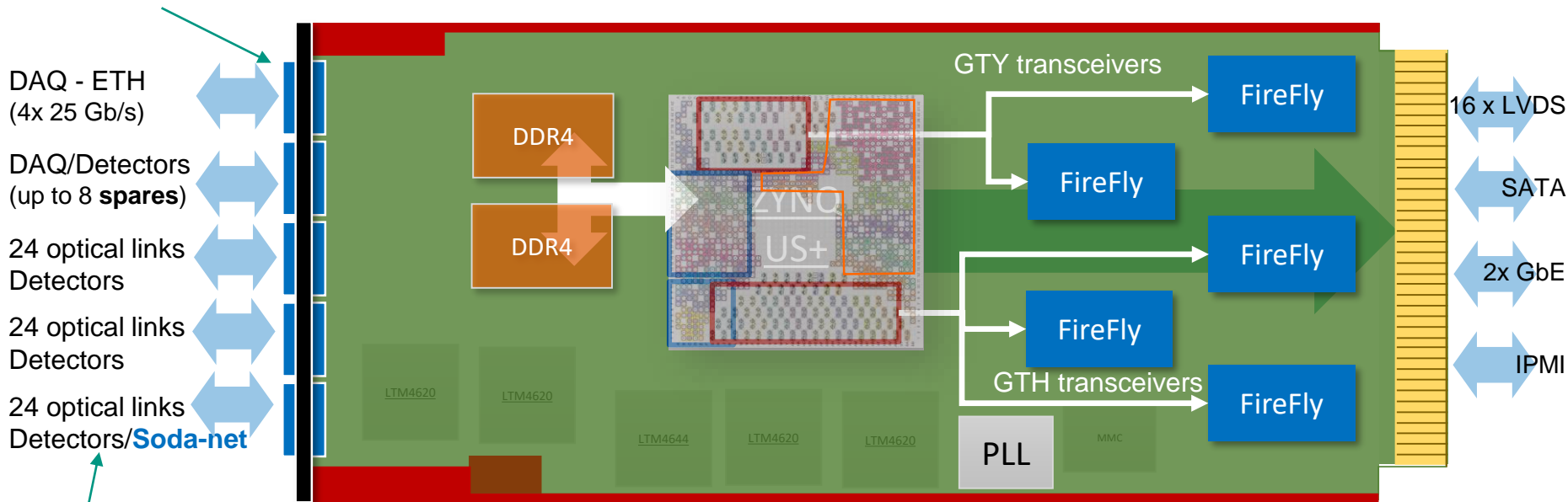
- 80 % of the schematic completed
 - ZYNQ infrastructure, clock distribution, Firefly, DDR4 memory, power supplies, etc.
- PCB placement started
 - SODIMM – DDR4 memory not suitable for an AMC form-factor
 - SODIMM replaced with a “chip soldered” 4GB, 64-bit, 2,666MT/s memory attached to the processing system (PS)
- Currently designed by Xpedition (Mentor) → Altium

Development of the MVD Multiplexer Board (MMB)

AMC-card of the MVD off-detector electronics

Optical connectors

AMC edge connector



Optical links designed to be operated by LpGBT

Soda-net by GTH or GTR transceivers

Si5341

Ultra-low jitter of 90 fs rms