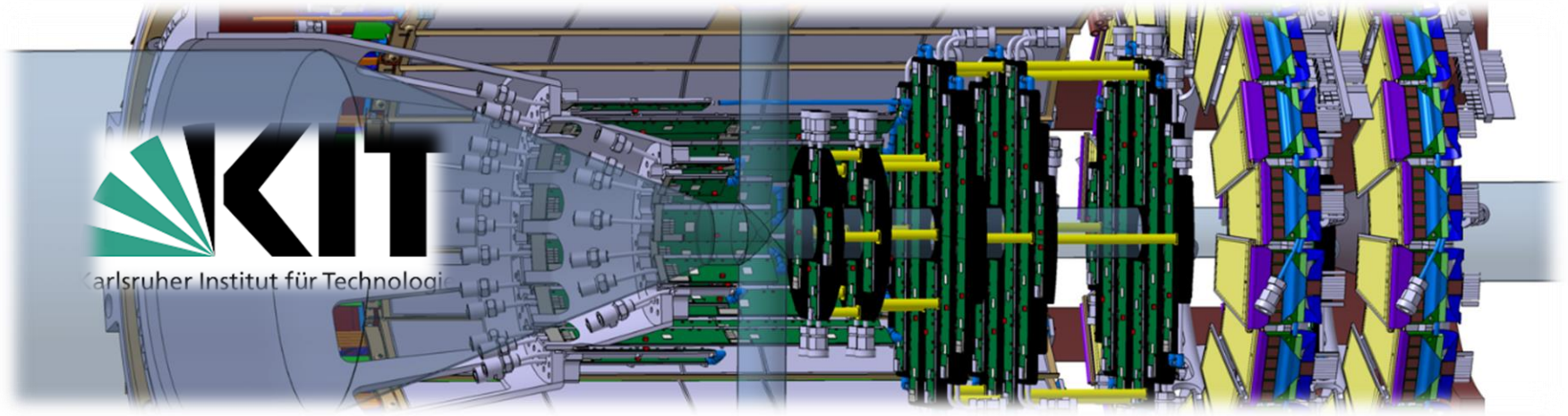
Karlsruhe Institute of Technology

PANDA Collab. Meeting, 30 May, 2022

Status of DAQ development

Michele Caselle, Vladimir Sidorenko, Kai Lukas Unger, Olena Manzhura



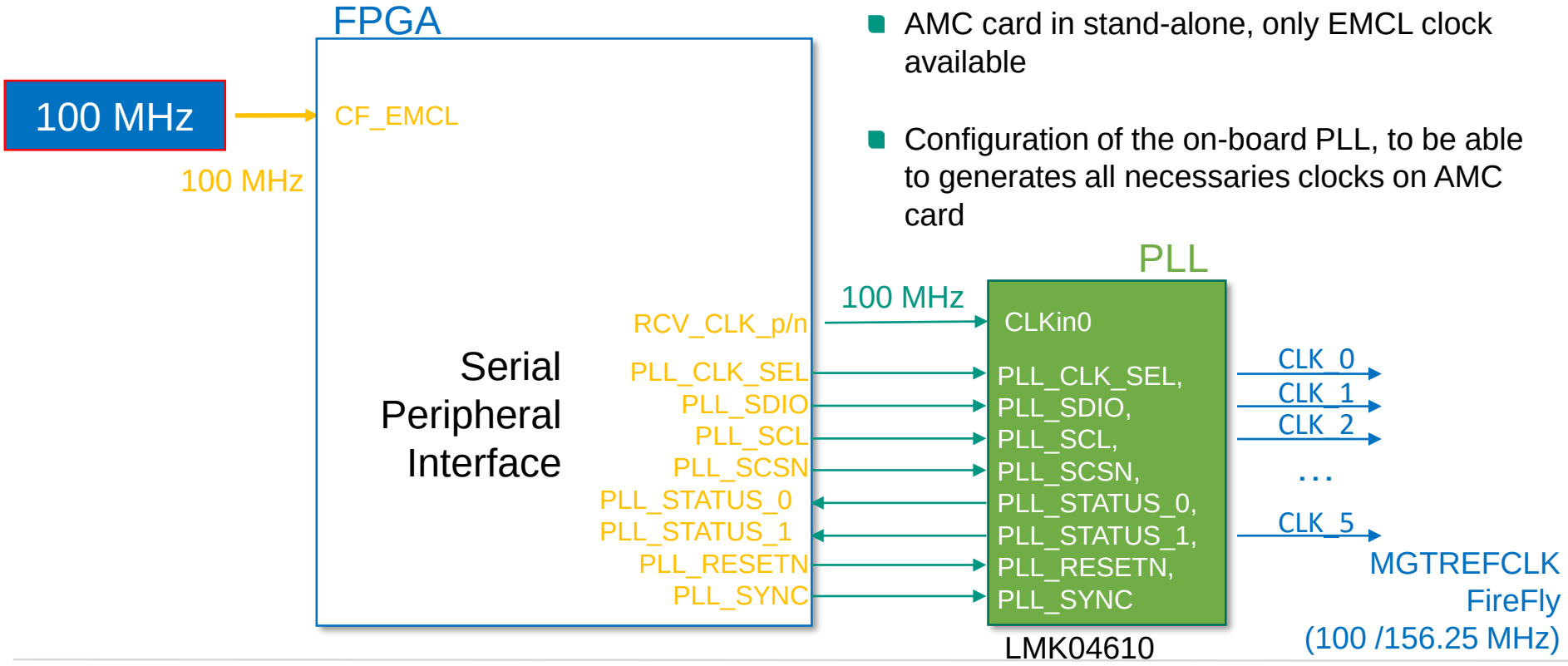
Summary of the DAQ activities at KIT

Hardware, firmware and System-on-Chip

- Hardware:
  - Development of the Module Data Concentrator ASIC for the PANDA microstrip (UMC 110 nm) *→ see MVD session (Caselle/Sidorenko's slide)*
  - Development of the MVD Multiplexer Board (MMB) – AMC card
    - Similar design of the PANDA-DC (Pawel)
- Firmware common infrastructure:
  - Development of a ETH data lnk operating from few Gb/s up to 100 Gb/s
    - First implementation on UltraScale+ RFSoC ZCU216 *(by Olena)*
  - Development of initial firmware for the PANDA-DC

PLL configuration of PANDA-DC card

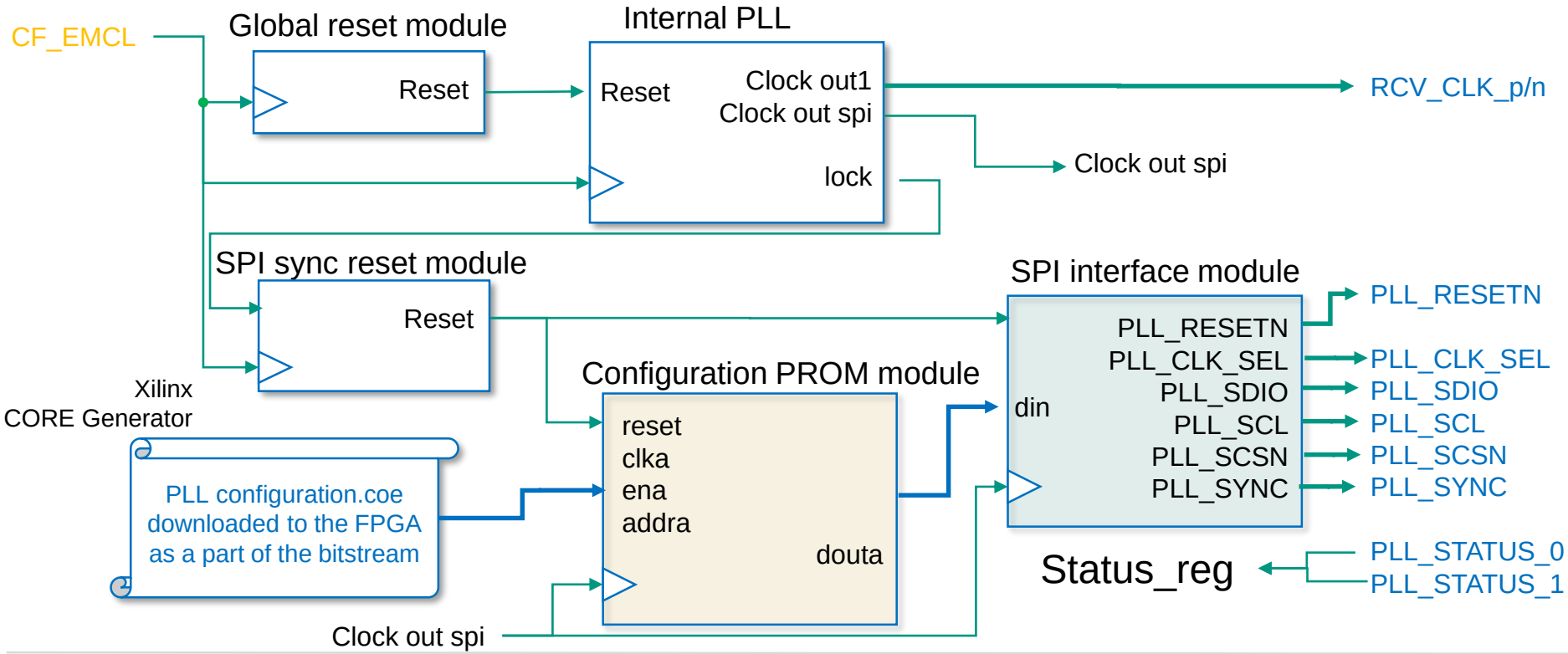
Initial firmware, configuration of the on-board PLL at start-up



- AMC card in stand-alone, only EMCL clock available
- Configuration of the on-board PLL, to be able to generates all necessaries clocks on AMC card

PLL configuration of PANDA-DC card

Firmware architecture



PLL configuration of PANDA-DC card

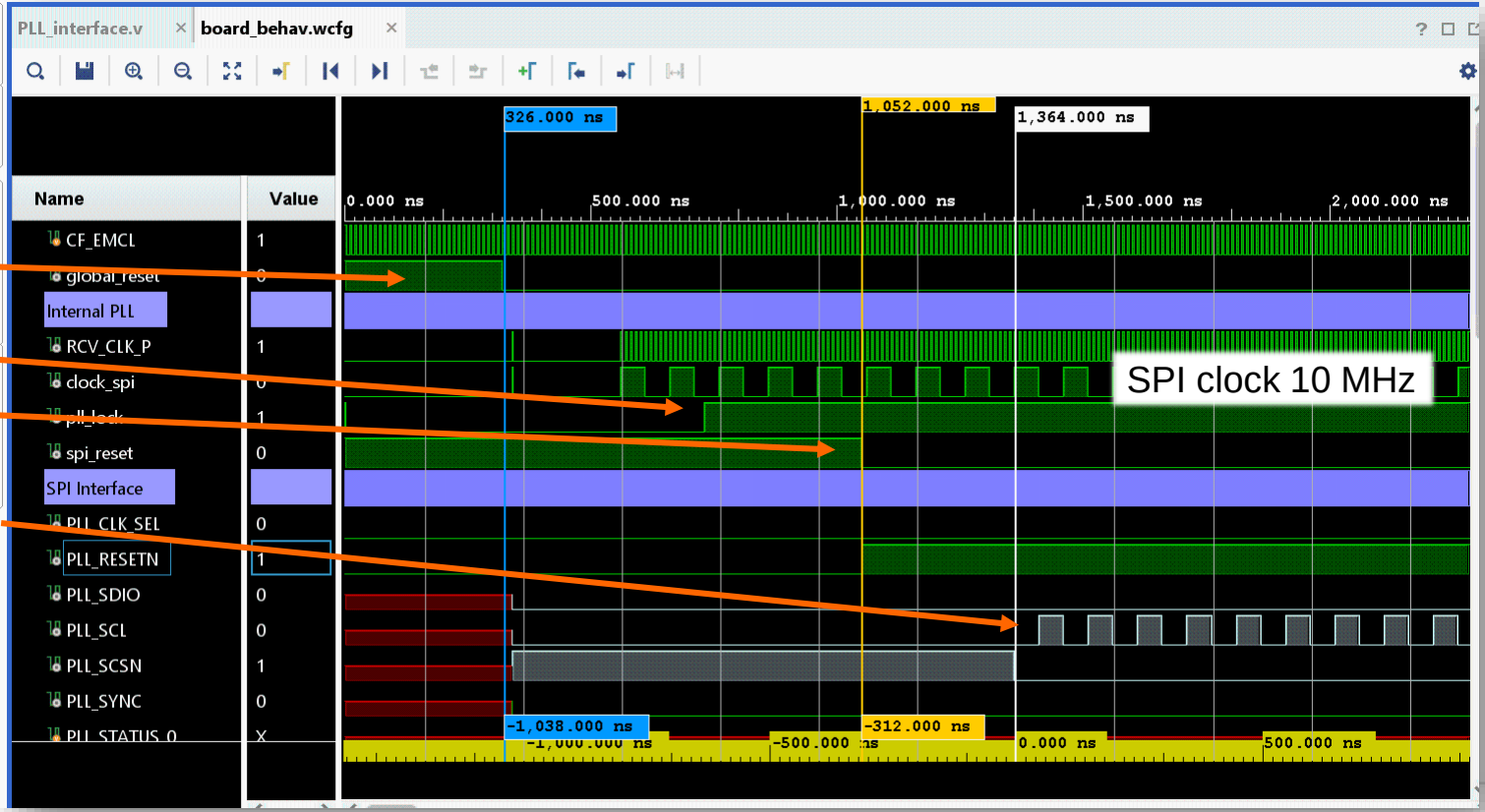
Simulation

Global reset

Int. PLL lock

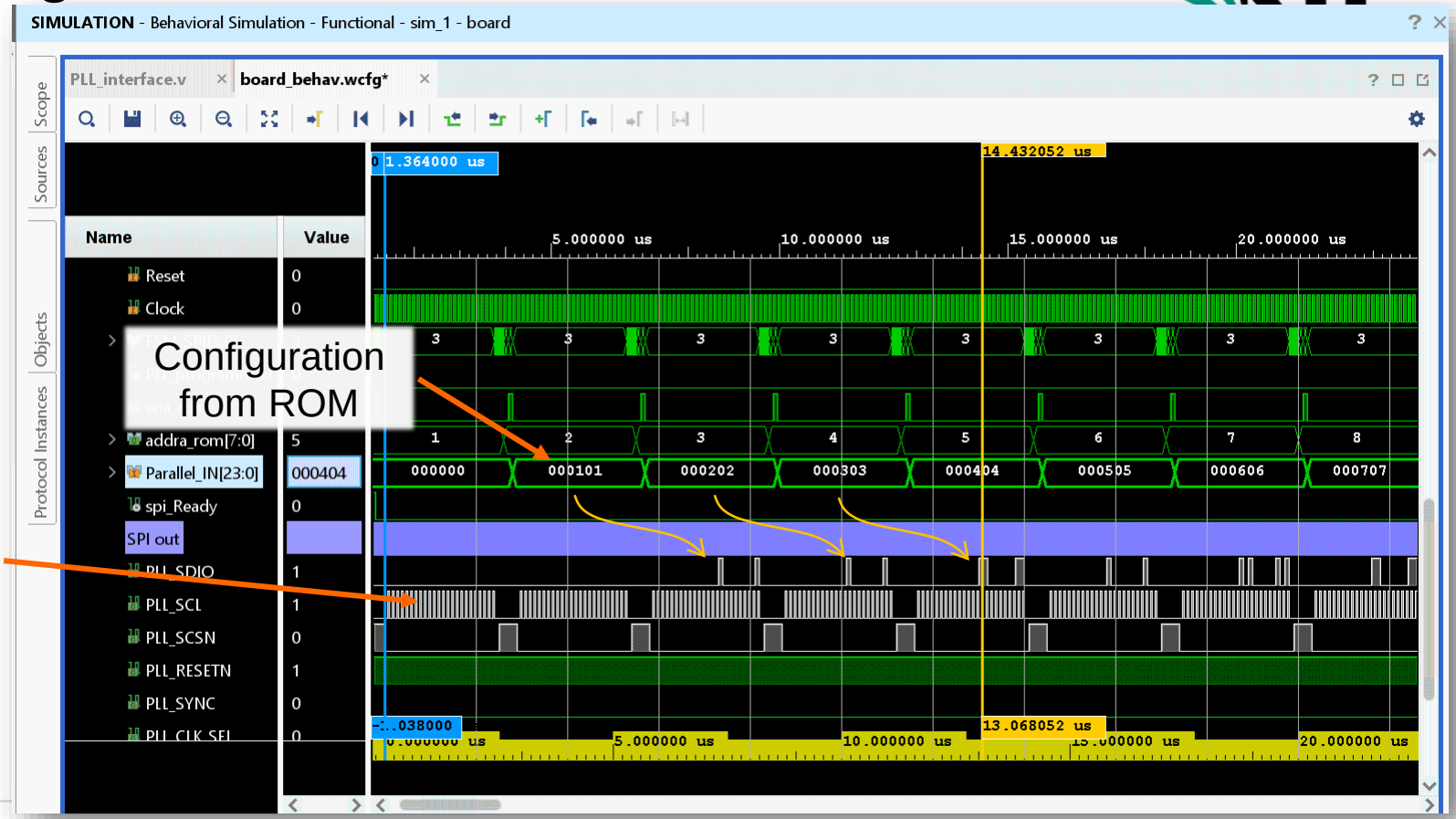
Sync. reset

Start SPI programming



PLL configuration of PANDA-DC card

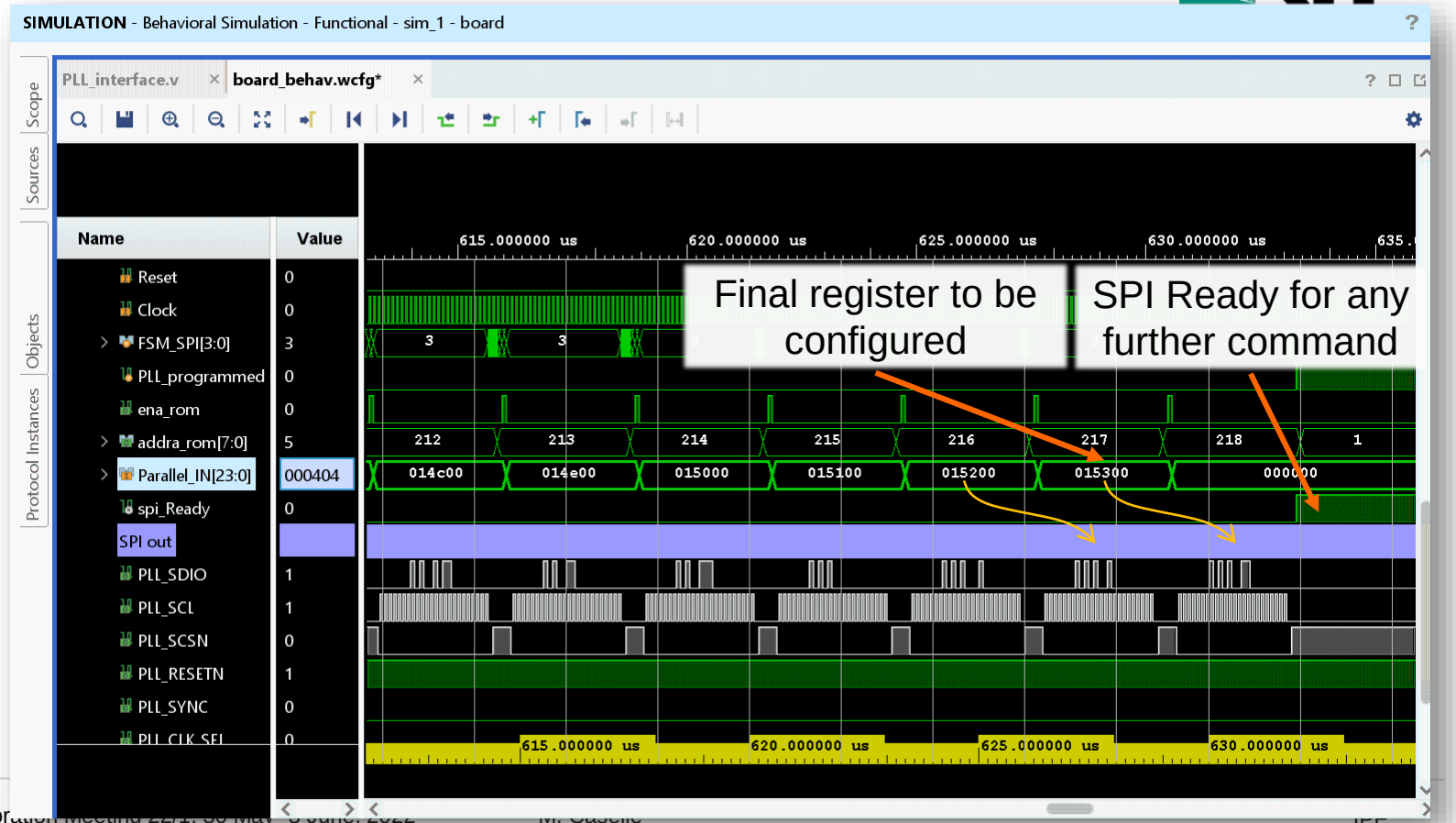
Simulation



SPI signals to LMK04610

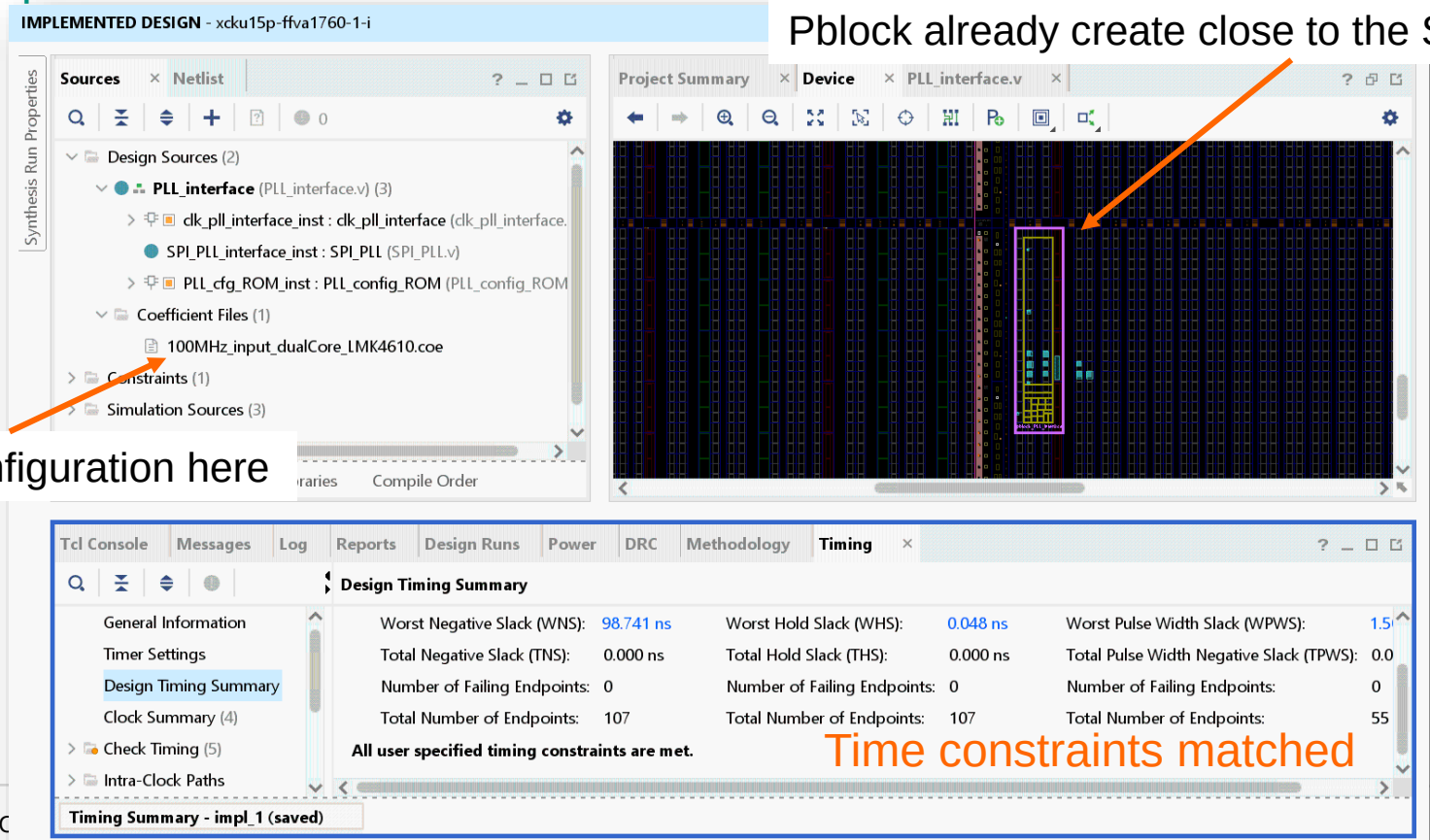
PLL configuration of PANDA-DC card

Simulation



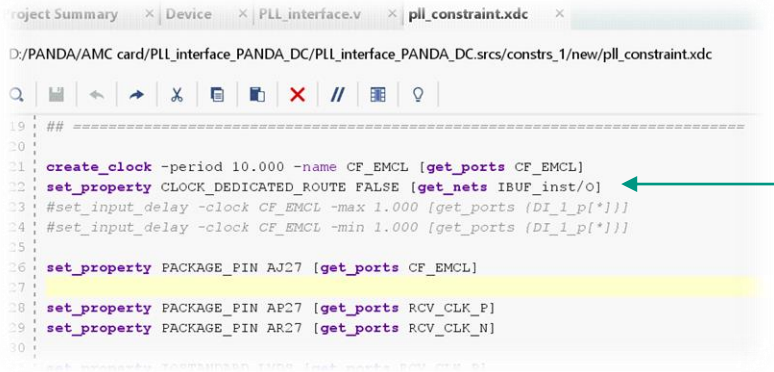
PLL configuration of PANDA-DC card

FPGA implementation



What's next

- First version of the FPGA firmware ready to be tested
  - Constraint_file.xdc → already prepared for the AMC card (I/Os + FPGA definition)
  - Bitstream file generated



EMCL clock not optimized as main FPGA clock
"Clock_dedicated_route" constraint needs to be applied

- Add dedicated clock in the next version
- How to test the firmware ?
- How to inform that all operations are successfully performed ?

Thanks for your attention

backup

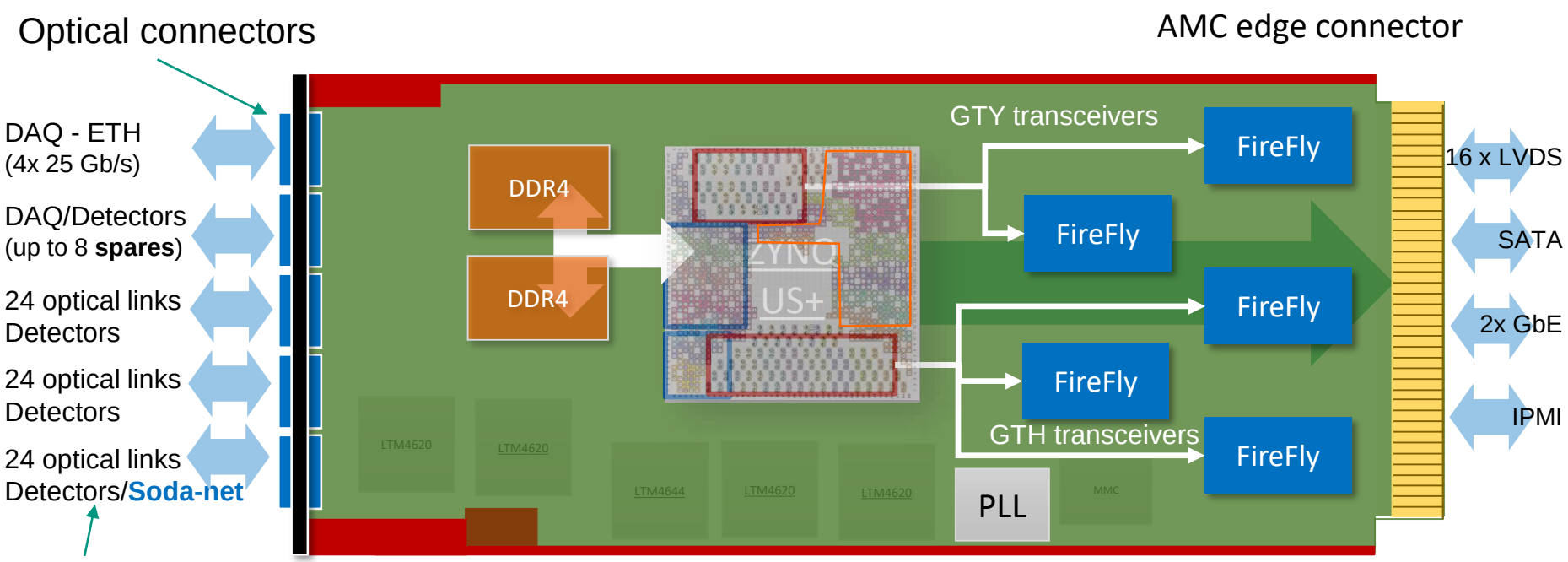
Development of the MVD Multiplexer Board (MMB)

AMC-card of the MVD off-detector electronics

- 80 % of the schematic completed
  - ZYNQ infrastructure, clock distribution, Firefly, DDR4 memory, power supplies, etc.
- PCB placement started
  - SODIMM – DDR4 memory not suitable for an AMC form-factor
  - SODIMM replaced with a “chip soldered” 4GB, 64-bit, 2,666MT/s memory attached to the processing system (PS)
- Currently designed by Xpedition (Mentor) → Altium

Development of the MVD Multiplexer Board (MMB)

AMC-card of the MVD off-detector electronics



Optical links designed to be operated by LpGBT

Soda-net by GTH or GTR transceivers

Si5341

Ultra-low jitter of 90 fs rms