



Upgrade of FT read-out

A. Malige

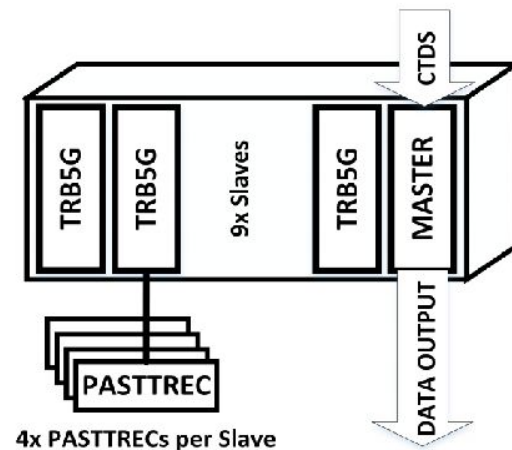
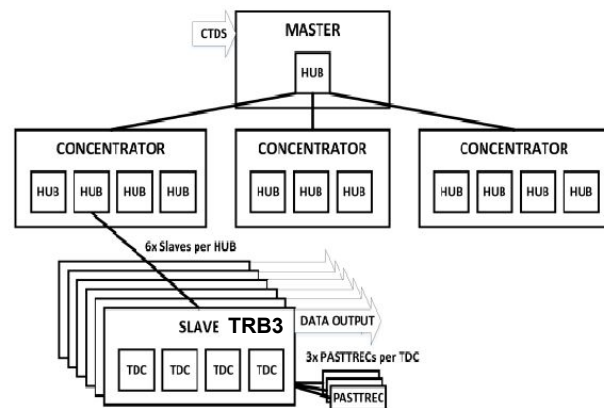
Jagiellonian University and AGH University of Science and Technology,
Krakow, Poland

PANDA Collaboration meeting - May 2022



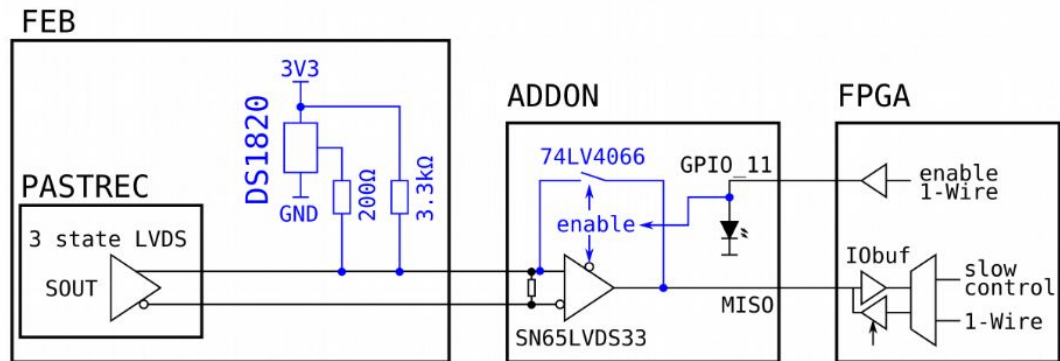
Requirements

- TRB5sc as FT-STs digitizing platform
 - Read-out system capable of handling larger data volumes (ex: PANDA HL-mode [DAQ TDR])
 - Hardware-FPGA (ecp5um) with smaller form-factor
 - Mountable on crates with backplane (communication & power)
 - Add-on card interfacing 64 channels (4 FEBs)
 - STS+FT sub-system uses over 264+764 FEBs
 - TRB3 → 5 ECP3 FPGA's → 12 FEBs
 - TRB5sc → 1 ECP5UM FPGA → 4 FEBs
 - Downscale from 430 ECP3s to 257 ECP5UM's
- Temperature sensor with chip ID
 - Database for PASTTREC configs (baseline, TOT characteristics)
 - Monitor temperature (STS)

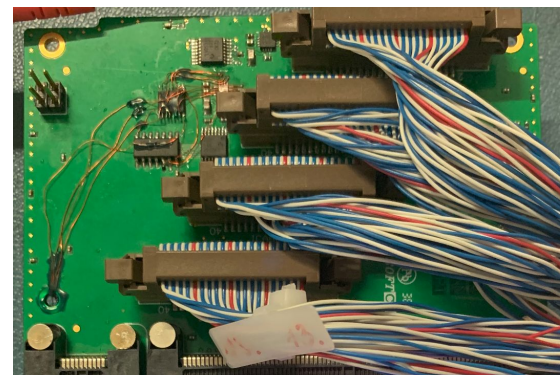
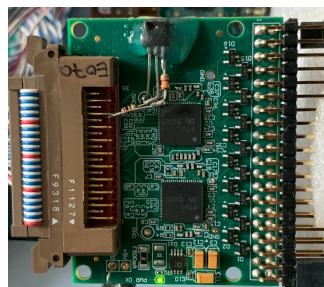


Hardware Modifications

- FEB
 - DS1820 on FEB's with bonded PASTTREC's
 - Low-power cons - connected to the data-line through 200 Ω series resistor.

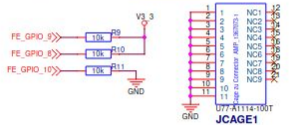
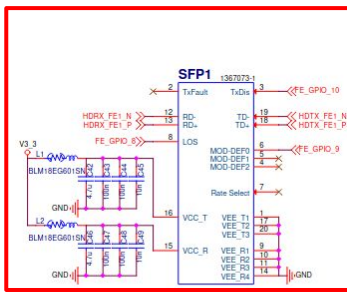
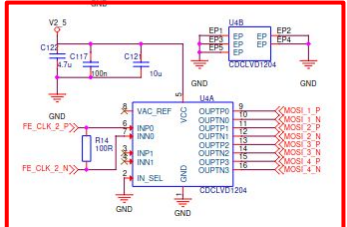
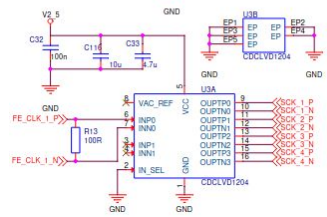
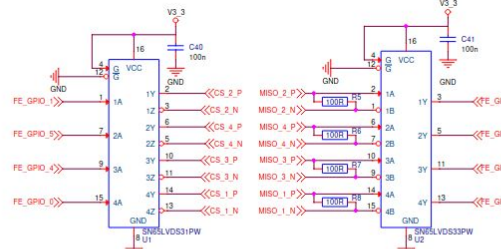


- Add-on
 - Data lines for PASTTREC + DS1820 (CS used for reset)
 - Solutions presented in last meeting (J.Moron, AGH)
- TRB5sc - No changes

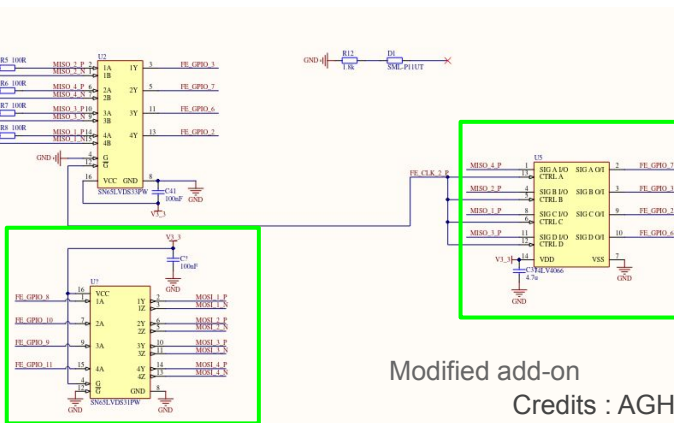
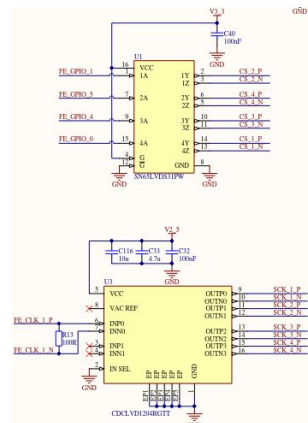


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Add-on for TRB5sc

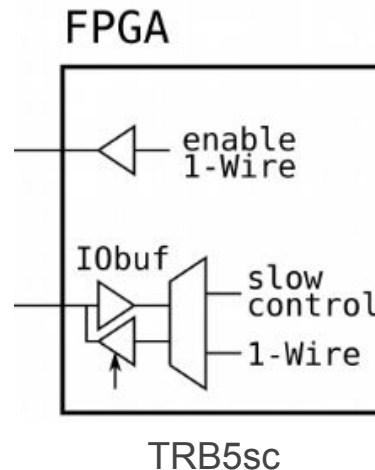


Modified add-on
Credits : AGH

Firmware and Software

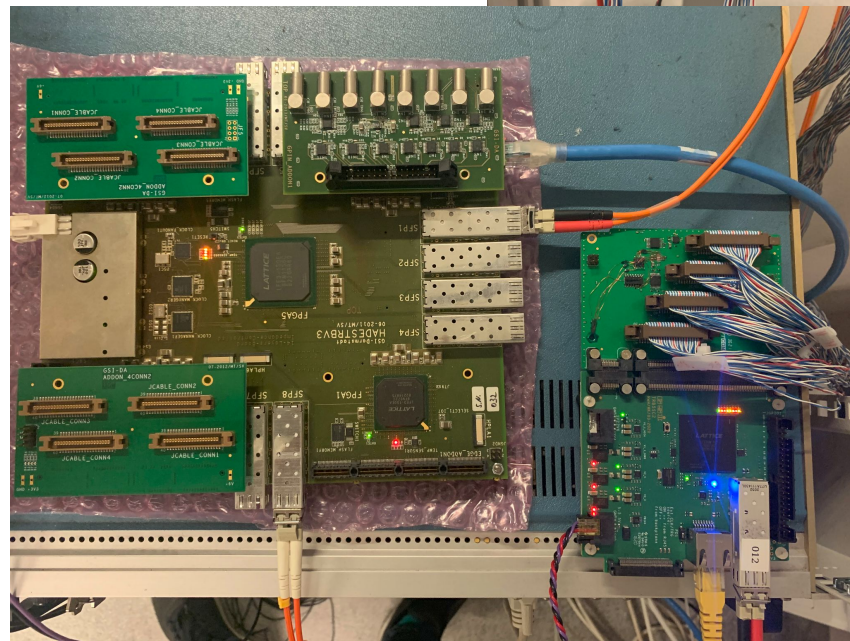
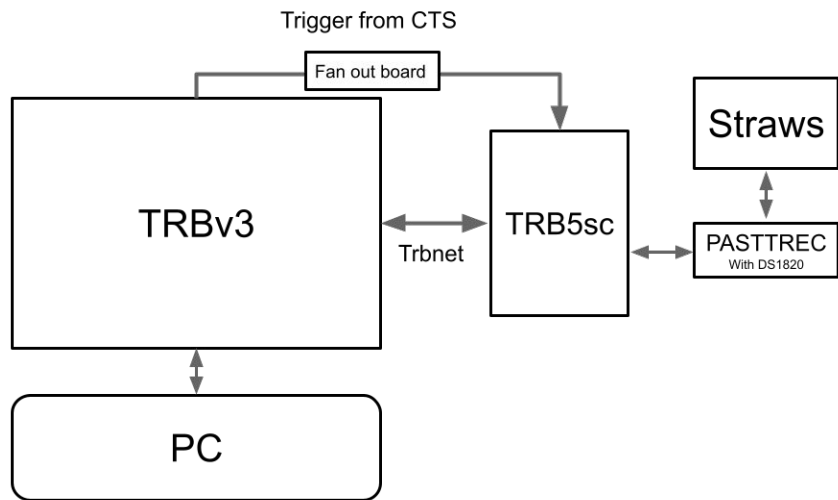
- Firmware - TRB5sc
 - 1 master Onewire core for 4 FEBs
 - Onewire-SPI switching & readback via 'trbcmd' (5 bits)
 - Control & Status Regs : 12-bit temp, 64-bit chipID output
 - trbcmd w 0x6500 0x23 0x3* - 1wire ON
 - trbcmd w 0x6500 0x23 0x0* - 1wire OFF
 - trbcmd r 0x6500 0x8* - Read temp
 - MOSI lines added for PASTTREC-SPI
- Software
 - Updated 'pasttrectools' software for TRB5sc
 - Can handle 4-conns & Onewire functionalities

Reg - 0x23 - 5 bits
 0 0 0 0 0
 FEB select Switch



Lab Tests

- TRBv3 used to interface TRB5 with PASTTRECs
- Tests
 - Switching SPI-Onewire, reading temp-ID
 - 4 seconds for 1 read-cycle
 - Pasttrec configs, baseline scans, trigger
 - Straw data - TOT from Fe⁵⁵



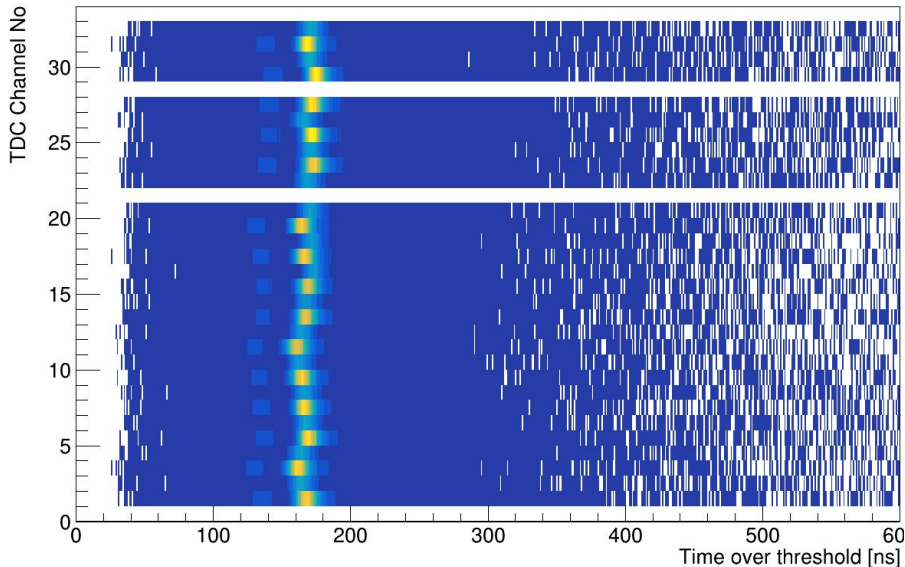
Lab Tests

```

~/go4/new_release/trb3/trb5sc_tests/tr5sc_pasttrec_utils> asic_tempid.py 0x6500
INFO: Trbnet library not found.
Temperature in 0x6500 cable 0 is      :      27.750 °C
Temperature in 0x6500 cable 1 is      :      27.562 °C
Temperature in 0x6500 cable 2 is      :      26.500 °C
Temperature in 0x6500 cable 3 is      :      25.688 °C
Chip ID in 0x6500 cable 0 is          :      1b00000d9e778128
Chip ID in 0x6500 cable 1 is          :      3400000d9d49a028
Chip ID in 0x6500 cable 2 is          :      7400000d9e0f5a28
Chip ID in 0x6500 cable 3 is          :      d100000d9e3cdd28

(0) pandastraws@pandastraws (main) 10:20:40
~/go4/new_release/trb3/trb5sc_tests/tr5sc_pasttrec_utils> asic_read.py 0x6500
INFO: Trbnet library not found.
TDC Cable Asic Reg#  0  1  2  3  4  5  6  7  8  9  10  11
0x6500 0  0      0x1e 0x1e 0x15 0x0a 0x16 0x14 0x12 0x19 0x1e 0x14 0x14 0x1a
0x6500 0  1      0x1e 0x1e 0x15 0x0a 0x1a 0x13 0x18 0x0e 0x17 0x17 0x14 0x1a
0x6500 1  0      0x1e 0x1e 0x15 0x0a 0x17 0x18 0x18 0x17 0x17 0x17 0x17 0x17
0x6500 1  1      0x1e 0x1e 0x15 0x0a 0x17 0x17 0x17 0x17 0x17 0x17 0x16 0x17
0x6500 2  0      0x1e 0x1e 0x15 0x0a 0x16 0x14 0x12 0x19 0x1e 0x14 0x14 0x1a
0x6500 2  1      0x1e 0x1e 0x15 0x0a 0x1a 0x13 0x18 0x0e 0x17 0x17 0x14 0x1a
0x6500 3  0      0x1e 0x1e 0x15 0x0a 0x17 0x18 0x18 0x17 0x17 0x17 0x17 0x17
0x6500 3  1      0x1e 0x1e 0x15 0x0a 0x17 0x17 0x17 0x17 0x17 0x17 0x16 0x17
    
```

Checks	Result
PASTTREC 4conn SPI	Pass
PASTTREC 4conn 1wire	Pass
Switching SPI-1wire	Pass
PASTTREC settings during switching	Pass
TDC	32 ch



Summary & Outlook

- PANDA FT milestone reached:
 - Readout with TRB5sc tested successfully
 - Prototype production of modified add-on
 - All FEBs to be implemented with DS1820
- Future Plans
 - Low-resolution TDC with 65 ch.
 - Database for PASTTRECs

Thank you