Karlsruhe Institute of Technology

PANDA Collab. Meeting, 30 May, 2022

Status of MDC and MMB development

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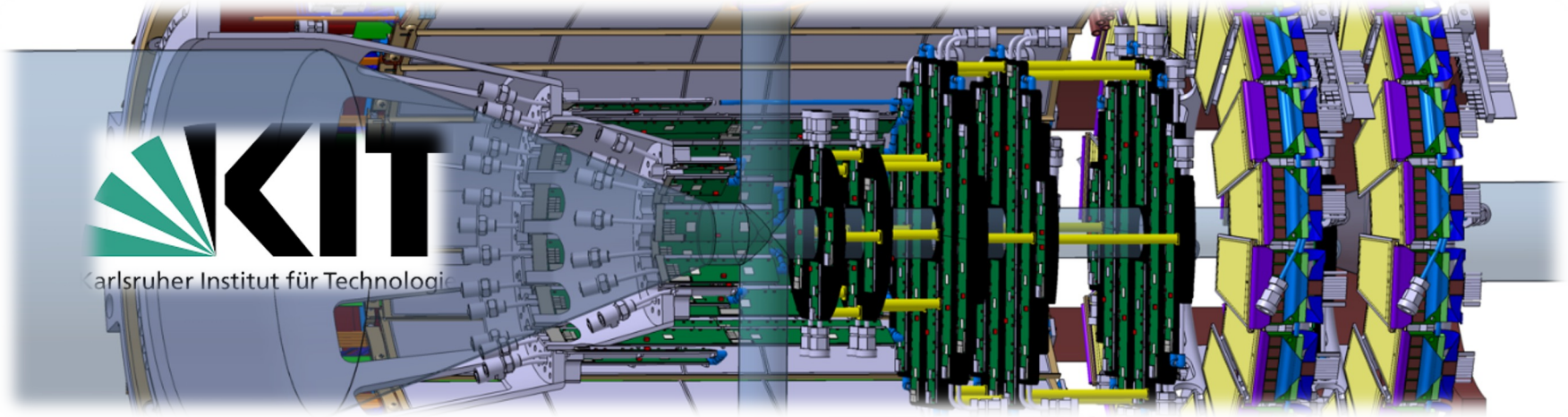


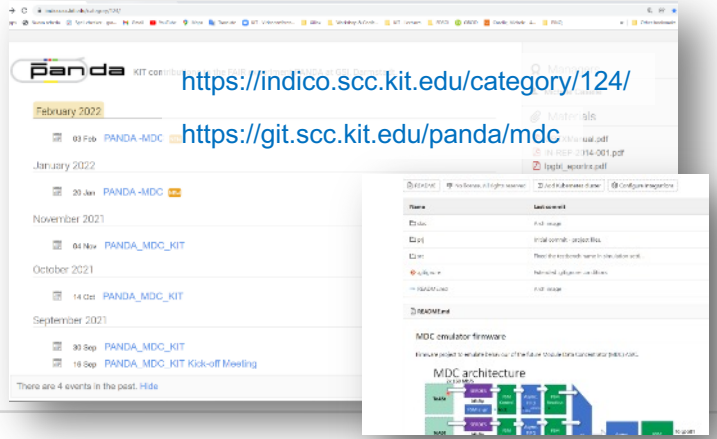
Outline

- Panda team at KIT
- MDC ASIC status
- HDL simulation environment
- MMB status
- Conclusions

Established PANDA group at KIT

Development of the MDC/MVD-DAQ and processing by AI

- KIT team:
  - Prof. Jürgen Becker (main professor),
  - M. Caselle (Coordinator),
  - K.- L. Unger, V. Sidorenko (ASIC / FPGA),
  - O. Manzhura (MMB card),
  - A. Kopmann, S. Chilingaryan, T. Dritschler, G Heine (DAQ & ML)

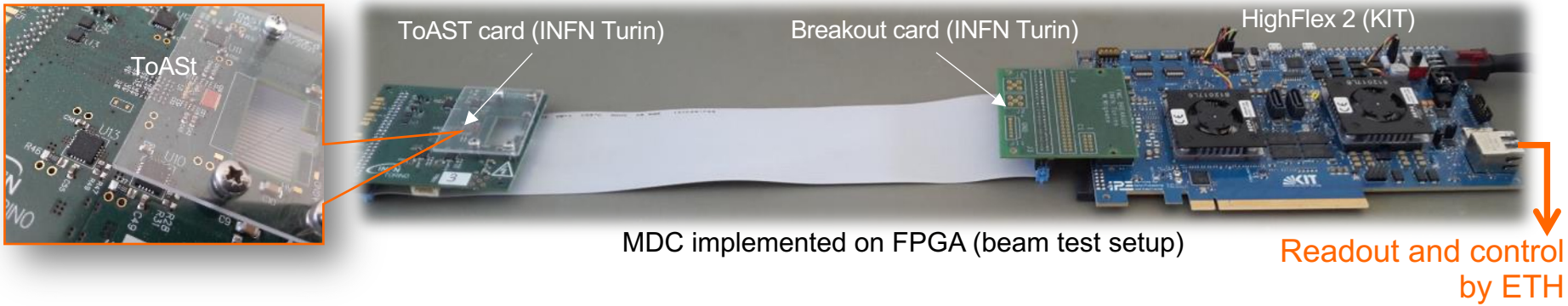


- KIT tasks are:
  - Development of the Module Data Concentrator (MDC)
  - Development of the MVD Multiplexer readout Board (MMB)
  - Beam test (2022/2023)
  - Track Reconstruction using Geometric Deep Learning in (STT) at PANDA Experiment
- Establish bi-weeks meetings

Module Data Concentrator ASIC

Radiation-tolerant ASIC local controller of the microstrip detector modules

- MDC ASICs will be develop in *UMC 110 nm CMOS*, same CMOS technology of the ToASt ASICs, both the ToASt and MDC will be manufactured in the same engineering runs
  - Step 1: MDC architecture will be implemented on FPGA (HighFlex readout card)
  - Step 2: MDC ASIC development



- **Milestone**: design the first prototype of “baby-MDC in UMC 110 nm, within 2022

Status of the Module Data Concentrator ASIC

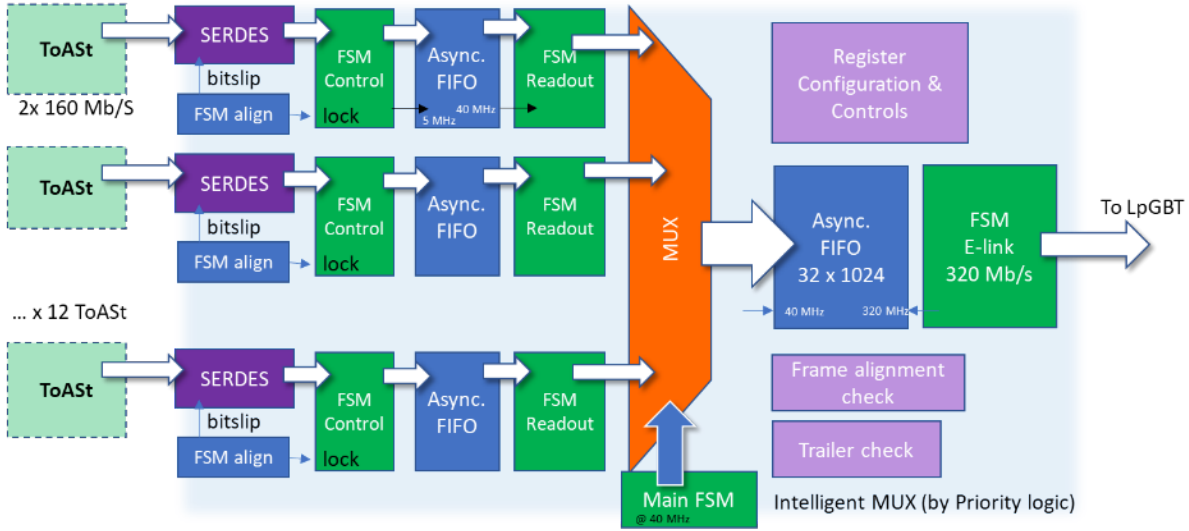
MDC architecture implemented on FPGA

(to be test with the ToASt)

Features:

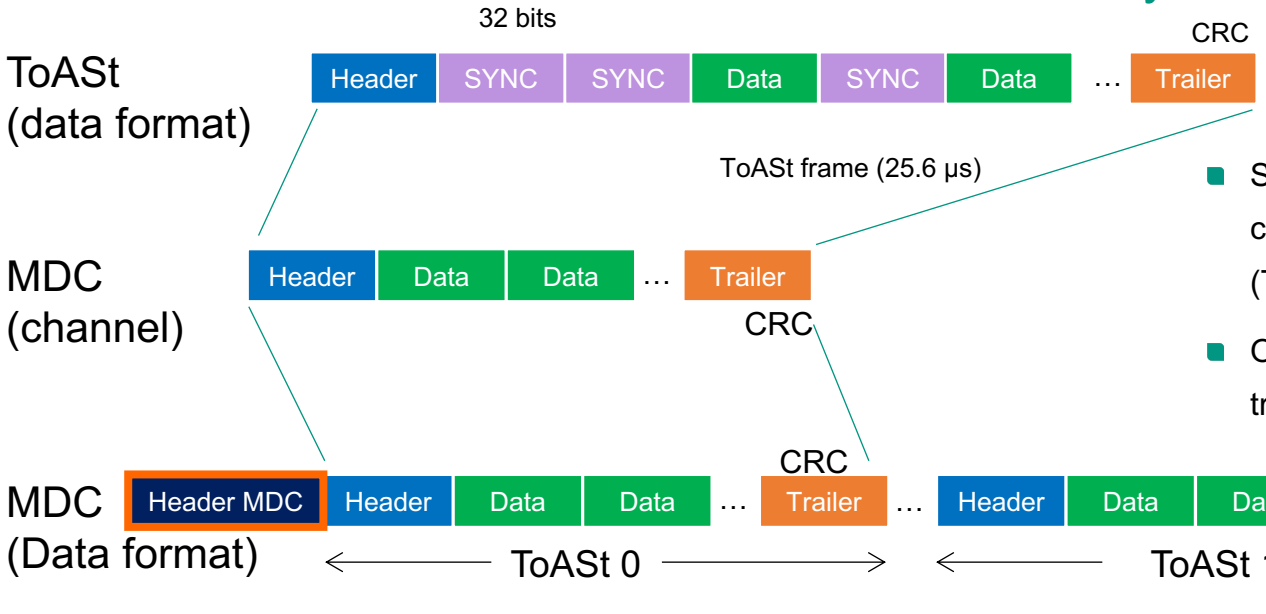
- Designed to readout up to 12 ToASt
- Dynamic configuration of the number of ToASt ASICs and high-speed links
- Inactive links are kept in low-power mode
- Intelligent multiplexing logic to balance the data occupancy from the ToASt within the detector module

MDC architecture implemented



Module Data Concentrator (Data Format)

MDC data format and real-time data consistency check

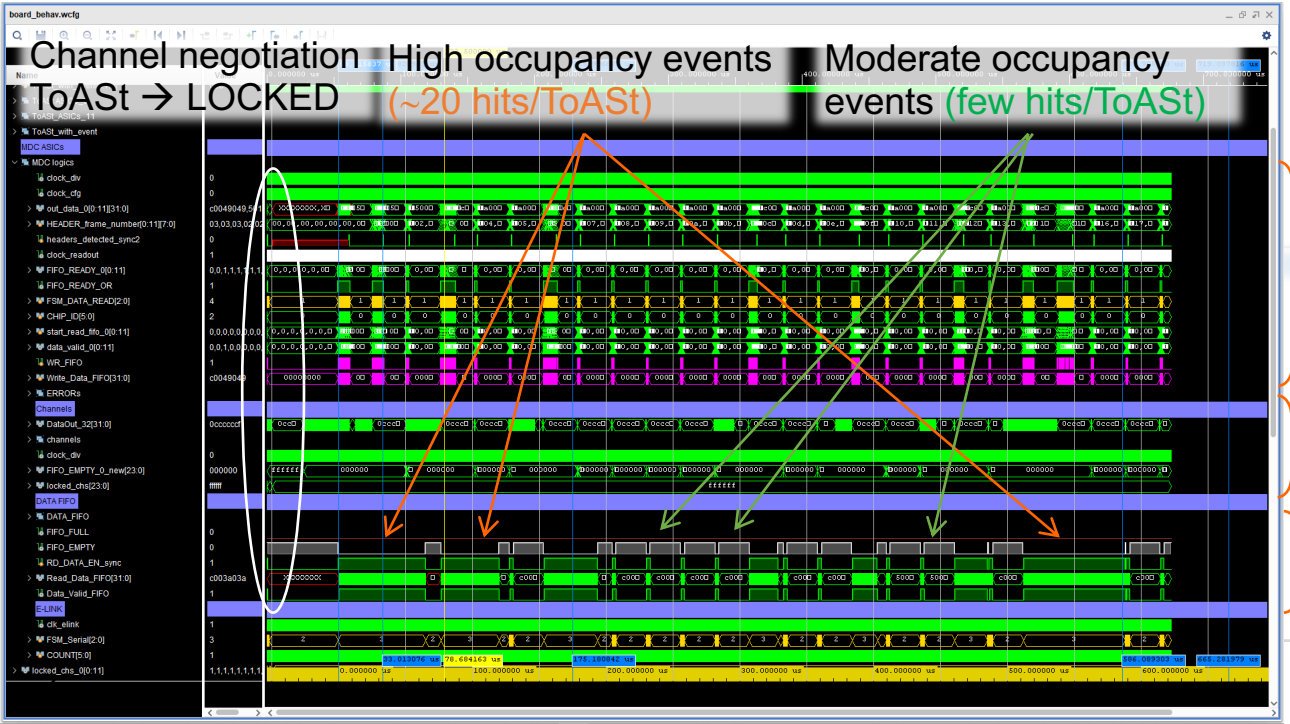


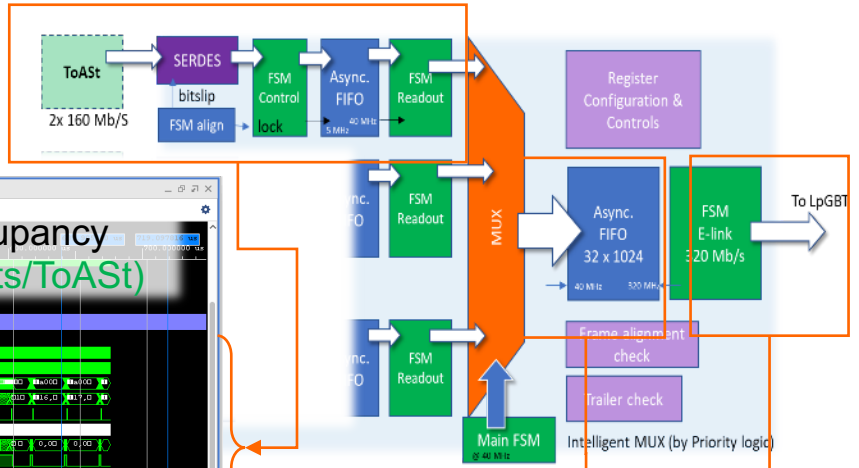
- SYNC packets → to check the communication between TX_ch channel (ToASt) and MDC
- Only HEADER, DATA and TRAILER transmitted

- **Frame number** alignment → performed on MDC and packed in the MDC Header
- CRC data check and correction → performed on the FPGA/ZYNQ (off-detector electronics)
- MDC **Header** and **Trailer** (32 bits) free to any further metadata to be sent to off-detector acquisition

Test bench environment

Preliminary test/performance and logic behaviour of the MDC

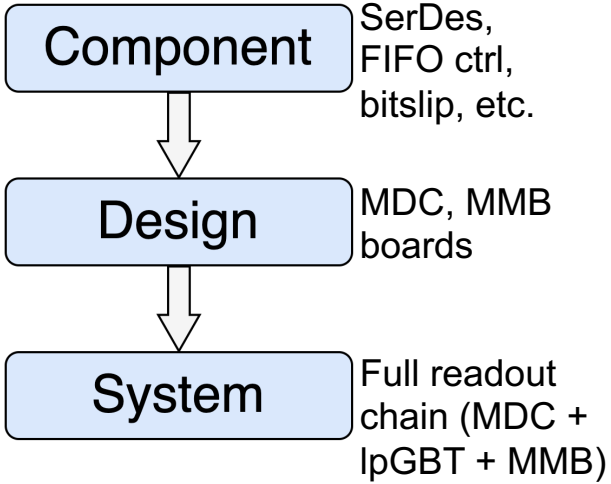




Event occupancy random distributed

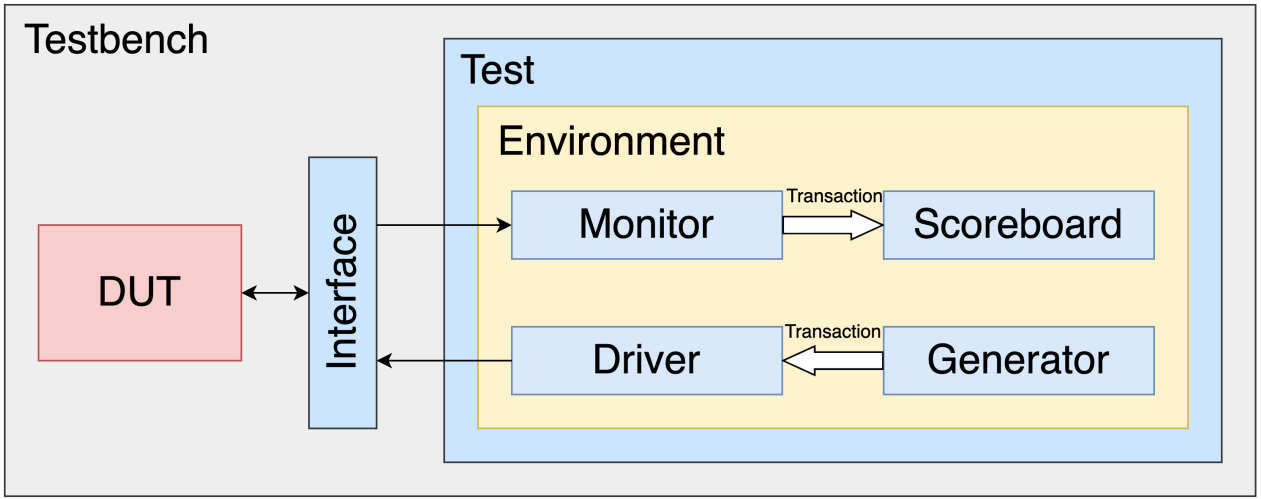
Structured simulation framework

Verification flow:

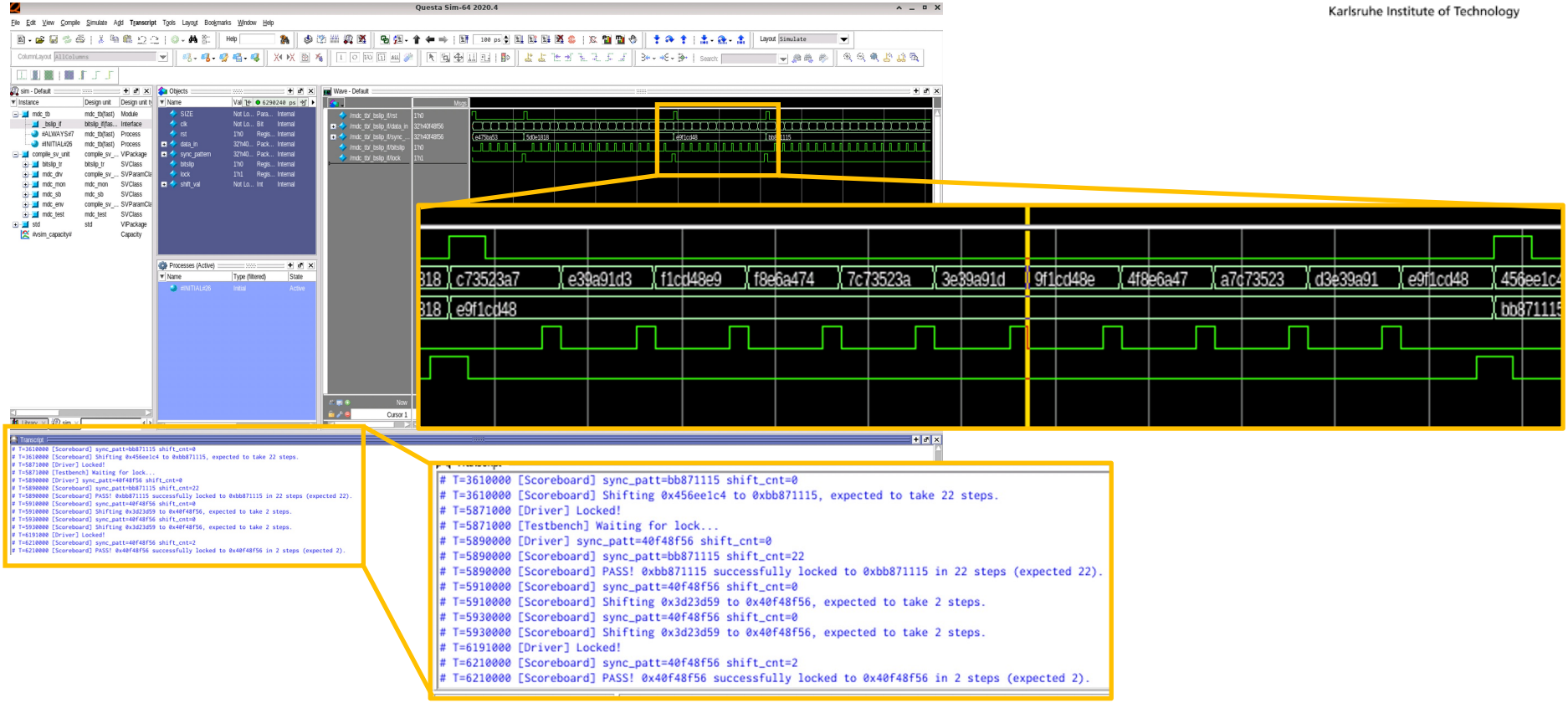


Tools:

- SystemVerilog
- QuestaSim (possibly VCS in future)



Structured simulation framework

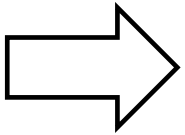


Structured simulation framework

Advantages of the QuestaSim + SystemVerilog approach:

- Scalable and reusable structure
- Complicated and randomized test scenarios
- Can be integrated into a Gitlab CI pipeline

But:
QuestaSim does not allow to see internal DUT signals in an SV testbench!

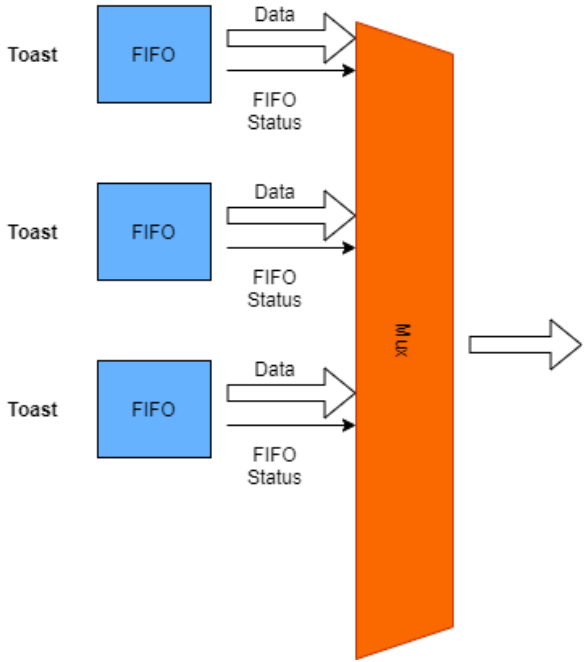


Good for the design- and system-level verification, not so useful for early stages of development (component level)

Multiplexer

Mux architecture

- Two possible Mux implementation
  - Round Robin
    - Fair Scheduling
    - Problem handling uneven link load
  - Priority
    - Fullest FIFO first
    - Problem with low data rate links
  - Both solution need to be tested

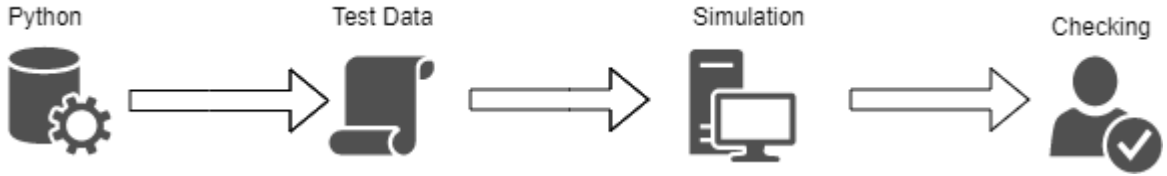


Component-level testbench evolution

Next test steps of the MDC

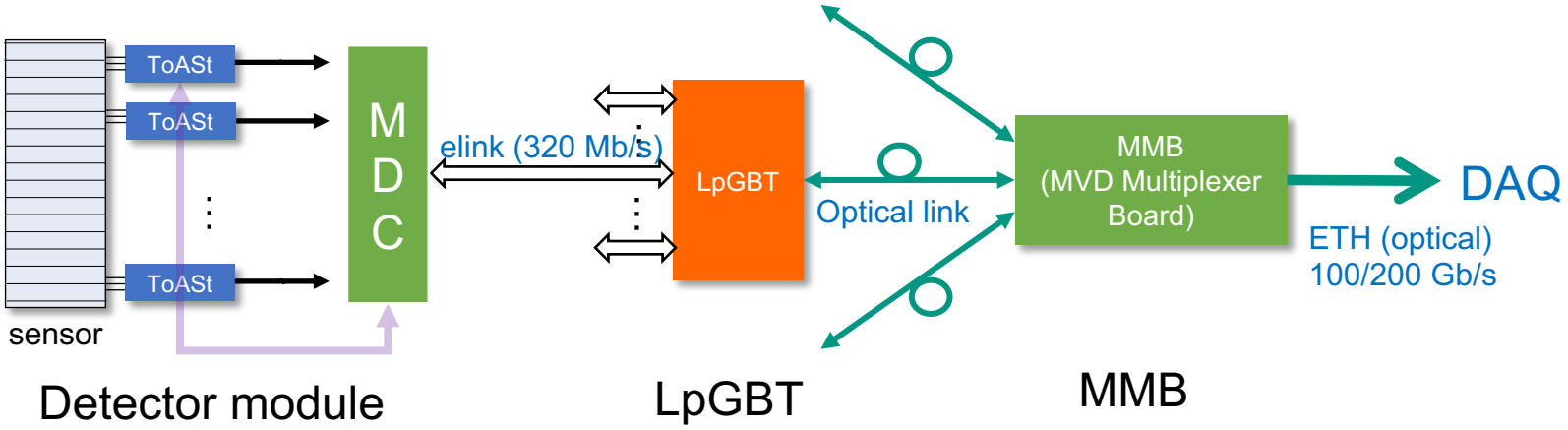
- Statistics is needed for the final design decision
  - Which Mux Scheduling algorithms
  - Length of the FIFOs
  - …
- Automated Data generation needed

Tools:
- SystemVerilog
- Python
- Vivado Simulator



Status of the MMB - AMC Readout card

Very-flexible, heterogenous and high-performance back-end



MVD Multiplexer Board features:

- Up to 60 optical links from/to detectors (GBTs)
- Up to 100 Gb/s ETH to DAQ (upstream)
- Additional spares transceivers for both LpGBT and DAQ optical links

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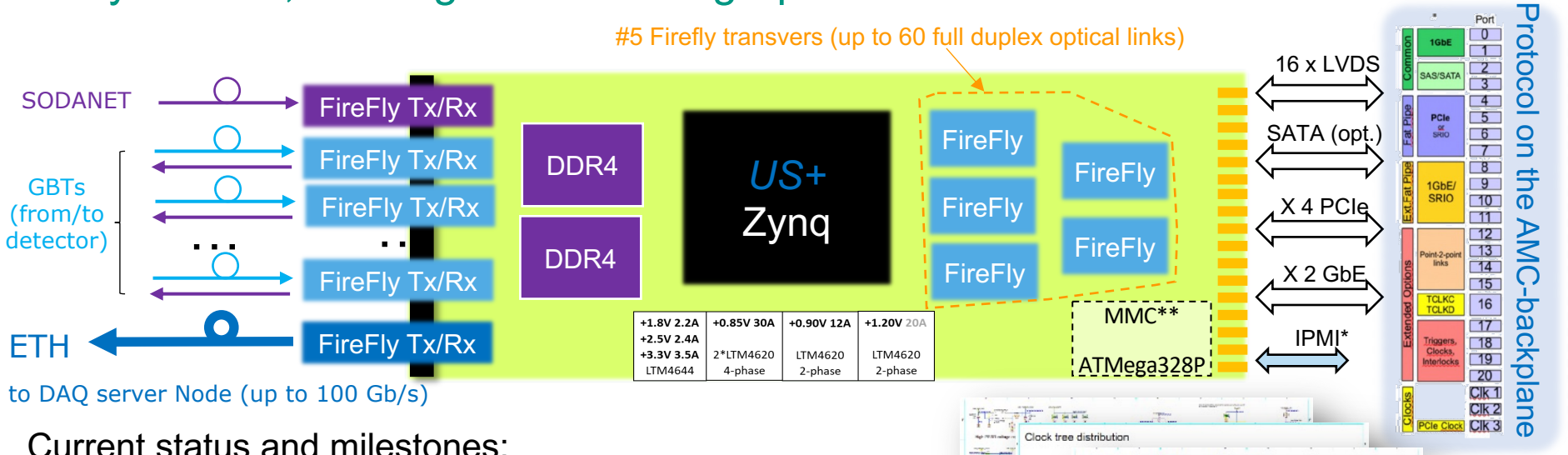
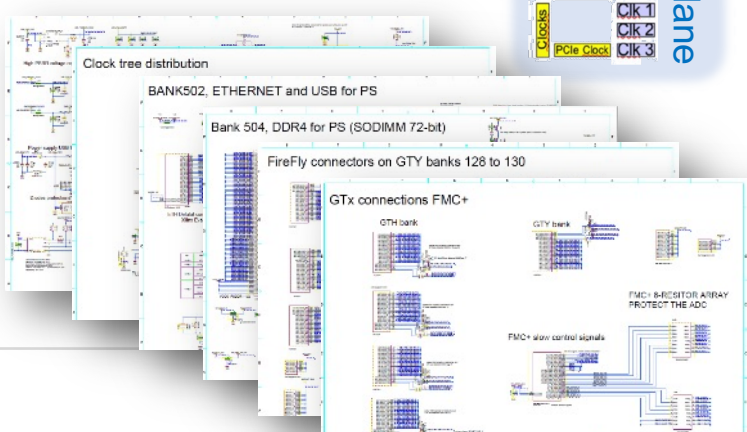


Current status and milestones:

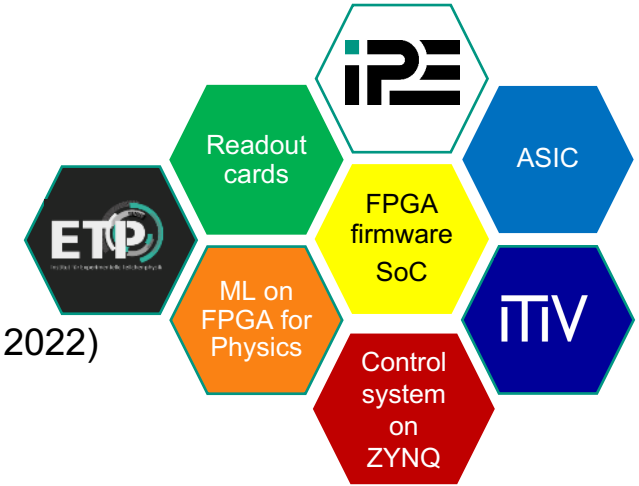
- 80 % of schematic completed (ZYNQ, UDIMM and Firefly)
- 50 % of the FPGA firmware completed

➔ **Milestone**: first MMB readout card, within 2022



Conclusions

- Established PANDA group at KIT
  - Development of the MDC (ASIC)
  - Development of the MMB AMC card
  - SoC integration (SODANET, DQM, data processing on Zynq)
- Important milestones !!!:
  - Development of the first MDC in UMC 110nm (before the end of 2022)
  - Validation of the digital behaviour with one/more ToASt
  - Preparation to the beam test 2022/23



- We rely in the interface/synergies we other teams/institutions within PANDA
  - Close collaboration with UPSALLA and Jagiellonian University in common development of the firmware of PANDA data concentrator AMC card
  - Weekly meeting with Julich (Tobias Stockmanns team), Track Reconstruction using Geometric Deep Learning on FPGA/Versal

Thank you!