

# Development of TRBv3 & *FIRST* Results of *FIRST* Test Beam

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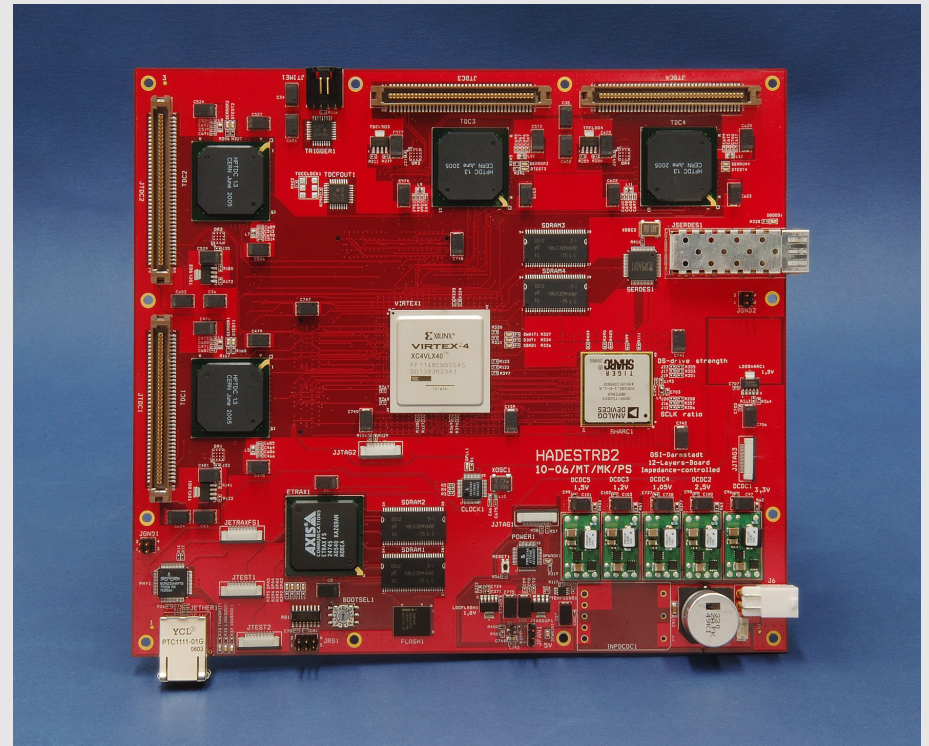
*XL. PANDA Collaboration Meeting  
5 March 2012, GSI Darmstadt, Germany*

# Outline

- Motivation
- TDC in FPGA
- Laboratory test results
- DIRC Prototype test beam setup and first results
- Conclusion & Outlook

# Motivation

- to have high resolution, high channel density, low cost
- to replace ASIC-HPTDCs from CERN
- to provide solutions for different requirements e.g. higher resolution, zero dead time
- to provide different measurement capabilities, e.g. ToF, Charge
- to use in different detectors for different experiments

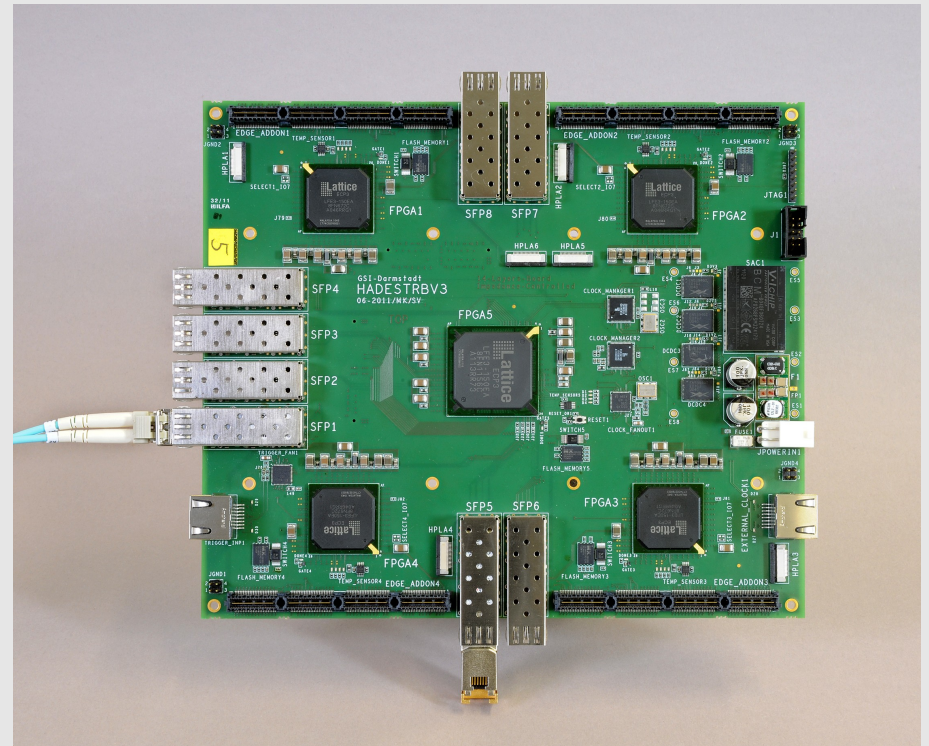


TDC Readout Board v2

Photo by Gaby Otto, GSI Darmstadt, 22.12.2006.

# Motivation

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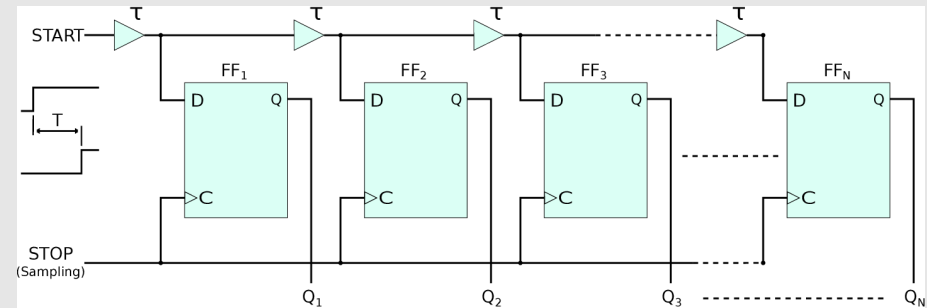
TDC Readout Board v3

Photo by Gaby Otto, GSI Darmstadt, 22.12.2006.

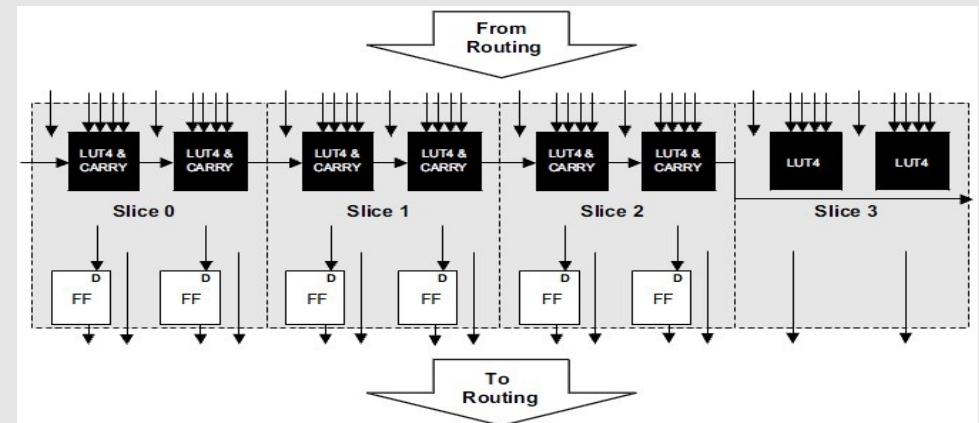
# TDC in FPGA

## Tapped Delay Line Method

- Tapped delay line is used for fine time measurements – suits well with the FPGA architecture
- Delay elements are realised by LUTs
- Fast carry chain structure forms the delay line
- Registers are used to sample the delay line



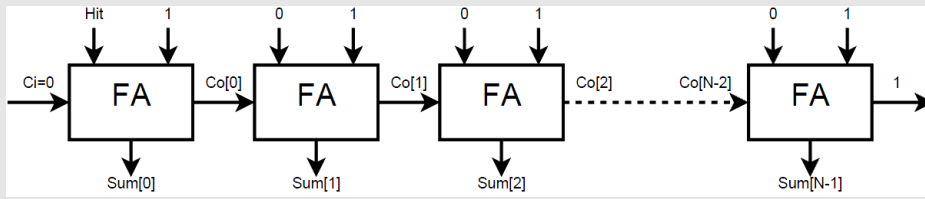
Tapped Delay Line Method [1]



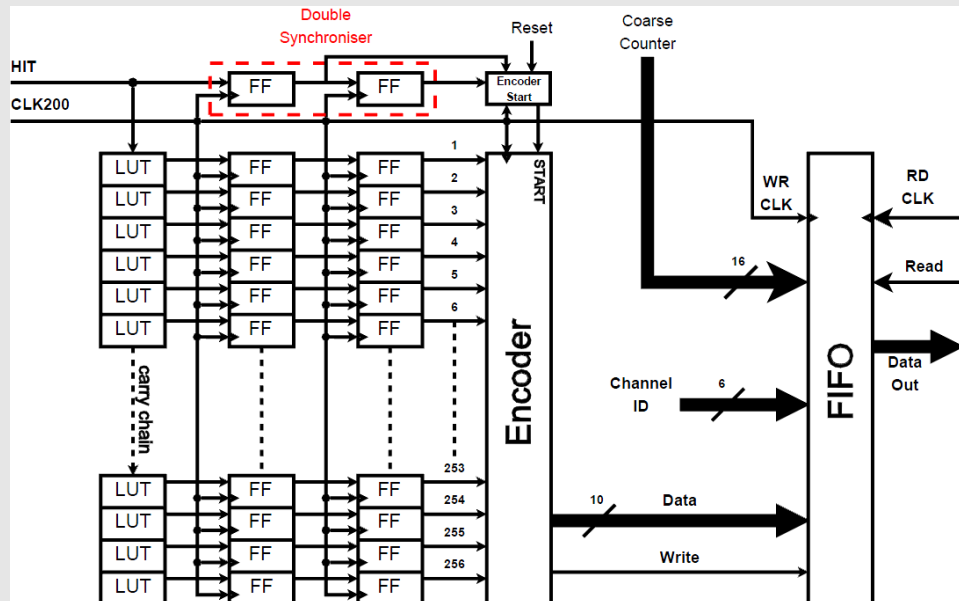
PFU Diagramm [2]

# TDC in FPGA

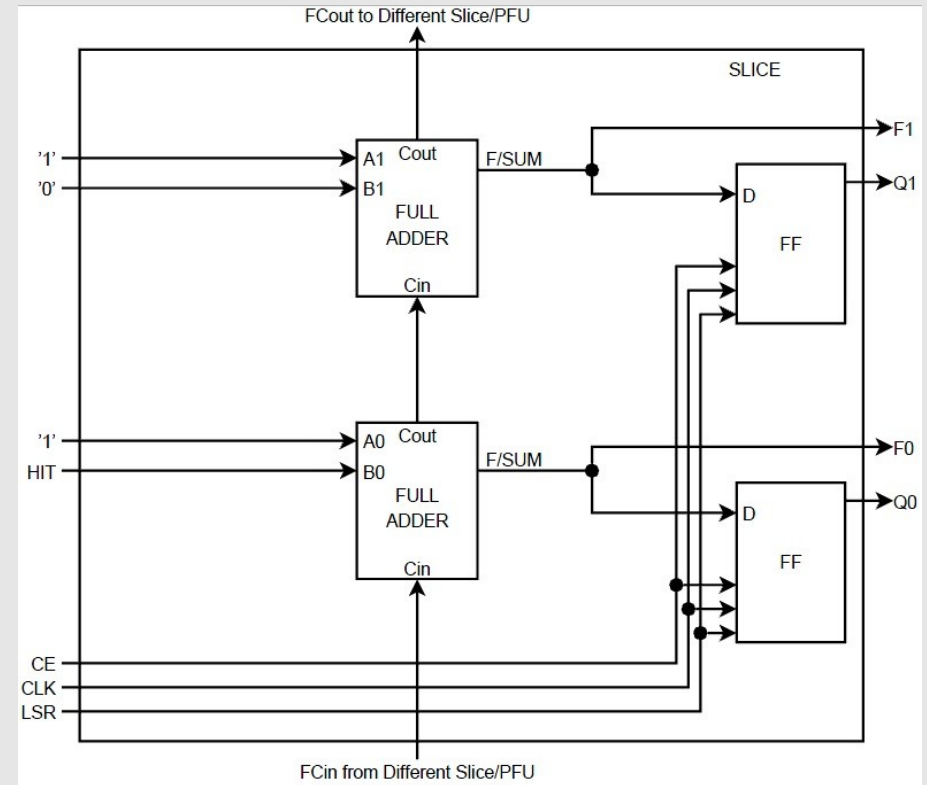
## Architecture of the TDC



Delay line is realised with Full Adders [3]



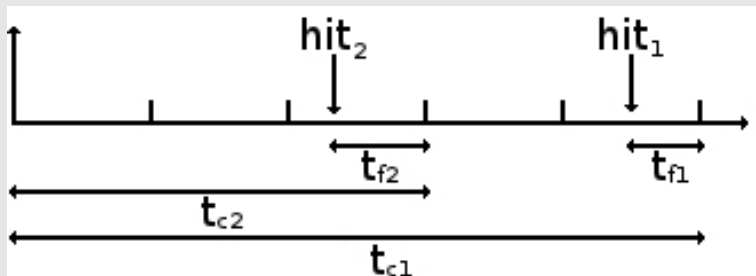
TDC Architecture



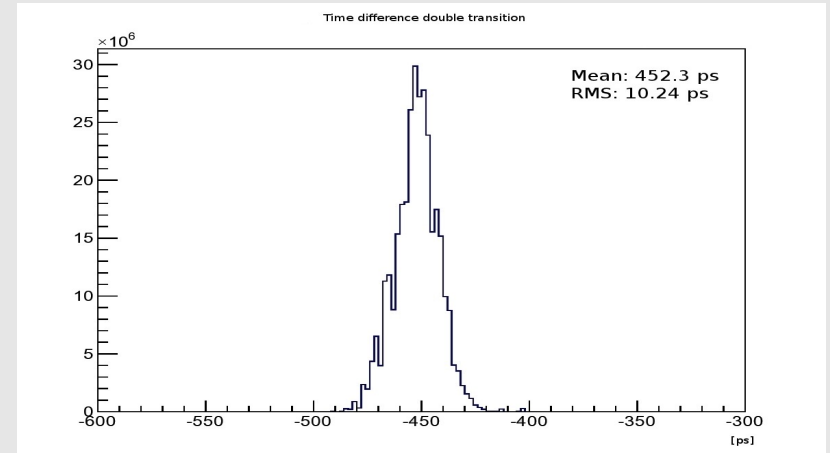
Slice diagram with LUTs programmed as Full Adders

# Laboratory Test Results

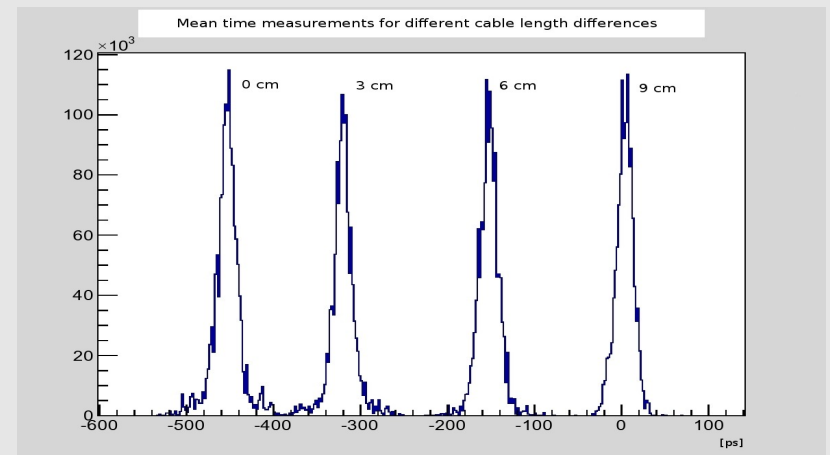
- Time difference measured between 2 channels
- $\Delta t = (t_{\text{coarse1}} - t_{\text{coarse2}}) - (t_{\text{fine1}} - t_{\text{fine2}})$
- RMS measured: 10.34 ps against the same clock
- Resolution:  $10.34 \text{ ps} / \sqrt{2} = 7.3 \text{ ps RMS}$



Time difference between two measurements



Time resolution test

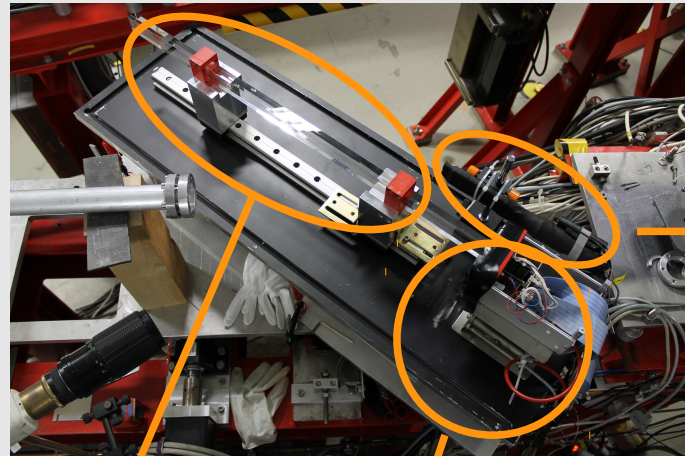


Mean measurement test



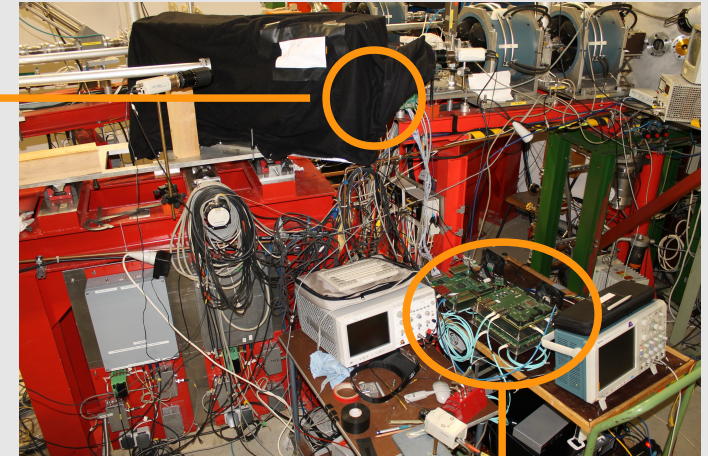
# DIRC Prototype Test Beam @ MAMI

25 February 2012

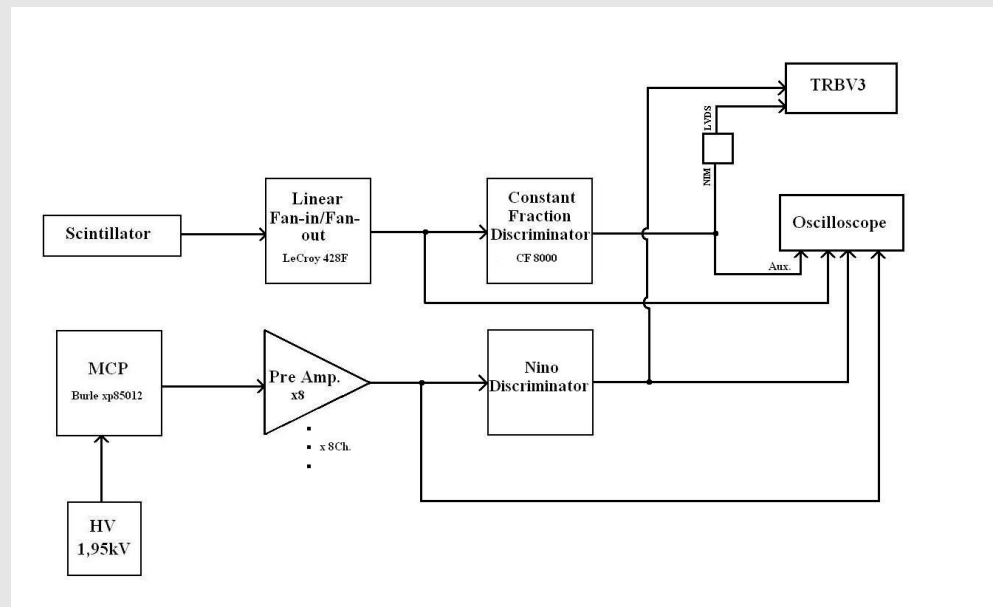


Discriminator

Scintillator



Electron beam  
Beam energy: 855 MeV  
Beam spread:  $0,3^\circ$

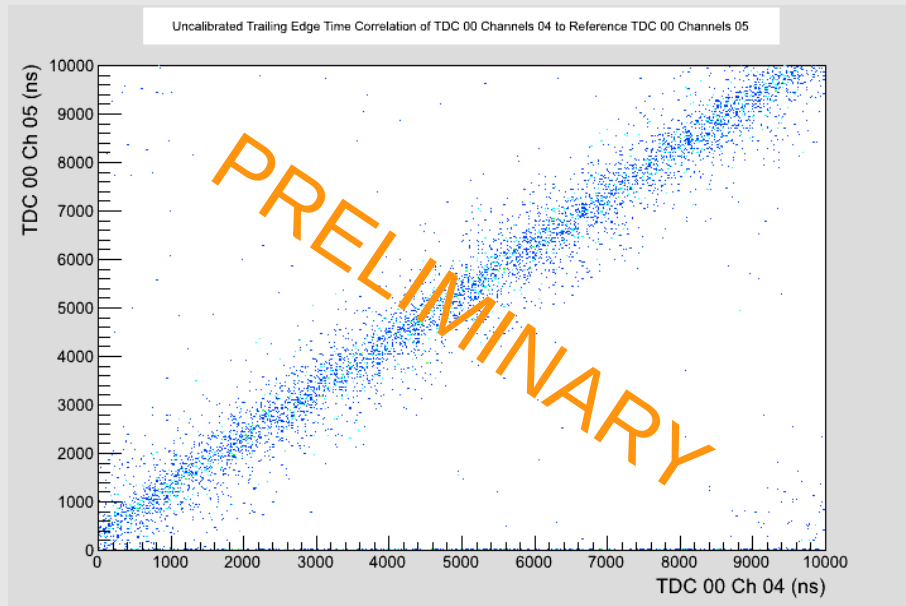


TRB3  
&  
Readout  
Electronics  
  
Triggerless!

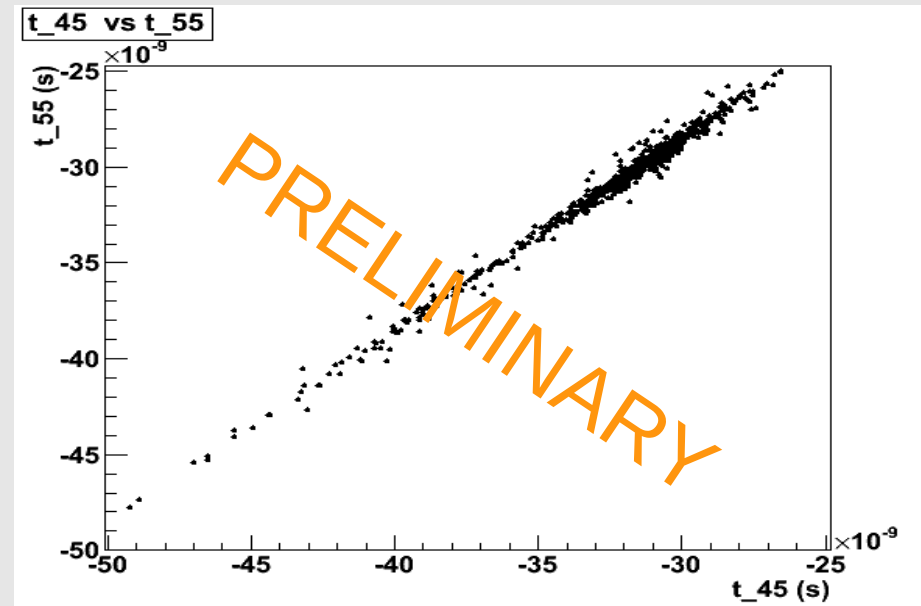


# FIRST Results from the FIRST Beam

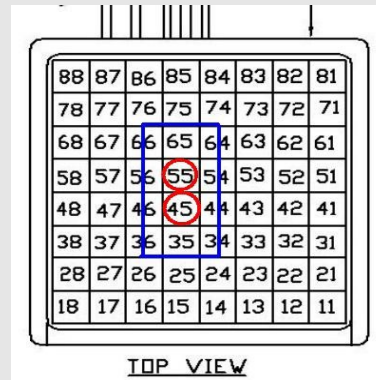
## Time Correlation between pixel 45 & 55



TDC result

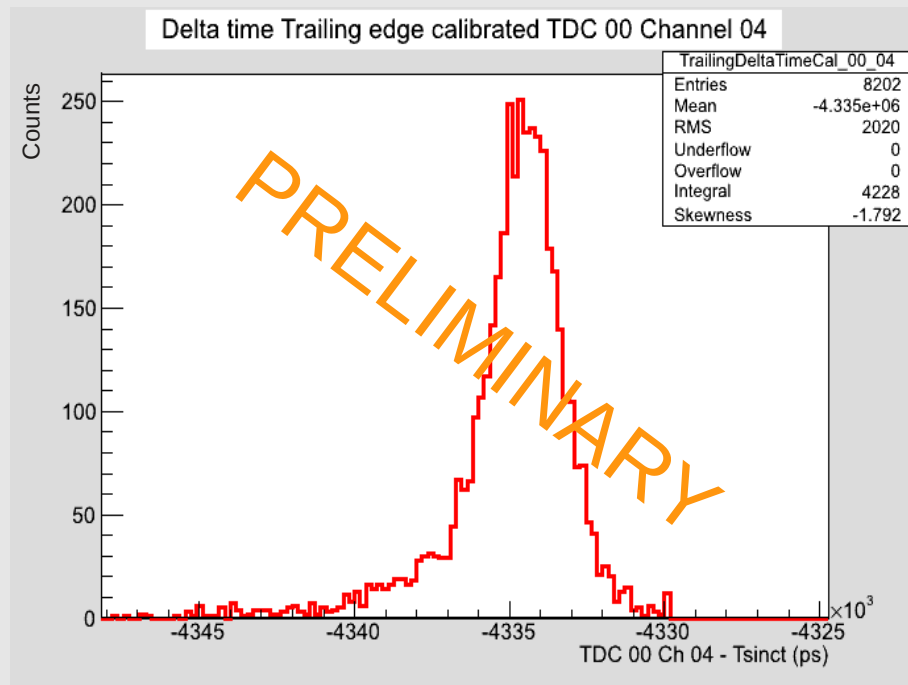


Oscilloscope result

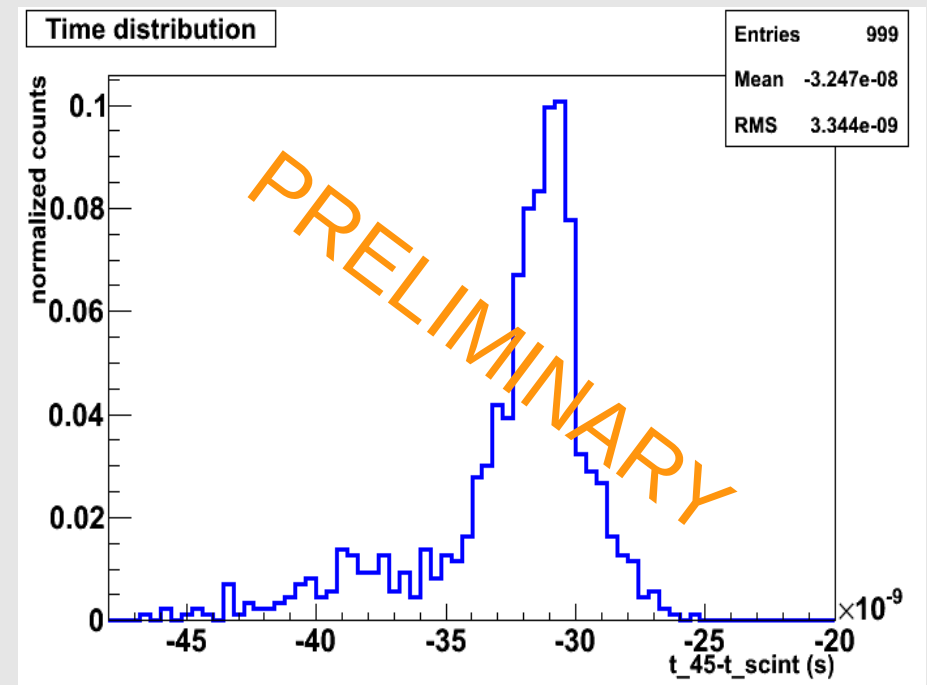


# FIRST Results from the FIRST Beam

Measured time difference between the pixel 45 and scintillator



TDC result

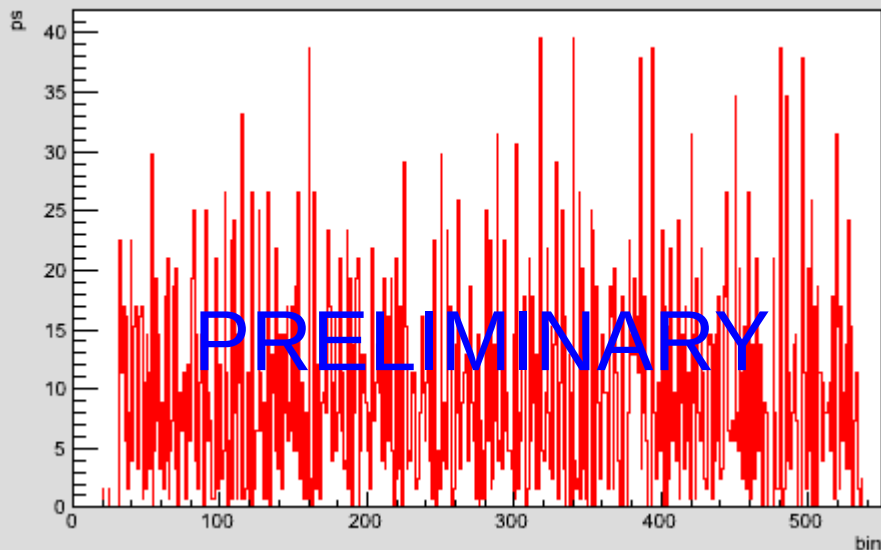


Oscilloscope result

# *FIRST* Results from the *FIRST* Beam

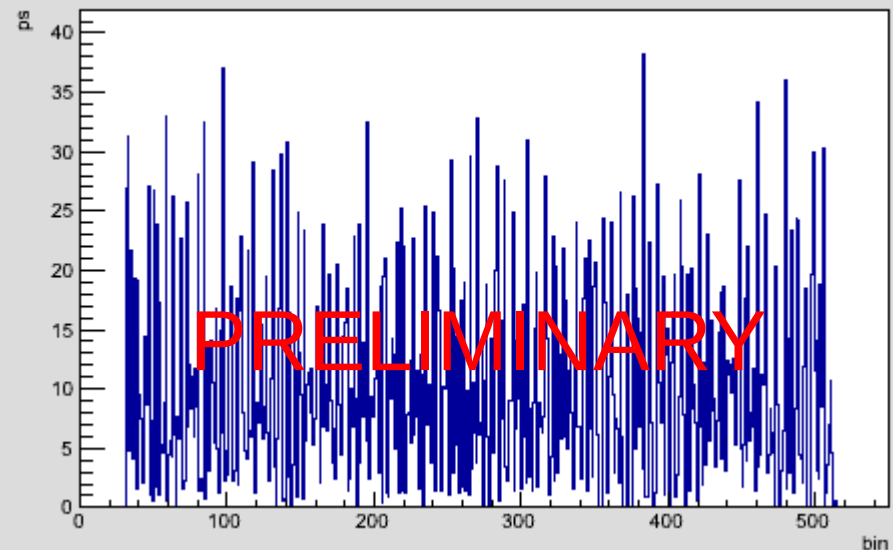
Bin width comparison of Beam results and Lab results

Binwidth Histogram of TDC 00 Channel 04



Beam result

Binwidth Histogram of TDC 03 Channel 04



Lab result

# Conclusion & Outlook

- Multi-Purpose TDC in FPGA chip has been developed
- The first board has been tested with real beam for the **FIRST** time!
- For test purposes 6 channels were used
- Time data was taken successfully with the electronics prototype
- Time distribution and correlation information of the pixels are consistent with the oscilloscope
- For more tests the TDC will be tested in the next Hades beam time during April and DIRC prototype beam time in May
- More time information will be collected (rising and falling edges – ToT – of the signals)
- More channels will be implemented

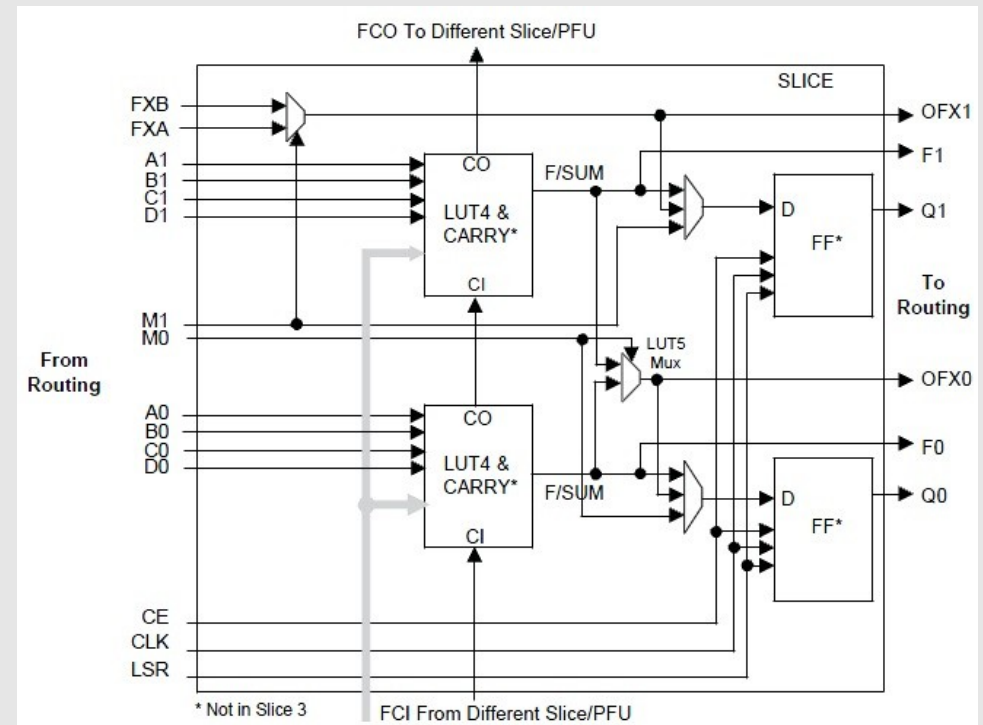
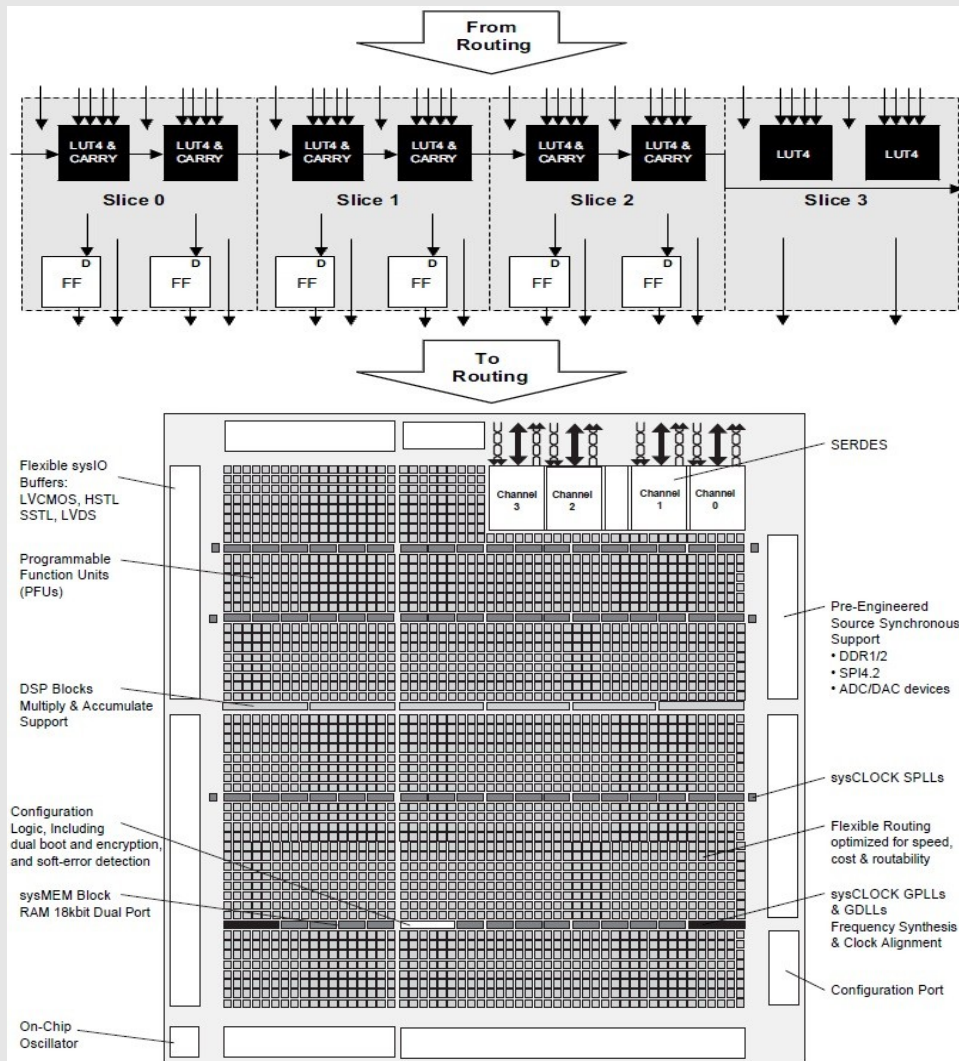
# References

- [1] J. Kalisz, Review of methods for time interval measurements with picosecond resolution, Metrologia, 2004.
- [2] LatticeECP2/M Family Handbook, HB1003, Version 04.3, March 2009.
- [3] J. Song et al., A high-resolution time-to-digital converter implemented in field-programmable-gate-arrays, IEEE TRANSACTIONS ON NUCLEAR SCIENCE, 2006.



# Backup Slides

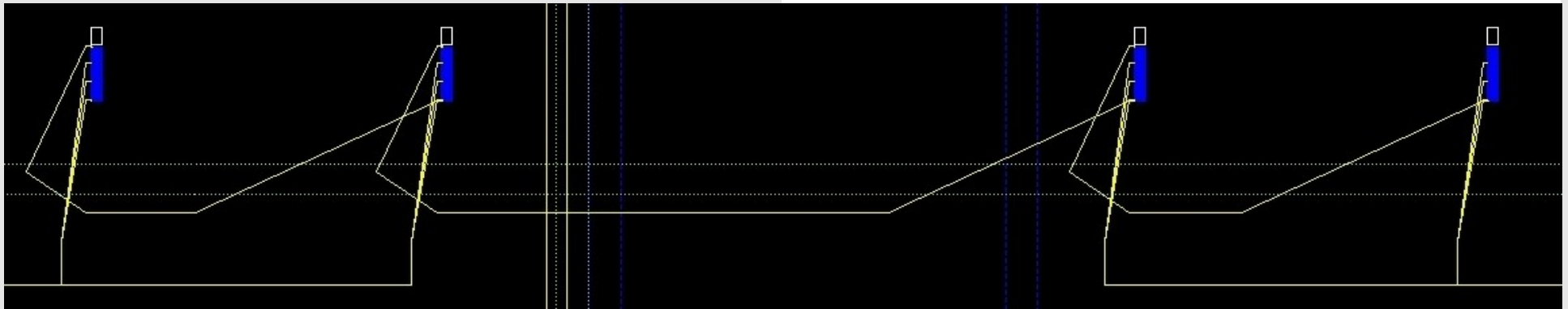
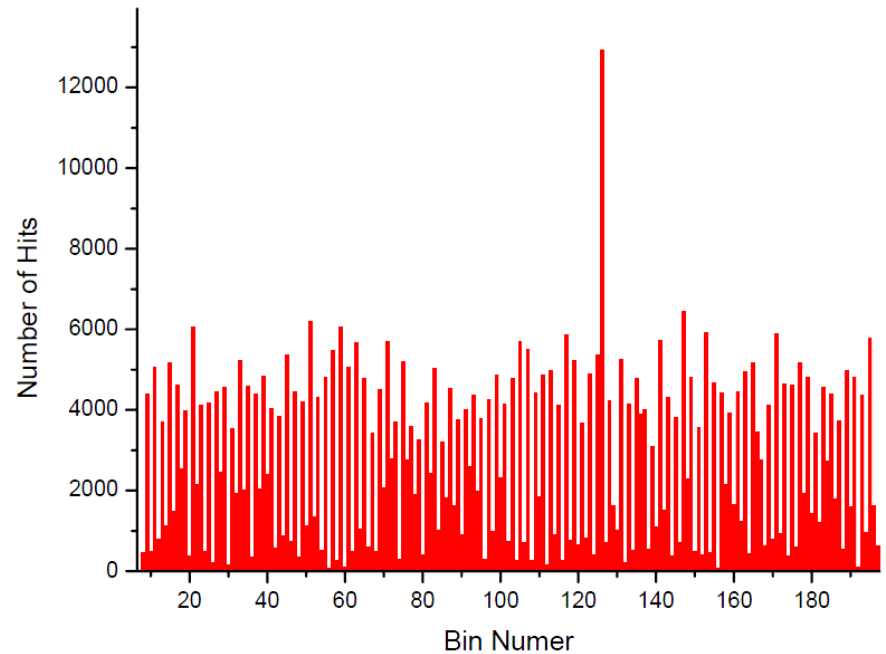
# Architecture of Time-to-Digital Converter



Lattice ECP2M FPGA Slice Diagram, PFU Diagram and Floorplan

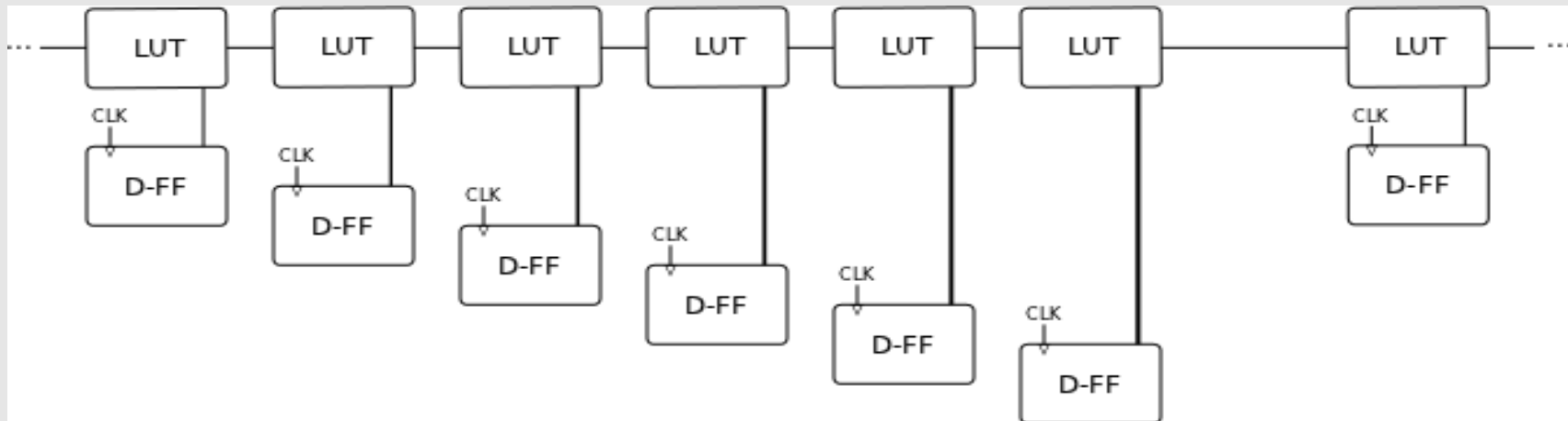
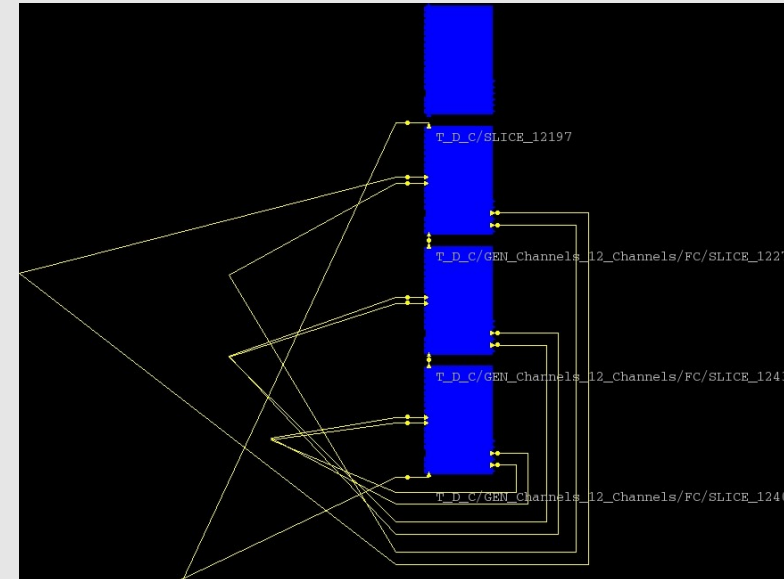
# Architectural Effects of FPGA

- Effect of primary clock line in the FPGA
- Effect of longer inter-slice routings
- Effect of PFU architecture

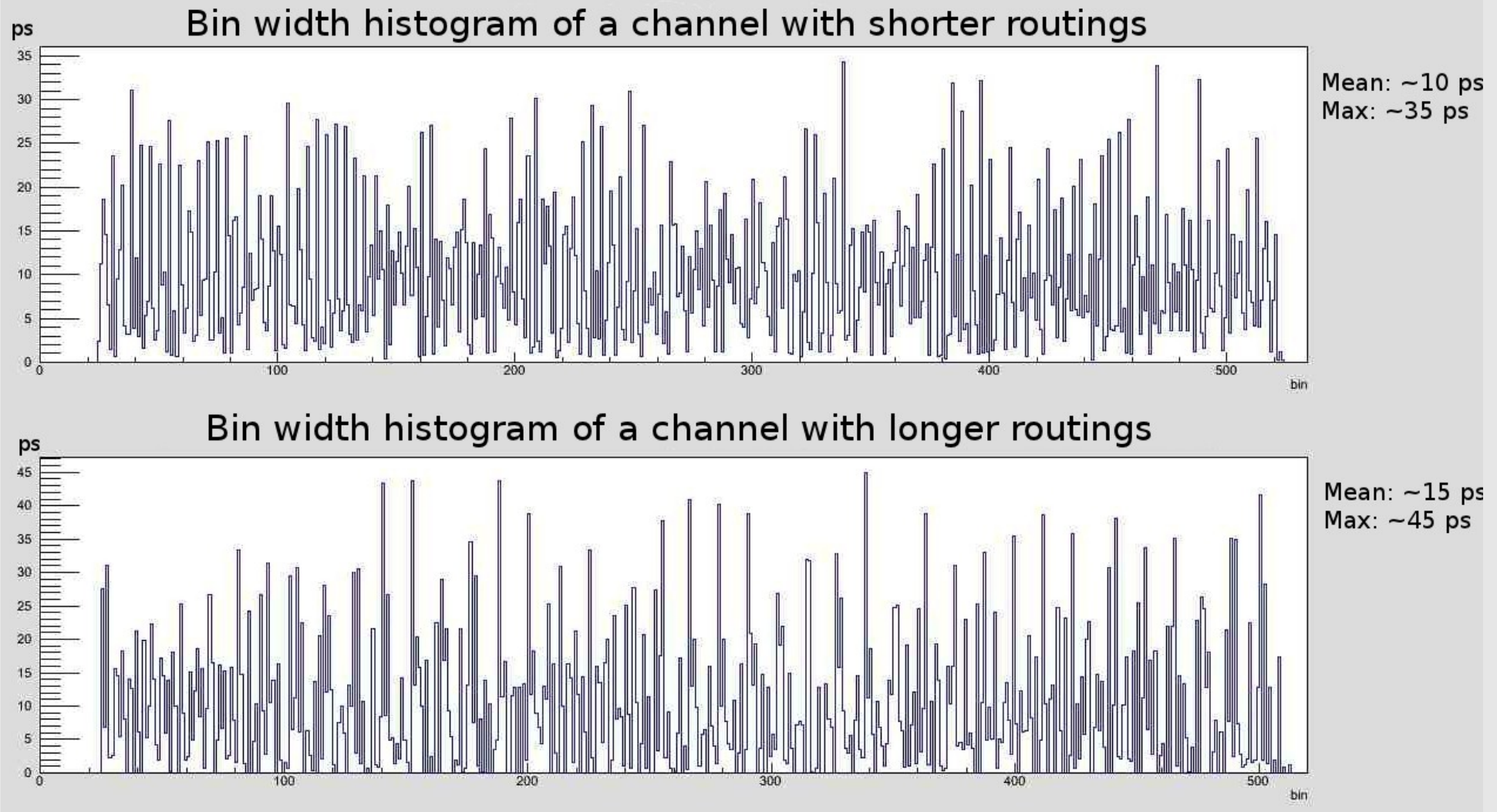


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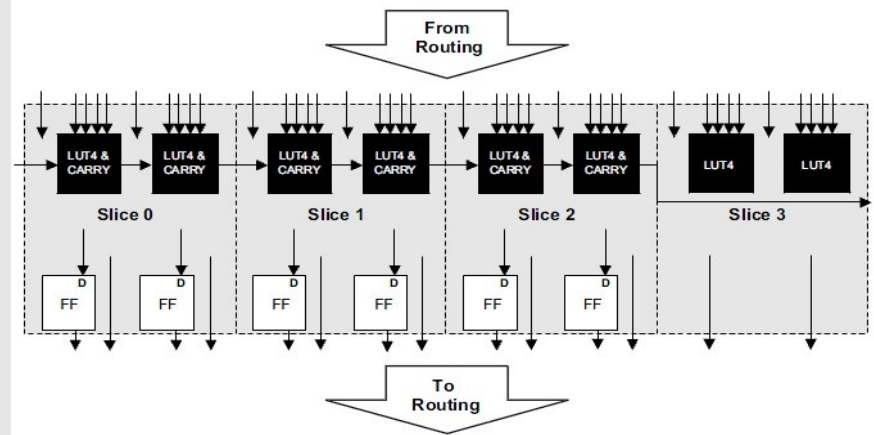
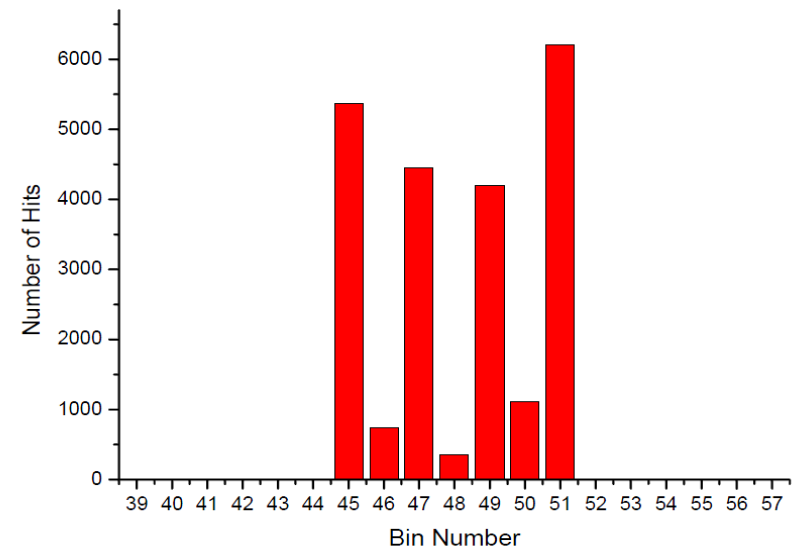
# Architectural Effects of FPGA





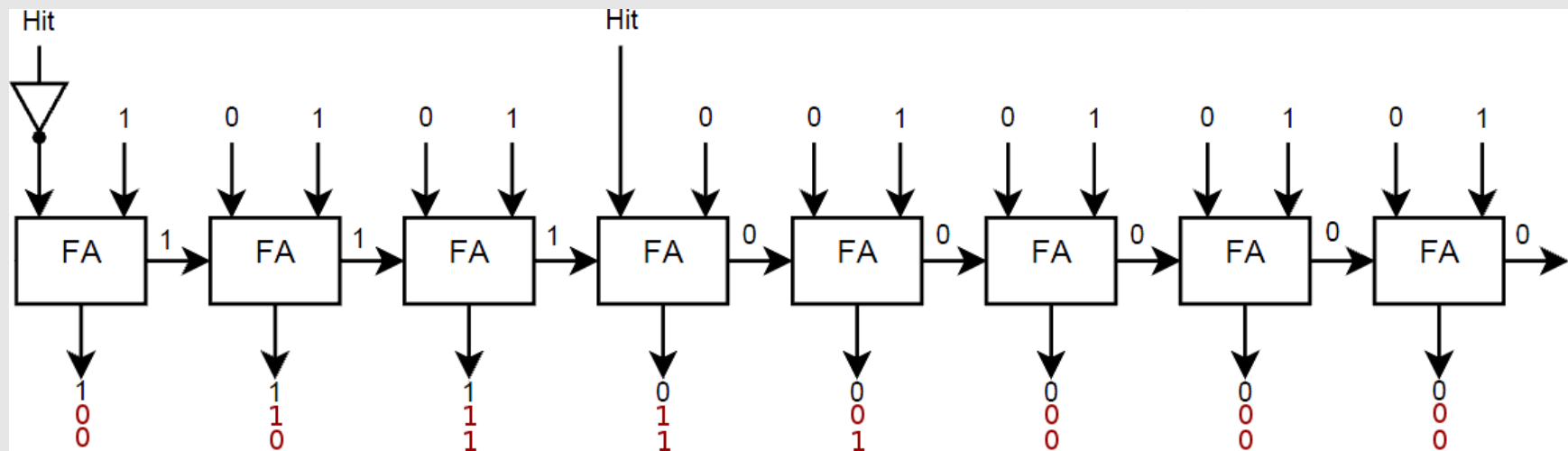
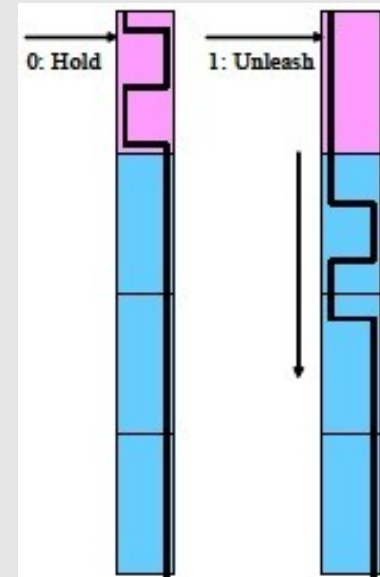
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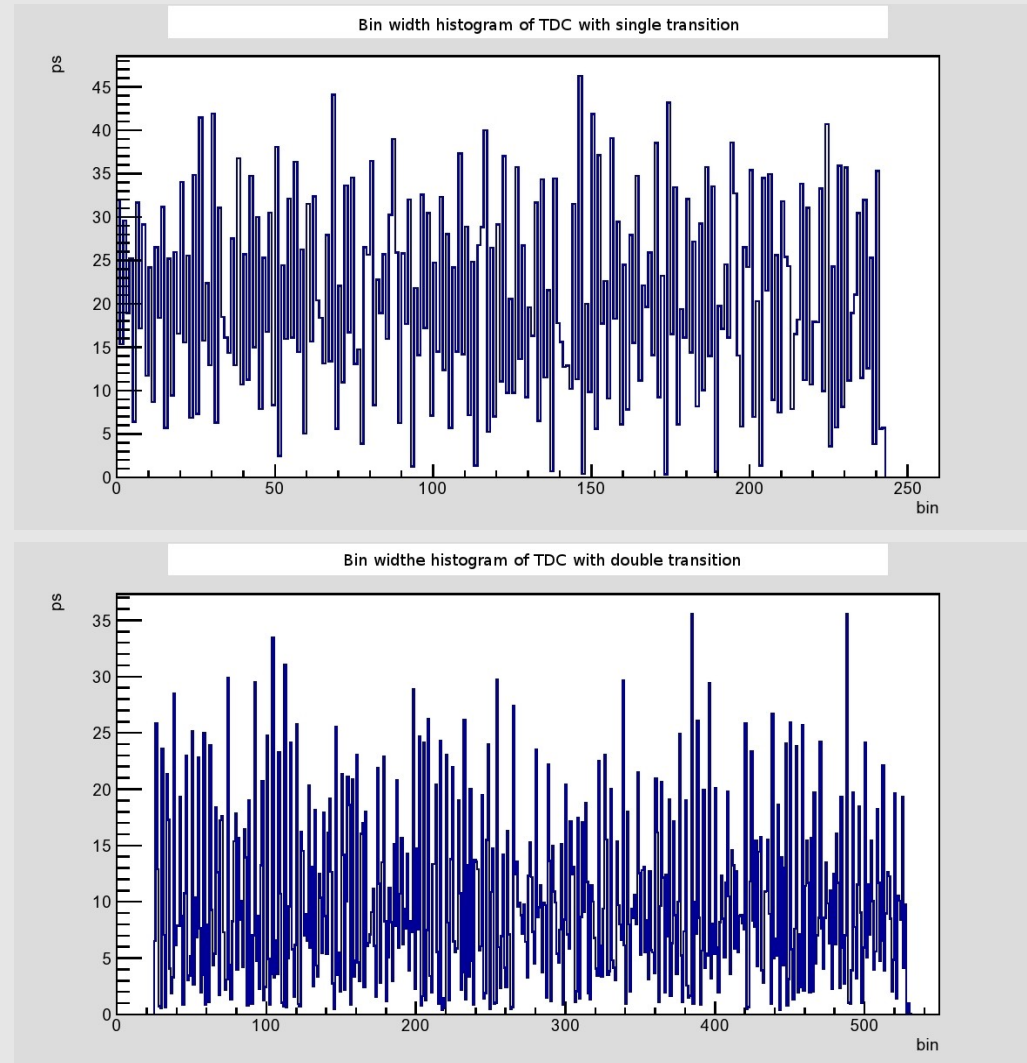
# Wave Union Launcher

- More than one delay line is necessary in order to reduce the effect of wide bins
- Wave union launcher is implemented
- Bin widths & non-linearities are reduced



# Wave Union Launcher

- More virtual bins
- Narrower bins
- Homogeneous bin distribution

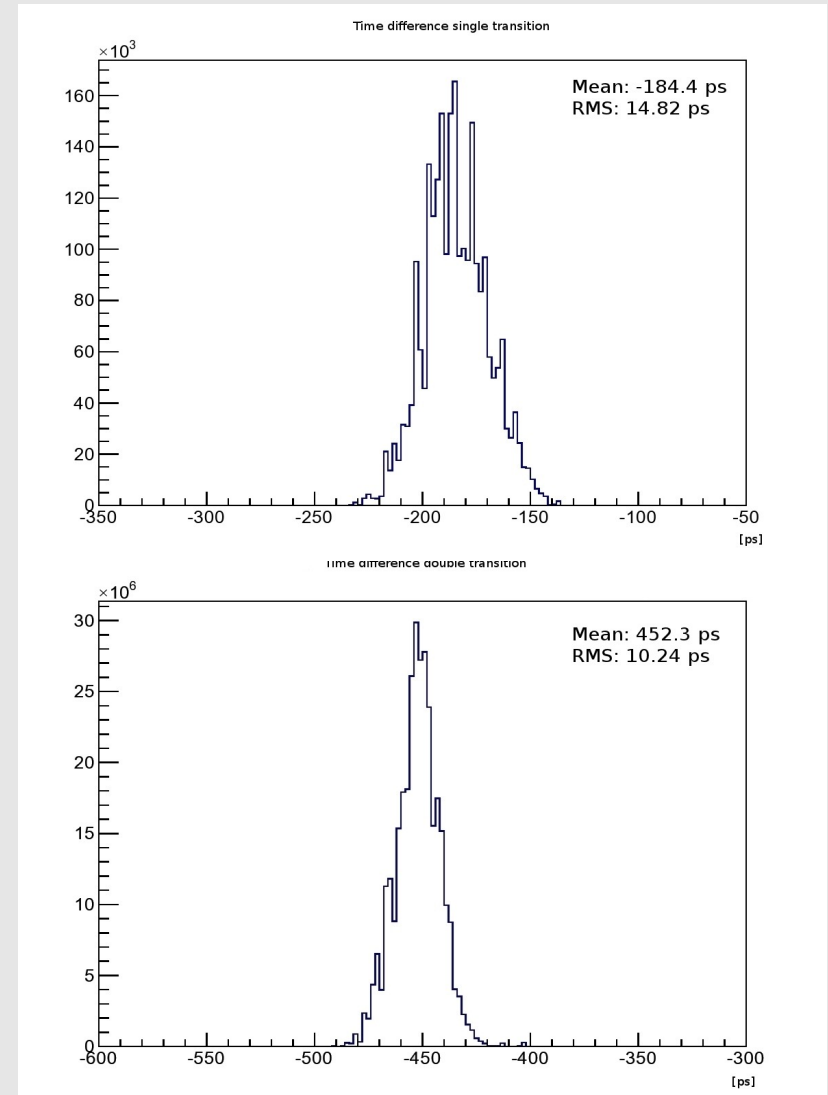
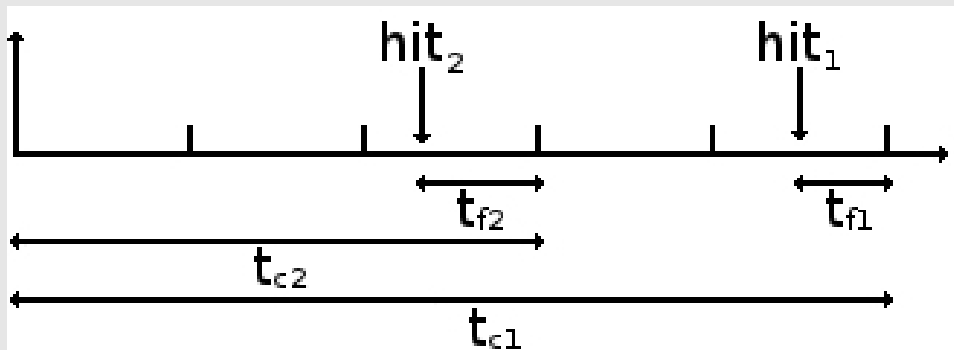


Bins: ~240  
Mean: ~20 ps  
Max: ~45 ps

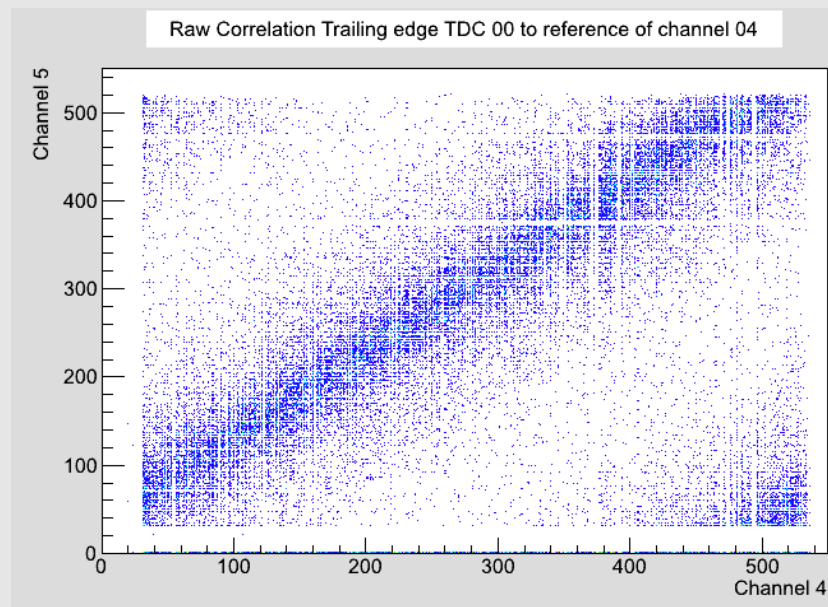
Bins: ~520  
Mean: ~10 ps  
Max: ~35 ps

# Statistical Error & Resolution

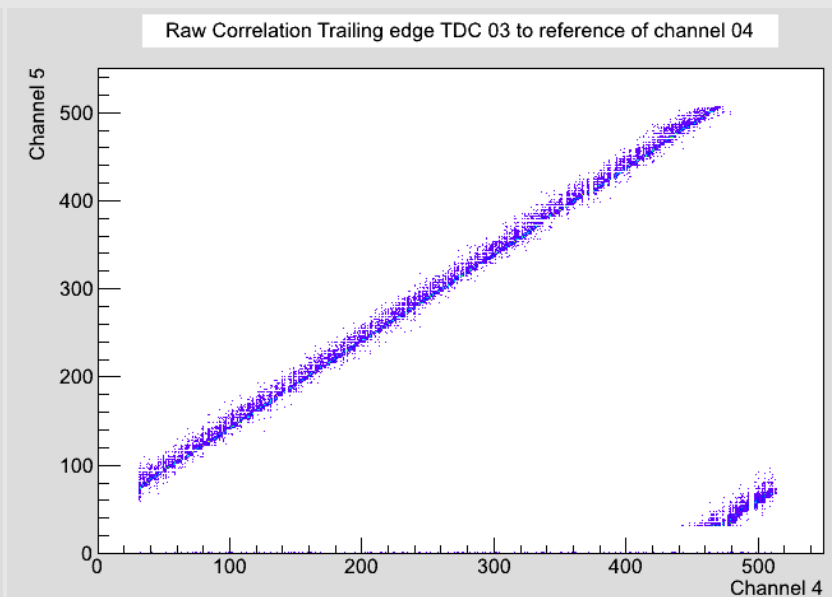
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- RMS measured: 10.34 ps  
against same clock
- Resolution:  $10.34 \text{ ps} / \sqrt{2} = 7.3 \text{ ps}$
- Effect of 2 transitions:  
 $14.82 \text{ ps} / 10.34 \text{ ps} = 1.43 \text{ factor}$



# Fine Time Correlation



Beam result



Lab result