EMC-Readout Development

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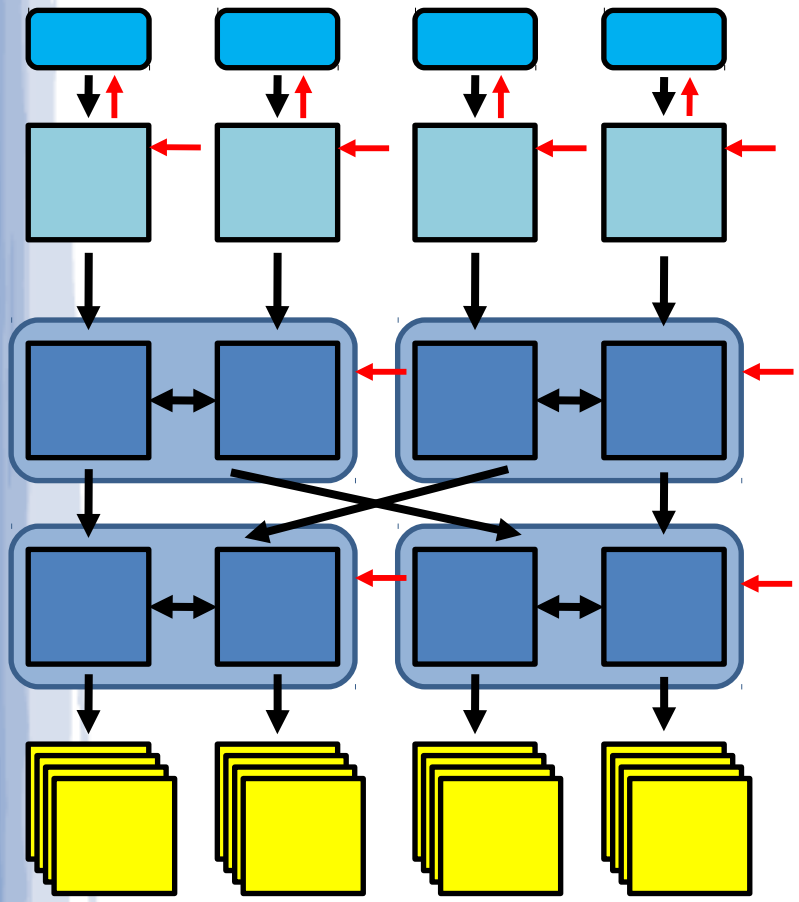
for the PANDA collaboration

PANDA Readout

using **Data links** (←) and Time distribution (←) "SODA"

[I. Konorov et al., NSS/MIC Conf. Rec., 2009 IEEE, DOI 10.1109/NSSMIC.2009.5402172]



Detector Front-ends — Hit detection, feature-extraction

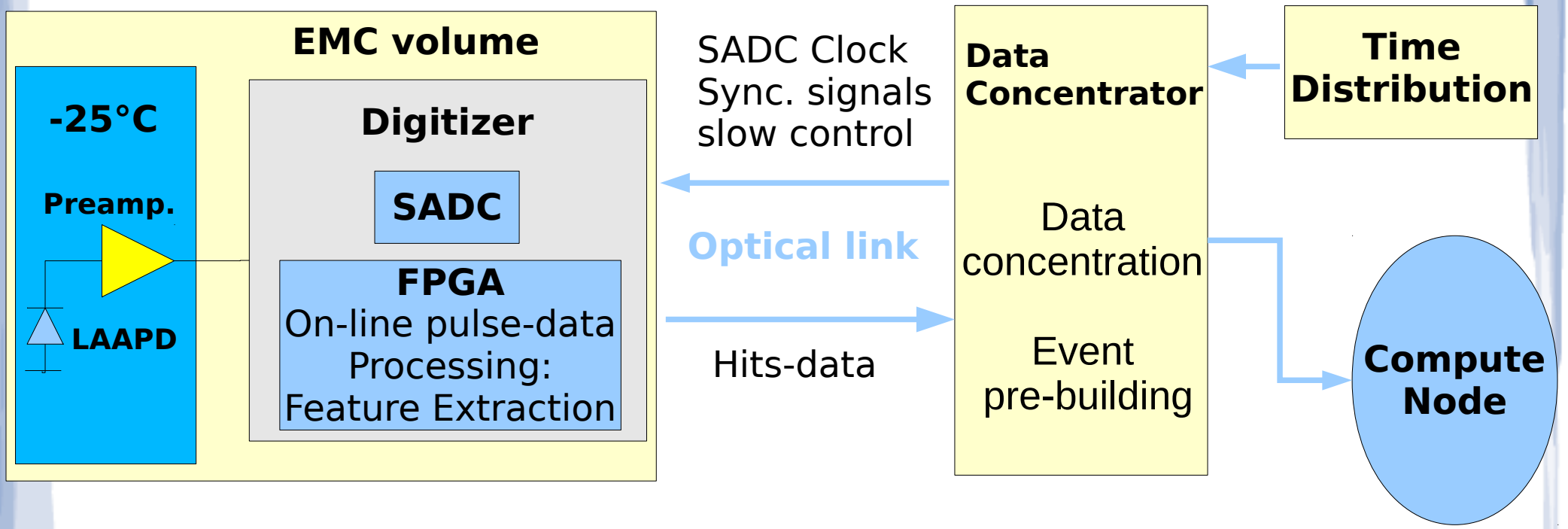
Data Concentrator — Combine several Front-Ends

First Stage "Event" Builder

Second Stage "Event" Builder — Time-ordering (building physics events)

Compute Node — On-line processing of complete events, Accept/reject decision

Readout for Electromagnetic Calorimeter



Key components of the readout:

- Digitizer module with on-line pulse-processing
- Data-concentrator with time-ordered output
- Synchronous optical-link connection (clock-signal distribution)
- High-level on-line data processing

Digitizer Prototype Hardware

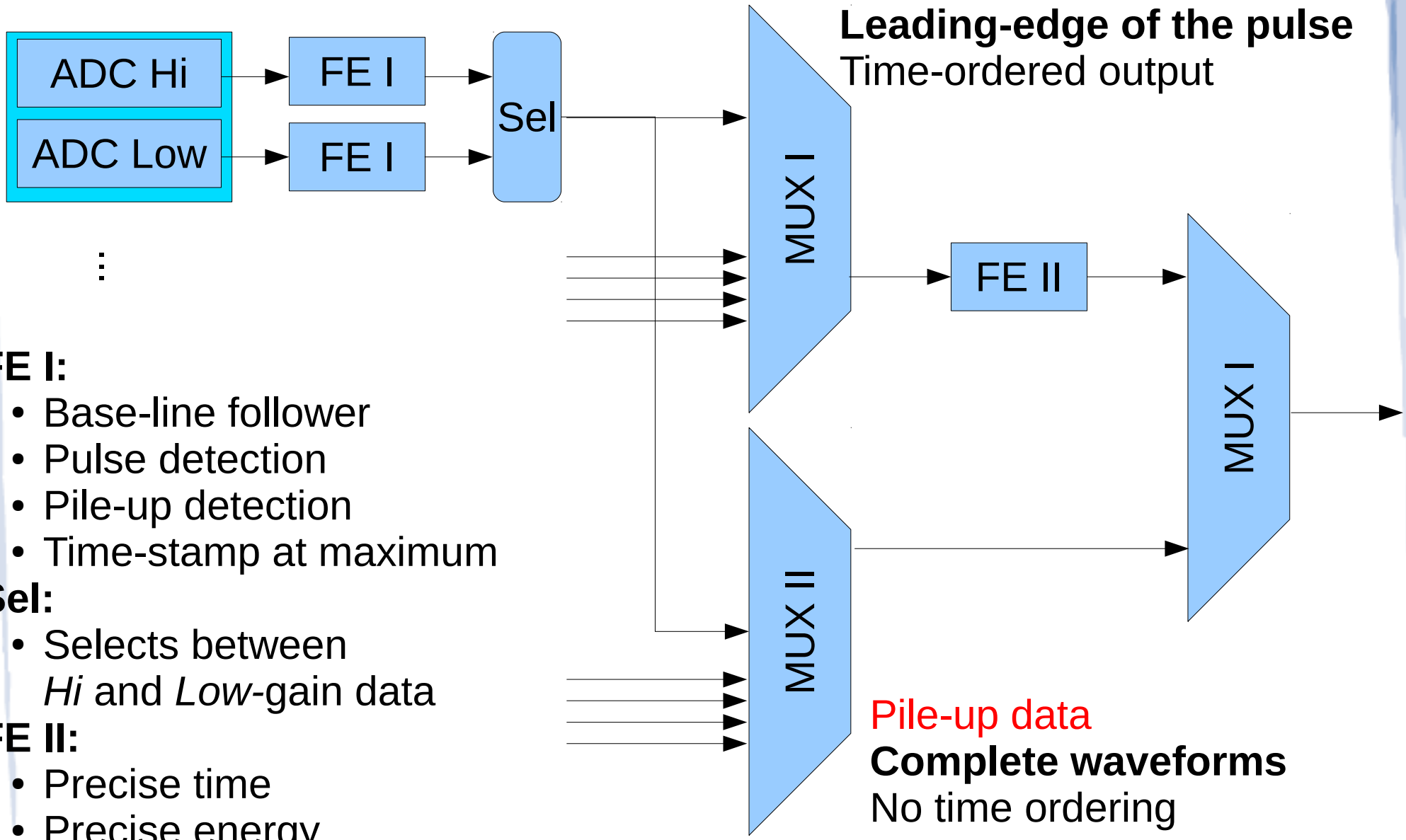
Current prototype
(developed by P. Marciniewski)

- 16 channels
- 125 MHz sampling rate
- Only partial support of a time-synchronisation via optical link

Prototype in development
(is being developed by P. Marciniewski)

- 64 channels (32 inputs with shaping amplifiers and dual-range output)
- Complete SODA compatibility
- 14 bit, 80 MHz
- Two Xilinx Virtex 6 FPGAs with cross-links
- Two independent optical-links connections (for redundancy)

Digitizer Prototype Firmware

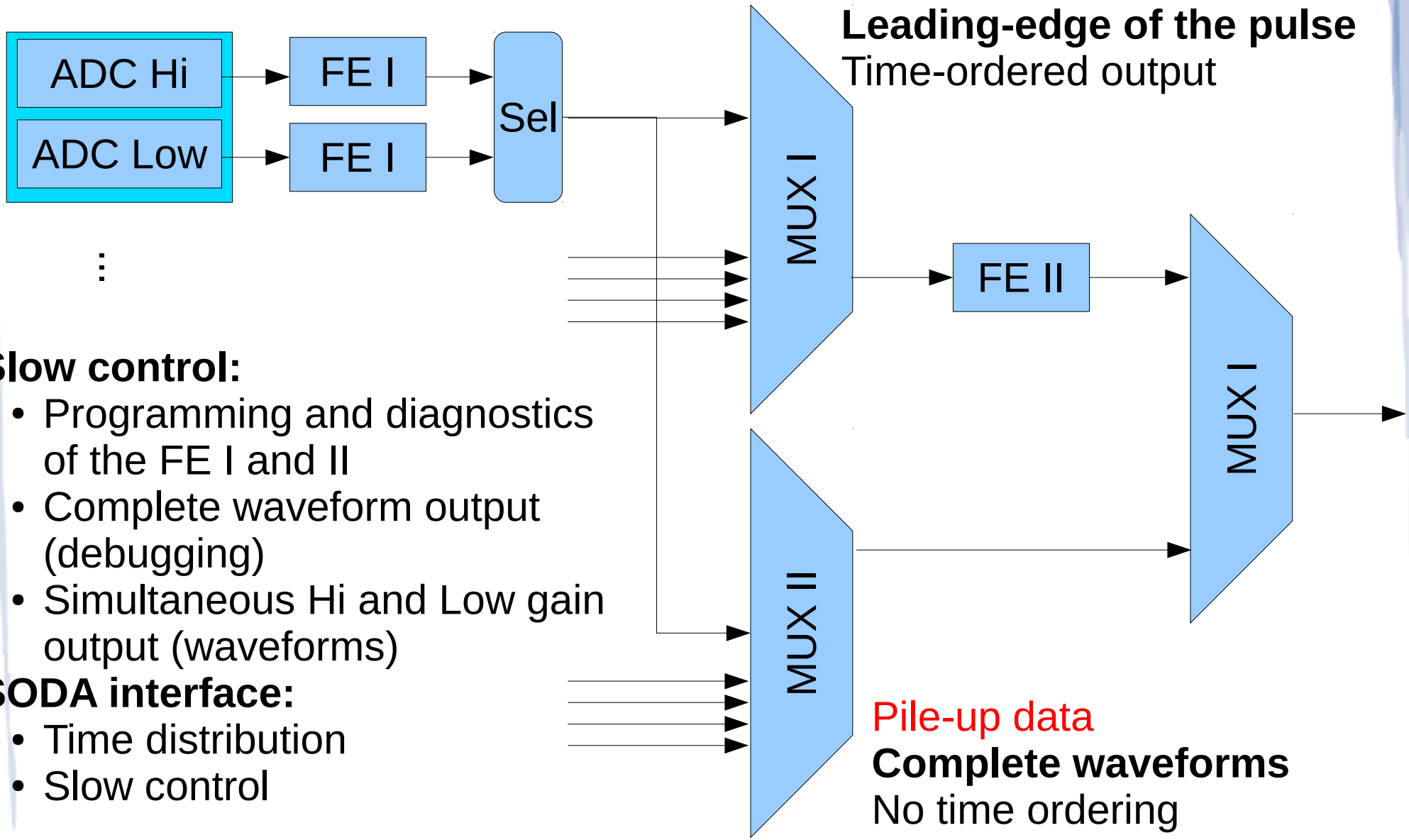


FE I:
- Base-line follower
- Pulse detection
- Pile-up detection
- Time-stamp at maximum

Sel:
- Selects between *Hi* and *Low*-gain data

FE II:
- Precise time
- Precise energy

Digitizer Prototype Firmware



Slow control:

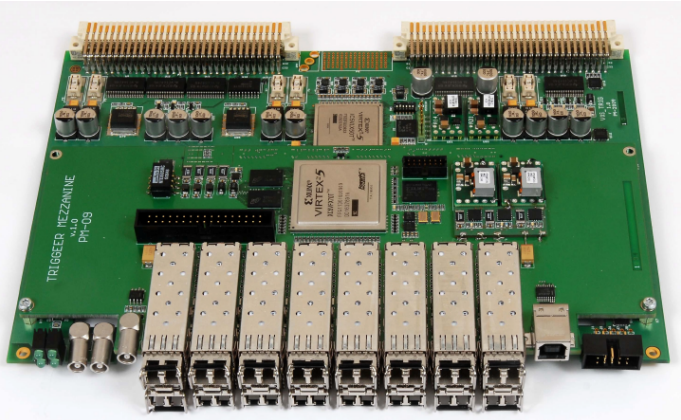
- Programming and diagnostics of the FE I and II
- Complete waveform output (debugging)
- Simultaneous Hi and Low gain output (waveforms)

SODA interface:

- Time distribution
- Slow control

Data Concentrator

Hardware:



Data Concentrator:
(developed by P. Marciniewski)

- 16 channels
- Xilinx Virtex-5 FXT for data processing

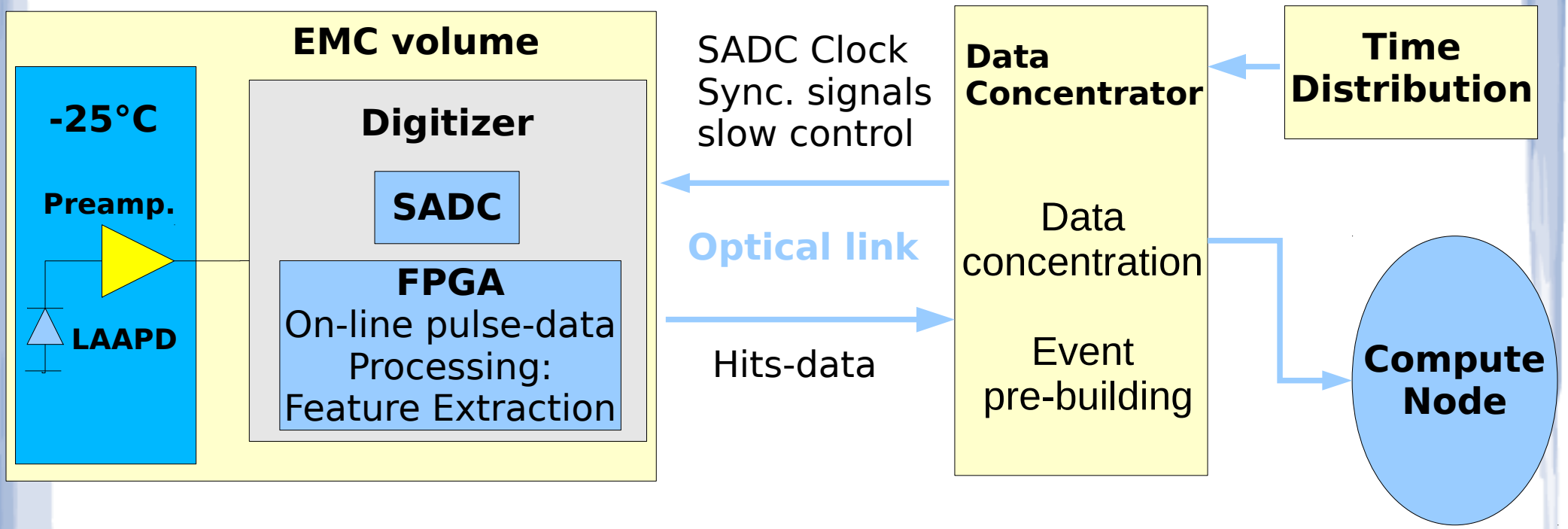
Firmware:

- Complete SODA functionality (synchronous redistribution of SODA commands) (precision of time synchronisation verified)
- Time-ordered multiplexing
- Separation of slow-control data from the main data stream

To be implemented:

- Pile-up recovery block (recovery logic is defined and verified)
- Energy calibration of the data
- Combination of two channels, which belong to the same crystal

Functionality of the EMC Readout

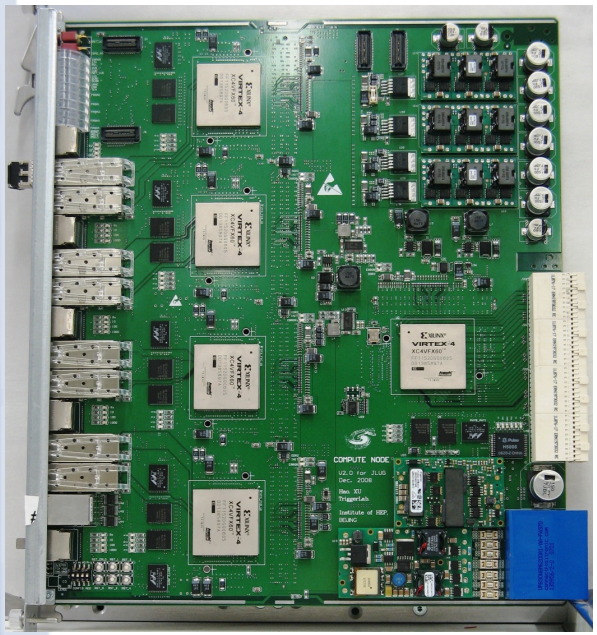


Current status of the readout:

- Data, collected by digitizers, are stored in the DDR memory of a compute node
- The DDR memory of a compute node is read out by embedded Linux, which runs in FPGA power-pc core

Readout prototype is ready for tests with beams

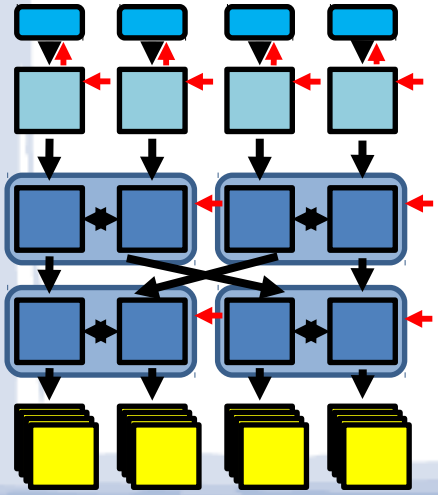
Desired Functionality of EMC readout



Compute-node functionality:

- Final time-sorting of the data using precise time-stamps
- Merge pile-up data with non-pile up
- Perform event building based on time stamps
- Perform clustering

Tasks are too complicated to have pipe-lined design → asynchronous design



Time-ordering network is required in order to construct complete EMC events, which are ready to be combined with data from other subdetectors

Summary: EMC readout

- Prototype of the trigger-less readout of the EMC for limited number of channels is constructed and tested with pulsers
  → ready for beam verifications
- Time-ordering network for event building should be designed
  - Hardware?
  - Firmware?
- Final stage of the event-building for the EMC can be implemented and tested without time-ordering network (for one data concentrator module) ← work in progress

What Do We Need for Further Development?

- SODA protocol (first draft fixed)
- Definition of data concentrator:
  - Is hardware common for all subsystems?
  - Define standard interface between FEE and DAQ
- Protocol for the time-ordering network
- Hardware for the time-ordering network

These issues should be discussed as soon as possible!
(Rauischholzhausen workshop!)

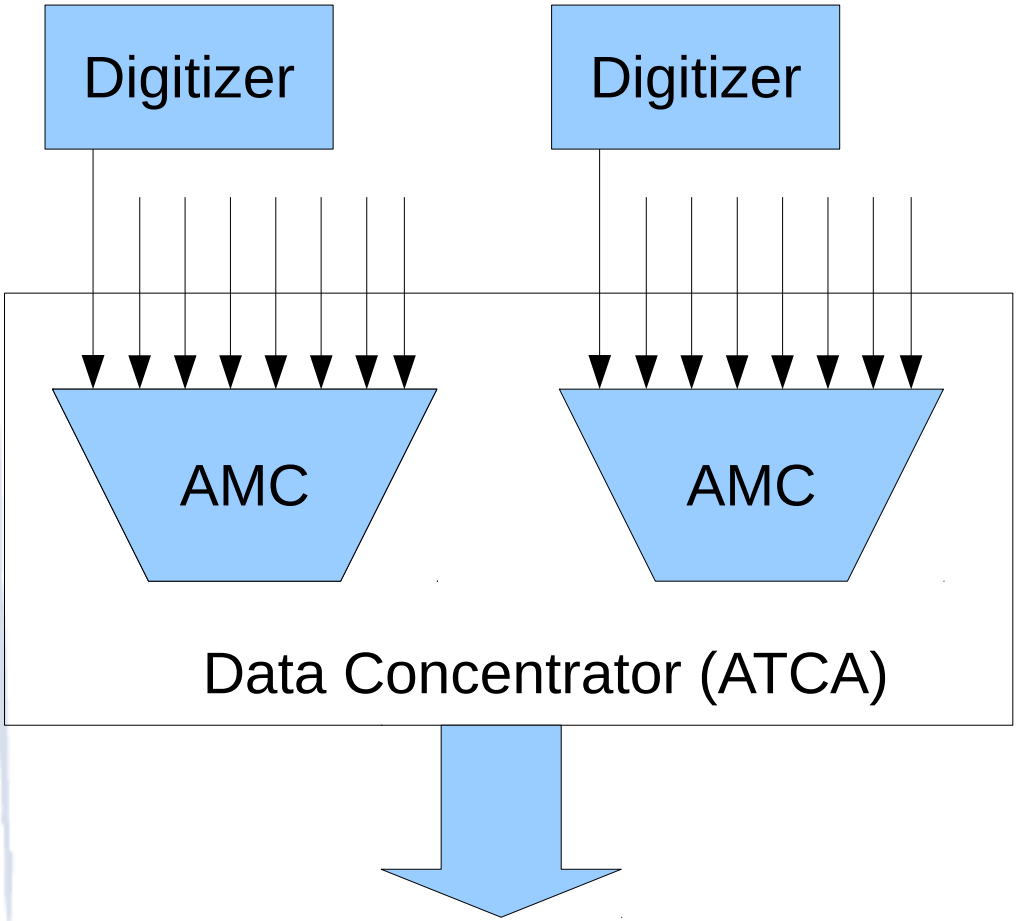
Extra Slides

Hardware for Data-Concentrator

Boundary conditions:

- Has standard interface to the PANDA event-building network
- ATCA compatible (AMC cards)
- Interface to digitizers (8 optical links/AMC card) and ATCA back-plain (fast serial links)
- Has interface to SODA (via back-plain)
- Has enough FPGA resources (can be specified once full-functional prototype, based on the existing hardware, is developed and tested)

Interface to DAQ
Forward End-Cap



To time-ordering network/compute nodes
(back-plain connections)

# input channels:	**6941×2**
# digitizers:	**217**
# AMC cards:	**28**
# ATCA carriers:	**7**

Interface to DAQ
Barrel and Backward End-Cap

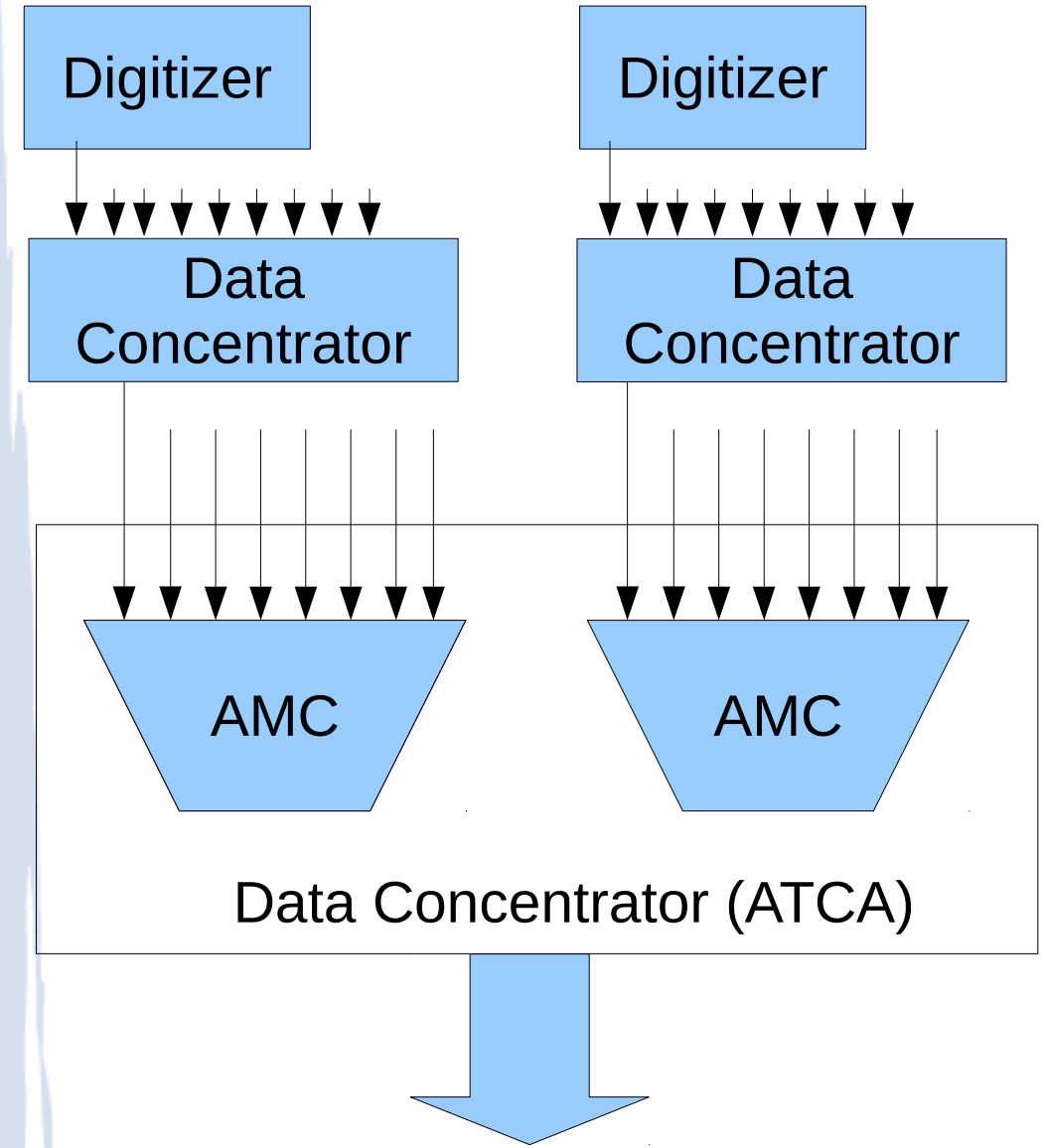
Hit-rate per channel is low in comparison with the forward end-cap.
Therefore, more channels can be combined together

Data concentrator module:

- Combines many (32) optical-link connections with one FPGA (Kintex-7)
- Each optical-link intrface can be used as:
  - SODA input
  - Interface to digitizer
  - Interface to Data Multiplexer

- Can be used to combine different amount of channels (forward, middle and backward regions):
  - 4×(**6 channels → 1**)
  - 2×(**14 channels → 1**)
  - 1×(**30 channels → 1**)

Interface to DAQ
Barrel and Backward End-Cap



To time-ordering network/compute nodes
(back-plain connections)

input channels: **(600+11360)×2**
digitizers: **1196**

data concentrators: **46**

AMC cards: **12**

ATCA carriers: **3**