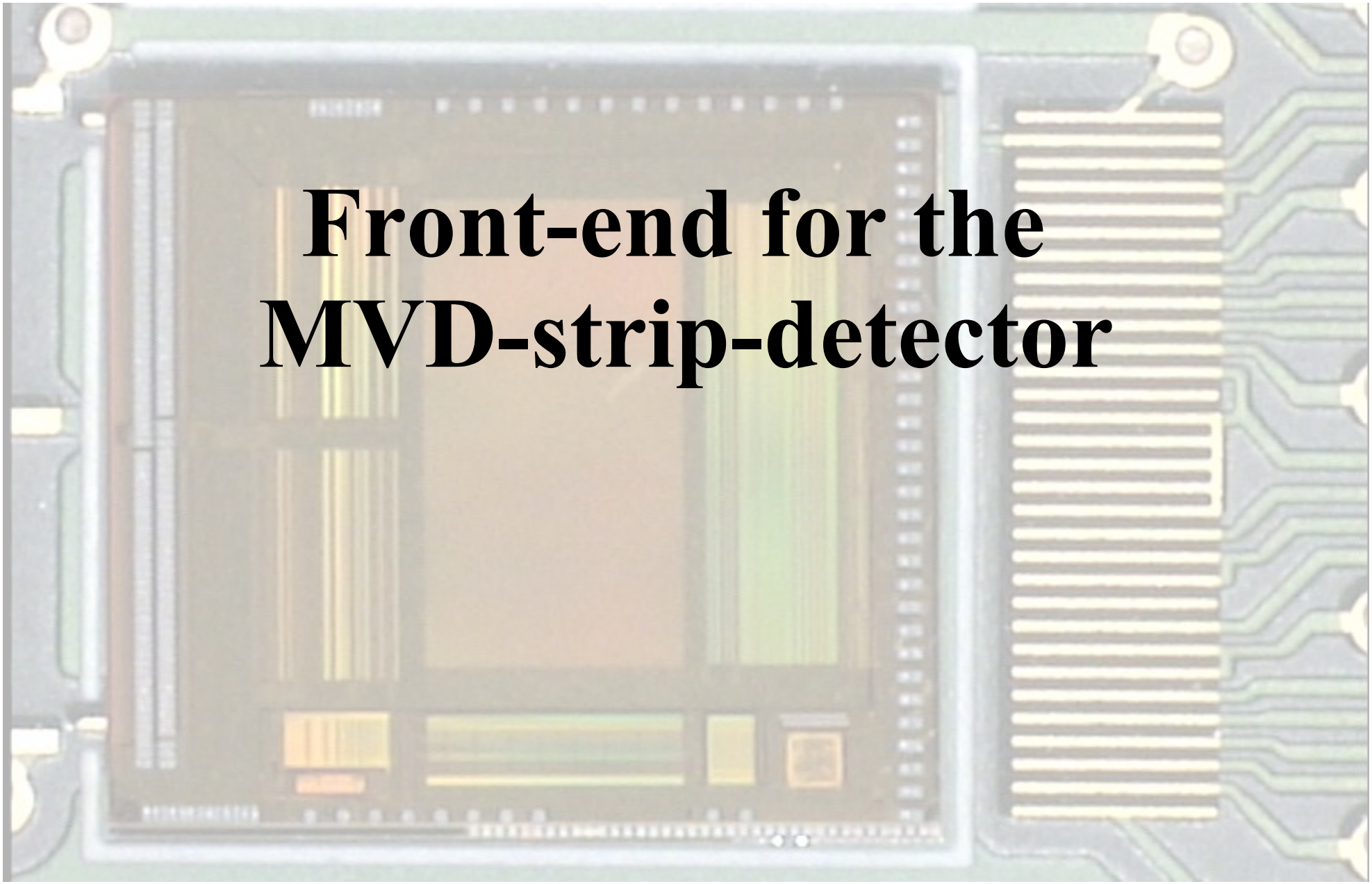


Front-end for the MVD-strip-detector

XL PANDA Meeting, MVD Subgroup Meeting - March 05, 2012

Requirements

- PANDA specific requirements:
  - self triggering
  - precise time resolution
  - fully digital hit information

=> not many front-end types available to comply with these requirements

Requirements

hint: (go to next slide)

Parameter	Value	Remarks
Geometry		
width	≤ 8 mm	
depth	≤ 8 mm	
input pad pitch	≈ 50 µm	
pad configuration	lateral pads occupied only for diagnostic functions, should be left unconnected for final setup	
channels per front-end	$2^6 \ldots 2^8$	default: 128 channels
Input Compliance		
sensor capacitances, fully depleted sensor		
	< 10 pF	rect. short strips
	< 50 pF	rect. long strips + ganging
	< 20 pF	trapezoidal sensor
input polarity	either	selectable via slow control
input ENC	< 800 e$^-$	$C_{\text{sensor}} = 10$ pF
	$< 1{,}000$ e$^-$	$C_{\text{sensor}} = 25$ pF
Signal		
dynamic range	240 ke$^-$ ($\approx$38.5 fC)	
min. SNR for MIPS	12	22,500 e$^-$ for MIPs in 300 µm silicon, guaranteed within lifetime
peaking time	$\approx 5 \ldots 25$ ns	typical Si drift times
digitisation resolution	≥ 8 bit	
Power		
overall power dissipation	< 1 W	assuming 128 channels per front-end
Dynamical		
trigger	internally generated	when charge pulse exceeds adjustable threshold value
time stamp resolution	< 20 ns	
dead time / ch	< 6 µs	baseline restored to 1%
overshoot recovery time / ch	< 25 µs	
average hit rates / ch (poissonian mean)		derived from simulations at a beam momentum of 15 GeV/c
hot spots	9,000 s^{-1}	$\overline{p}p$
	40,000 s^{-1}	$\overline{p}Au$
average occupancy	6,000 s^{-1}	$\overline{p}p$
	30,000 s^{-1}	$\overline{p}Au$
Interface		
slow control	any	low pincount, e.g. I^{2}C
data	sparsified data	

Technical Design Report for the:
PANDA
Micro Vertex Detector

PANDA Collaboration

30th November 2011

Section 4.2.1, Table 4.3

Options

- adapted ToPix(3)
- FAIR/STS-XYTER
- (modified) FSSR2
- ILC calorimeter development by M. Idzik

Options

- other then the aforementioned?

  => looked through several experiments

  (BNL, JLAB, Fermi-lab, (S)LHC, AMS, ...)
- in most of the cases even the APV25 is more suitable

Options

- Comparison

Parameter	adapted ToPix	STS-XYTER	FSSR2
input pad pitch	≈ 50 µm	50 µm	50 µm
channels per front-end	128	128	128
dynamical range	100 fC	15 fC	25 fC
ENC	1,000 e^- @ 20 pF	700 e^- @ 28 pF	240 e^- + 35 e^-/pF
peaking time	6 ns	80 ns	65 ns
power consumption	0.8 mW/ch	1.2 mW/ch	4.0 mW/ch
trigger	self-triggering	self-triggering	self-triggering
digitisation technique	ToT	ToT	Flash-ADC
digitisation resolution	10 bit	4 – 6 bit	3 bit Flash-ADC
time resolution	1.85 ns @ 155 MHz	1.85 ns @ 155 MHz	132 ns time stamp
data interface	e-link - SLVS	up to 2.5 Gbps	LVDS
number of data lines	1 pair	1 pair	1 to 6 pairs
slow control	custom (serial)	custom	custom LVDS
process	0.13 µm CMOS	UMC 0.18 µm	0.25 µm CMOS
radiation hardness	> 10 MRad	10 MRad	up to 20 MRad

Technical Design Report for the:
PANDA
Micro Vertex Detector

PANDA Collaboration

30th November 2011

Section 4.2.2, Table 4.4

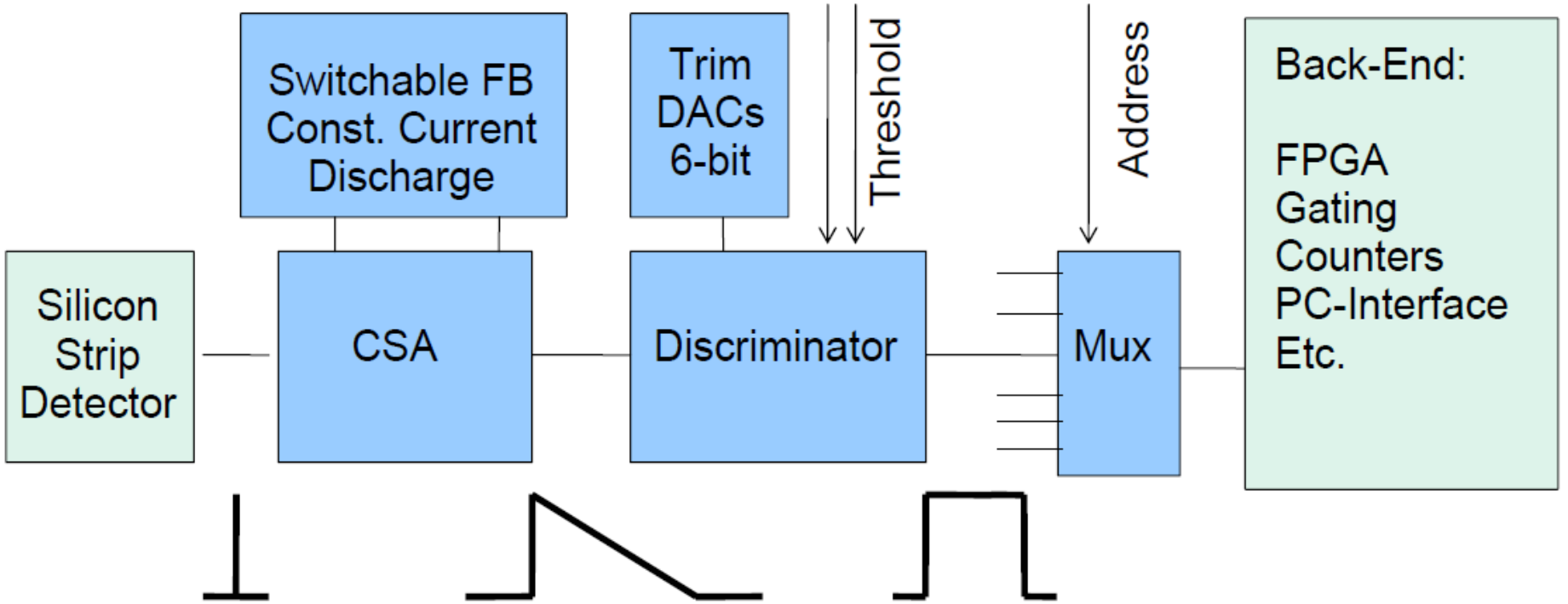
STS-XYTER

- development by R. Szczygiel et al., AGH Krakow – in early prototype state
- self triggered architecture
- low power and low resolution dedicated for silicon strip detectors
- ToT-based digitization

Low Power STS-XYTER in Second Iteration

Chip Overview - Architecture

UMC 0.180 technology for radiation hardness



- Time over threshold energy conversion (ToT)
- 2.3 mW/channel at 500 ENC/30pF (c.f. ~20mW on n-XYTER)
- 4 to 6 bit resolution **we favor high resolution**
- 30 channels

R. Szczygiel et al., AGH Krakow

STS-XYTER

- latest test results as of January 2012
- shown on CBM FEE/DAQ/FLES Workshop

TOT01 -> TOT02 evolution

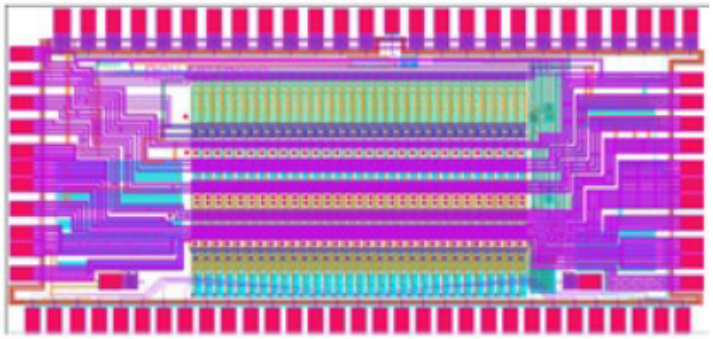
Major modifications:

-> added digital back-end (fast serial interface)

-> rad-hard layout of AFE (ELT NMOS transistors)

-> improved CSA core (boosted folded cascode)

-> improved constant-current FB (more linear at low charges)



Design parameters:

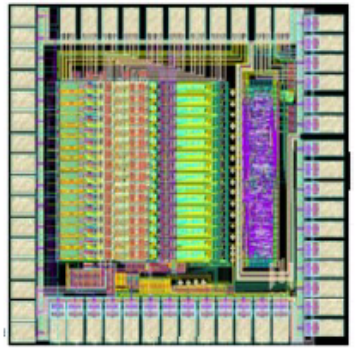
-> optimized for low noise ~750 e- @30pF AC-coupled detector

-> power consumption: 2.1 mW / analogue channel

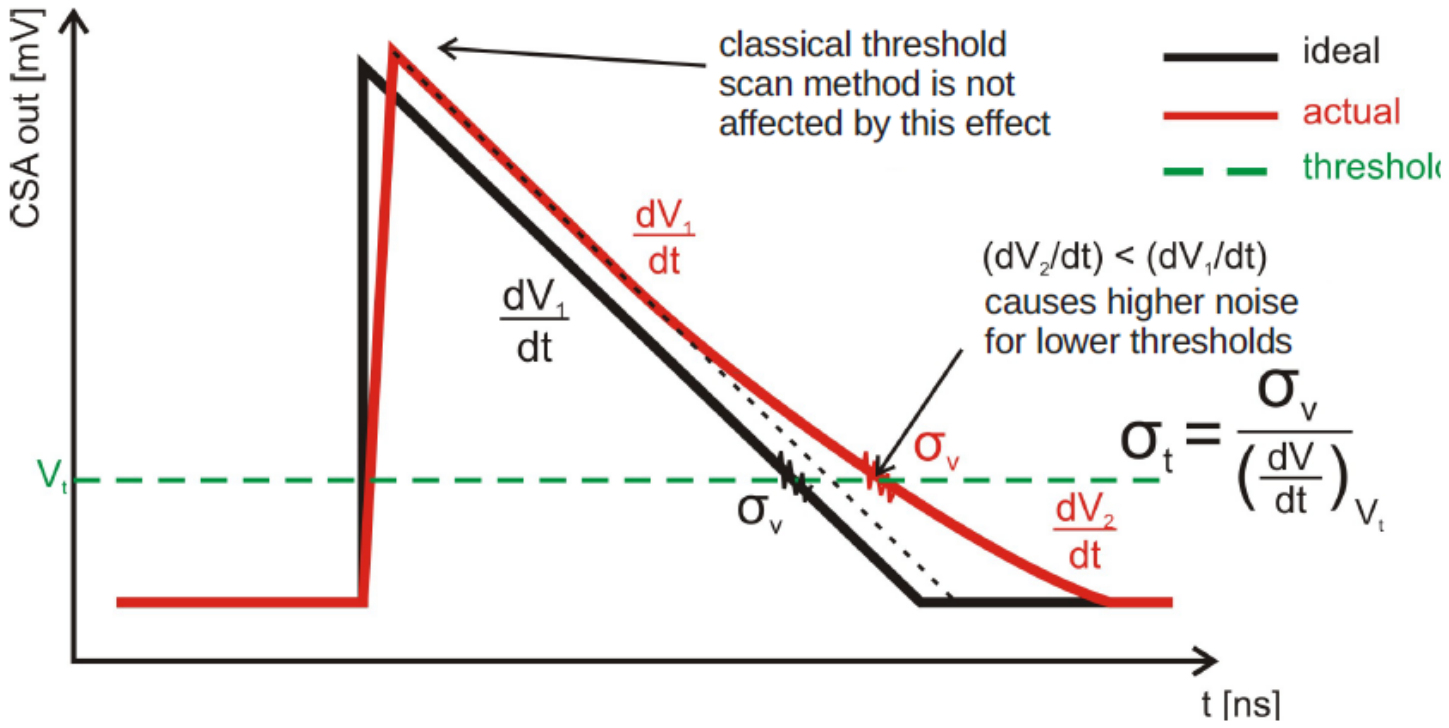
-> peaking time: ~80 ns

-> Technology: UMC 180nm CMOS 1.8V

-> 16 channels, 50 µm pitch



Issues discovered during TOT01 development and tests



Remedies:

-> reduce operation of the feedback current mirror below Vdsat

(reduce the Vdsat by increasing W/L while keepeing the parameters of the mirror at acceptable level)

-> increasing gain of the CSA core (using boosted folded-cascode amplifier)

Parameter summary

Die parameters			
Technology	UMC 180 nm CMOS	Die size	1.5 mm x 1.5 mm 2.25 mm^2
Number of pads / channels	56 / 16	Channel pitch / length	50 µm / 820 µm
Measured chip performance			
No detector (C_{det}=0pF), ASIC#1		**2cm detector (Cdet=3pF), ASIC#2**	
Voltage gain	=55 mV/fC +-0.36 mV/fC	Voltage gain	=54.7 mV/fC +-0.64 mV/fC
Time gain	=216 ns/fC +-7.54 ns/fC	Time gain	=198 ns/fC +-8.97 ns/fC
$ENC_{thr.scan}$	196 e-	$ENC_{thr.scan}$	240 e-
$ENC_{tot.scan}$	286 e-	$ENC_{tot.scan}$	350 e-
Measured static power consumption			
CSA	1.25 mW	Semi-digital back-end	330 µW
Discriminator + DAC	530 µW	Total (w/o digital back-end)	2.1 mW/channel
Simulated performance of the CSA core (not directly measurable)			
Gain	7000 V/V	Bandwidth	1.3 MHz
GBW	9 GHz		

Noise:

(thr scan)
ENC=196+14.6*Cdet
ENC@30pF = 634 e-

(tot scan)
ENC=286+21.3*Cdet
ENC@30pF = 925 e-

Pros & cons

Pros:

- infinite dynamic range
- low power consumption
- simple architecture

Cons:

- sensitivity to leakage currents
- pulse length dependant on signal amplitude
- wideband → noise
- timewalk (timestamp precision vs noise)

STS-XYTER

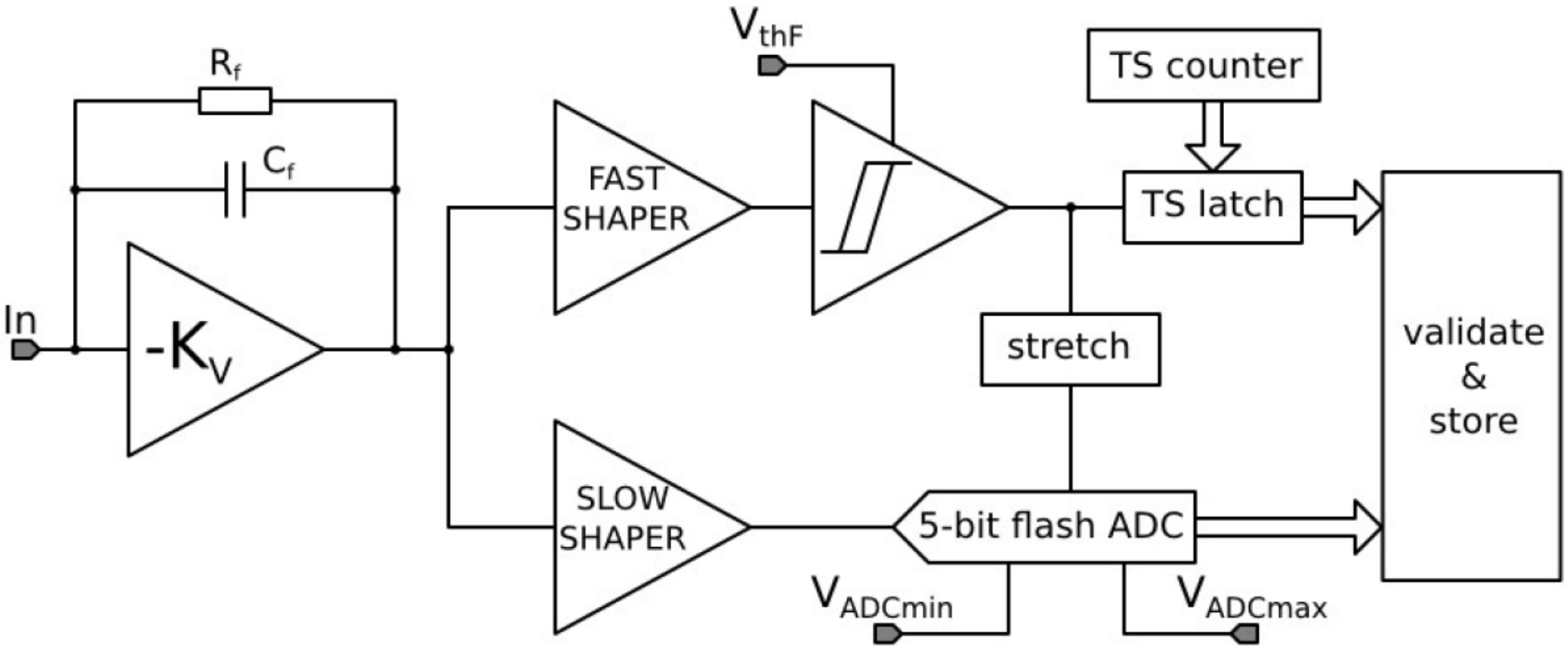
- Designer not happy with:
  - time resolution (time walk)
  - threshold dispersion
- reasons are due to a mixture of:
  - noise level of CBM sensors + long cables and
  - low signals time walk

=> new architecture for STS ASIC!!

STS ASIC working specifications

- 128 channels
- CBMnet backend
- Linear range 1-12 fC (typical input charge = 2 fC)
- Power < 10 mW / channel
- Time measurement < 10 ns resolution
- Detector: DC (AC?), 30 pF total capacitance
- Dual polarity
- Recovery from overload
- Leakage current compensation

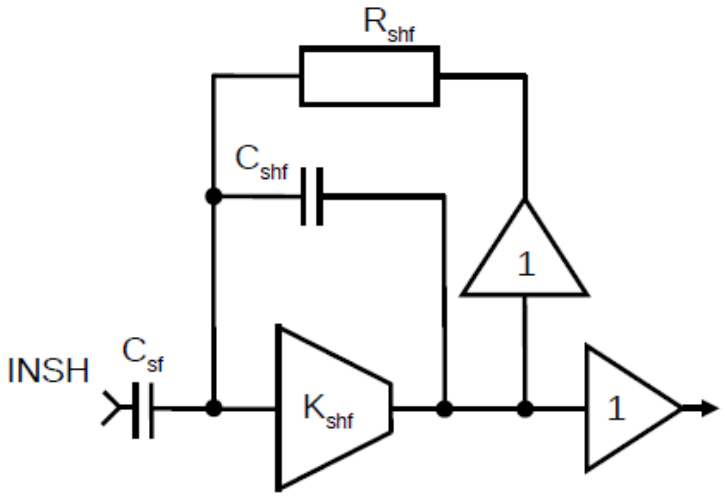
Block diagram of a single channel



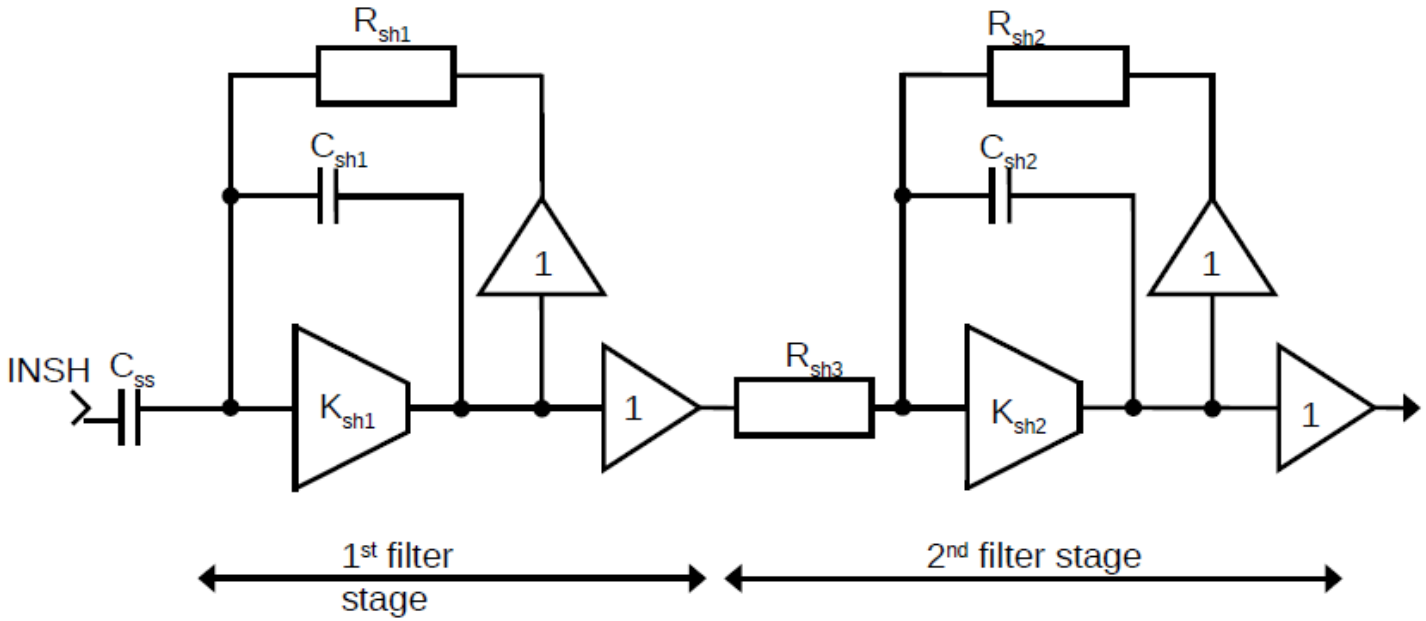
$V_{thF} < V_{ADCmin}$ –> the time measurement is validated by the energy measurement – worst cases dropped

Fast CR-RC and slow CR-$(RC)^2$ shapers

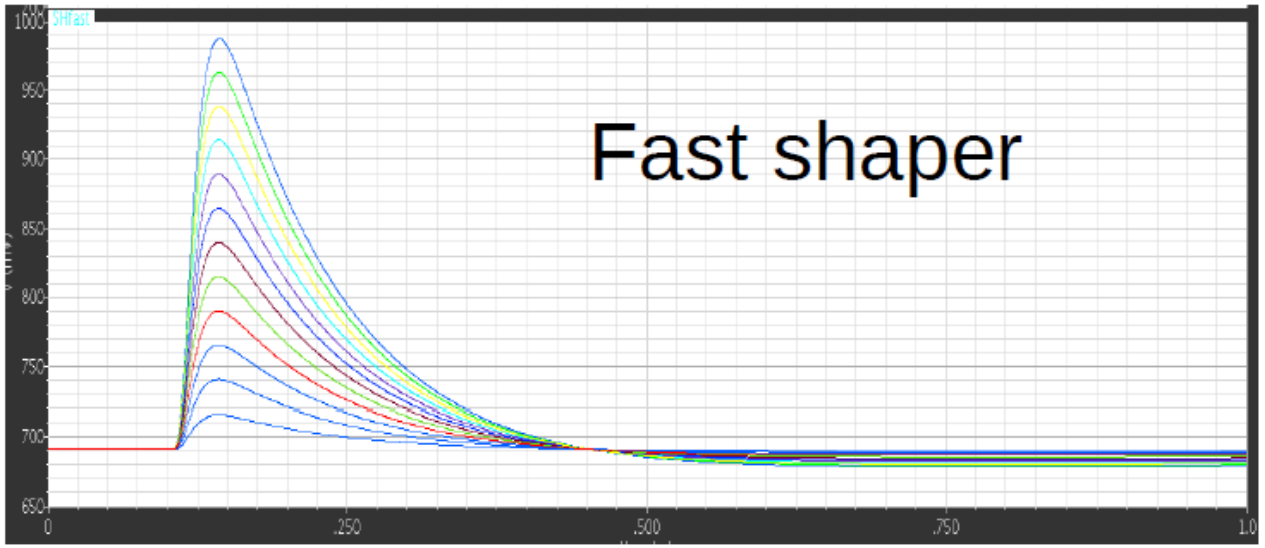
FAST



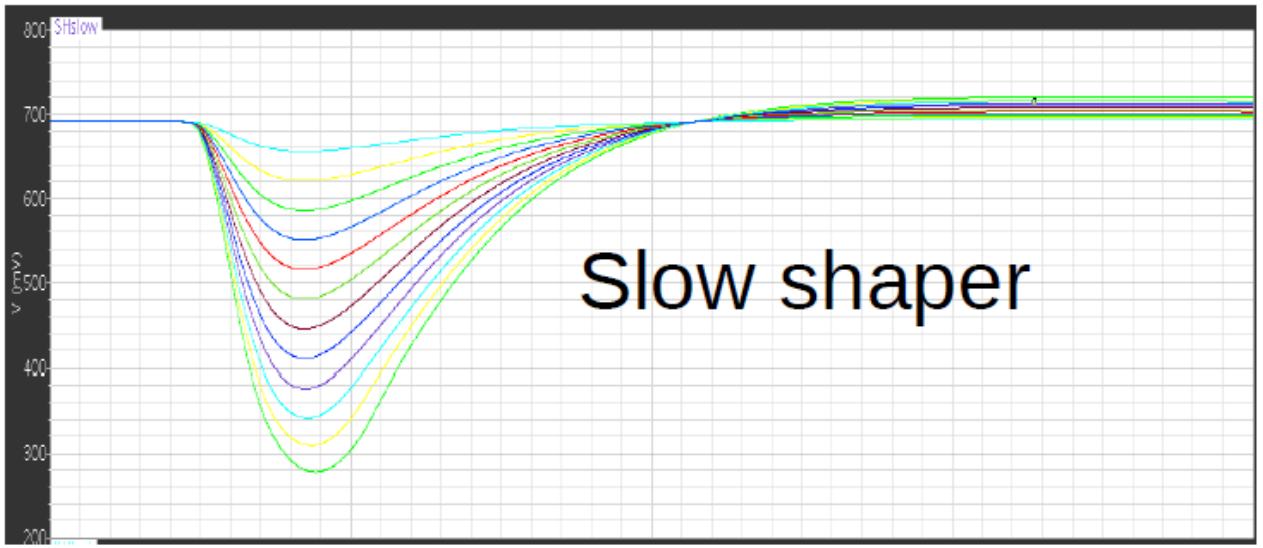
SLOW



Timing and ENC: Qin = 1-12fC, PWR =5.5mW



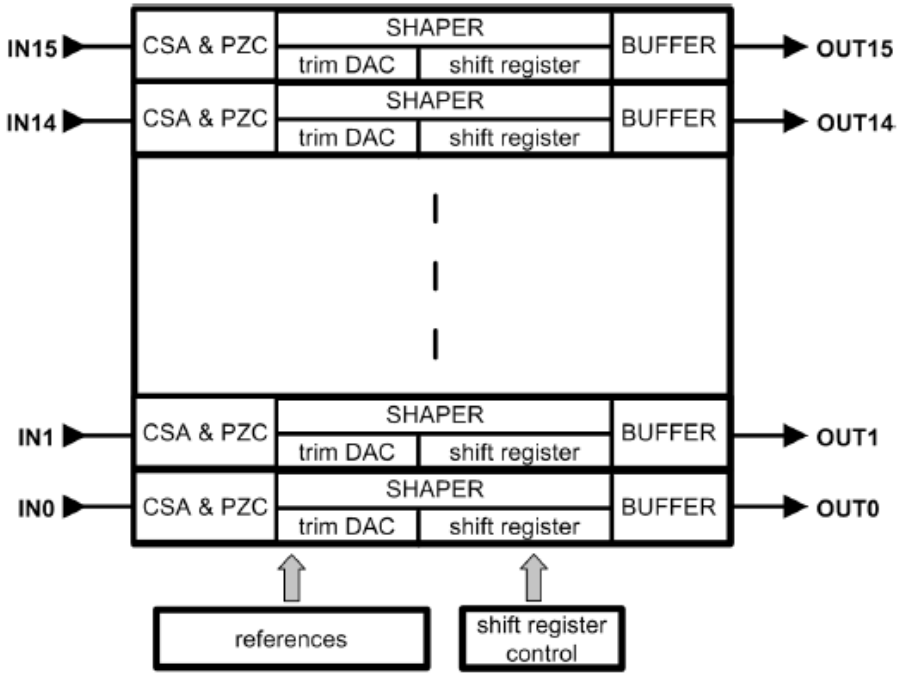
Tp = 38ns
ENC = 1020 el

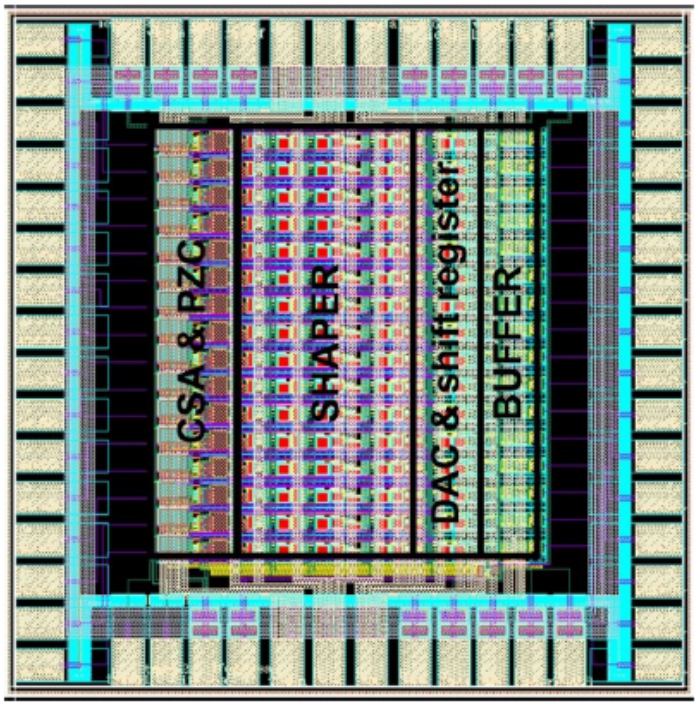


Tp = 95ns
ENC = 624 el

Only simulation!!!

Our prototype: FSDR16 chip, tested 2011/2012





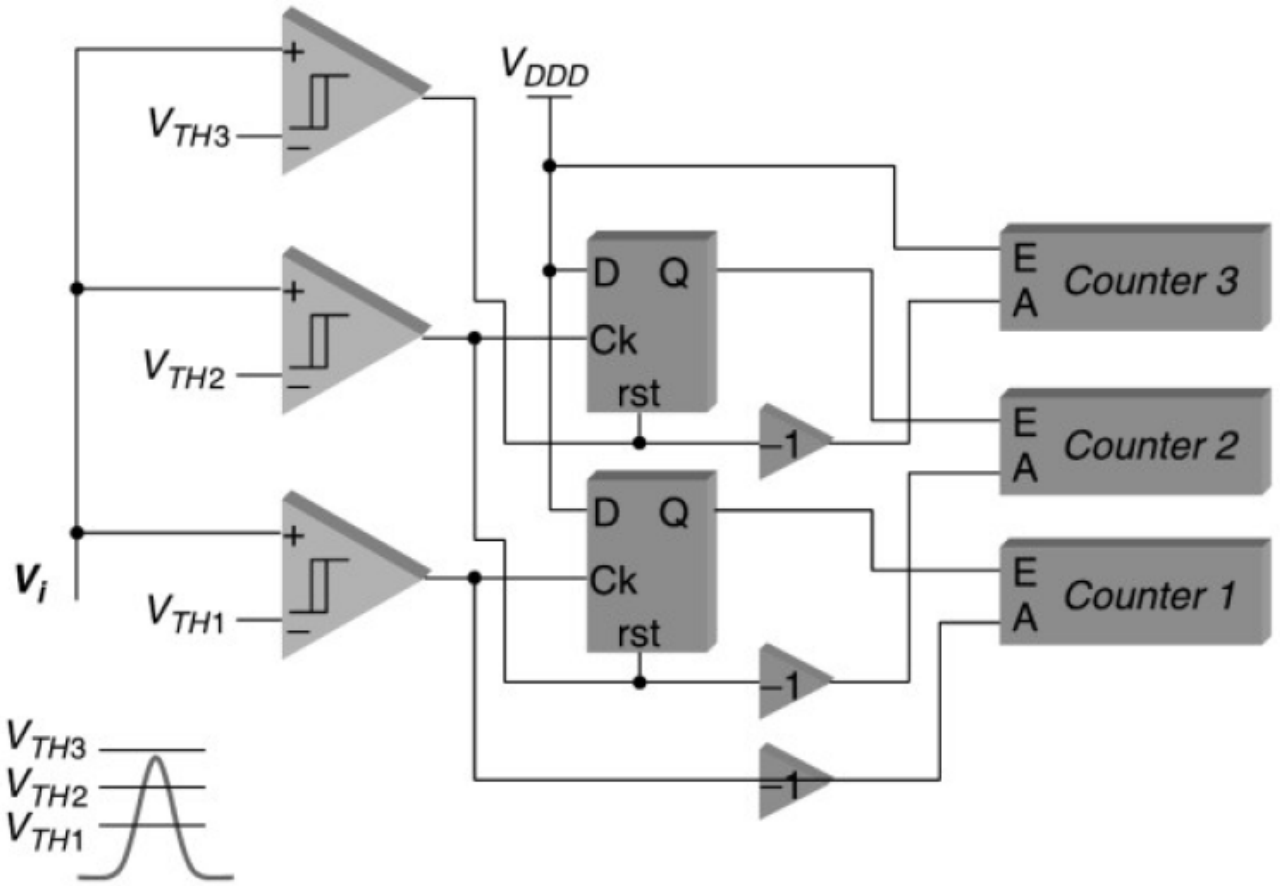
FSDR16 – features:

- implemented in UMC 180nm CMOS,
- dedicated for silicon strip detectors,
- two programmable shaper types which allow to make a comparison between typical CR-$(RC)^5$ shaper based on real poles and a nearly true Gaussian shaper based on complex poles,
- two switchable peaking time tp for each of shaper types

FSDR16 – block diagram:

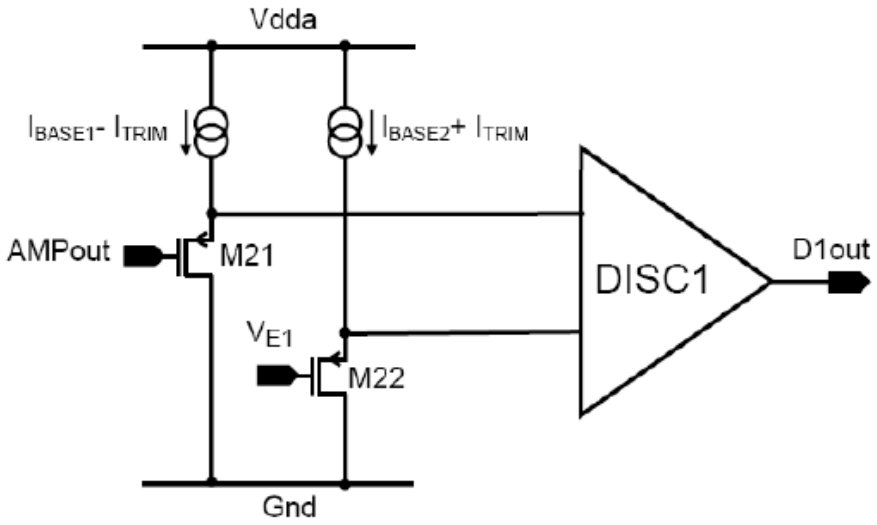
- contains 16 channels,
- 16 analog inputs, 16 analog outputs,
- single channel is built with an analog (CSA, PZC, shaper) and digital (shift register) part
- DC voltage shaper output spread is corrected by a 7-bit trim DAC separately in ech channel.

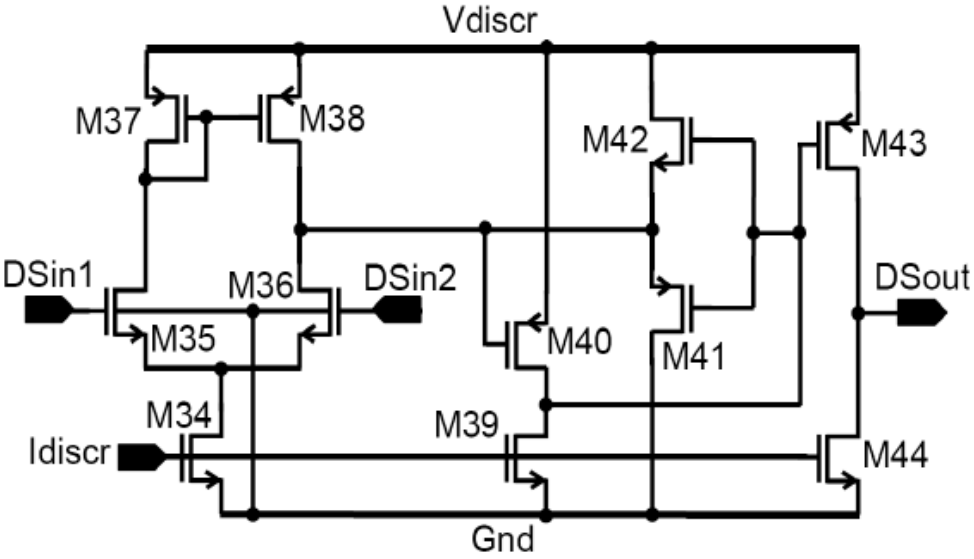
Energy measurements: 5-bit flash ADC



Small discriminator

Option 1: discriminator with trimming





Area: 20 x 50 um^2

(40 x 50 um^2 with register)

PWR: 10 – 20 uW

Option 2: discriminator with automatic offset cancellation

Conclusions

- Separated channels for time and amplitude measurements – independent optimization for timestamp precision and noise
- Expected better noise than ToT
- Expected better timing precision than ToT
- Needs more power than ToT
- Possible time measurement correction using ADC value
- Most components of well known architecture (CSA, shapers, discriminators, trimming DACs)

- Deadline: July 2012

STS-XYTER

- ToT-version results were actuallynot bad
  - noise of 925e$^-$@30pF
  - 2,1 mW per channel (analog part only)
- STS-XYTER primary development for CBM
  - CBMnet backend (can be deactivated)

=> option dropped in ranking

ToPix3

- adaptation of analog circuits for strip detectors
- would provide comparable readout structures between pixel and strip part
- work by Alberto Potenza, Turin showed feasibility
- how can we bring it on?

Summary

- front-end – decision needed urgent
- decision needed in order to specify:
  - hybrid design
  - power and cooling rating
  - interface to module controller
  - slow control

AGH UNIVERSITY OF SCIENCE AND TECHNOLOGY

TOT02
STS prototype readout ASIC status

Robert Szczygieł, robert.szczygiel@agh.edu.pl
Krzysztof Kasiński, kasinski@agh.edu.pl
Paweł Gryboś pawel.grybos@agh.edu.pl

Department of Measurement and Instrumentation
AGH – UST Kraków, Poland

CBM FEE/DAQ/FLES Workshop
January 25-27, 2012
ZITI, University of Heidelberg

Agenda

- TOT01 -> TOT02 evolution (improvements)
- Problems discovered with TOT01 ASIC and remedies for them
- Methodology, test setup, error sources
- Measurements and results
- Summary and conclusions

TOT01 -> TOT02 evolution

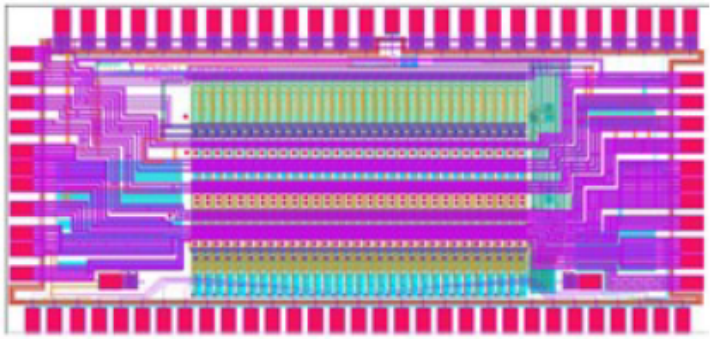
Major modifications:

-> added digital back-end (fast serial interface)

-> rad-hard layout of AFE (ELT NMOS transistors)

-> improved CSA core (boosted folded cascode)

-> improved constant-current FB (more linear at low charges)



Design parameters:

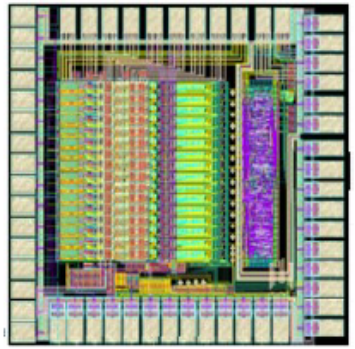
-> optimized for low noise ~750 e- @30pF AC-coupled detector

-> power consumption: 2.1 mW / analogue channel

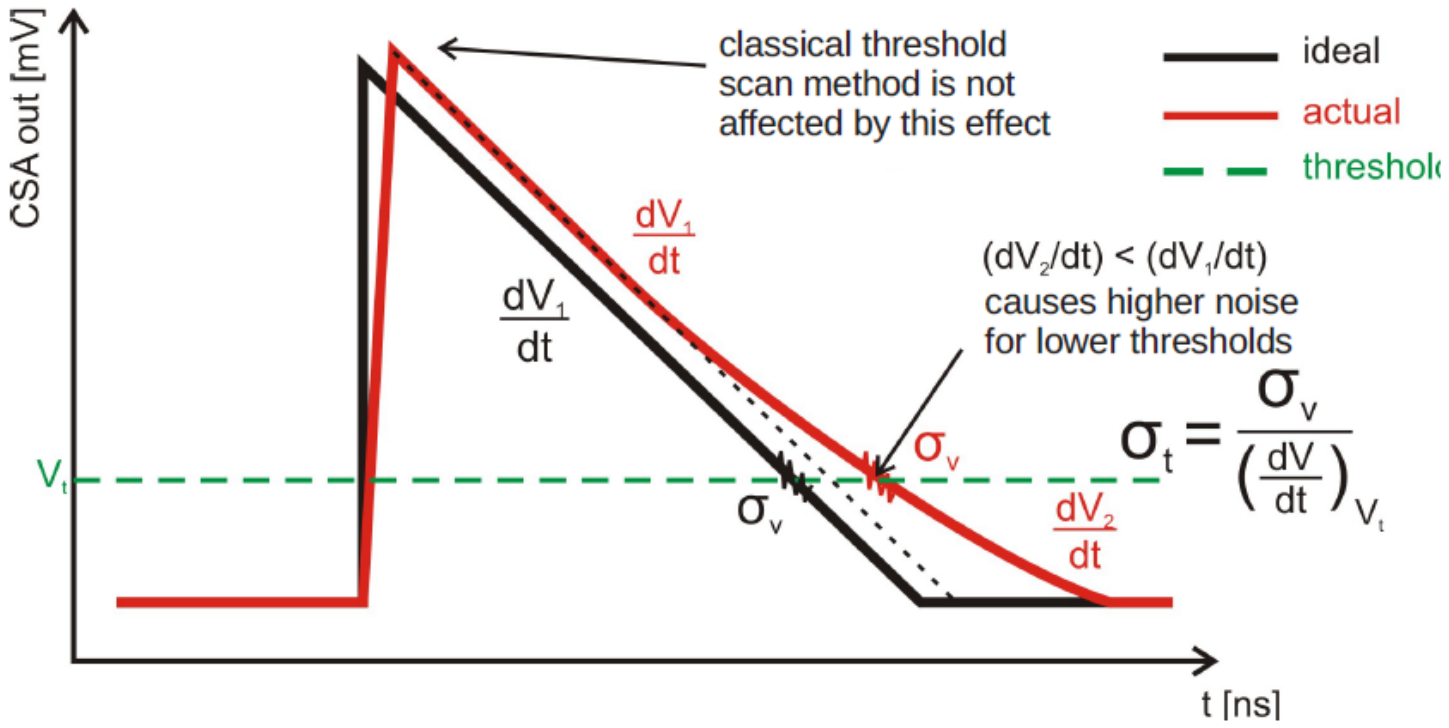
-> peaking time: ~80 ns

-> Technology: UMC 180nm CMOS 1.8V

-> 16 channels, 50 µm pitch



Issues discovered during TOT01 development and tests



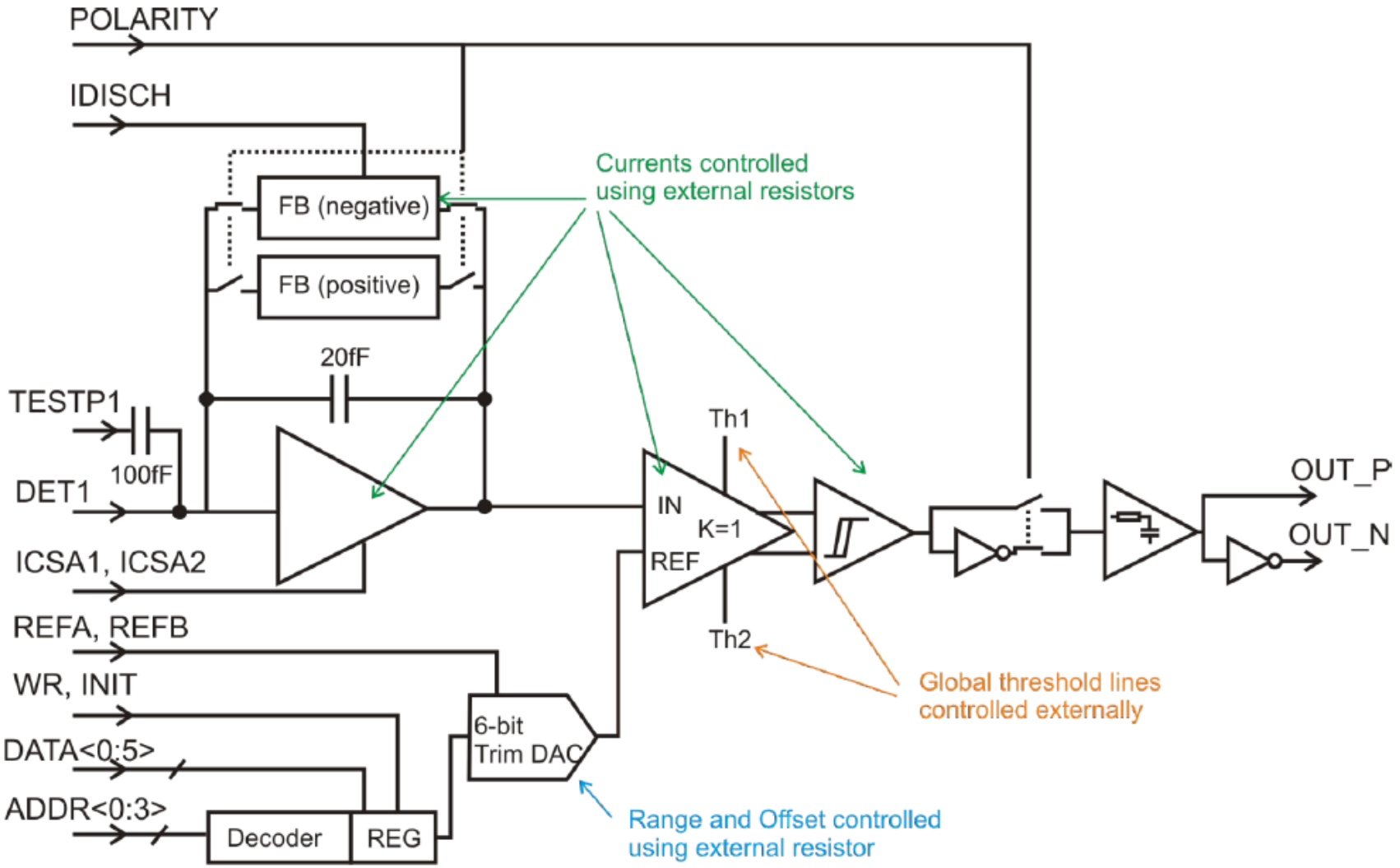
Remedies:

-> reduce operation of the feedback current mirror below Vdsat

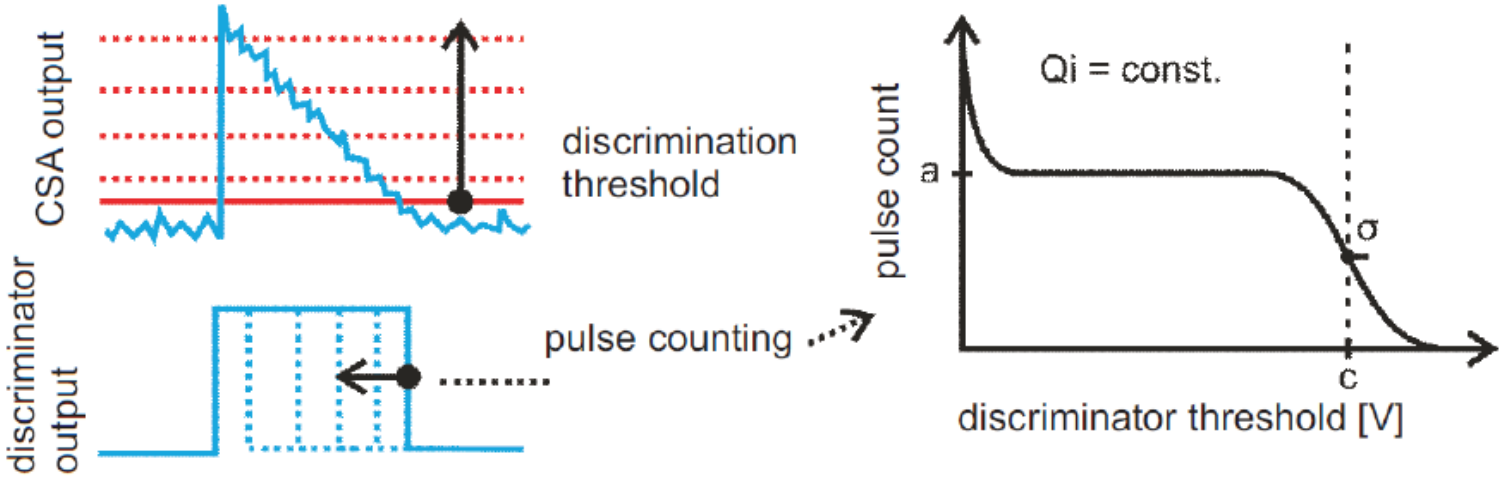
(reduce the Vdsat by increasing W/L while keepeing the parameters of the mirror at acceptable level)

-> increasing gain of the CSA core (using boosted folded-cascode amplifier)

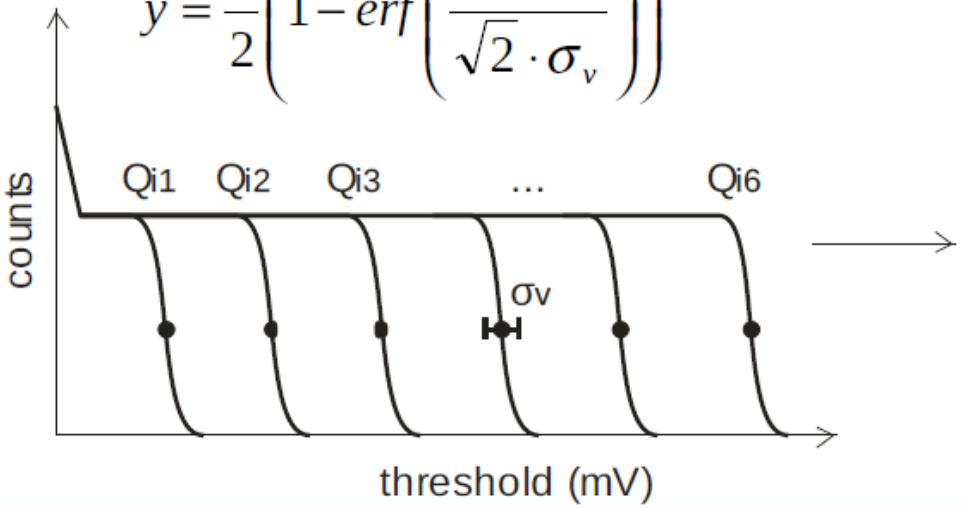
TOT02 overview - reminder



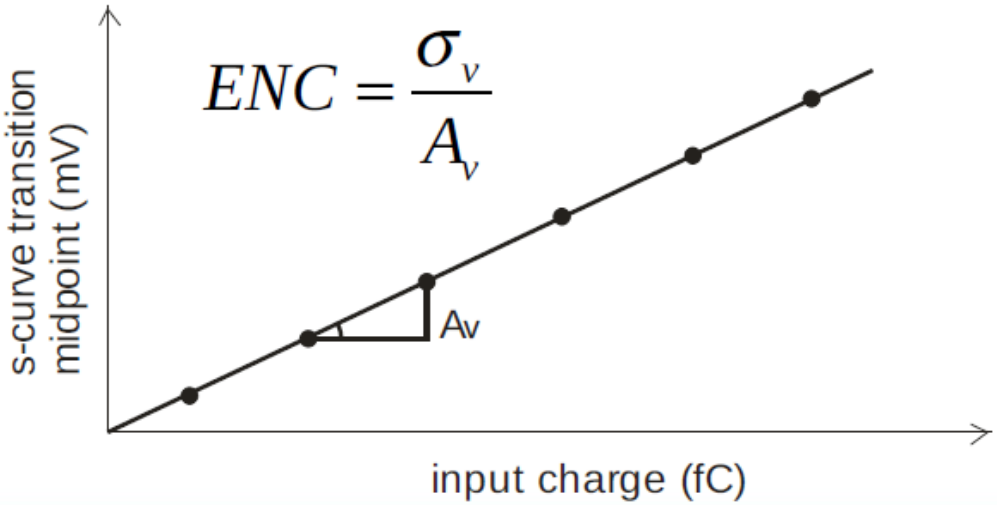
Methodology of characterization
THRESHOLD SCAN



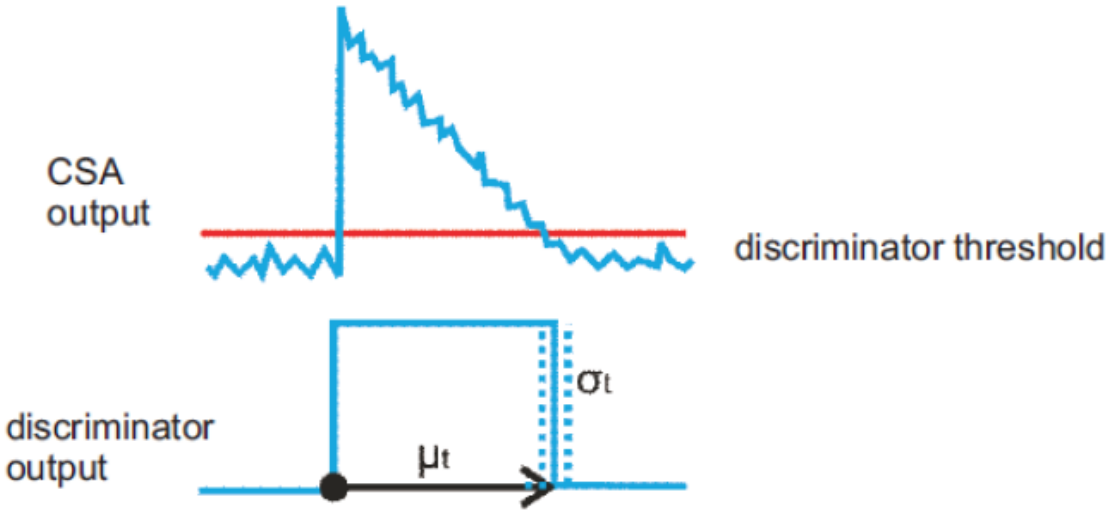
$$y = \frac{a}{2}\left(1 - erf\left(\frac{x-c}{\sqrt{2}\cdot\sigma_v}\right)\right)$$

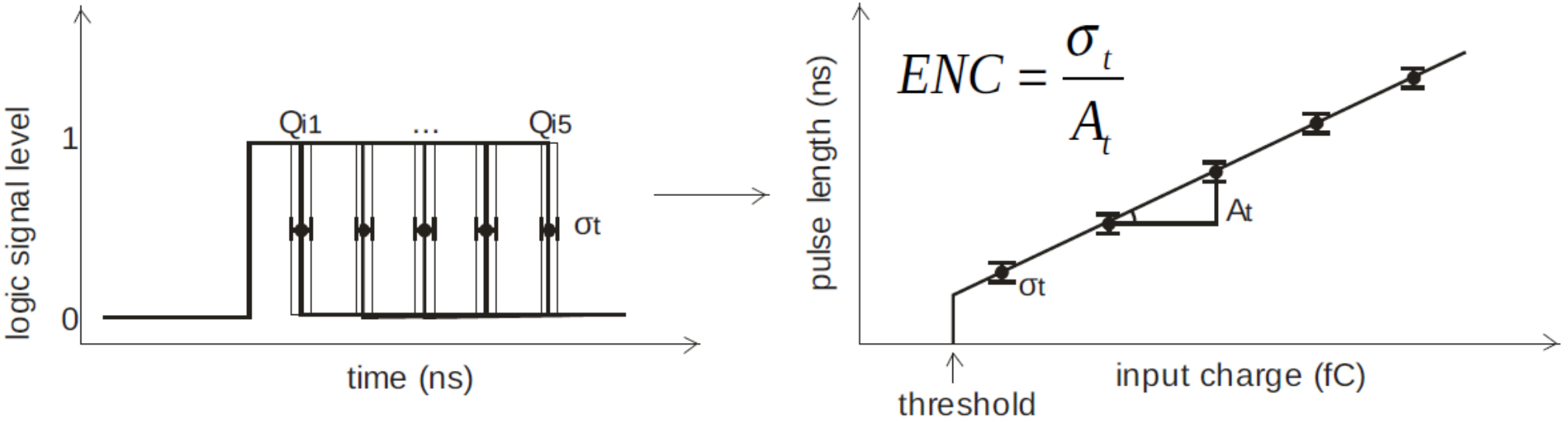


$$ENC = \frac{\sigma_v}{A_v}$$

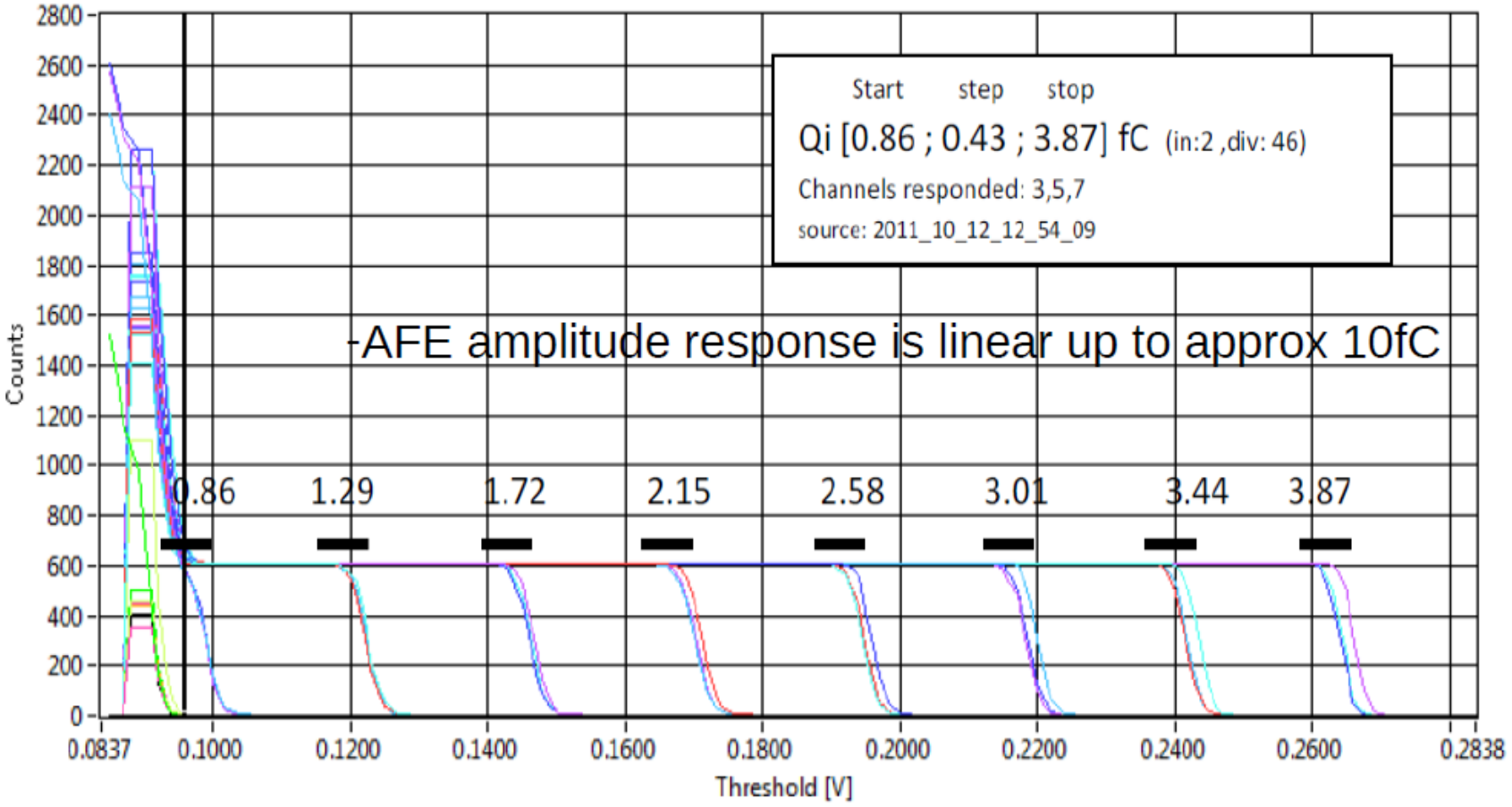


Methodology of characterization TOT SCAN



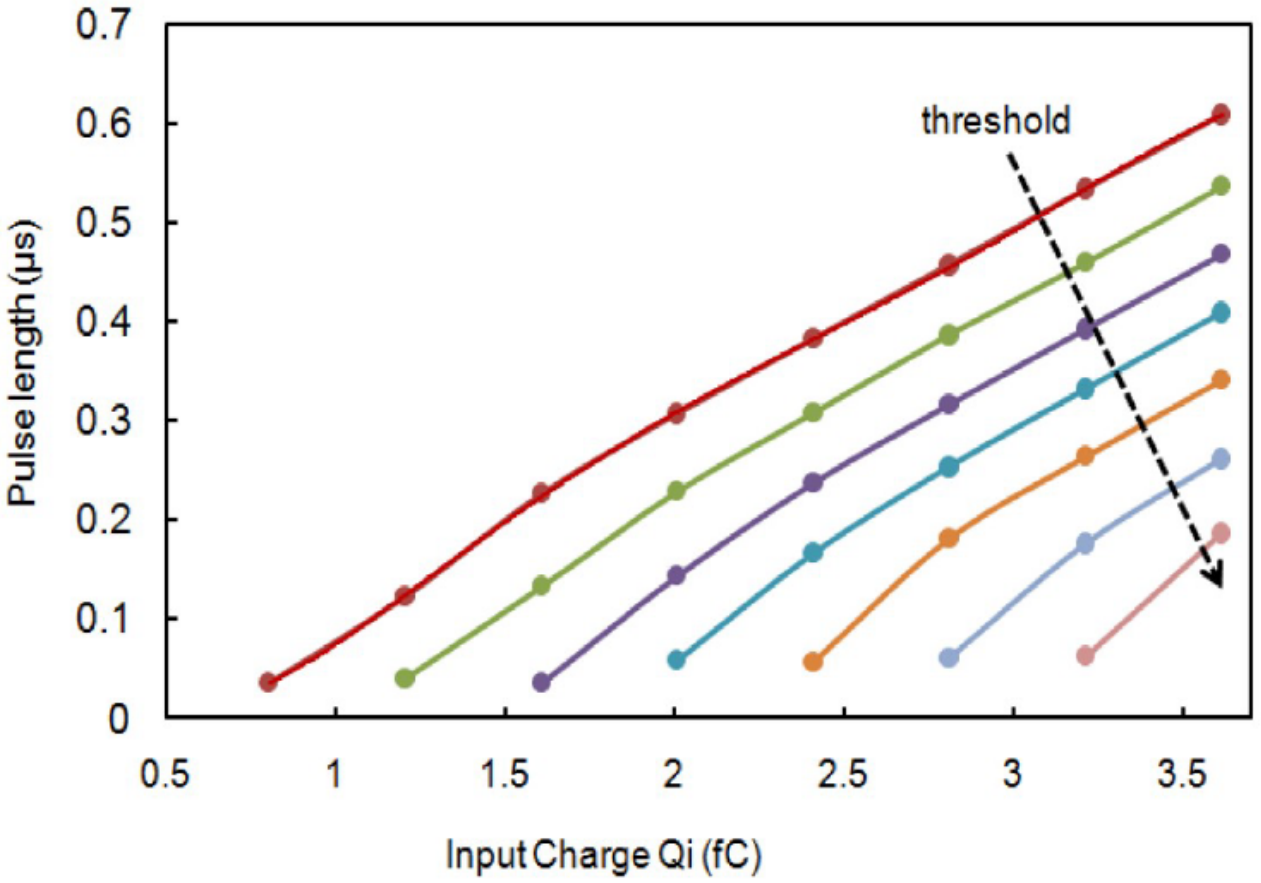


Characteristics – threshold scan

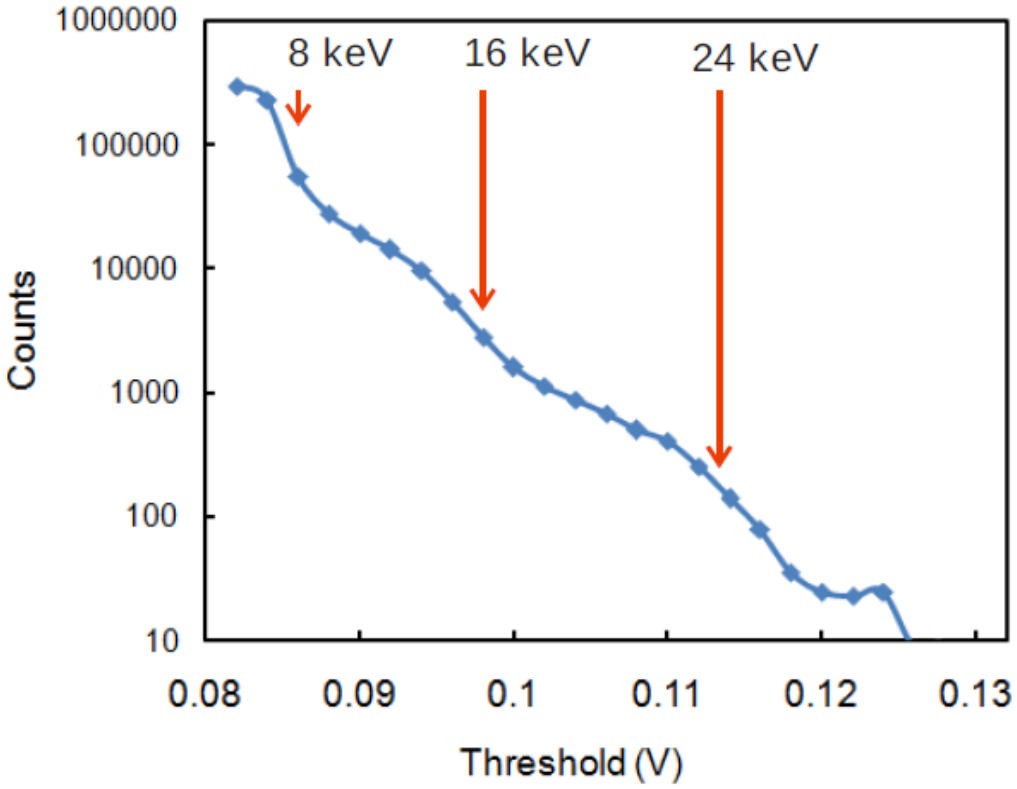


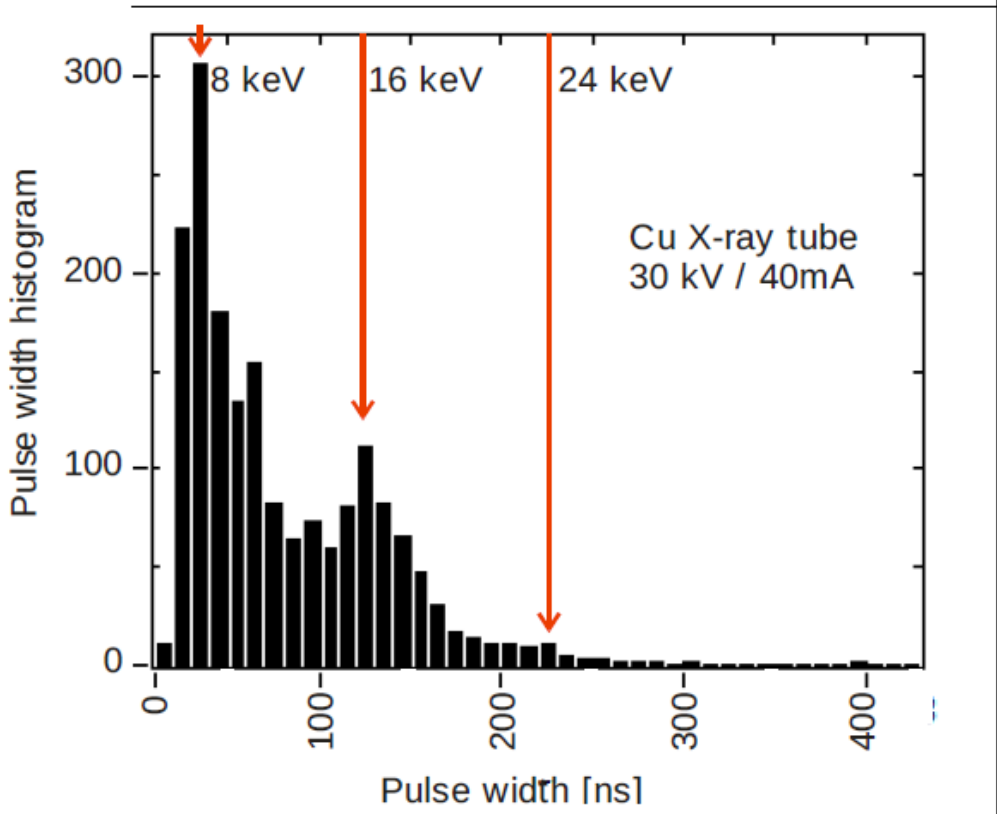
DC offset spread before correction	5.77 mV 654 e-	DC offset spread after correction	< 0.33 mV < 37.4 e-

Characteristics – ToT scan



X-ray irradiation





Tube parameters: Cu, V=40kV, I=40mA

Parameter summary

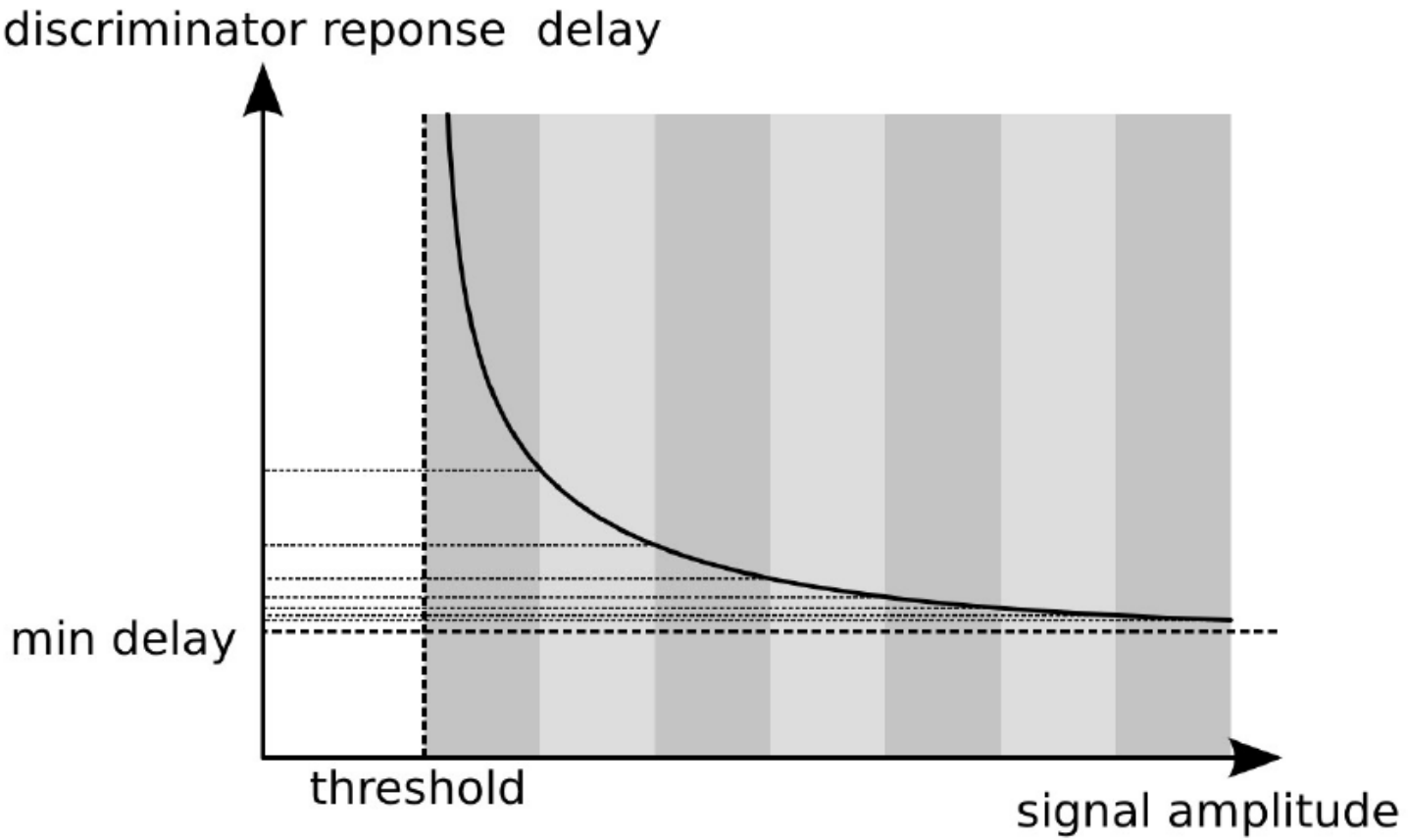
Die parameters			
Technology	UMC 180 nm CMOS	Die size	1.5 mm x 1.5 mm 2.25 mm^2
Number of pads / channels	56 / 16	Channel pitch / length	50 µm / 820 µm
Measured chip performance			
No detector (C_{det}=0pF), ASIC#1		**2cm detector (Cdet=3pF), ASIC#2**	
Voltage gain	=55 mV/fC +-0.36 mV/fC	Voltage gain	=54.7 mV/fC +-0.64 mV/fC
Time gain	=216 ns/fC +-7.54 ns/fC	Time gain	=198 ns/fC +-8.97 ns/fC
$ENC_{thr.scan}$	196 e-	$ENC_{thr.scan}$	240 e-
$ENC_{tot.scan}$	286 e-	$ENC_{tot.scan}$	350 e-
Measured static power consumption			
CSA	1.25 mW	Semi-digital back-end	330 µW
Discriminator + DAC	530 µW	Total (w/o digital back-end)	2.1 mW/channel
Simulated performance of the CSA core (not directly measurable)			
Gain	7000 V/V	Bandwidth	1.3 MHz
GBW	9 GHz		

Noise:

(thr scan)
ENC=196+14.6*Cdet
ENC@30pF = 634 e-

(tot scan)
ENC=286+21.3*Cdet
ENC@30pF = 925 e-

Timewalk



Timewalk dependent on:

- pulse rise time
- discriminator response time (amplitude over threshold, noise)

Pros & cons

Pros:

- infinite dynamic range
- low power consumption
- simple architecture

Cons:

- sensitivity to leakage currents
- pulse length dependant on signal amplitude
- wideband → noise
- timewalk (timestamp precision vs noise)

Proposed architecture of prototype readout ASIC for CBM STS

R. Szczygiel, P. Grybos, K. Kasinski, R. Kleczek

AGH UST Cracow, Poland

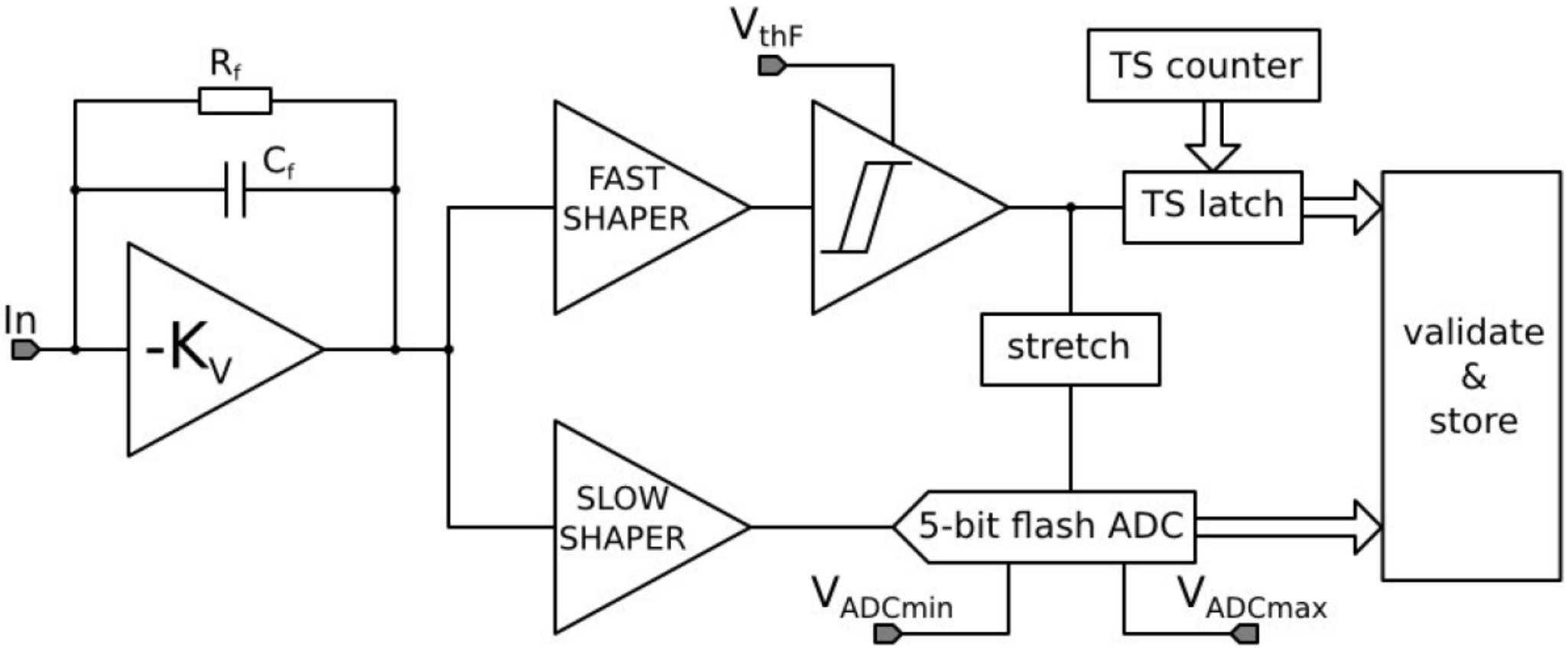
Outline

1. Requirements
2. Front-end architecure
3. Fast and slow channel
4. Time measurement
5. Amplitude measurements
6. Conclusions

STS ASIC working specifications

- 128 channels
- CBMnet backend
- Linear range 1-12 fC (typical input charge = 2 fC)
- Power < 10 mW / channel
- Time measurement < 10 ns resolution
- Detector: DC (AC?), 30 pF total capacitance
- Dual polarity
- Recovery from overload
- Leakage current compensation

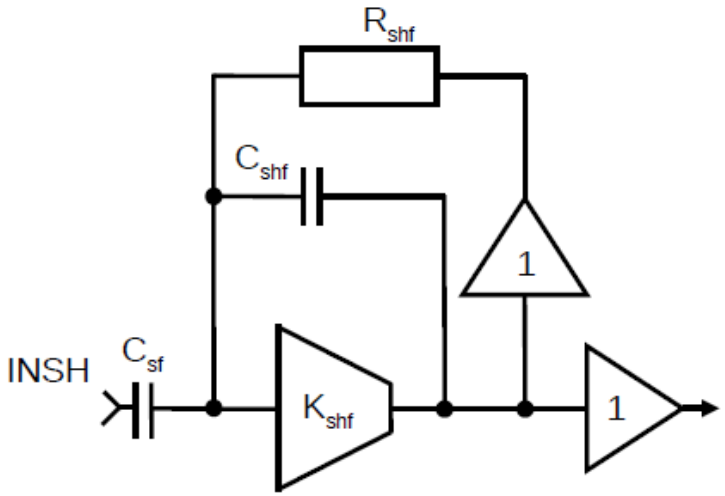
Block diagram of a single channel



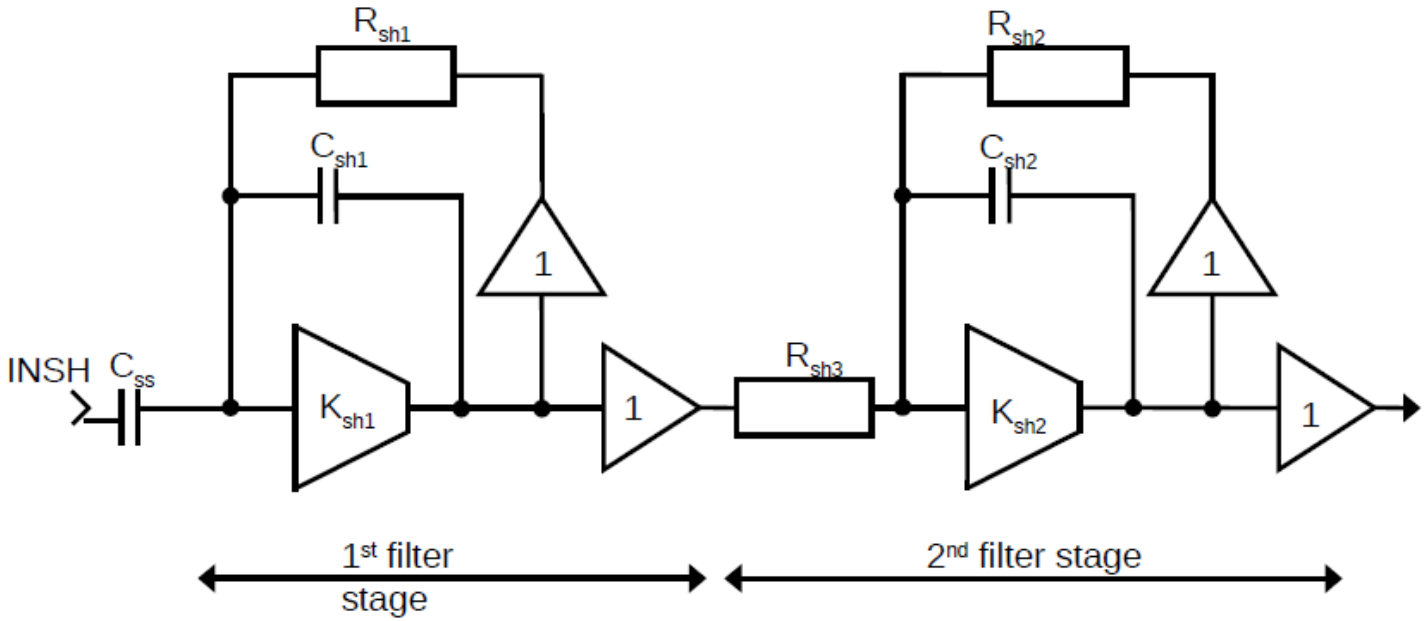
$V_{thF} < V_{ADCmin}$ –> the time measurement is validated by the energy measurement – worst cases dropped

Fast CR-RC and slow CR-$(RC)^2$ shapers

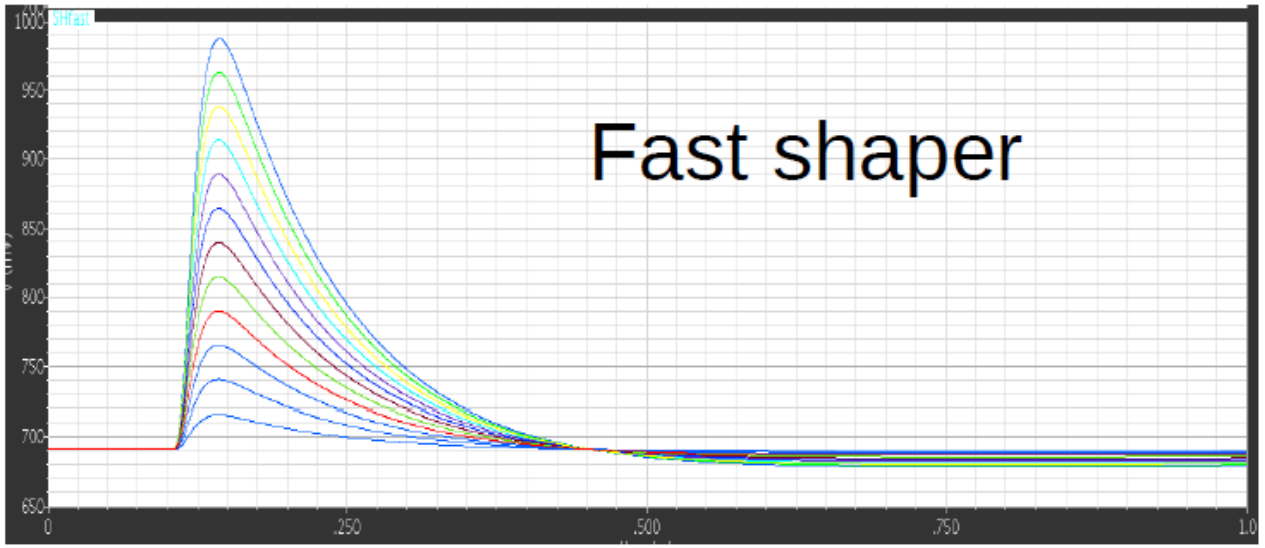
FAST



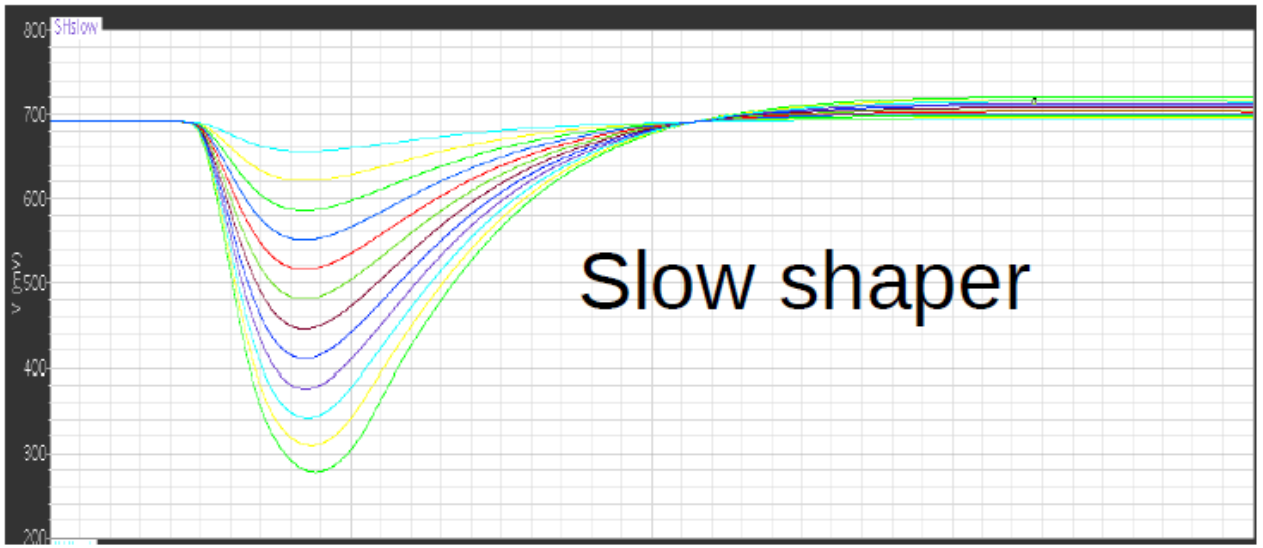
SLOW



Timing and ENC: Qin = 1-12fC, PWR =5.5mW



Tp = 38ns
ENC = 1020 el



Tp = 95ns
ENC = 624 el

Only simulation!!!

Measurements – other groups (UMC180)

NSS CONFERENCE RECORD, 2010 IEEE, KNOXVILLE, USA

SPADIC - A Self-Triggered
Pulse Amplification and Digitization ASIC

Tim Armbruster, Peter Fischer and Ivan Perić

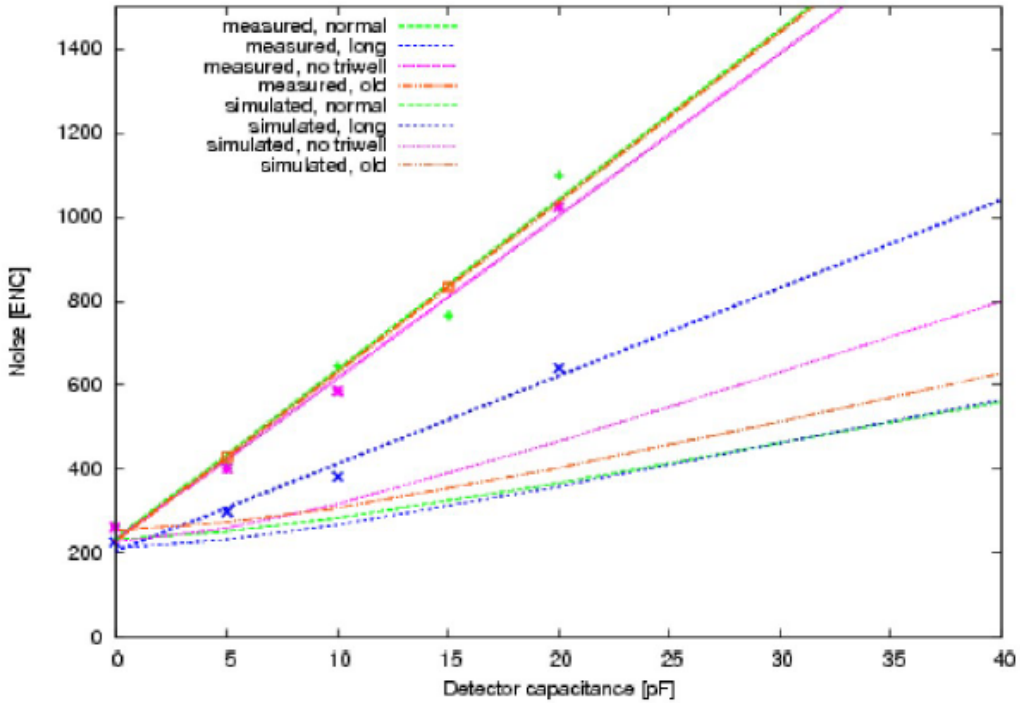


Fig. 7. Preamplifier noise vs. detector capacitance

C. Preamplifier and Shaper

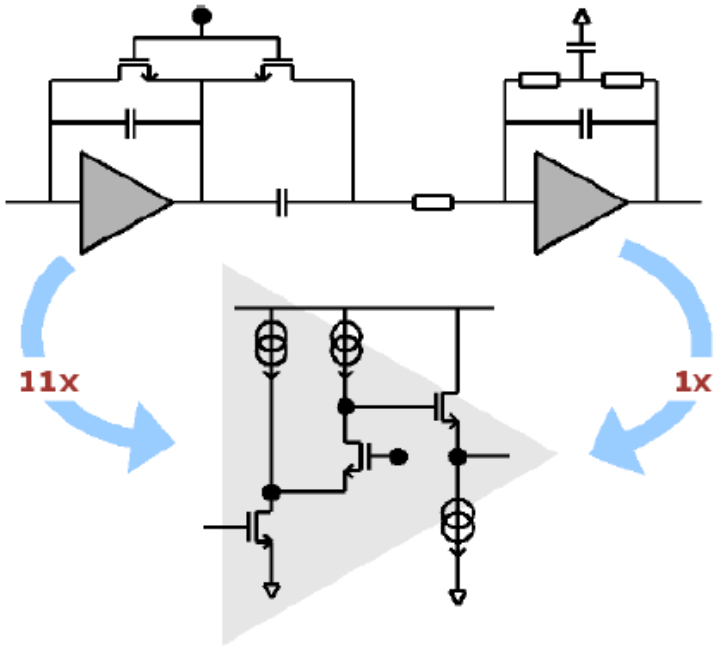
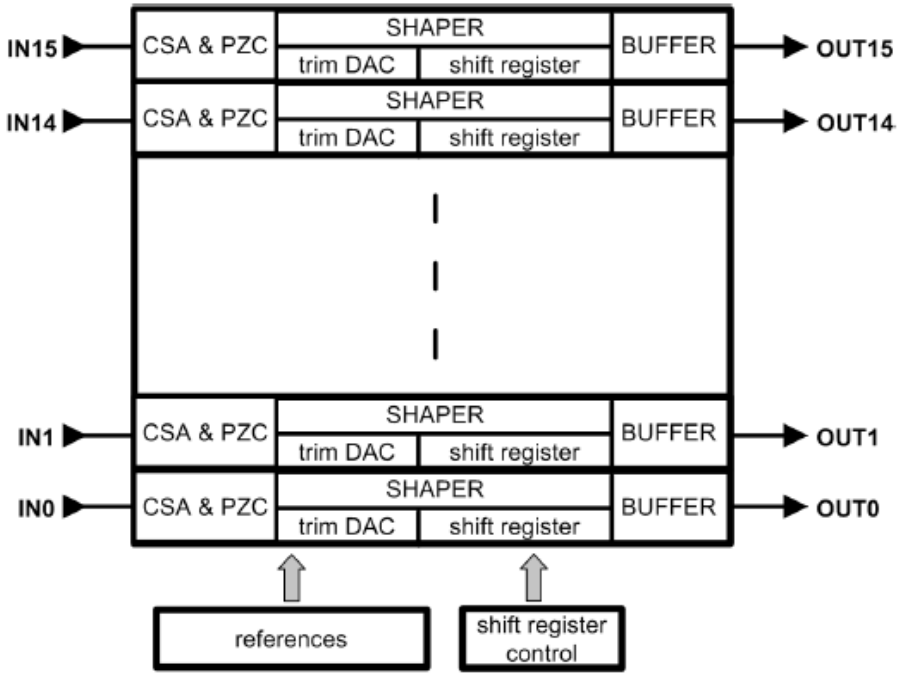
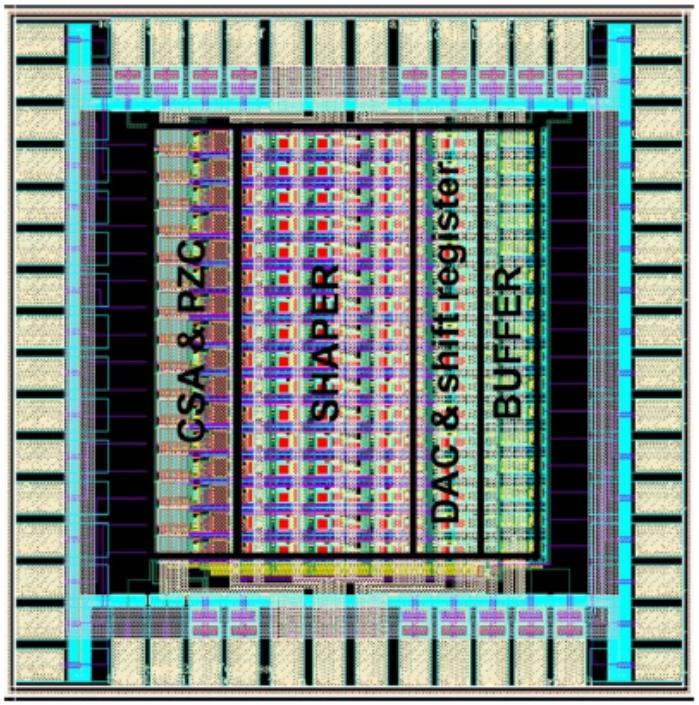


Fig. 4. Simplified preamp/shaper schematic

As sketched (Fig. 4) each amplifier channel basically consists of a single-ended preamplifier with NMOS input and a pole-zero cancellation feedback, a 2nd order T-feedback shaper (82 ns shaping-time) and a comparator (not shown)

Our prototype: FSDR16 chip, tested 2011/2012





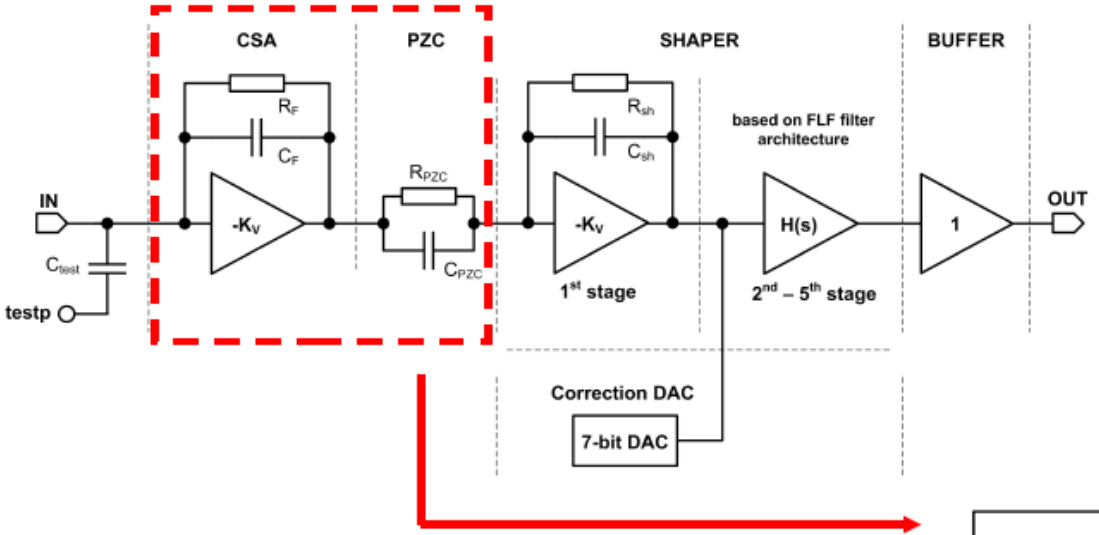
FSDR16 – features:

- implemented in UMC 180nm CMOS,
- dedicated for silicon strip detectors,
- two programmable shaper types which allow to make a comparison between typical CR-$(RC)^5$ shaper based on real poles and a nearly true Gaussian shaper based on complex poles,
- two switchable peaking time tp for each of shaper types

FSDR16 – block diagram:

- contains 16 channels,
- 16 analog inputs, 16 analog outputs,
- single channel is built with an analog (CSA, PZC, shaper) and digital (shift register) part
- DC voltage shaper output spread is corrected by a 7-bit trim DAC separately in ech channel.

FSDR16 – channel and CSA architectures

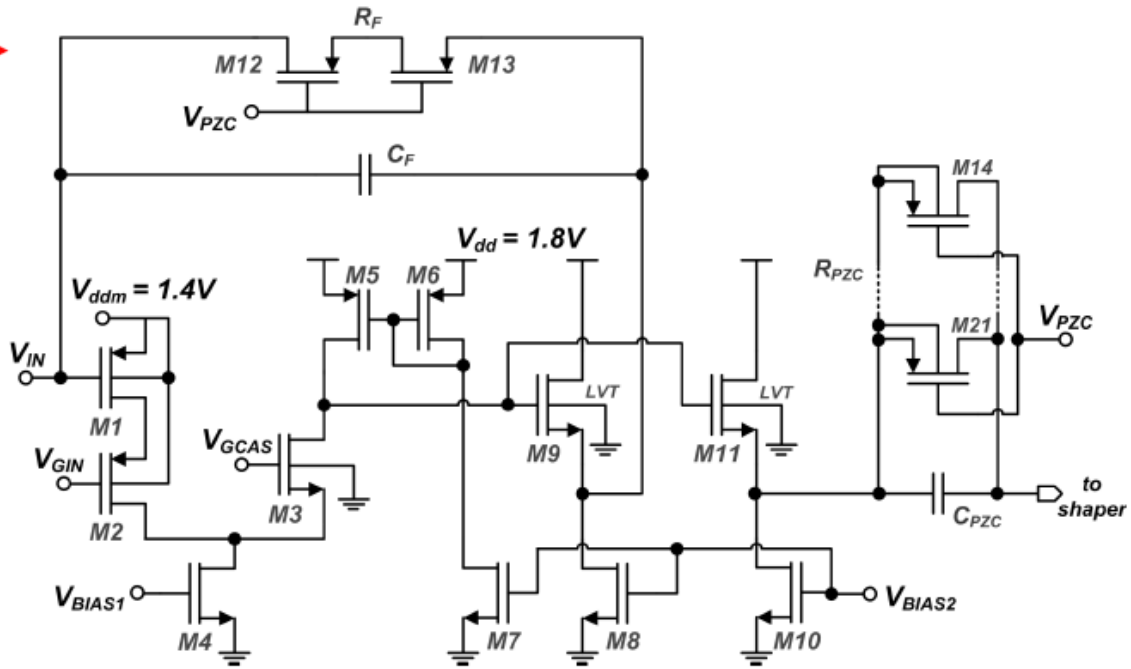


Channel architecture:

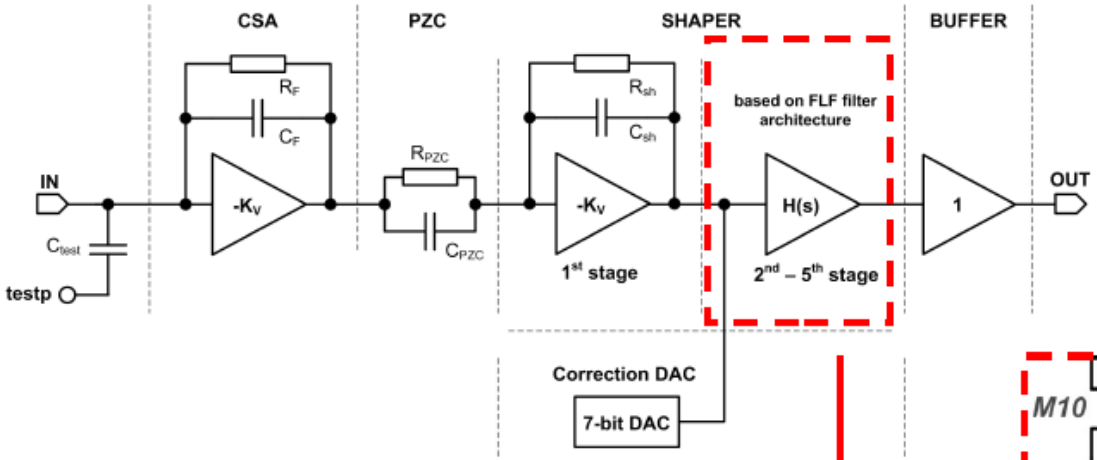
- Charge Sensitive Amplifier ,
- Pole-Zero Cancellation circuit,
- Pulse Shaping Amplifier (two options: CR-$(RC)^5$ or based on complex poles),
- output buffer,
- 7-bit trim DAC,
- 8-bit shift register.

CSA and PZC architectures:

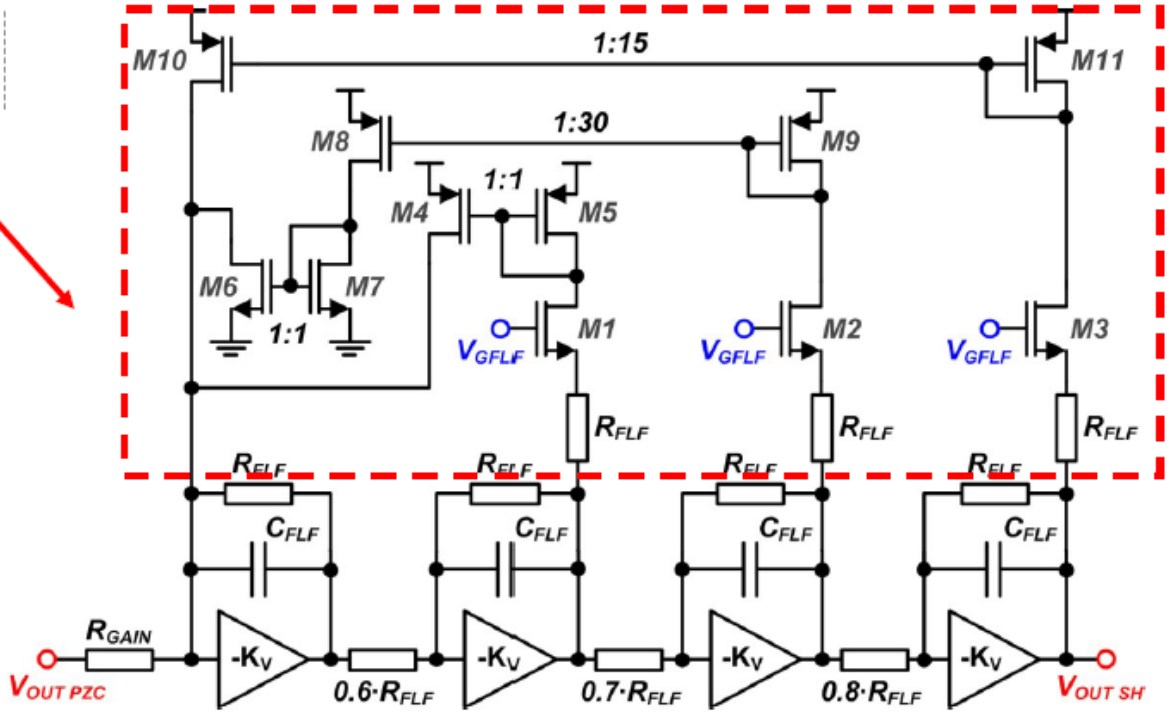
- CSA core: folded cascode architecture,
- input transistor optimized for detector capacitance C_{DET} of about 30pF,
- R_F and R_{PZC} resistors are a MOS transistors working in linear region.



FSDR16: shaper architecture, 5th , complex poles



The two complex conjugated poles pairs are obtained by the usage of the 4th order FLF architecture, based on the same single pole core – $R_{FLF} \cdot C_{FLF}$ time constatnt. The used feedback was realized as a weighted current sources.



Shaper architecture:

- shaper core: folded cascode architecture,
- when the feedback structure is turned on, the nearly true Gaussian filter based on complex poles is on,
- when the feedback structure is turned off, the typical CR-$(RC)^5$ filter is on.

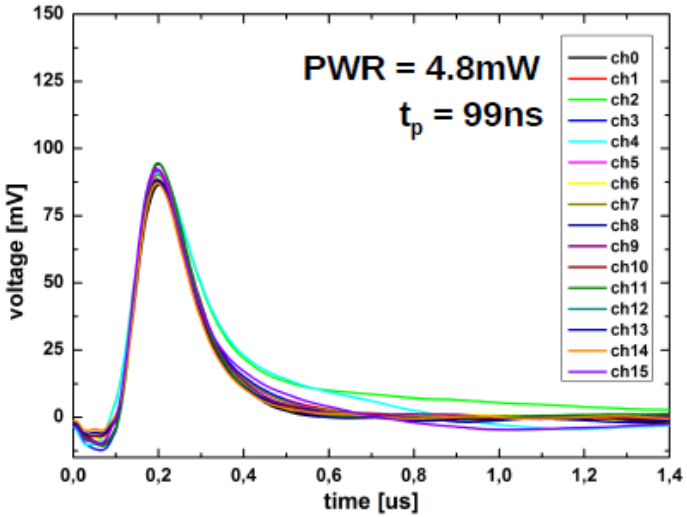
FSDR16 – measurements

waveforms for input charge q_{in}=1fC without attached detector

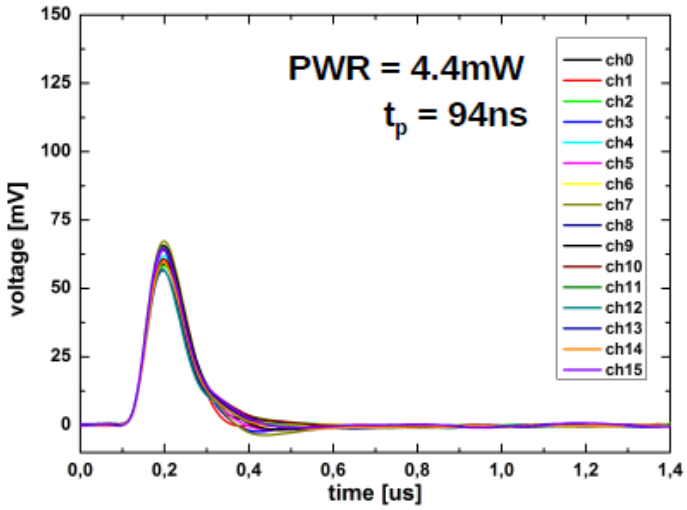
fast mode

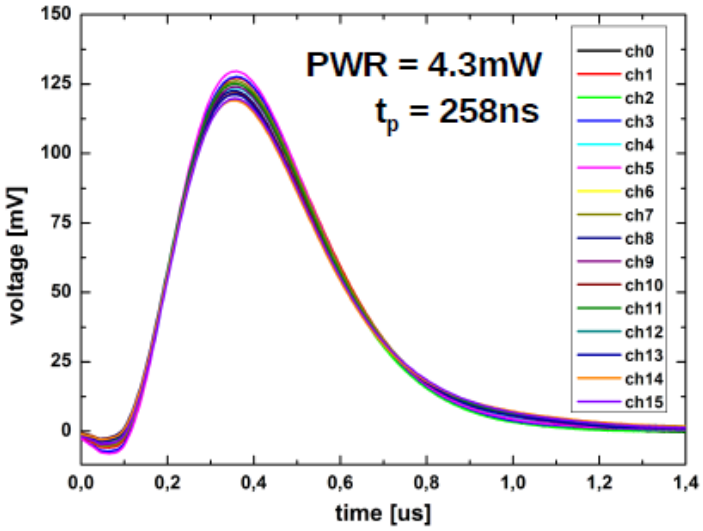
slow mode

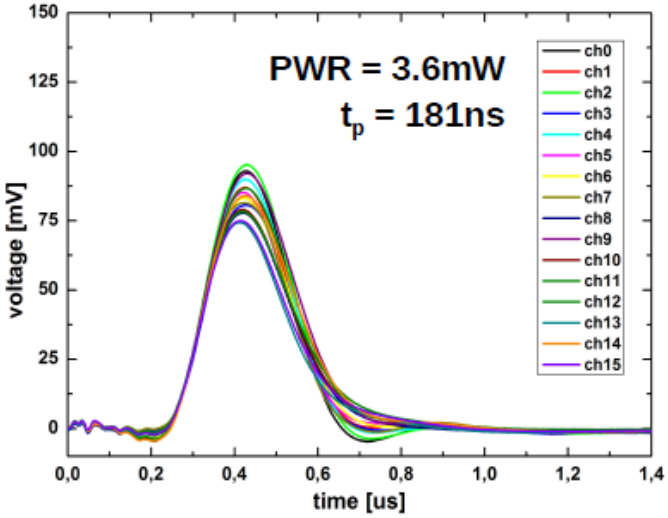
CR-(RC)^5 shaper
based on real poles



nearly true Gaussian shaper
based on complex poles







FSDR16 – measurements results

DC voltage, gain, peaking time t_p, pulse width t_w / peaking time t_p ratio measurement results

	DC voltage [mV]	spread [mV]	gain [mV/fC]	spread [mV/fC]	t_p [ns]	spread [ns]	t_w / t_p	spread
Complex fast	523	3	62	3.4	94	2.7	3.5	0.6
Complex slow	518	5.9	85	6.4	181	5.8	2.96	0.57
CR-(RC)^5 fast	522	2.1	91	2.6	99	7.9	5.32	0,75
CR-(RC)^5 slow	521	1.5	124	2.8	258	5.1	4.6	1.74

CR-(RC)^5 shaper:

fast mode: ENC = 214el + 13.3el/pF · C_{DET}

slow mode: ENC = 153el + 12el/pF · C_{DET}

Nearly true Gaussian shaper

fast mode: ENC = 246el + 23.7el/pF · C_{DET}

slow mode: ENC = 176el + 16.7el/pF · C_{DET}

ENC - measurements

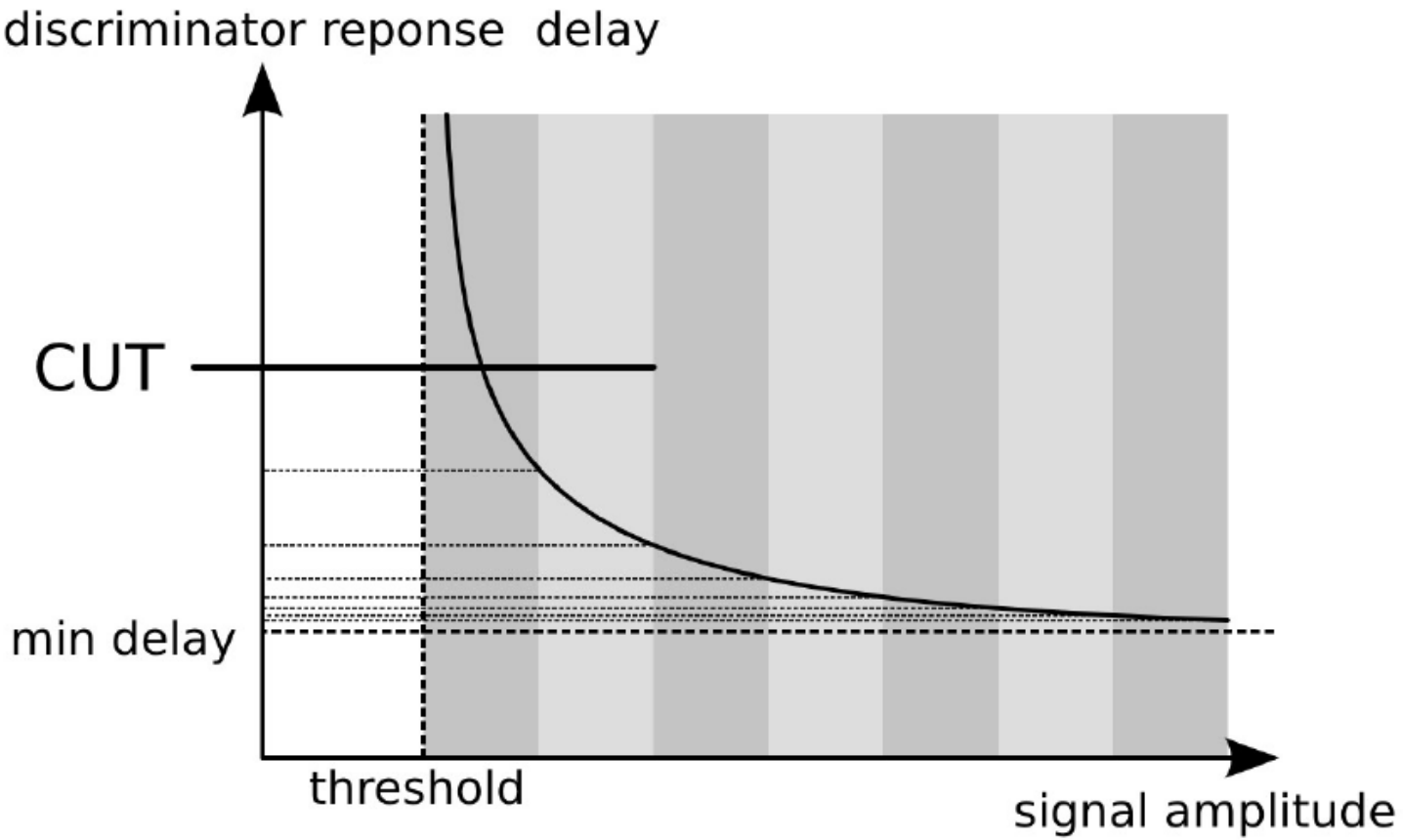
	ENC [e^-]	spread [e^-]	ENC at C_{DET}=3pF [e^-]	spread [e^-]	ENC at C_{DET}=30pF [e^-]
Complex fast	246	6.9	317	14.4	956
Complex slow	176	11.3	226	11.2	676
CR-(RC)^5 fast	214	5.3	254	5.3	614
CR-(RC)^5 slow	153	3.4	189	2.5	513

ENC - estimation

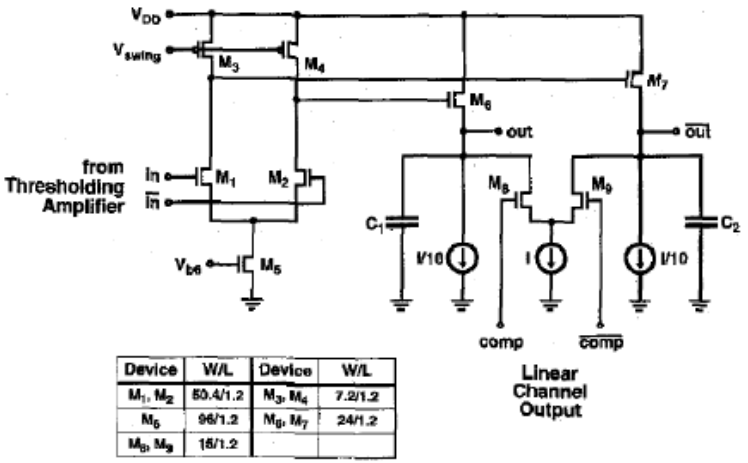
Shaper is very complex!

Time measurement : option 1

Fast shaping time and later validation using ADC value



Time walk compensation – option 2

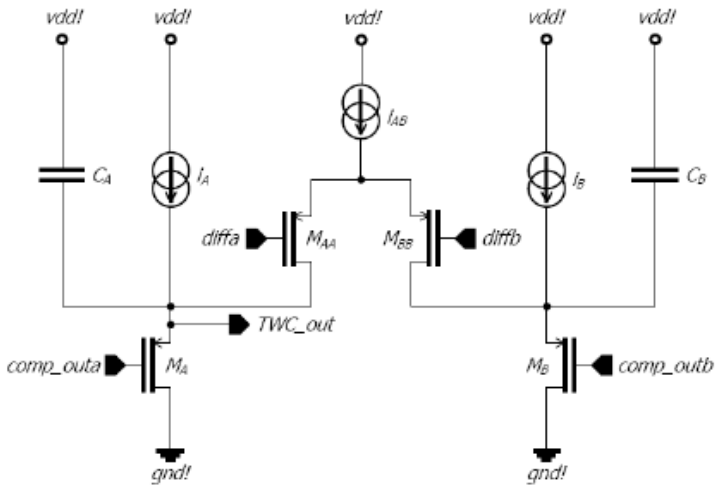


Device	W/L	Device	W/L
M_1, M_2	50.4/1.2	M_3, M_4	7.2/1.2
M_5	96/1.2	M_6, M_7	24/1.2
M_8, M_9	18/1.2		

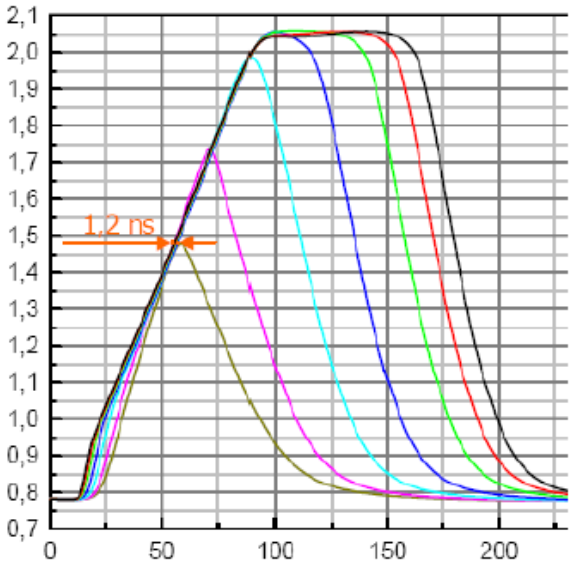
Fig. 12. Time walk compensation circuit. $I_{DS}(M_5) = 70\ \mu A$, $I = 100\ \mu A$, $C_1 = C_2 = 0.1$ pF.

A CMOS Multichannel IC for Pulse Timing Measurements with 1-mV Sensitivity

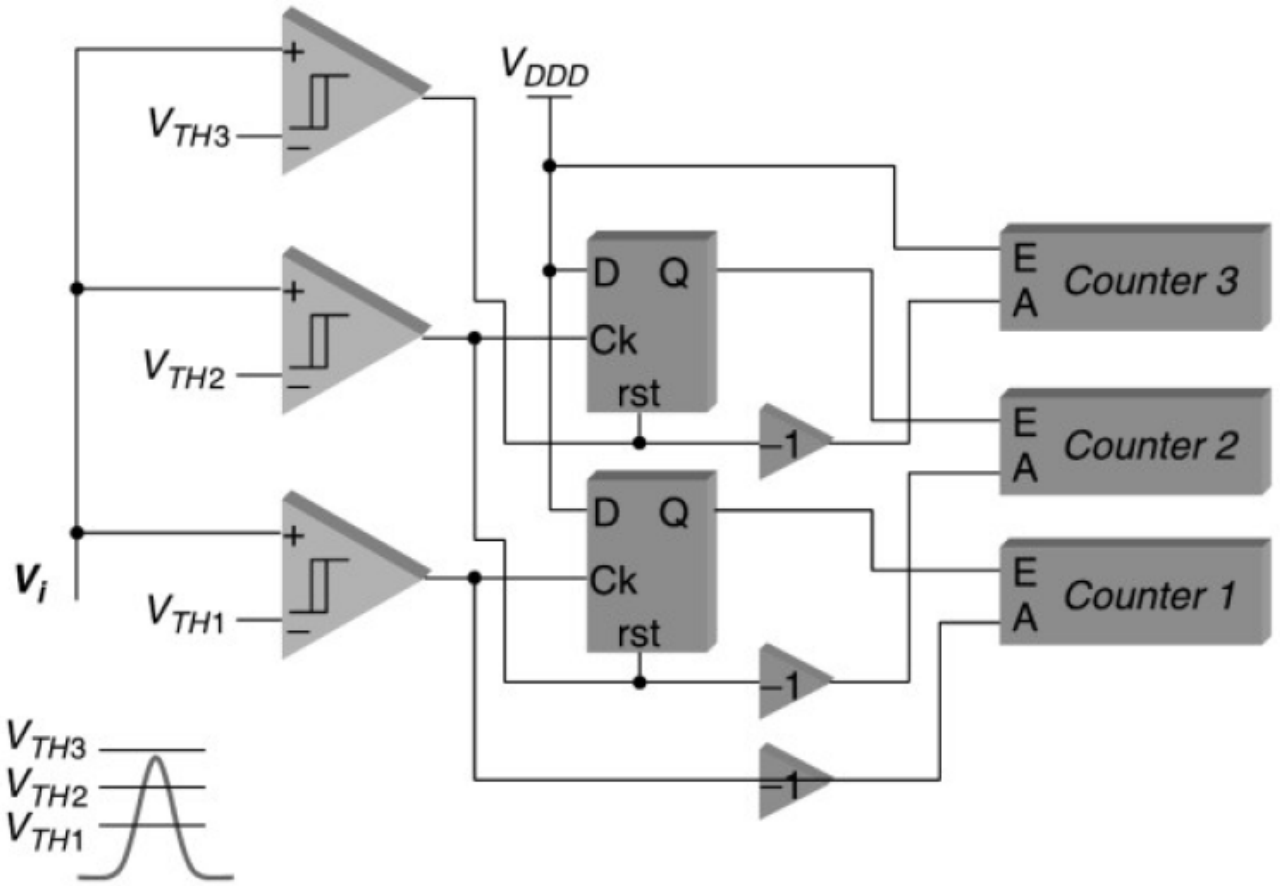
Marc J. Loinaz, *Student Member, IEEE*, and Bruce A. Wooley, *Fellow, IEEE*



PhD – T. Fiutowski

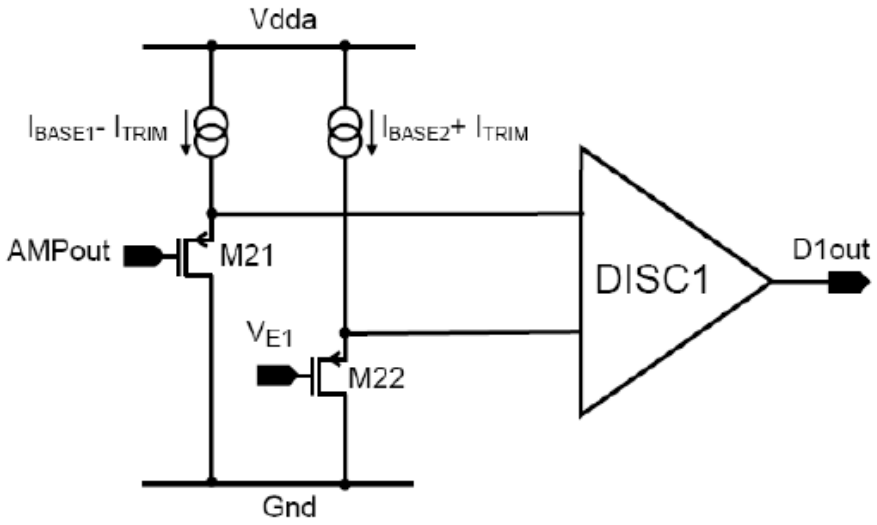


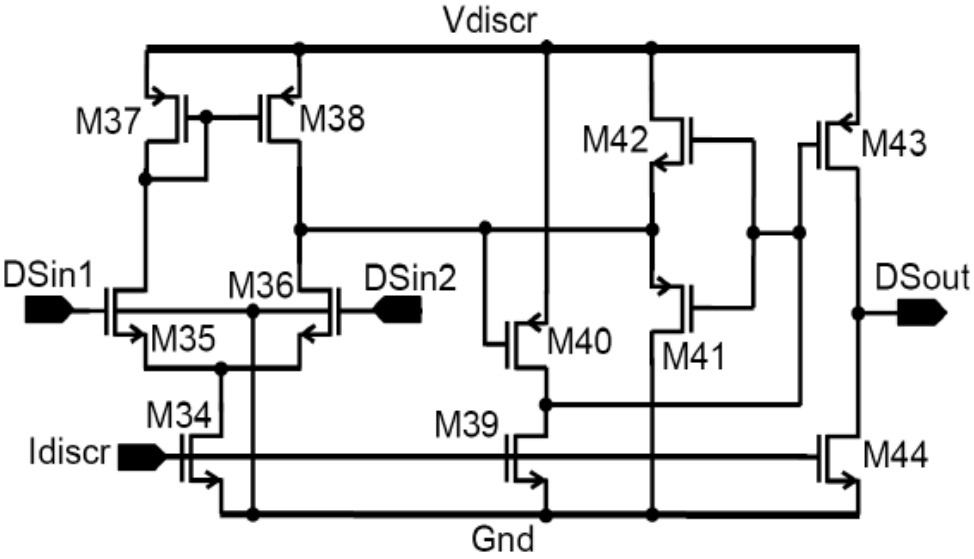
Energy measurements: 5-bit flash ADC



Small discriminator

Option 1: discriminator with trimming





Area: 20 x 50 um^2

(40 x 50 um^2 with register)

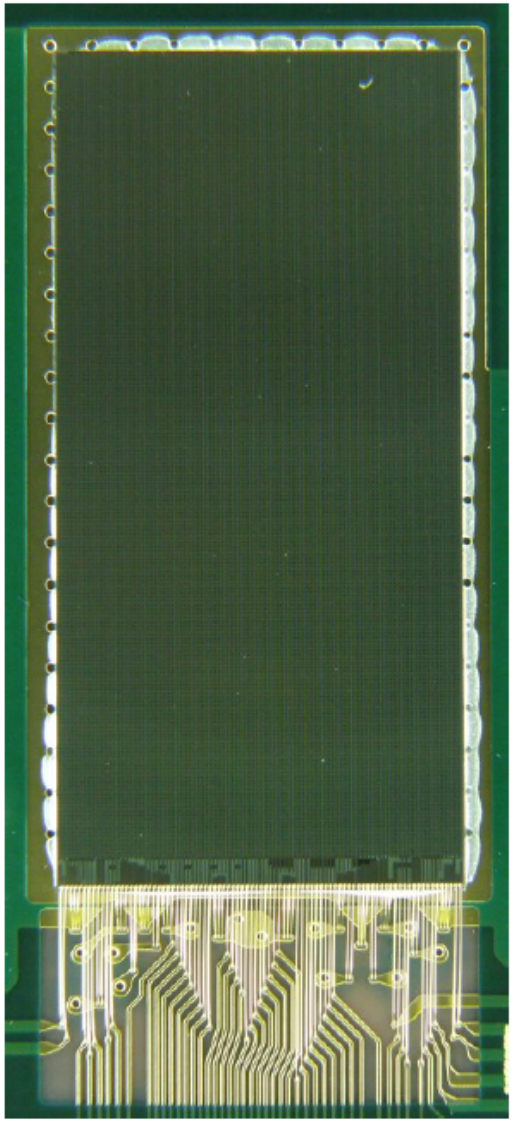
PWR: 10 – 20 uW

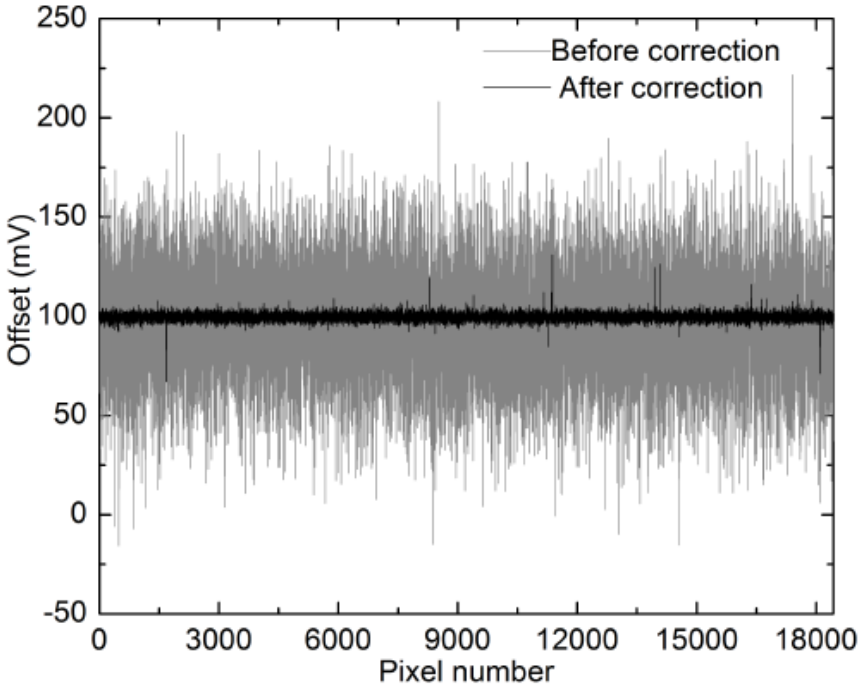
Option 2: discriminator with automatic offset cancellation

Triming DAC is necessary – see PXD18k chip (UMC180nm)

PXD18k – Fast Single Photon Counting Chip with Energy Window for Hybrid Pixel Detector

R. Szczygiel, P. Grybos *Member IEEE*, P. Maj, M. Zoladz





Results:

- before correction: sd = 15 mV

- 7-bit trim: sd = 0.76 mV

- 6-bit trim: sd = 1.19 mV

Trimming procedure: 40s

Conclusions

- Separated channels for time and amplitude measurements – independent optimization for timestamp precision and noise
- Expected better noise than ToT
- Expected better timing precision than ToT
- Needs more power than ToT
- Possible time measurement correction using ADC value
- Most components of well known architecture (CSA, shapers, discriminators, trimming DACs)

- Deadline: July 2012

Requirements

- some parameters depend each other:
  - hit rate → dead time, data link, buffer
  - digitization resolution → point resolution, PID
  - time resolution → event building
  - power consumption → cooling
  - supply → cabling effort

Requirements

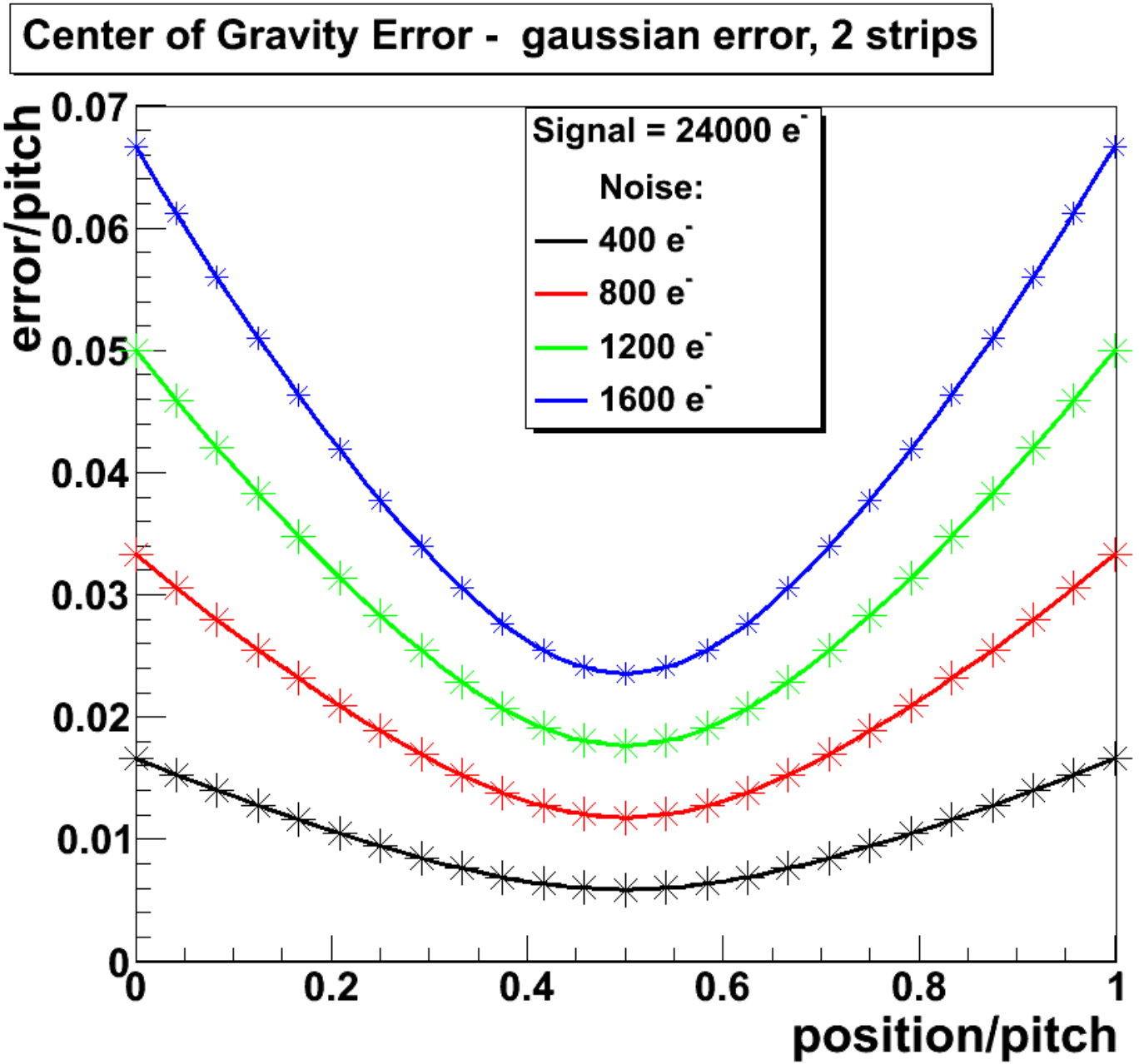
- radiation hardness, SEU mitigation
  → technology
- detector capacitance → noise
- shaping time → noise, dead time
- linearity → energy resolution
- dimension, pad layout → stave layout

Digitization Resolution

- important parameter for:
  - spatial resolution through clustering
  - PID through energy loss measurement

→ spatial resolution limited by noise

(as shown below)


Center of Gravity Error - gaussian error, 2 strips
Signal = 24000 e-
Noise:
400 e-
800 e-
1200 e-
1600 e-
error/pitch
0.07
0.06
0.05
0.04
0.03
0.02
0.01
0
0
0.2
0.4
0.6
0.8
1
position/pitch

Digitization Resolution

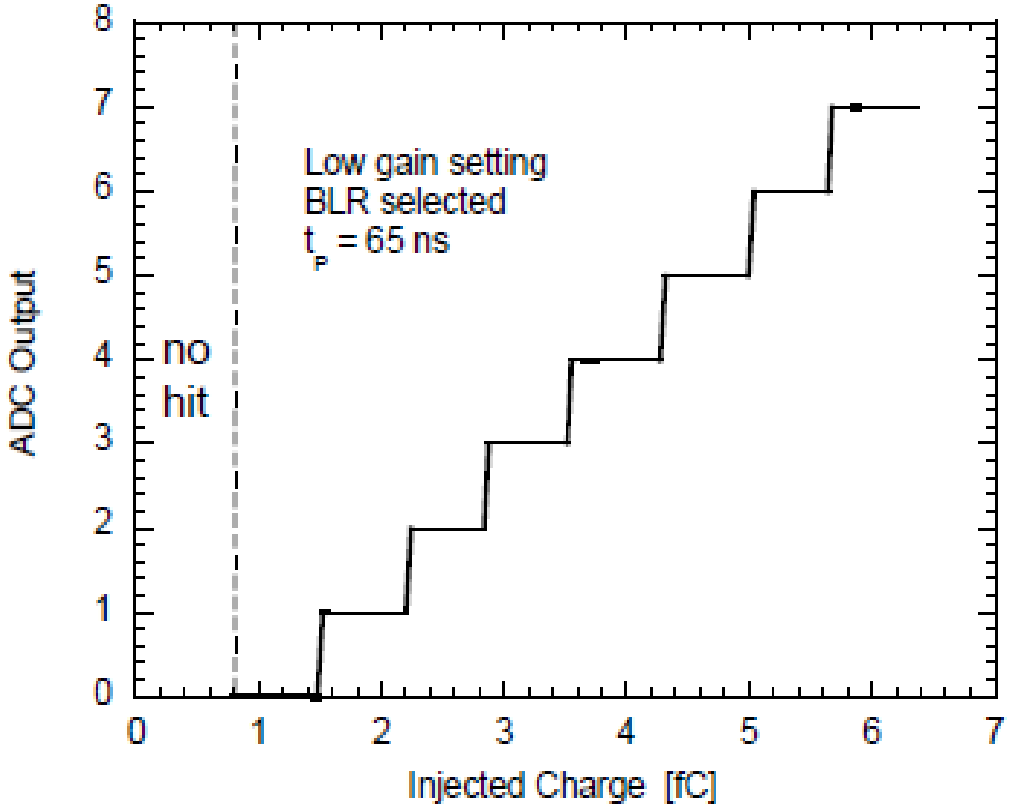
- central question:

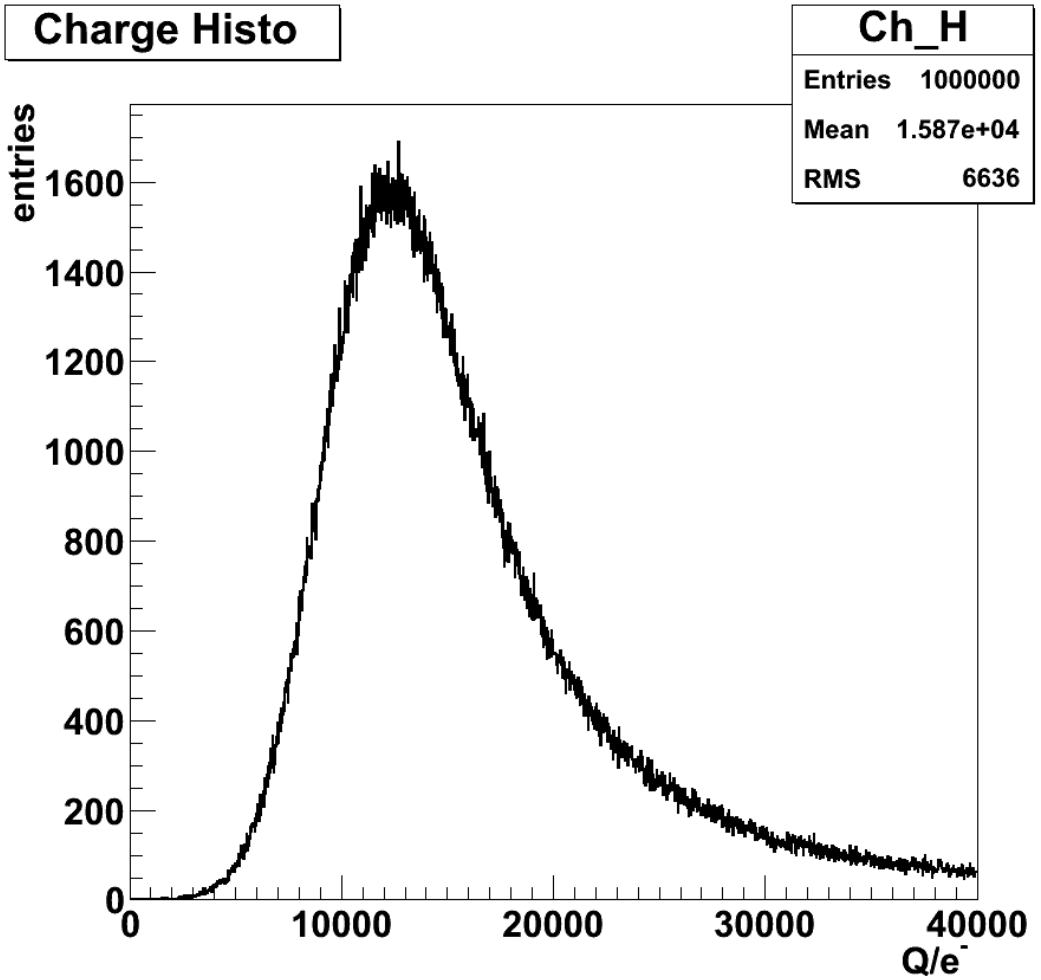
  How many bits of digitization resolution required?

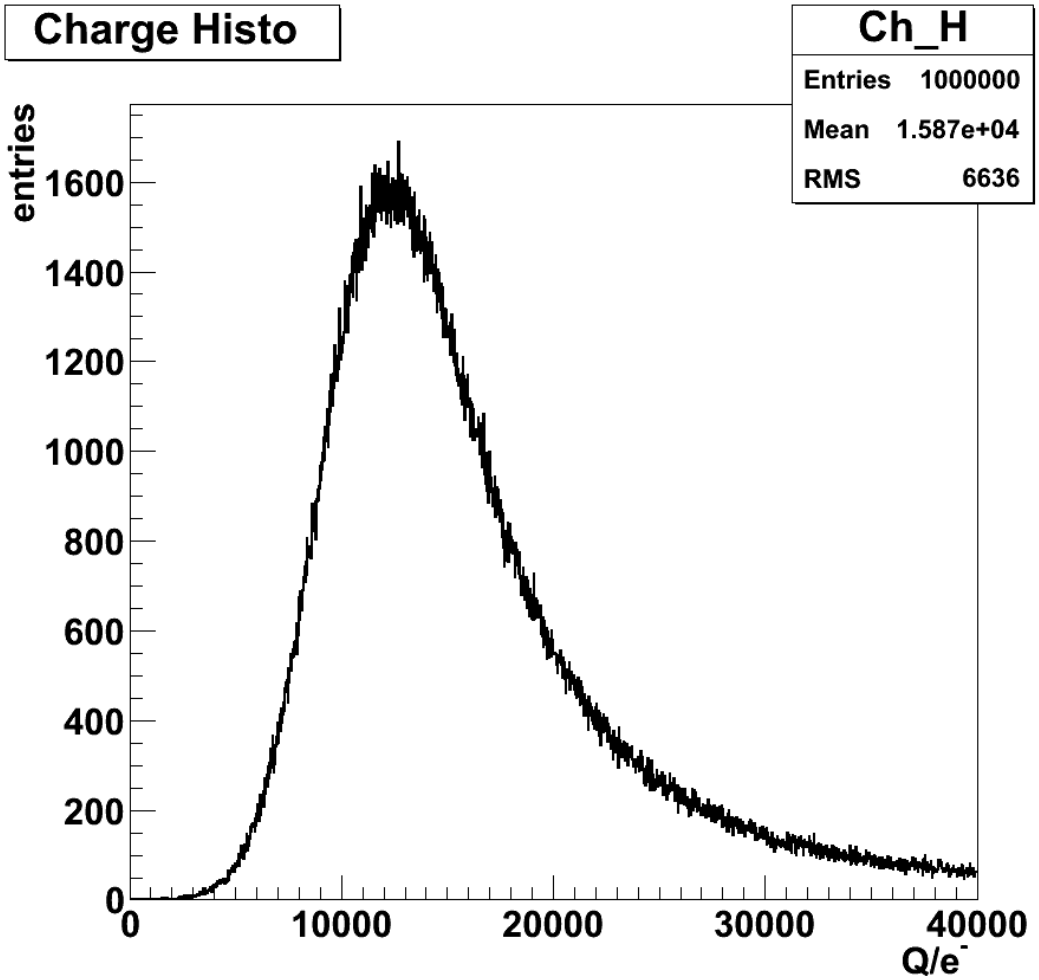
  - contributes to amount of data
  - provoke more power consumption

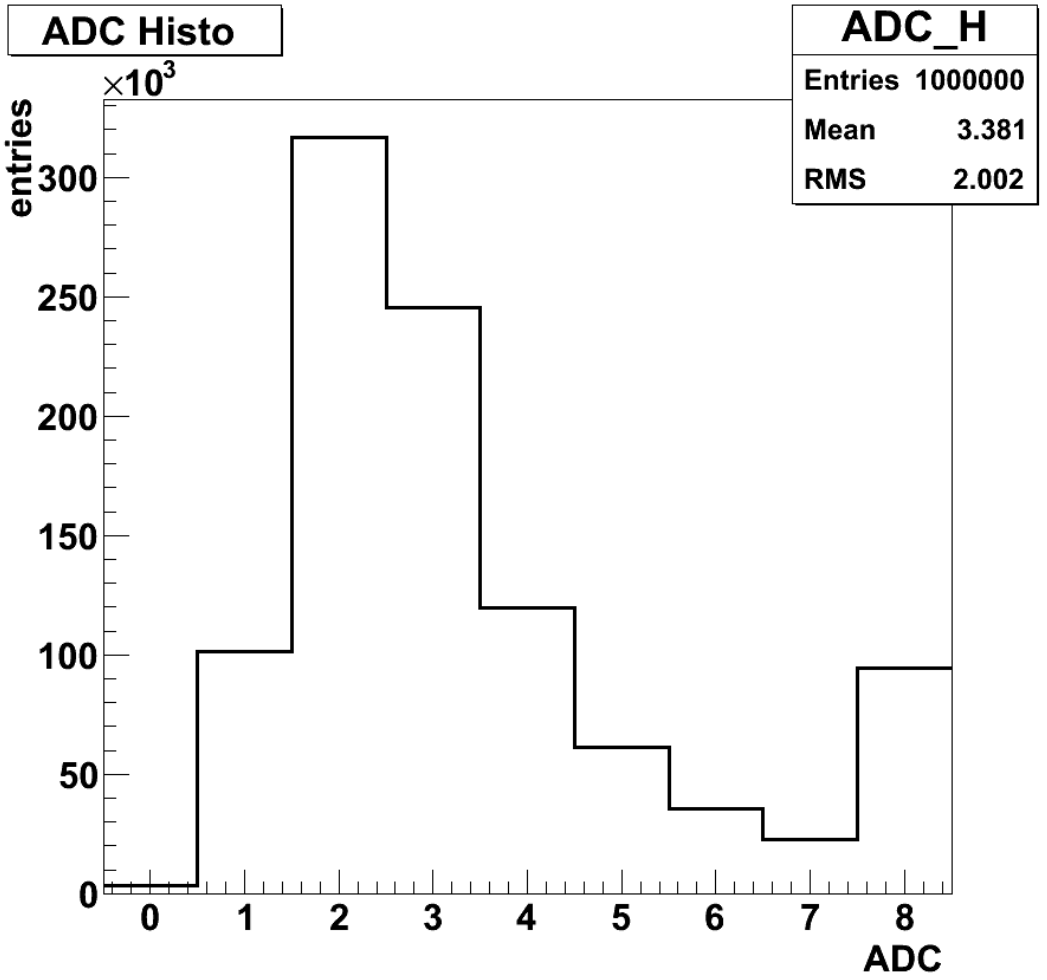
- Example: FSSR2 digitization centered around 1 MIP

(2005 IEEE Nuclear Science Symposium Conference Record)

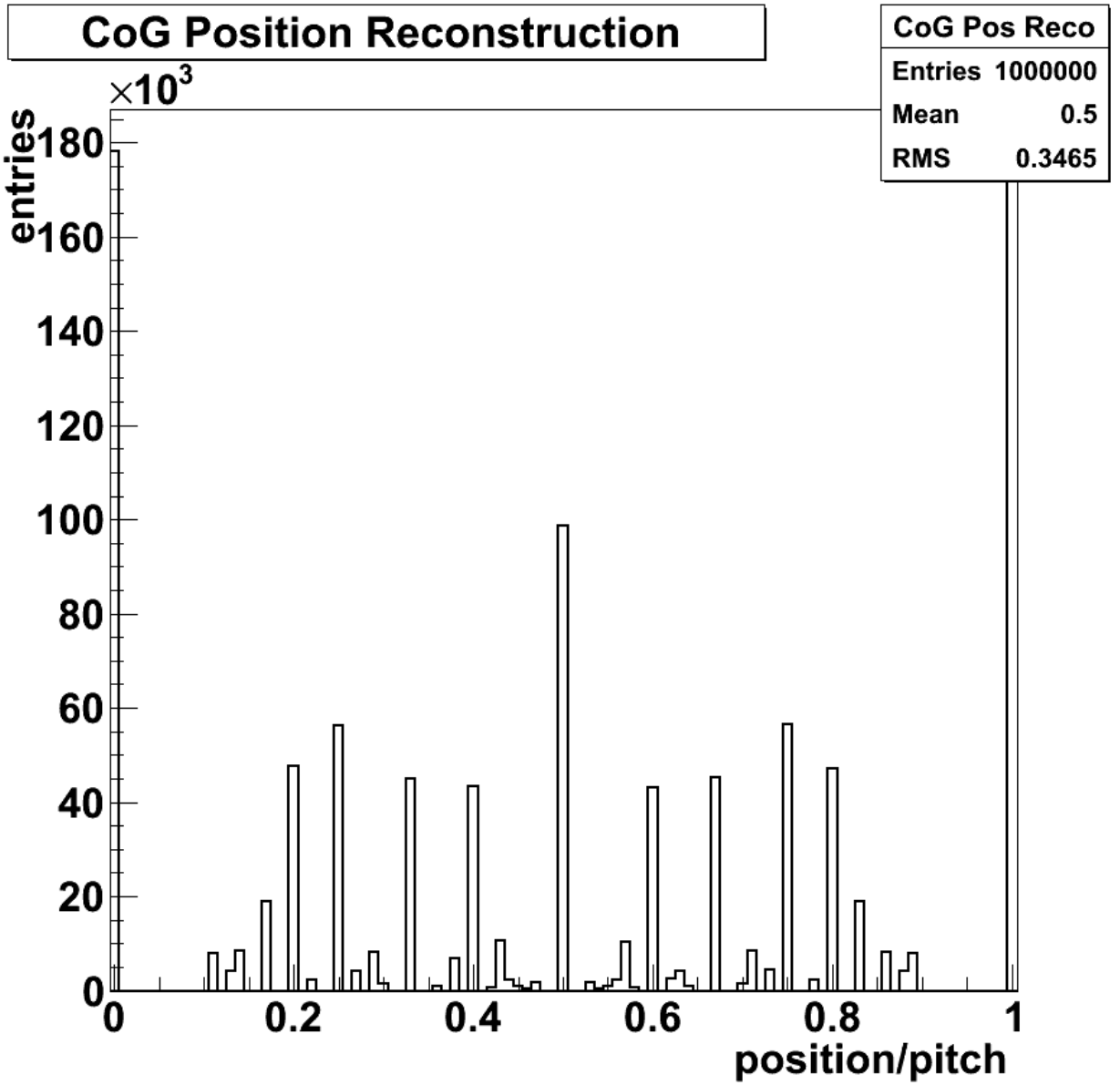



Charge Histo
Ch_H
Entries 1000000
Mean 1.587e+04
RMS 6636
entries
1600
1400
1200
1000
800
600
400
200
0
0
10000
20000
30000
40000
Q/e-

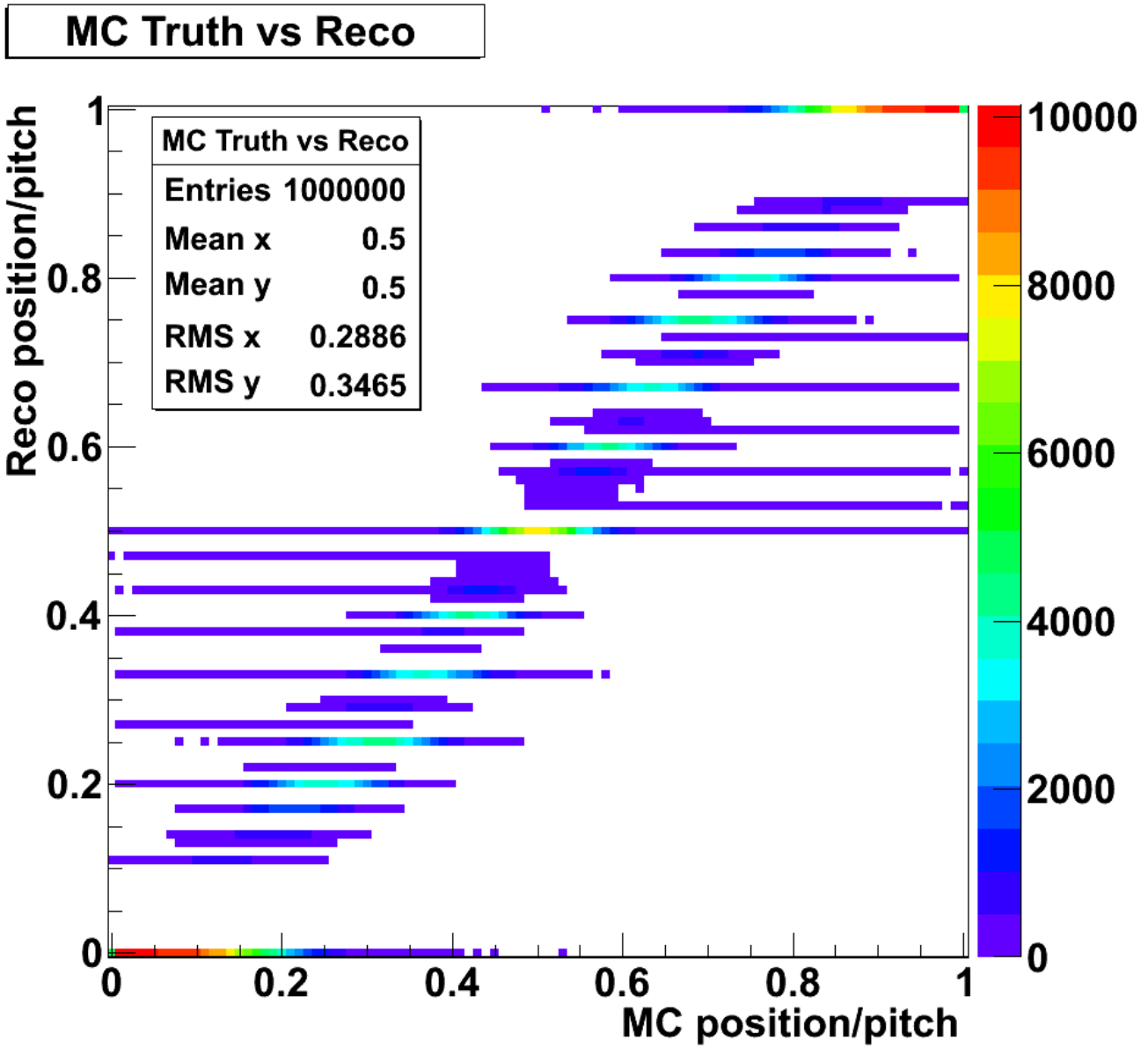

Charge Histo
Ch_H
Entries 1000000
Mean 1.587e+04
RMS 6636
entries
1600
1400
1200
1000
800
600
400
200
0
0
10000
20000
30000
40000
Q/e-


ADC Histo
ADC_H
Entries 1000000
Mean 3.381
RMS 2.002
×10^3
entries
300
250
200
150
100
50
0
0
1
2
3
4
5
6
7
8
ADC

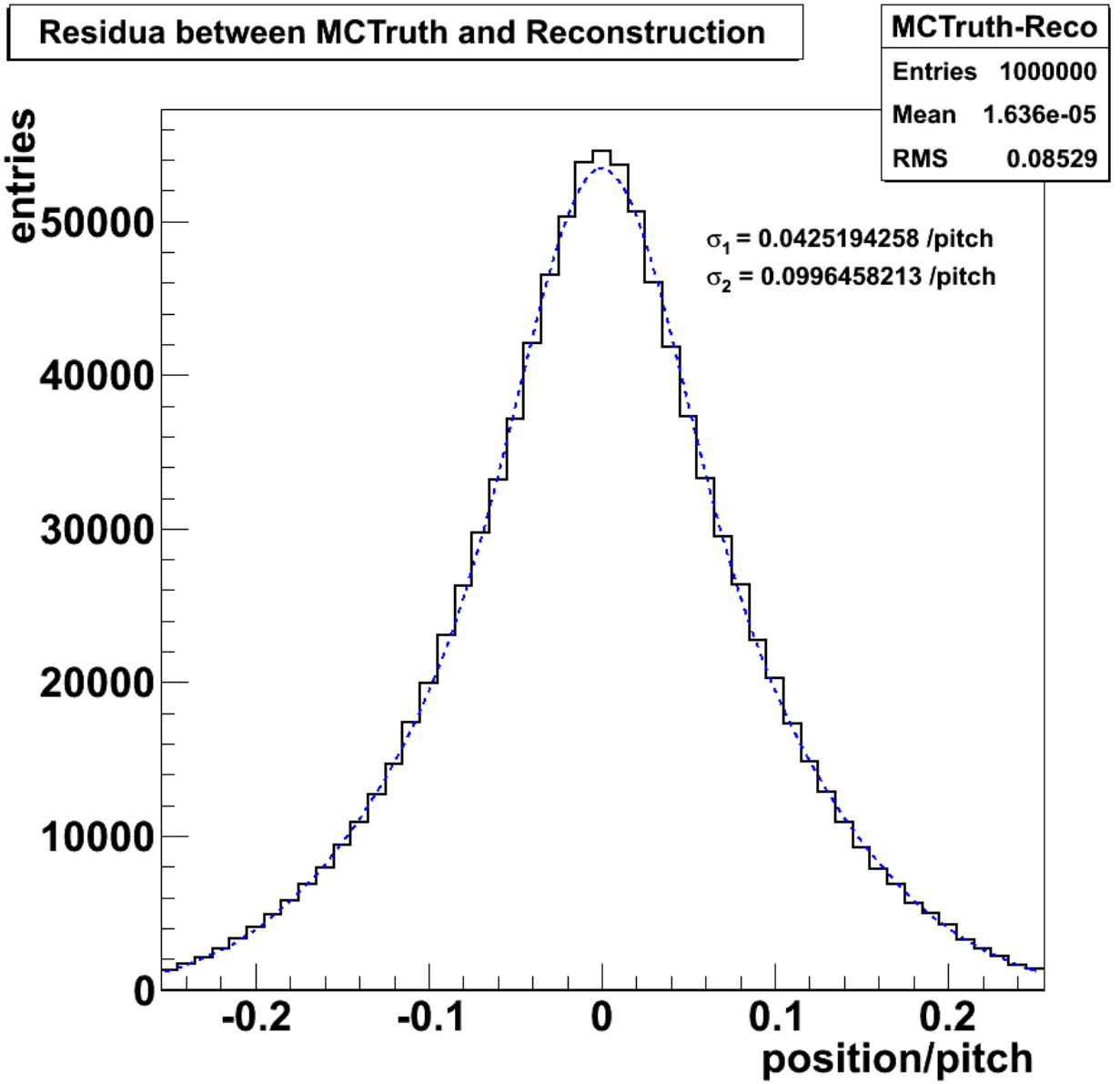
Simulation:
- 2 strip hit
- FSSR2 digi – 3 bit
- hit threshold = 5.000 e^-
- landau distributed signal
- signal = 24.000 e^-
- noise sigma = 800 e^-
- clustering: Center of Gravity



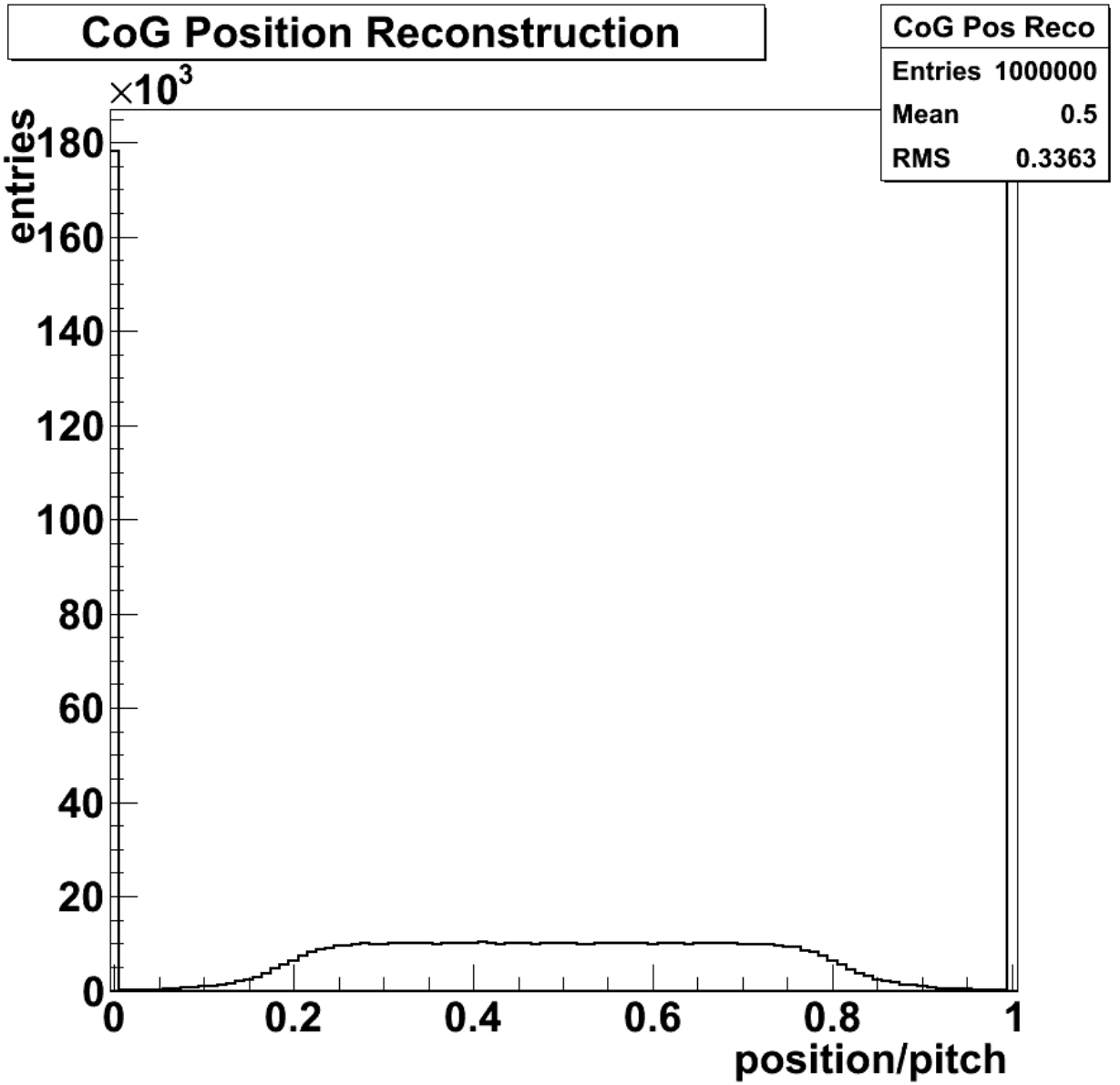
Simulation:
- 2 strip hit
- FSSR2 digi – 3 bit
- hit threshold = 5.000 e^-
- landau distributed signal
- signal = 24.000 e^-
- noise sigma = 800 e^-
- clustering: Center of Gravity



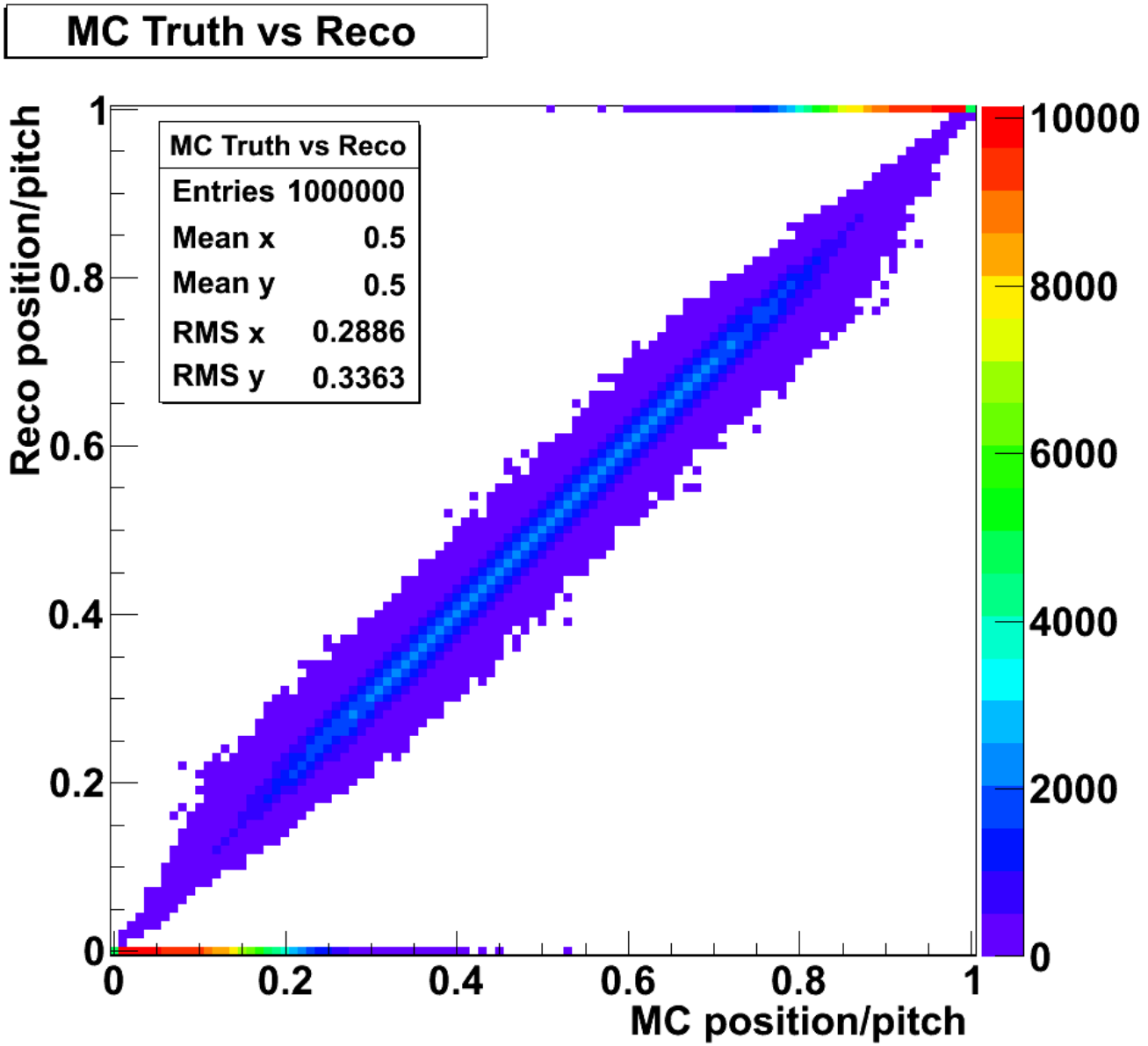
Simulation:
- 2 strip hit
- FSSR2 digi – 3 bit
- hit threshold = 5.000 e^-
- landau distributed signal
- signal = 24.000 e^-
- noise sigma = 800 e^-
- clustering: Center of Gravity



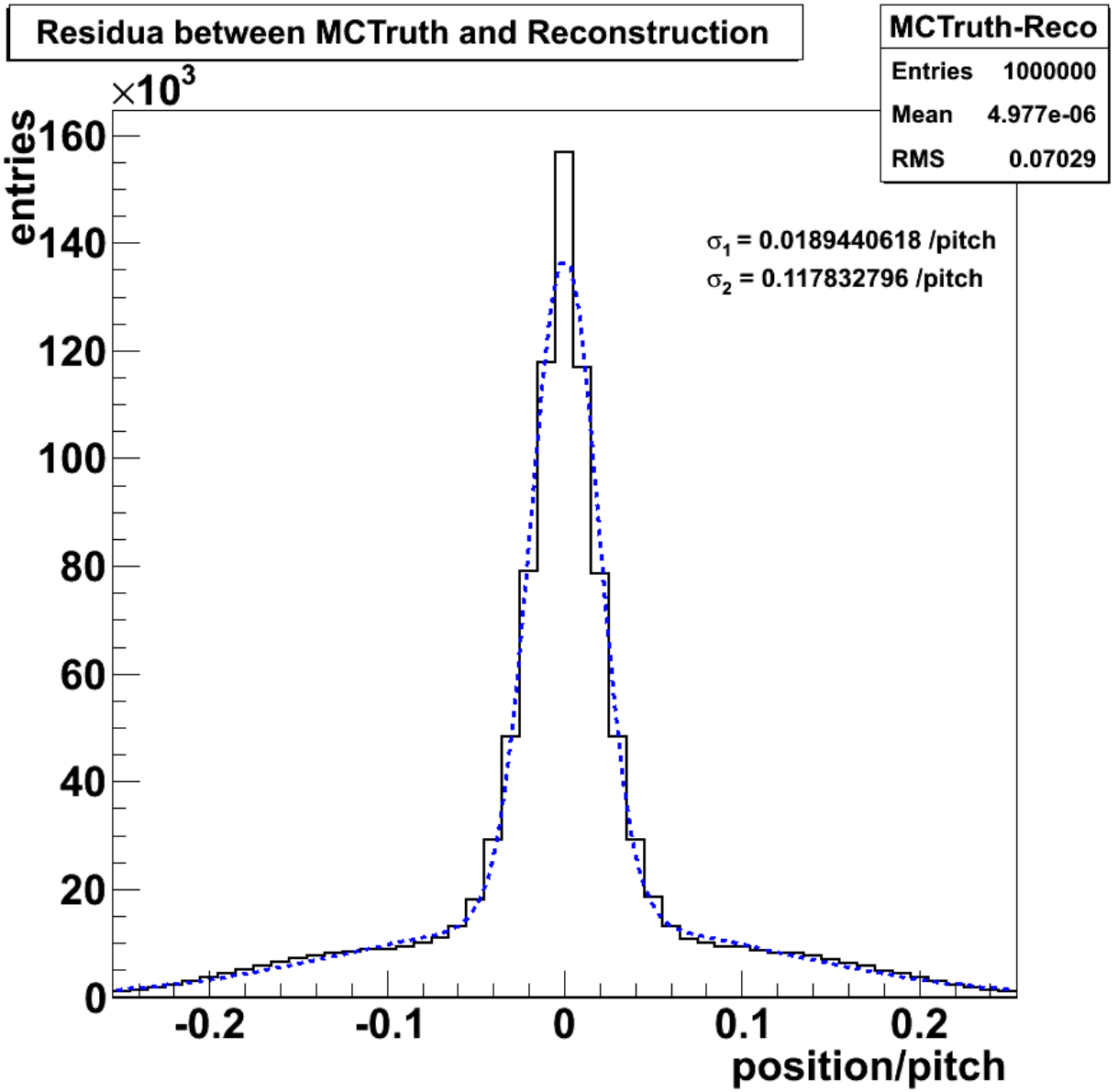
Simulation:
- 2 strip hit
- “analog” front-end
- hit threshold = 5.000 e^-
- landau distributed signal
- signal = 24.000 e^-
- noise sigma = 800 e^-
- clustering: Center of Gravity



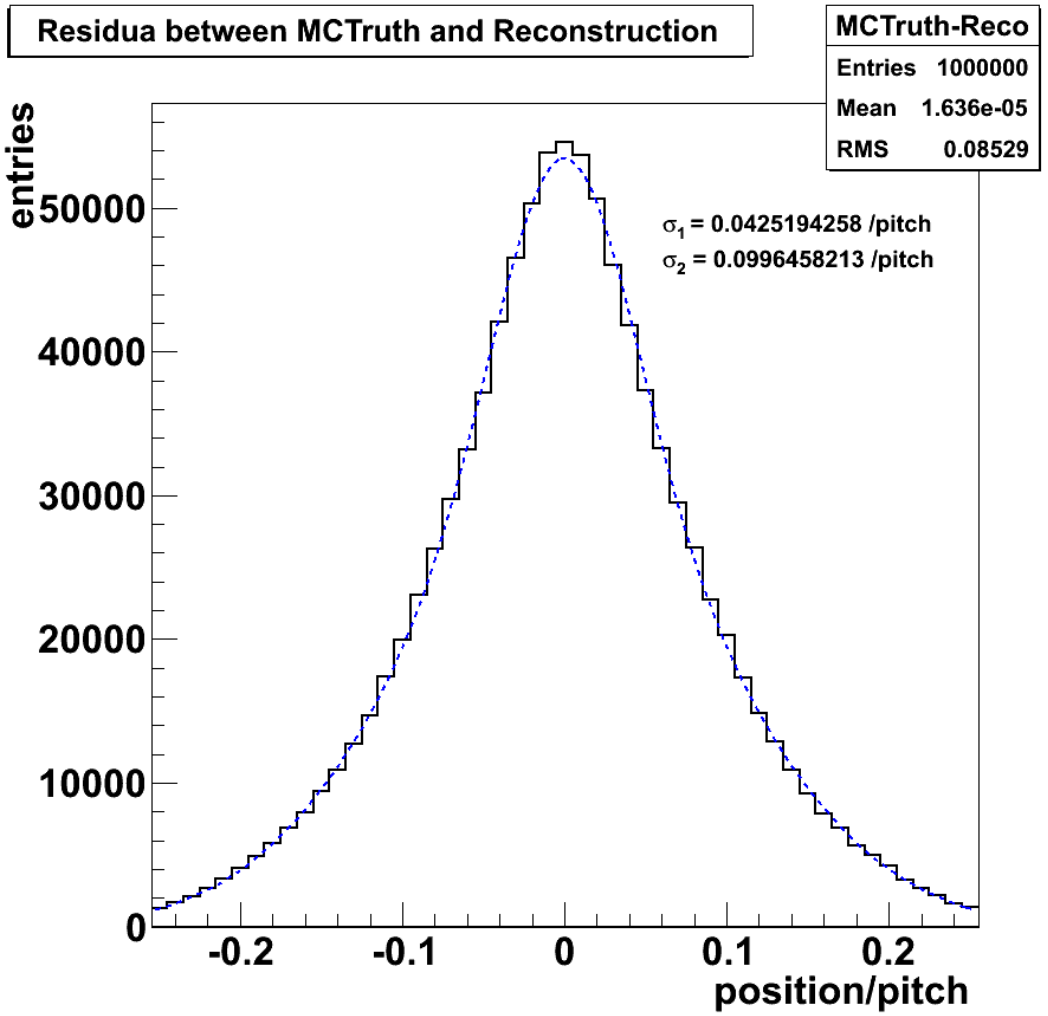
Simulation:
- 2 strip hit
- “analog” front-end
- hit threshold = 5.000 e^-
- landau distributed signal
- signal = 24.000 e^-
- noise sigma = 800 e^-
- clustering: Center of Gravity



Simulation:
- 2 strip hit
- “analog” front-end
- hit threshold = 5.000 e^-
- landau distributed signal
- signal = 24.000 e^-
- noise sigma = 800 e^-
- clustering: Center of Gravity



3-bit digital front-end



analog front-end