

## Upgrade of the detection setup of the gas-filled recoil separator GARIS-III

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The upgrade of the GARIS-III detection system was part of the overall upgrade of the experimental, with the newly developed superconducting RIKEN linear accelerator (SIRALC). The new superconductive tank, new 28 GHz SC–ECRIS ion source and overall higher beam energy/intensity available triggered a series of upgrade and new development of the detection setup of GARIS-III focal plane system: new detectors array and development of a digital acquisition electronics.

The complete silicon detector array has been replaced with new generation of Hamamatsu detectors. They have been developed in direct collaboration with the RIKEN team to fit the specification of our setup: 12x6cm<sup>2</sup> DSSDs surrounded by pixelized Side/Veto detectors. The full characterization of these detector is currently ongoing (resolution, dead layer, ...). The preliminary results indicate around 100 nm of dead layer measured on the side detectors. The preliminary optimization and characterization of these detector will be presented during this talk.

In addition, to the upgrade of the detector system, the transition to a digital electronic acquisition is also ongoing on the GARIS-III setup. This transition, coupled with the previous upgrade to fast CREMAT Inc. preamplifier (CR-110 and CR-111), lead to the reduction of the overall dead time of the detection setup bellow 100 ns (64 ns achieved in beam). This reduction led to the identification of very fast decays of reaction products in the region north-east of the <sup>208</sup>Pb. In addition, an increase of the energy resolution of about 5 keV on the average FWHM has also been observed compared to its analog counterpart. This transition to a digital electronic also opened the door the pulse shape analysis for the reduction of the background in the alpha spectrum. The preliminary results of this pulse shape analysis will be presented in addition to the results on the development and optimization of the in-beam condition for the digital electronic.