Readout Chain of the PANDA Electromagnetic Calorimeter

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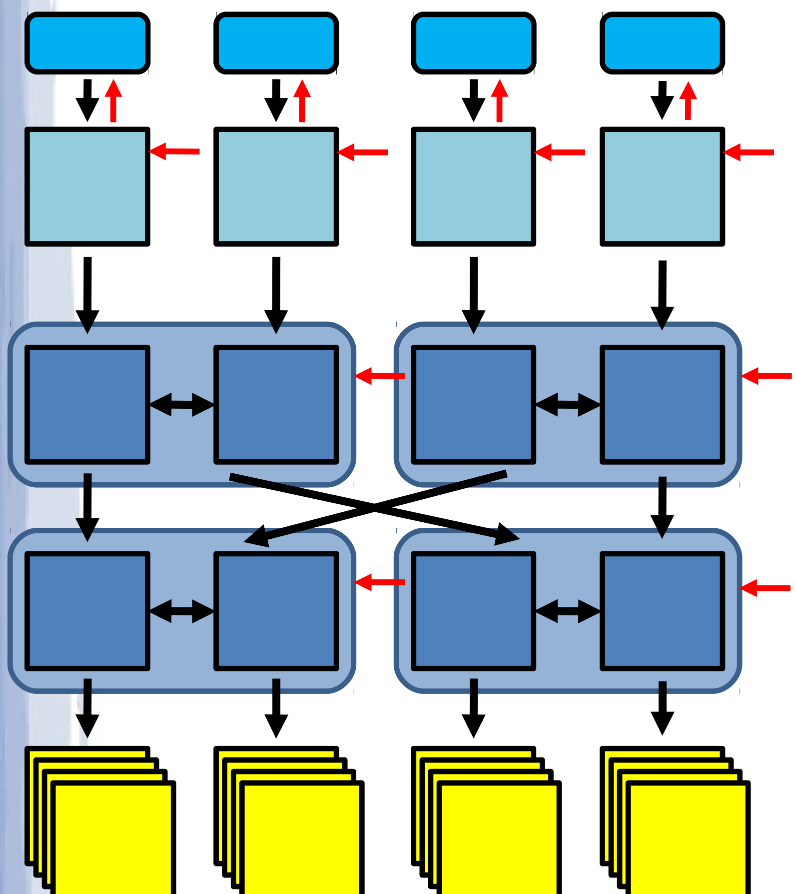
for the PANDA collaboration

PANDA Readout

using **Data links** (←) and Time distribution (←) "SODA"

[I. Konorov et al., NSS/MIC Conf. Rec., 2009 IEEE, DOI 10.1109/NSSMIC.2009.5402172]



Detector Front-ends — Hit detection, feature-extraction

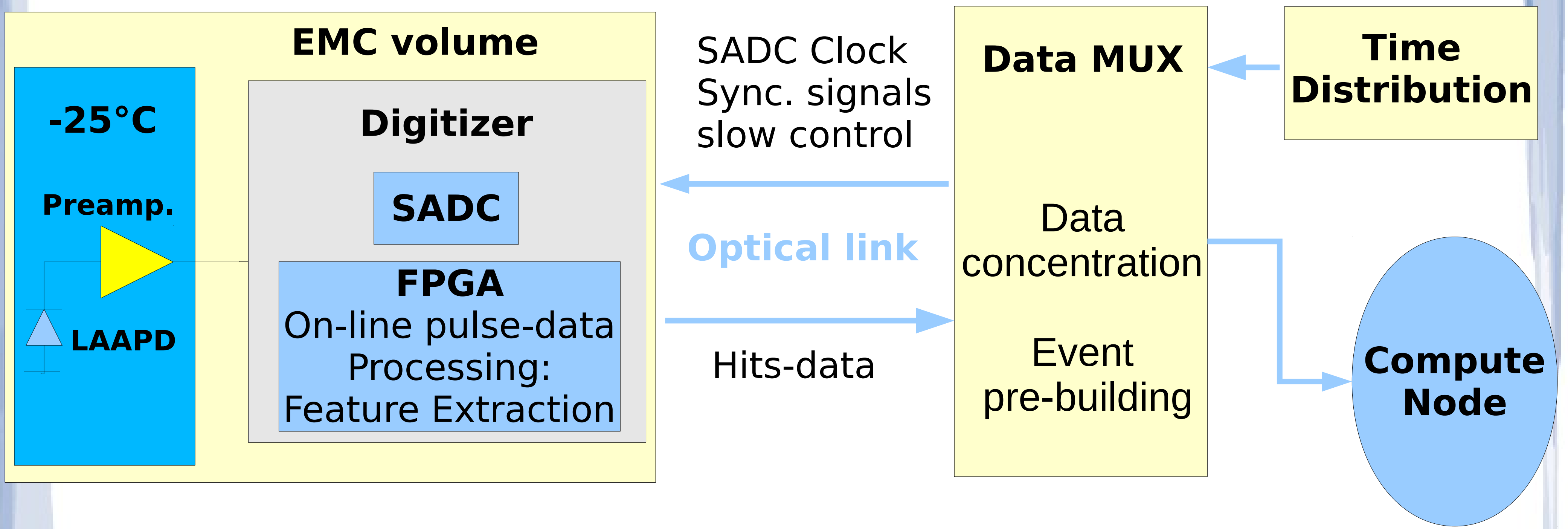
Data Concentrator — Combine several Front-Ends

First Stage "Event" Builder

Second Stage "Event" Builder — Time-ordering (building physics events)

Compute Node — On-line processing of complete events, Accept/reject decision

Readout for Electromagnetic Calorimeter



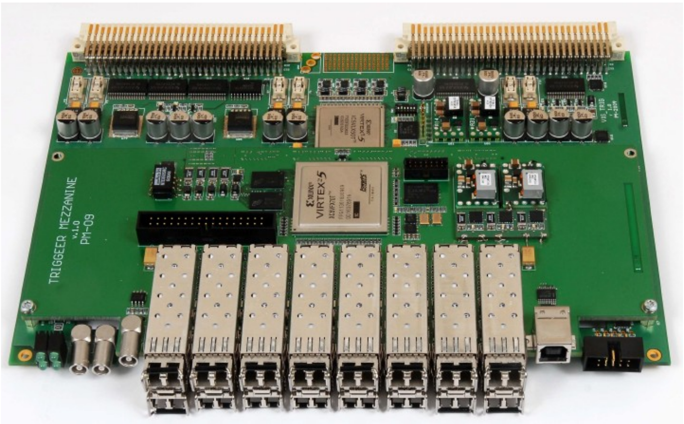
Key components of the readout:

- Digitizer module with on-line pulse-processing
- Data-multiplexer with time-ordered output
- Synchronous optical-link connection (clock-signal distribution)

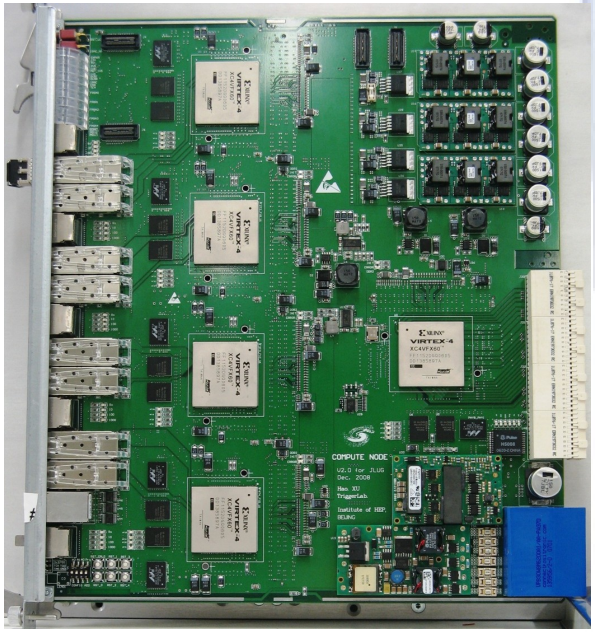
Readout-chain Prototype

- design readout architecture (define functionality of each electronic module)
- redesign/optimization of the feature-extraction algorithm
- development of a readout infrastructure (slow control, SODA interfaces)
- implement “basic” readout-chain prototype (using the feature-extraction algorithm from the stage I; not complete functionality of the infrastructure)

Digitizer:
(developed by P. Marciniewski)
- 16 channels
- 125 MHz sampling rate
- Only partial support of a time-synchronisation via optical link



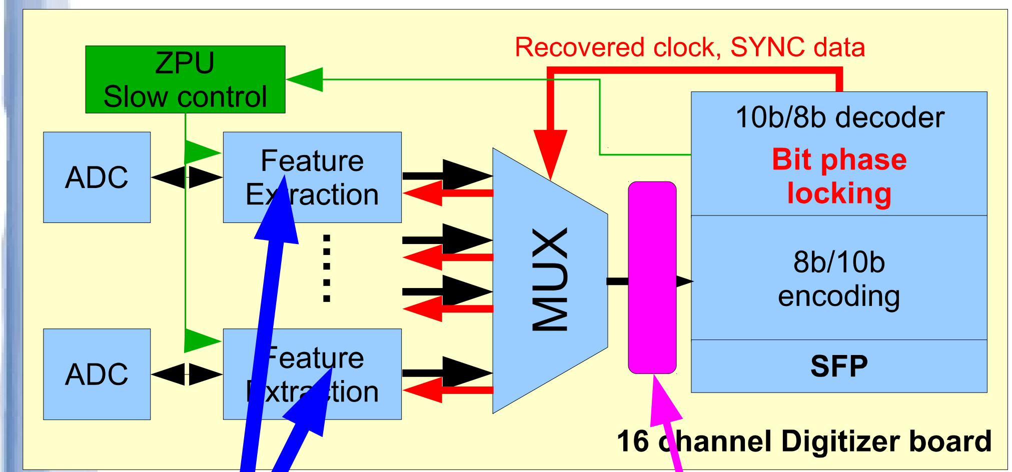
Data Multiplexer:
(developed by P. Marciniewski)
- 16 channels
- Xilinx Virtex-5 FXT for data processing



Compute Node:
(developed at Giessen and IHEP)

EMC Digitizer

Digitizer



Have to be **"Minimal" stages** with gain selection

One **"Standard" stage** has to be introduced (to serve 32 channels)

Hardware: implement redundancy and develop recovery procedures

Feature-extraction algorithm, which does everything (with pile-up recovery) is too bulky to clone it for all channels (up to 64)

Feature-extraction has to be done in "stages":

Minimal feature-extraction

- base-line follower (compensation)
- pulse detection and storage of a complete pulse waveform
- rough time-stamp estimation
- pile-up detection

Standard feature-extraction

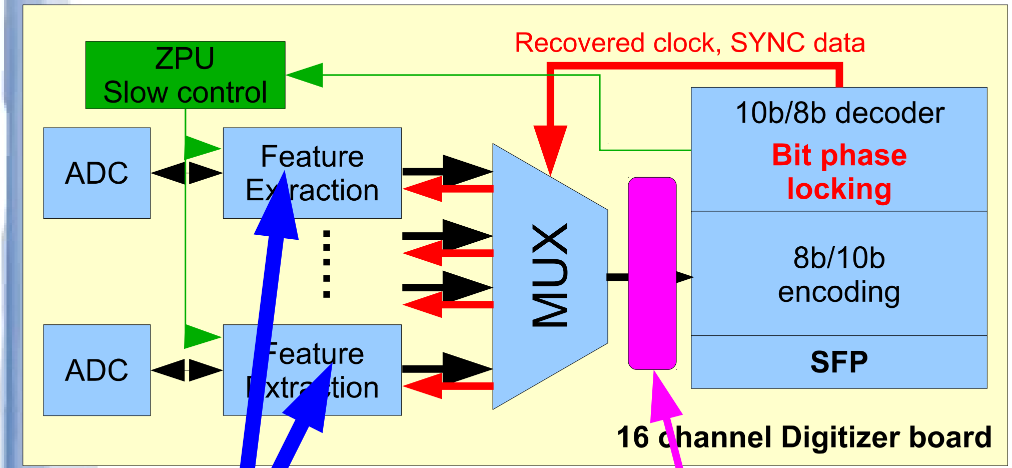
- precise energy and time

Advanced feature-extraction

- pile-up recovery

EMC Digitizer
Data Rates

Digitizer



Have to be **"Minimal" stages** with gain selection

One **"Standard" stage** has to be introduced (to serve 32 channels)

Hardware: implement redundancy and develop recovery procedures

Forward End-cap:

- hit-rate of 300 kHz → **~1.2 Gb**

Barrel End-cap:

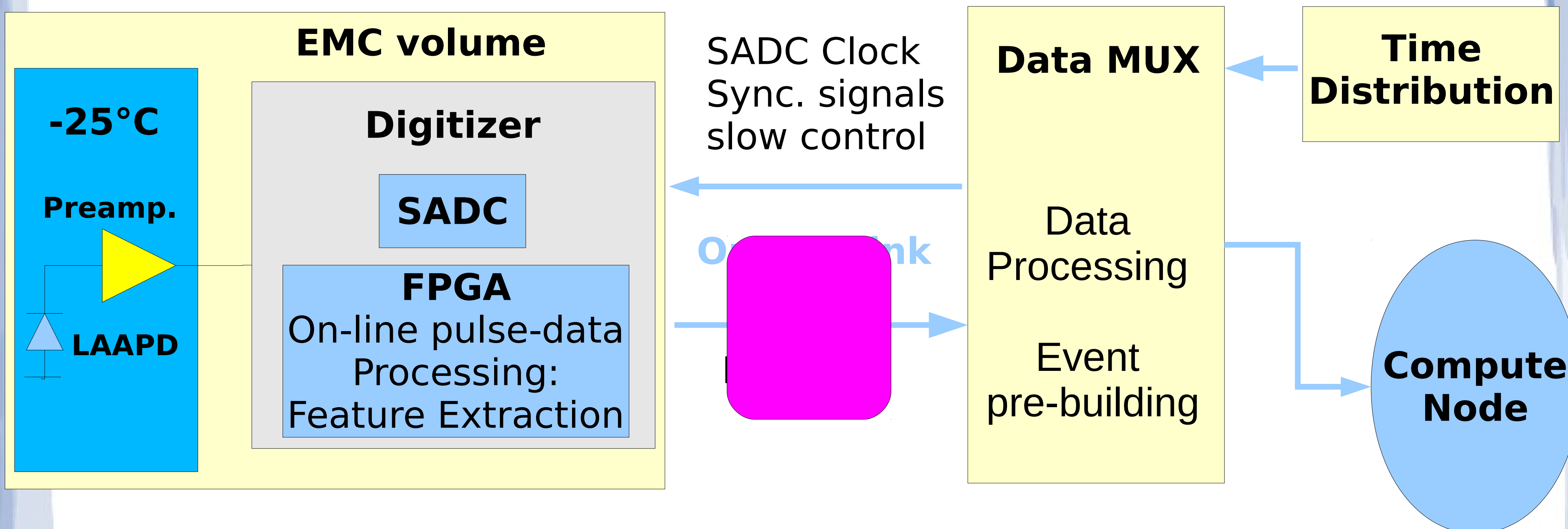
- Forward: hit-rate of <100 kHz → **~0.6 Gb**
- Middle: hit-rate of <50 kHz → **~0.27 Gb**
- Backward: hit-rate of <10 kHz → **~0.05 Gb**

Backward End-cap:

- hit-rate of <10 kHz → **~0.05 Gb**

Presented numbers correspond to the worst case scenario

Readout for Electromagnetic Calorimeter



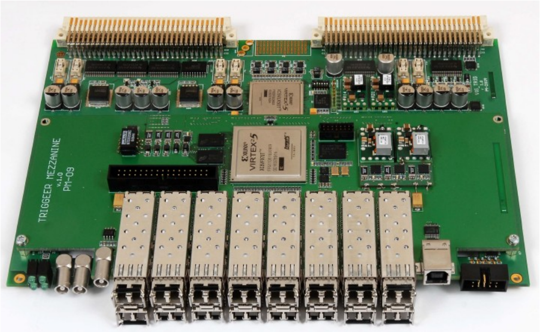
Due to low rates in the barrel EMC and backward EMC extra **data-concentration** stage has to be introduced

Data Multiplexer

Required functionality:

- Time-distribution functionality
- Separation of the hit-data and slow-control streams
- Combine information from two photo-sensors, reading out same crystal
  - Identification and correction of a nuclear counter effect
- Energy calibration of the combined data (linear of non-linear?)
- Time-ordering of the data
- Advanced feature-extraction (pile-up recovery)

Developments and tests can be be done with existing hardware



Hardware for Data-Multiplexer

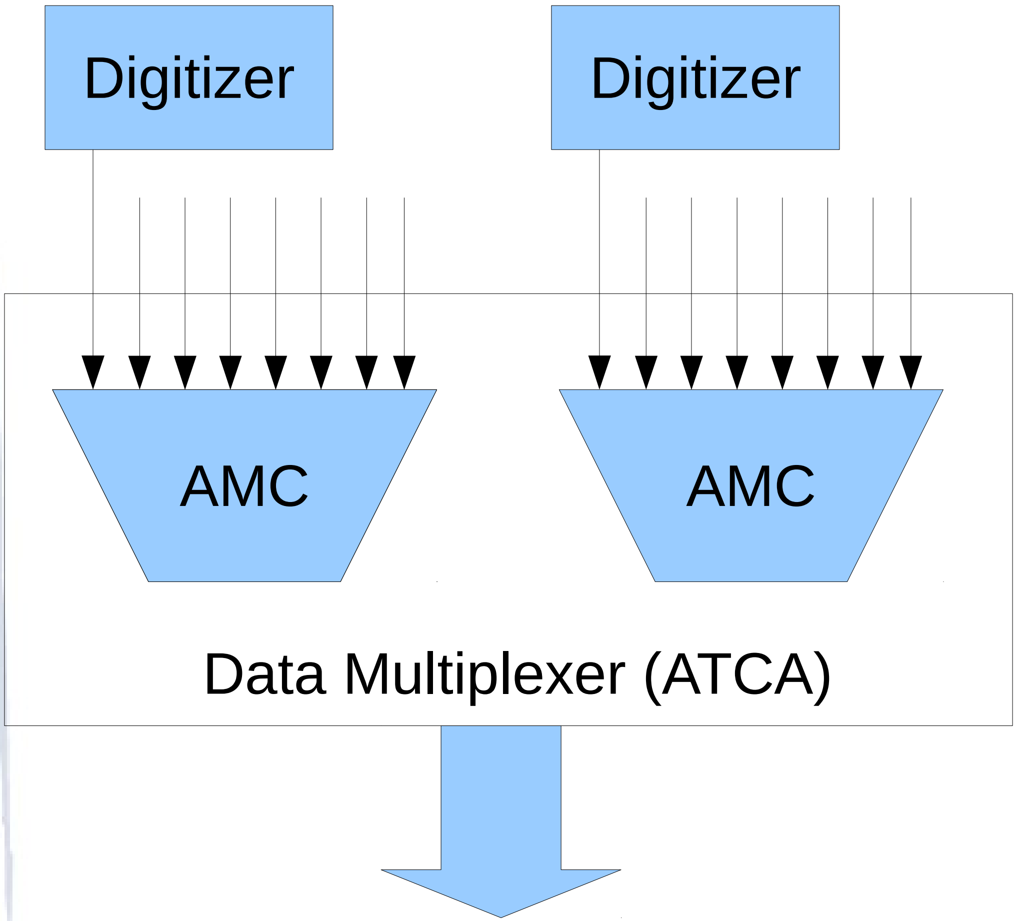
Boundary conditions:

- Has standard interface to the PANDA event-building network
- ATCA compatible (AMC cards)
- Interface to digitizers (8 optical links/AMC card) and ATCA back-plain (fast serial links)
- Has interface to SODA (via back-plain)
- Has enough FPGA resources (can be specified once full-functional prototype, based on the existing hardware, is developed and tested)

Assumptions:

- Maximum output data-rate per AMC card: **8 Gb** (mean 4 Gb)
- Mean hit-rate/channel for one digitizer (FW end-cap): **300 kHz**

Interface to DAQ
Forward End-Cap



To time-ordering network/compute nodes
(back-plain connections)

input channels: **6941×2**

digitizers: **217**

AMC cards: **28**

ATCA carriers: **7**

Interface to DAQ
Barrel and Backward End-Cap

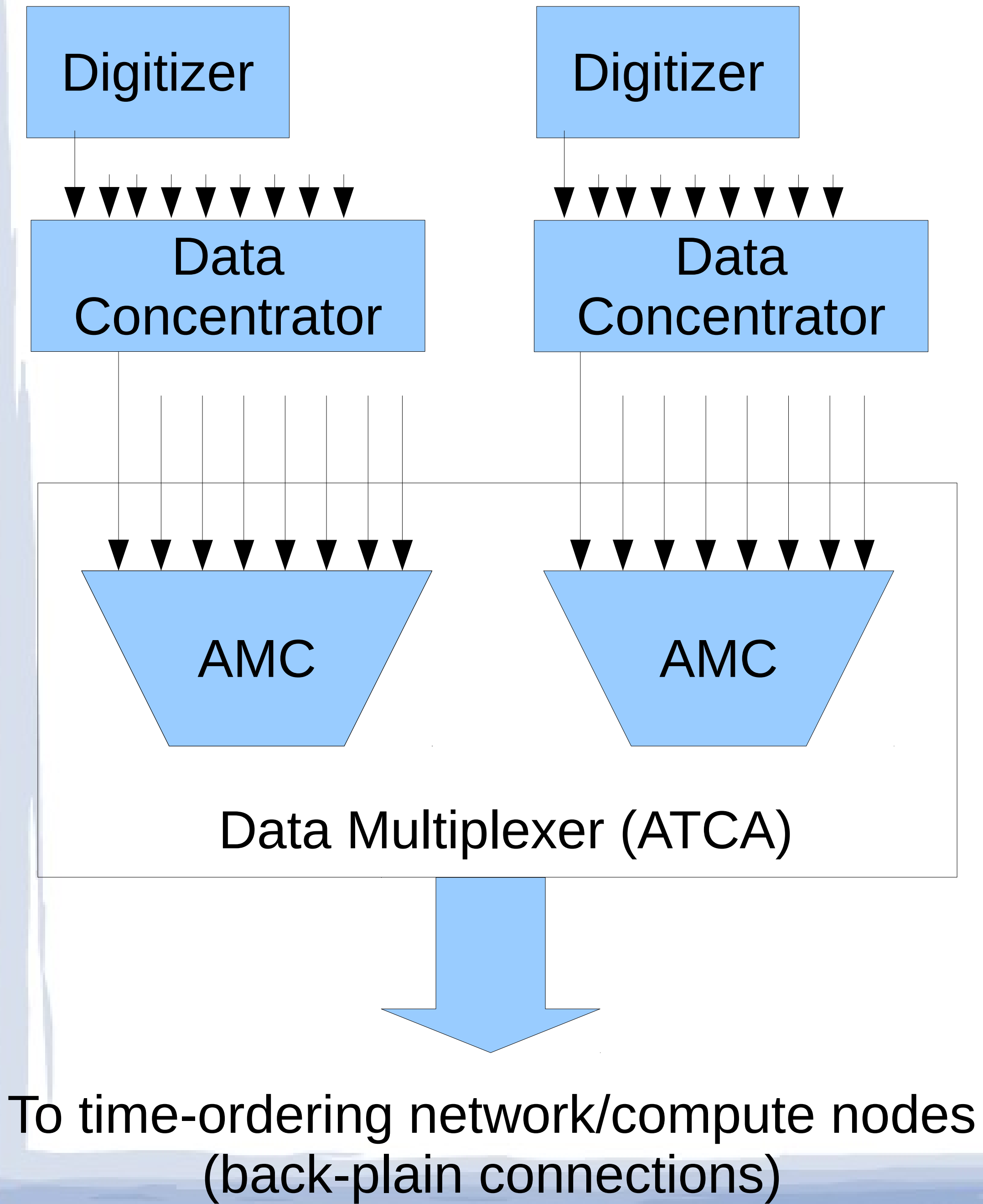
Hit-rate per channel is low in comparison with the forward end-cap. Therefore, more channels can be combined together

Data concentrator module:

- Combines many (32) optical-link connections with one FPGA (Kintex-7)
- Each optical-link intrface can be used as:
  - SODA input
  - Interface to digitizer
  - Interface to Data Multiplexer

- Can be used to combine different amount of channels (forward, middle and backward regions):
  - 4×(**6 channels → 1**)
  - 2×(**14 channels → 1**)
  - 1×(**30 channels → 1**)

Interface to DAQ
Barrel and Backward End-Cap



input channels: **(600+11360)×2**
digitizers: **1196**

data concentrators: **46**

AMC cards: **12**

ATCA carriers: **3**

Summary
DAQ interface

Data from complete EMC can be collected within one ATCA crate (10 carrier cards)

↓

Good for cluster finding (no boundaries)

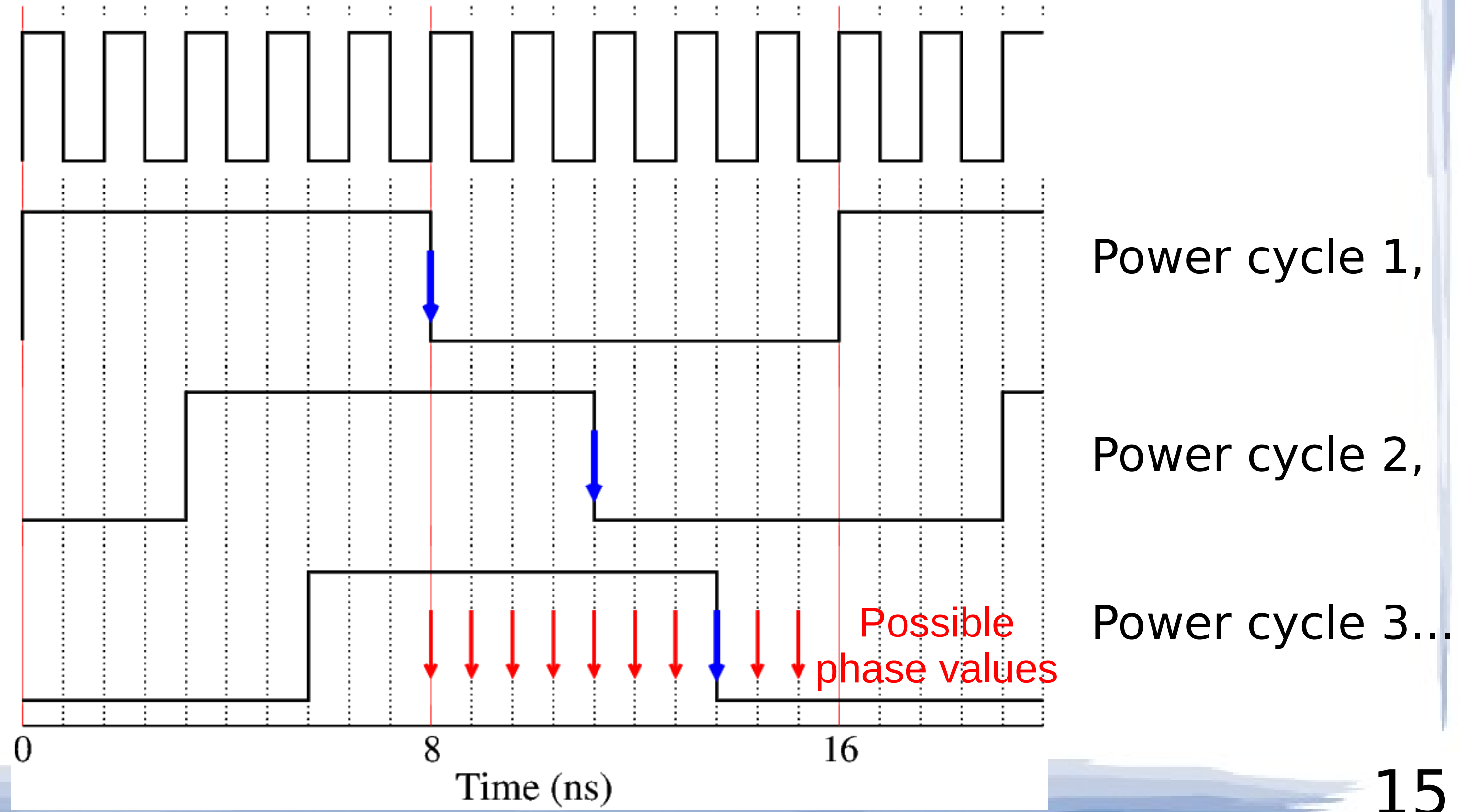
Synchronous optical link

Synchronous Optical-Link Connection

Standard implementation **does not guarantee stable phase** of the recovered clock (phase changes at power/reset cycle) → special arrangement needed

Serial clock
(1.25 GHz)

Parallel clock:
recovered clock,
used for SADC
(125 MHz)



Synchronous Optical-Link Connection

Standard implementation **does not guarantee stable phase** of the recovered clock (phase changes at power/reset cycle) →

Bit phase locking

Serial clock
(1.25 GHz)

Parallel clock:
recovered clock,
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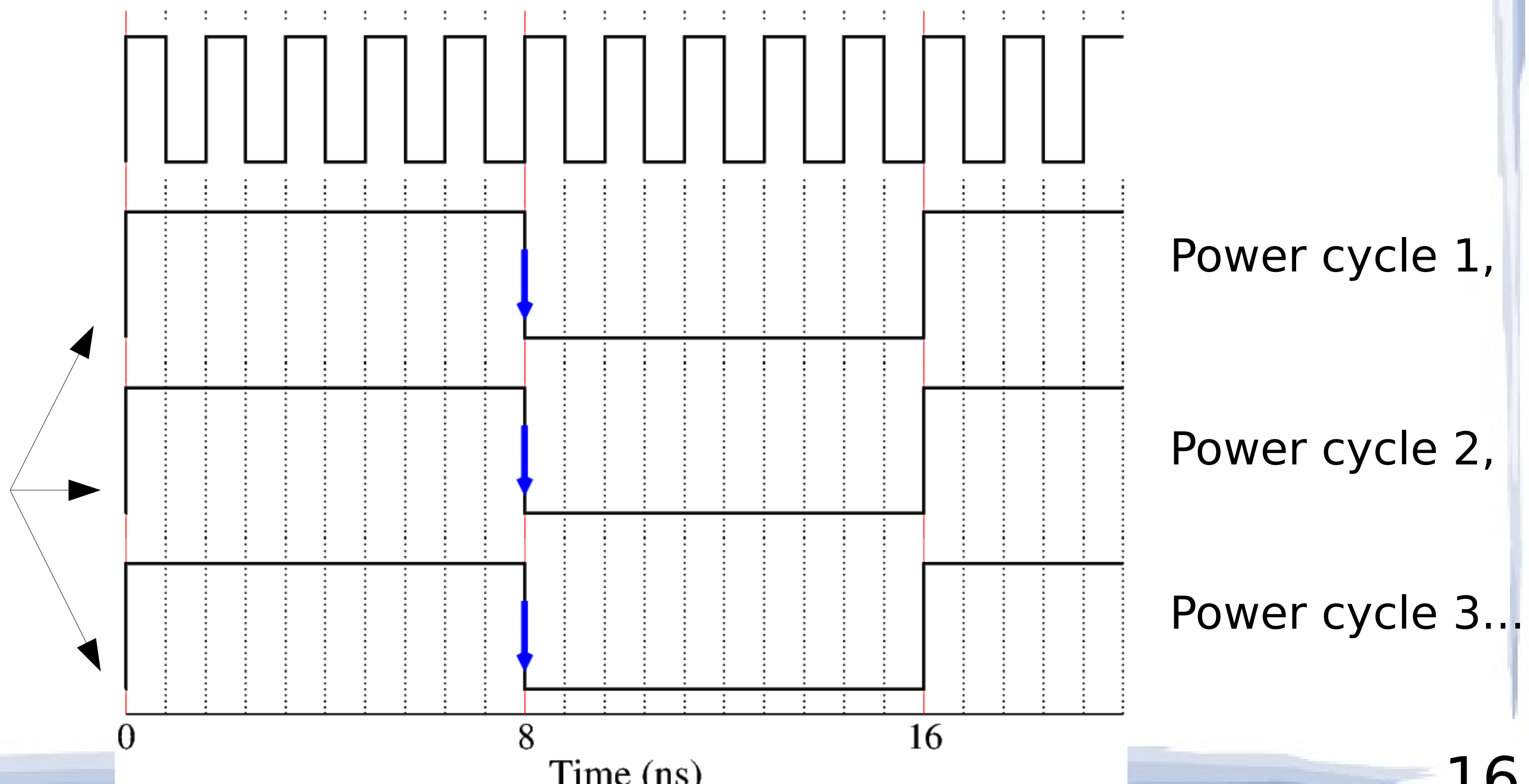


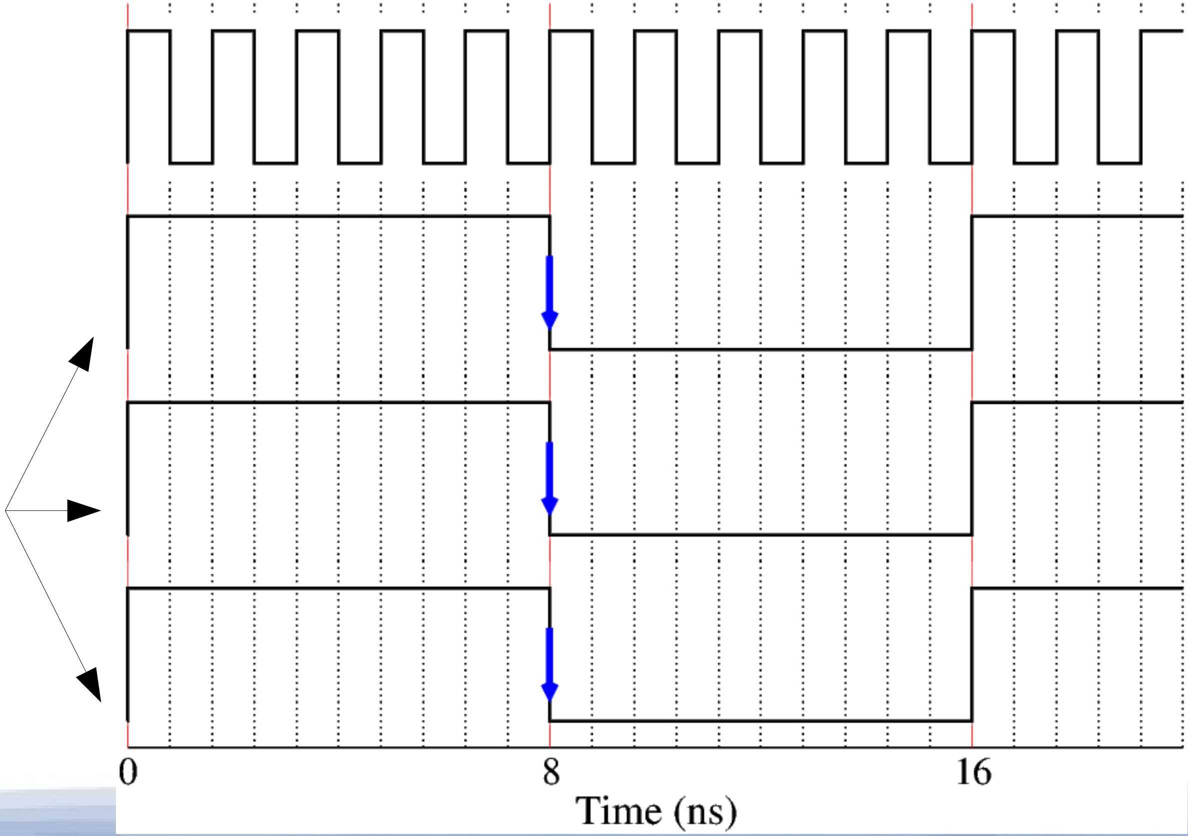
Bit Phase Locking

Solution:

- Configure the SerDes of the Xilinx FPGA in a special way:
  - a stable phase is guaranteed
  - the SerDes locks on a signal only once in 10 trials
- Special state machine resets the SerDes until it is locked on a signal

Serial clock
(1.25 GHz)

Parallel clock:
recovered clock,
used for SADC
(125 MHz)



Power cycle 1,

Power cycle 2,

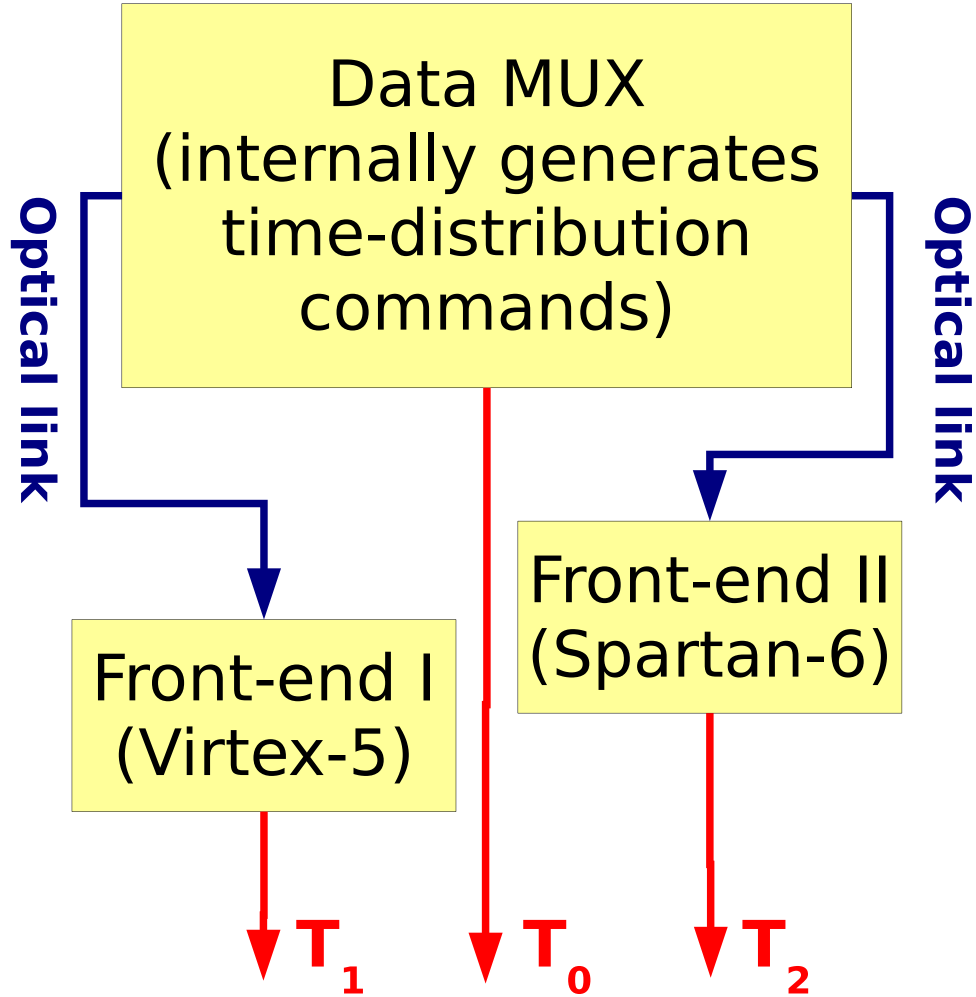
Power cycle 3...

Bit Phase Locking: Measurement Setup

Data MUX

Front-end I

Front-end II

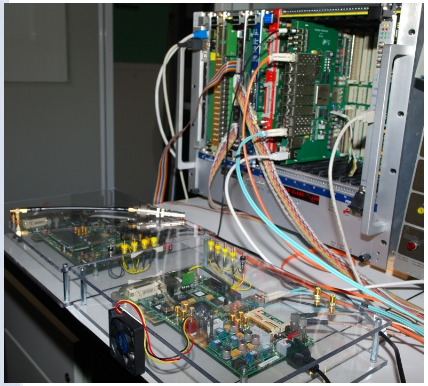


Send (MUX) and recovered (Front-end) synchronisation command

To time measurement (Caen TDC v775)

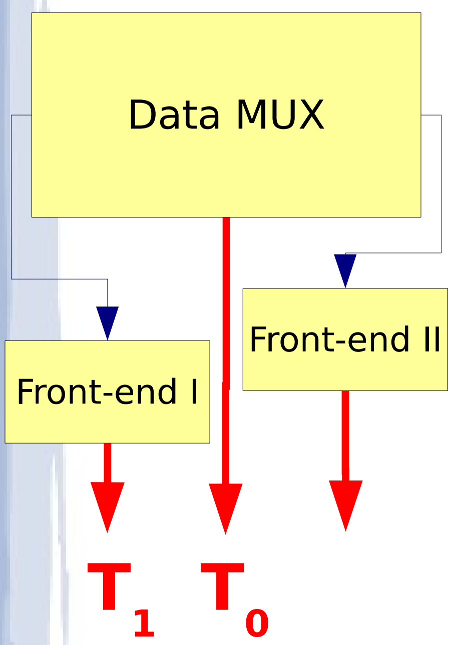
Time-difference between T_0, T_1 and T_2 should be **constant**!

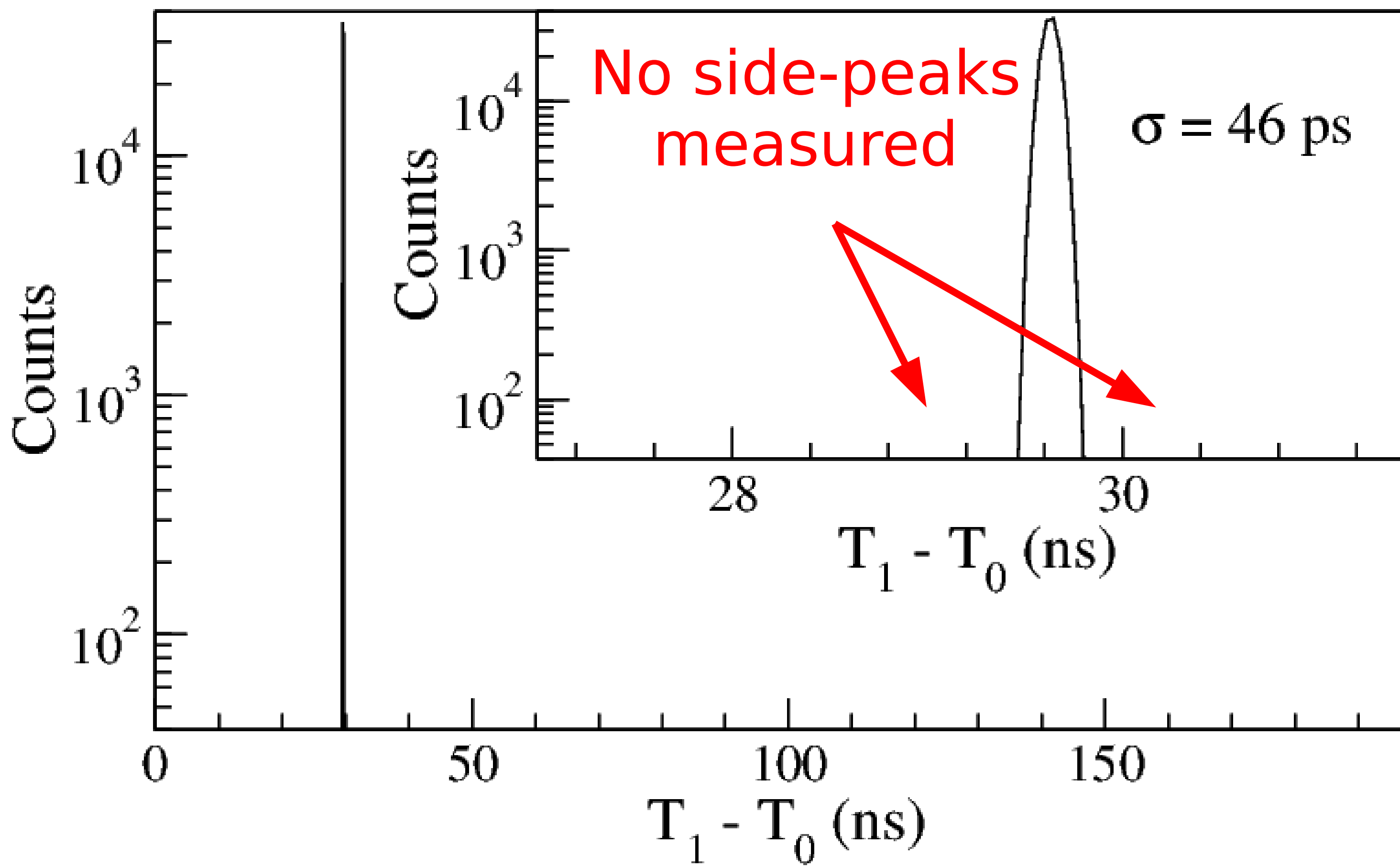
Bit Phase Locking: Stability of Recovered Phase



Measurement condition:

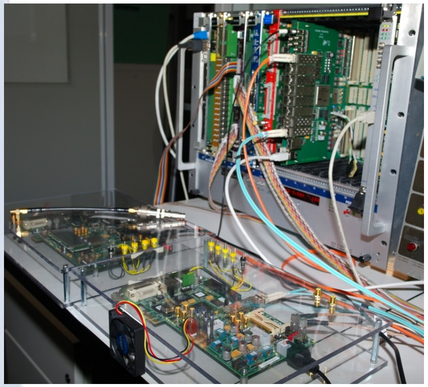
- Front-end board was periodically reset (disconnect optical fibre)

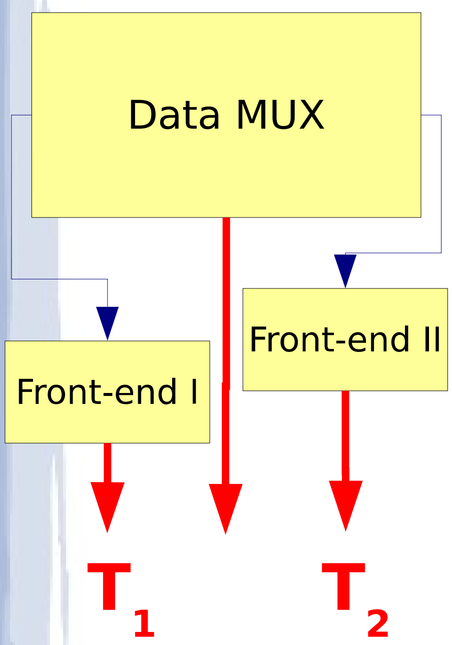




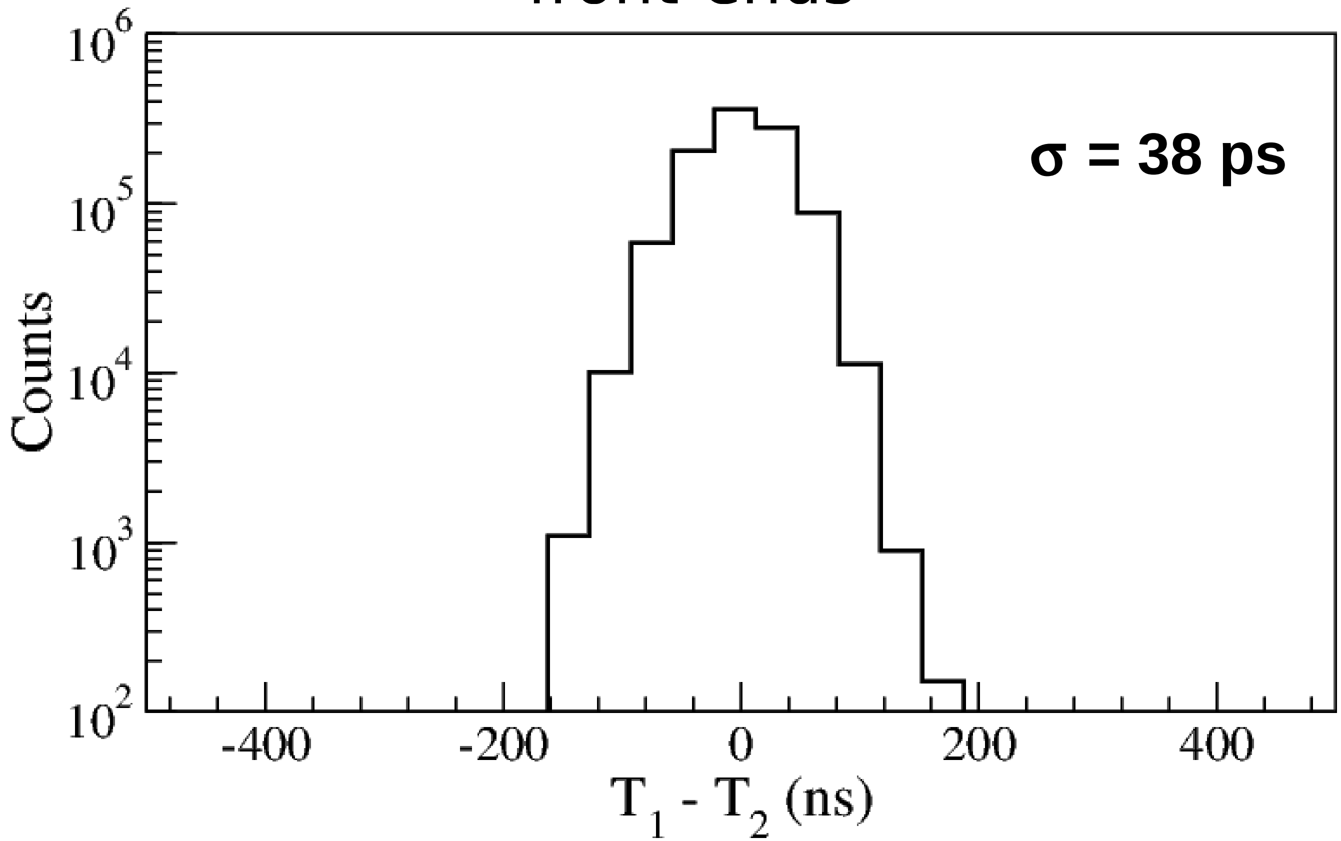
After reset SerDes locks at the same phase!

Bit Phase Locking: Stability of Recovered Phase





Difference of arrival times of synchronization commands to different front-ends



Lower limit of **jitter** induced by **measuring device** (e.g. TDC): 19 ps

Jitter of single channel < 23 ps!

Summary
synchronous serial link

- Optical-link connections between front-ends require special arrangement (bit phase locking):
  - Procedure is established for Xilinx GTP and GTX transceivers (Spartan-6, Virtex-5, Virtex-6, Artix-7, Kintex-7, Virtex-7)
  - Achievable clock jitter < 23 ps (without extra jitter cleaning)

Thank you for attention!