AGH UNIVERSITY OF SCIENCE AND TECHNOLOGY

Development of front-end electronics for STT readout

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Measurements with straw tubes done at UJ with the help of **P. Salabura and J. Smyrski** group

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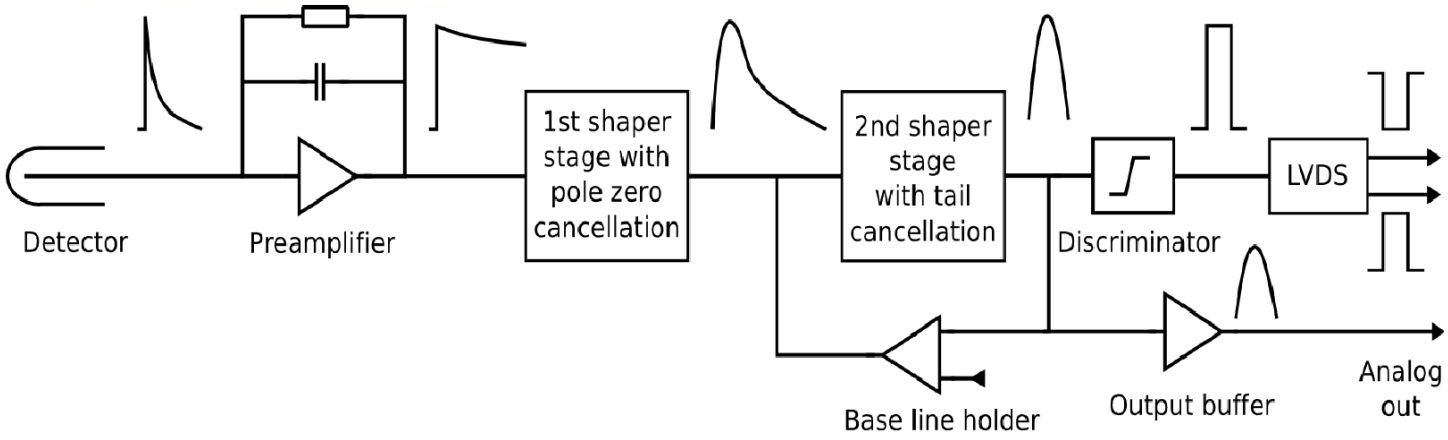
Outline

- Architecture and design
- Glimpse of measurements
- Summary

Front-end electronics design goals

- Fast readout of various sensors
  - straw tubes mainly, shaping with elimination of long ion tail needed
  - standard shaping for other sensors (delta-like sensor pulse)
- Precise (1-2 ns) time measurement
- TOT amplitude measurement
- LVDS differential output for time and TOT
- Additional analog output
- Detector capacitance up to ~30pF
- Variable gain from ~2mV/fC to ~20mV/fC
- Variable peaking time from 15ns to 40ns
- Stabilized baseline

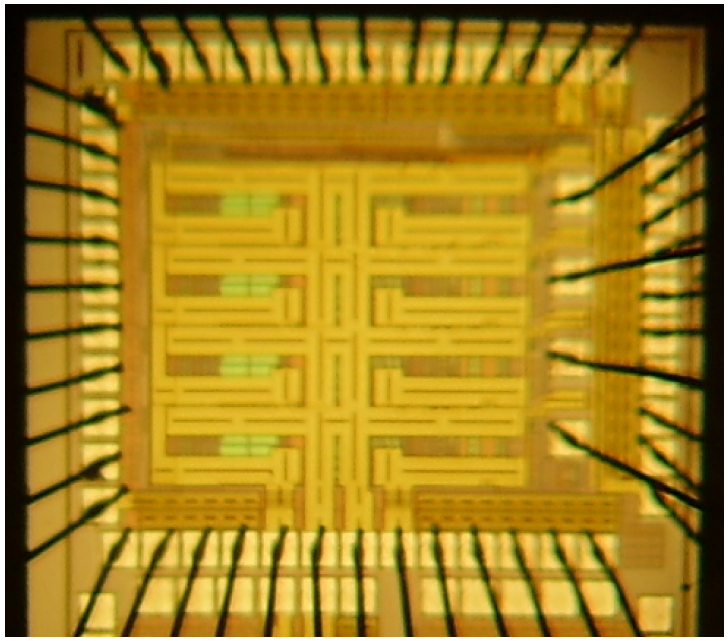
Front-end architecture



- Preamplifier with variable gain and time constant
- CR-RC^2 shaper with variable T_{peak} (default ~20ns for delta)
- Tail cancellation with two variable time constants
- Baseline stabilized by BLH circuit
- Leading edge discriminator for time measurements
- Fast LVDS output
- Buffered analog output

ASIC - First prototype

- ASIC designed and fabricated in AMS 0.35um technology
- Four channels implemented
- Peripherals not yet designed - reference and threshold voltages delivered externally - DACs, bandgap, etc.. need to be added in the future
- ~15.5mW/channel plus LVDS (~12mW)
- Channel size 200um x 1130um

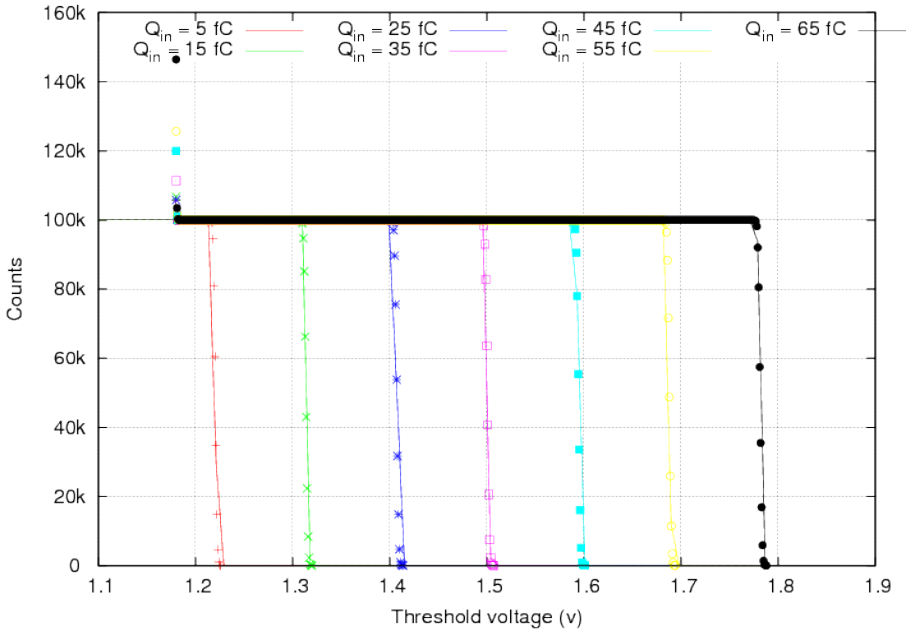


Glimpse of preliminary results

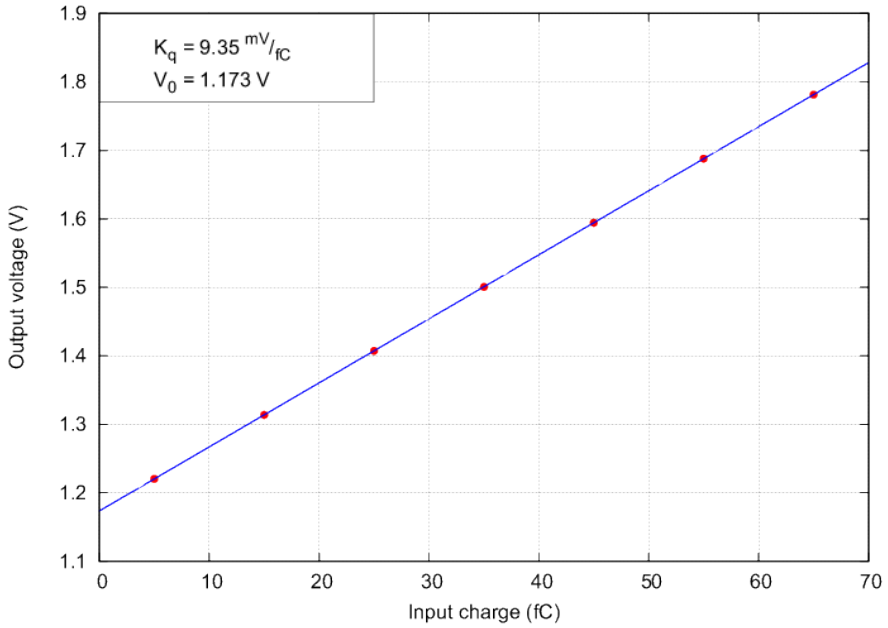
- Preliminary measurements veryfing the functionality and some of the parameters started
- Measurements stopped before completing chip characterization – setup containing the front-end had to be prepared for testbeam in Juelich (~2 weeks ago)
- Measurements will restart in few days.
- Here only some example plots...
- Some more results in other talk(s)

Example of S-curve and Gain measurement

Measurements ared done for configuration with CR-RC^2 shaping plus tail cancellation



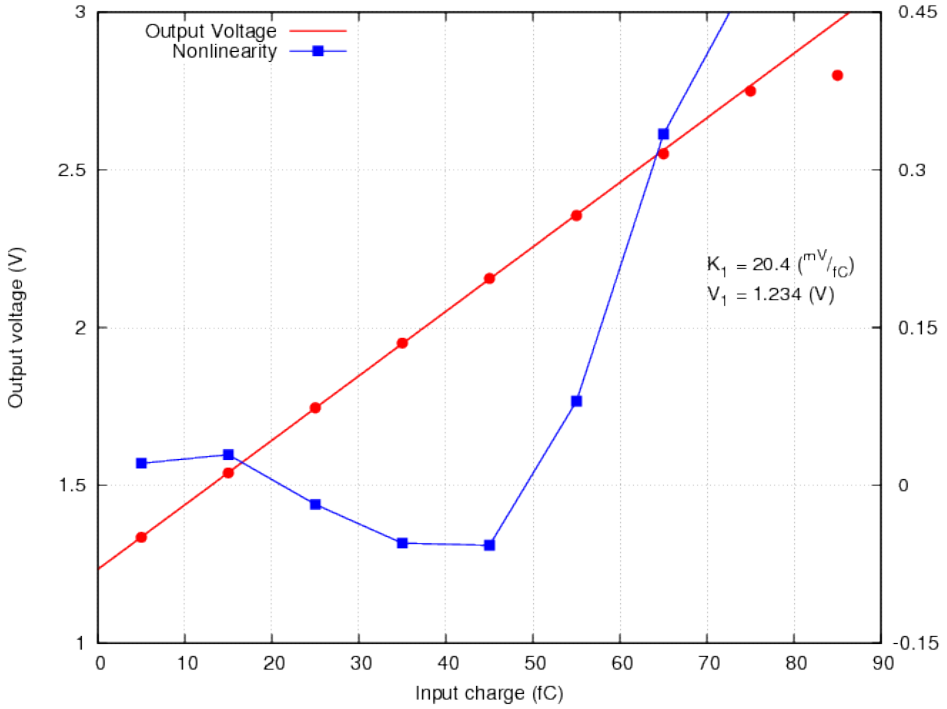
s-curves



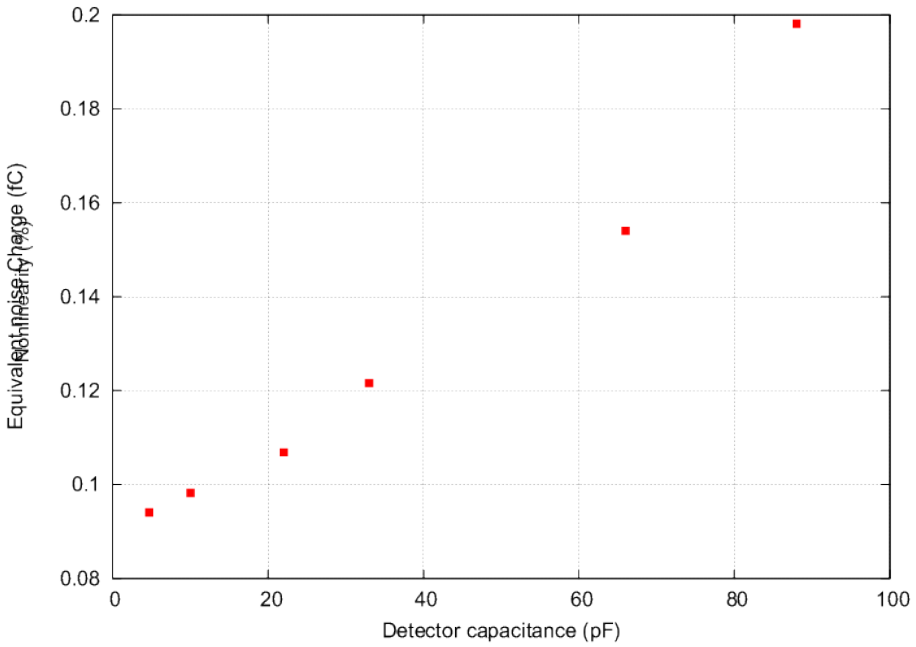
Gain

Example of Gain and Noise measurement

Measurements ared done for configuration with CR-RC^2 shaping, NO tail cancellation



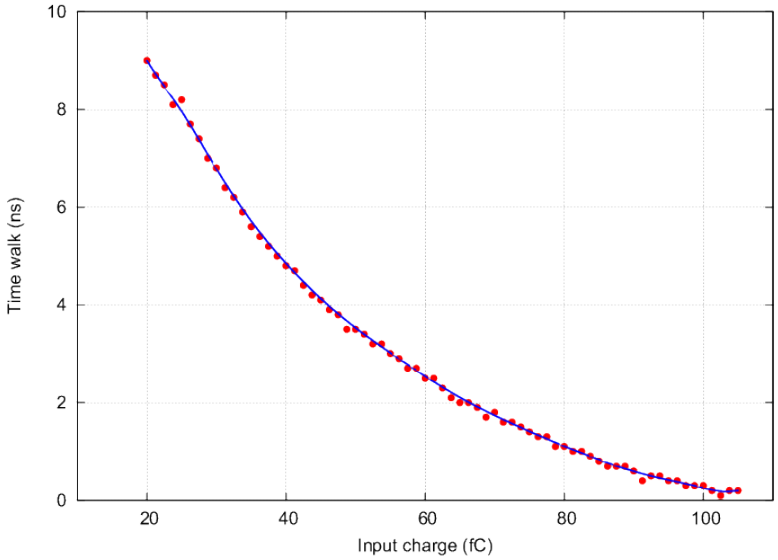
Gain



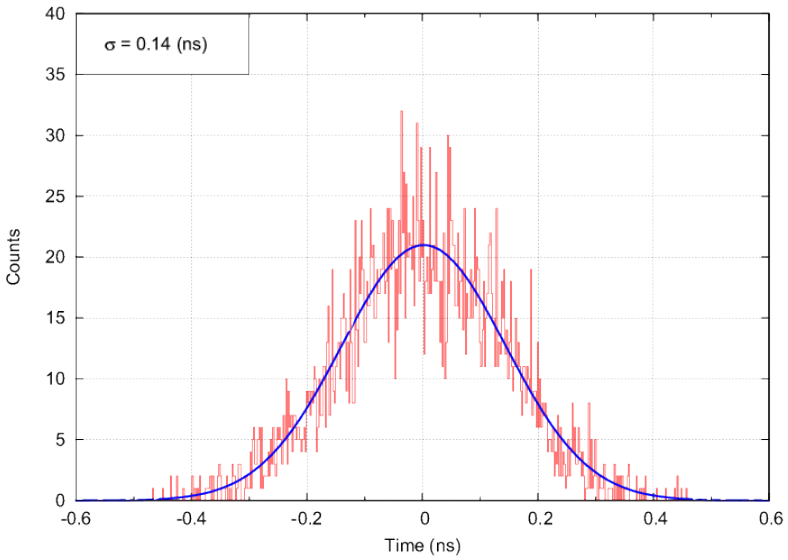
Noise

Timewalk and jitter example

Measurements ared done for configuration with CR-RC^2 shaping plus tail cancellation

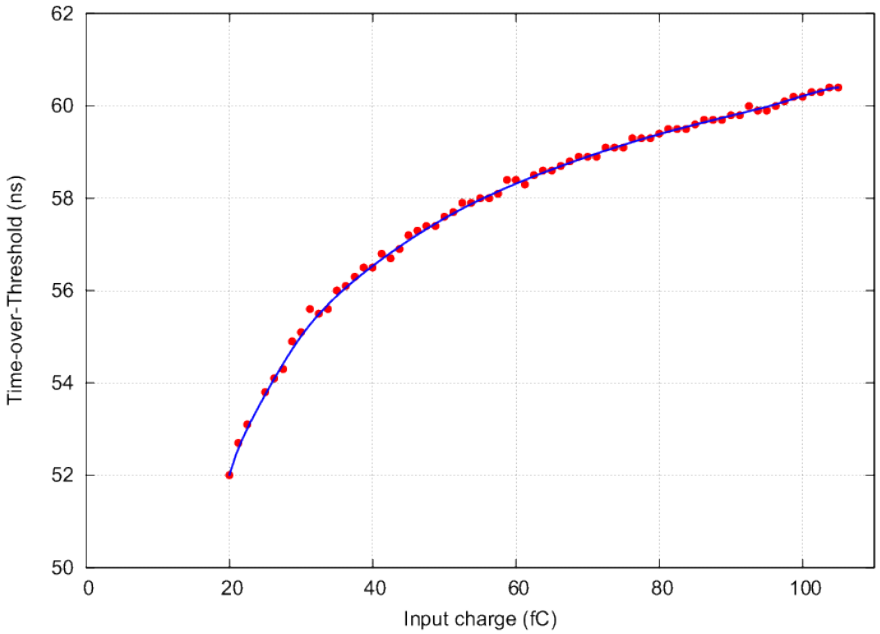


Timewalk

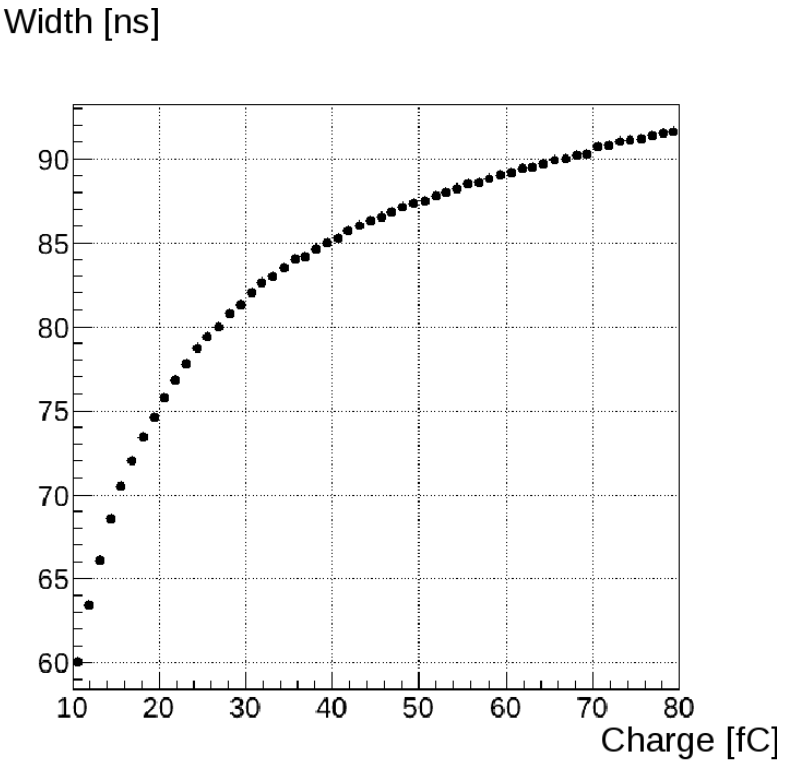


Jitter

TOT example

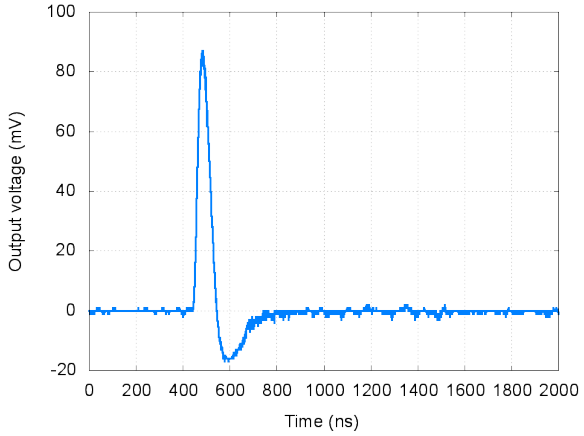


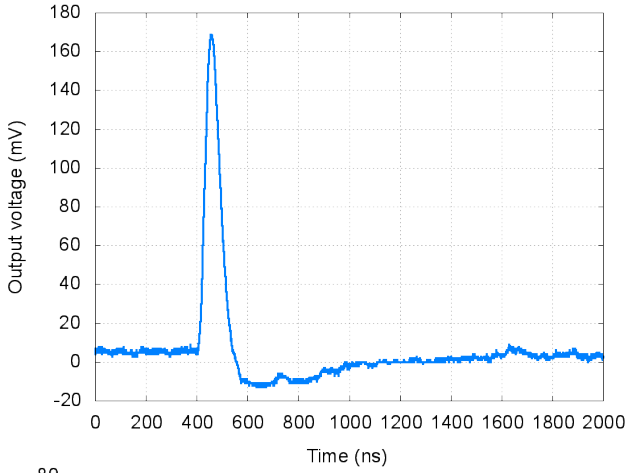
Configuration without tail cancellation

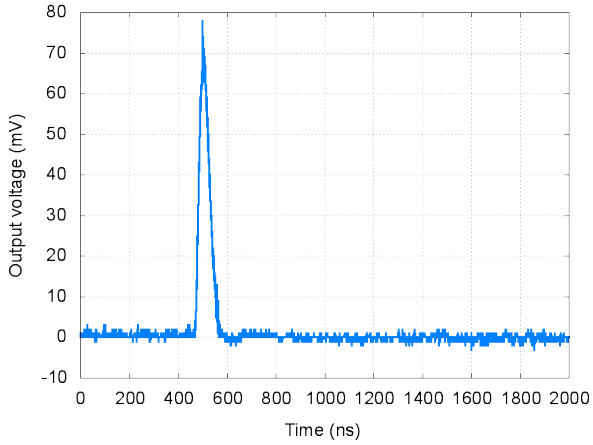


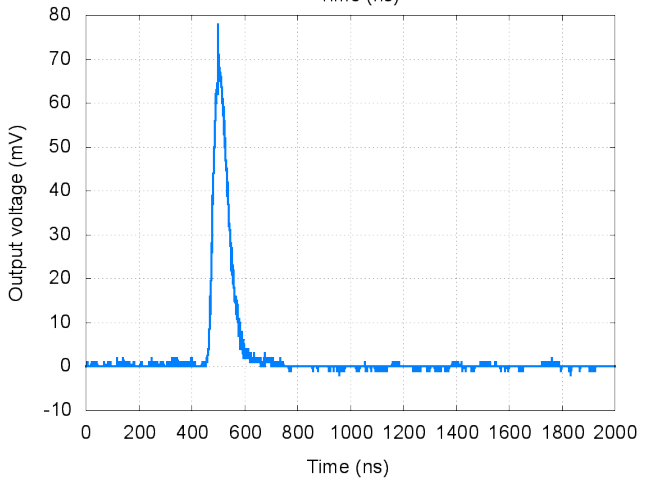
Configuration with tail cancellation

Examples of pulses from straw tube Tail canlellation



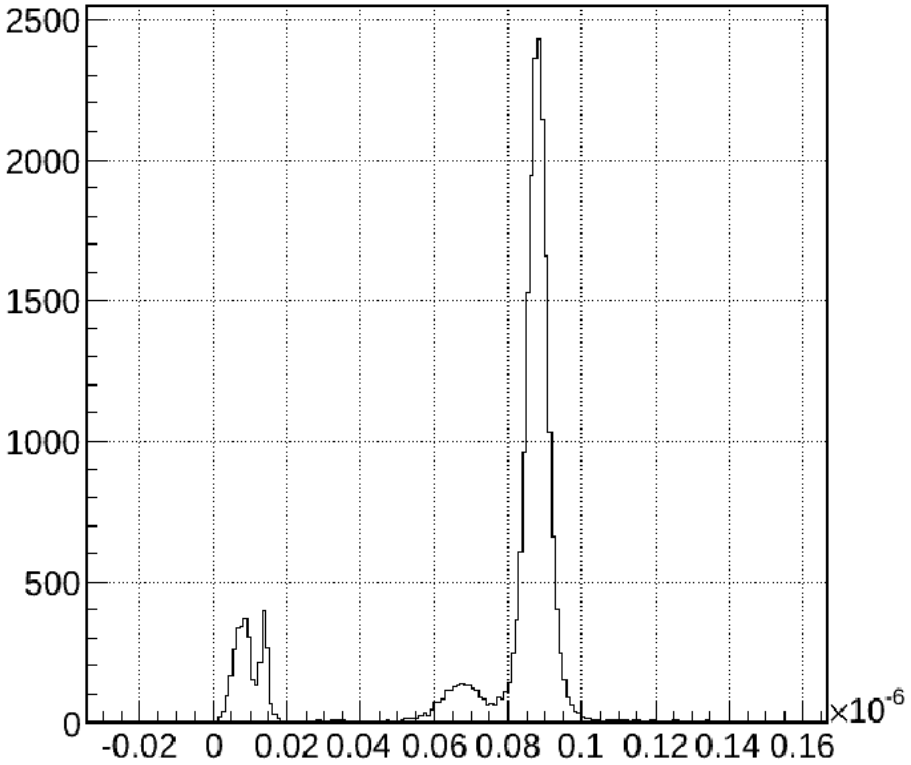




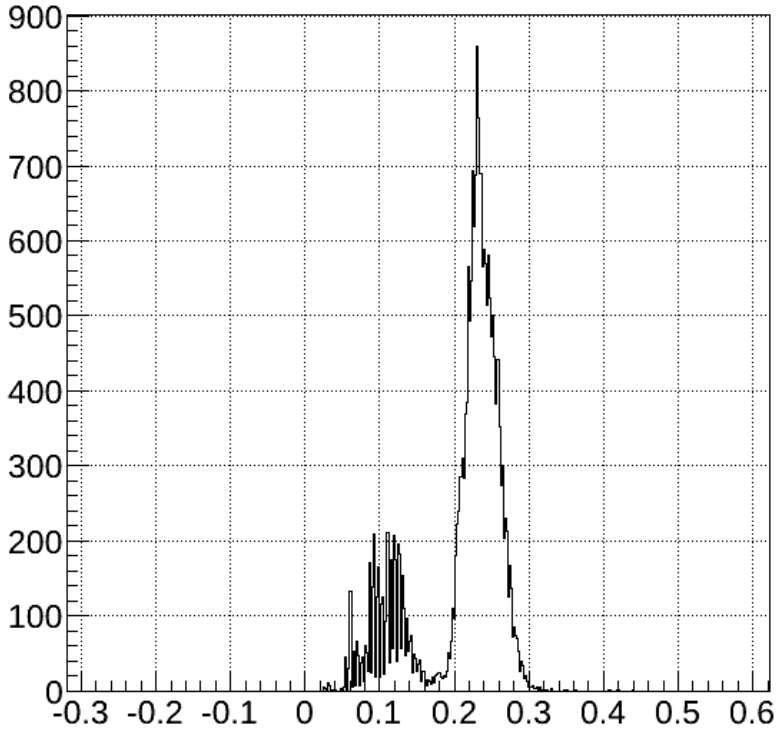


Tail cancellation network has ~4000 possible settings. Here only few are shown.

Example of Fe^{55} energy spectrum

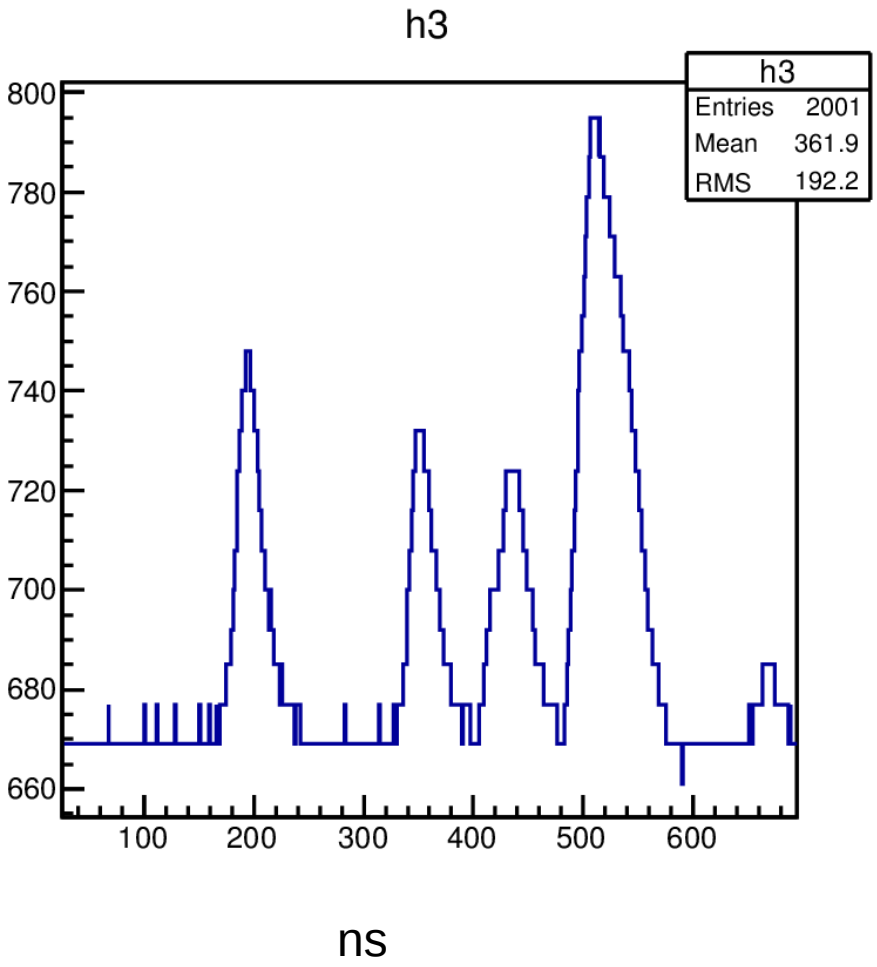


TOT measurement



Analog output measurement

Test beam results – will be covered in other talk here only example...



Summary and plans

- First prototype of front-end ASIC for STT produced
- Preliminary results encouraging
- Systematic tests in progress...
  - by now only the preliminary tests in configuration with tail cancellation done.
- Final architecture need to be decided based on TOT vs amplitude comparison
- Present chip comprises only basic channel functionality. In final one more channels and all peripherals need to be designed/added
- Present technology is AMS 0.35um, not yet fixed...
- Budget for PANDA at AGH-UST needs to be solved