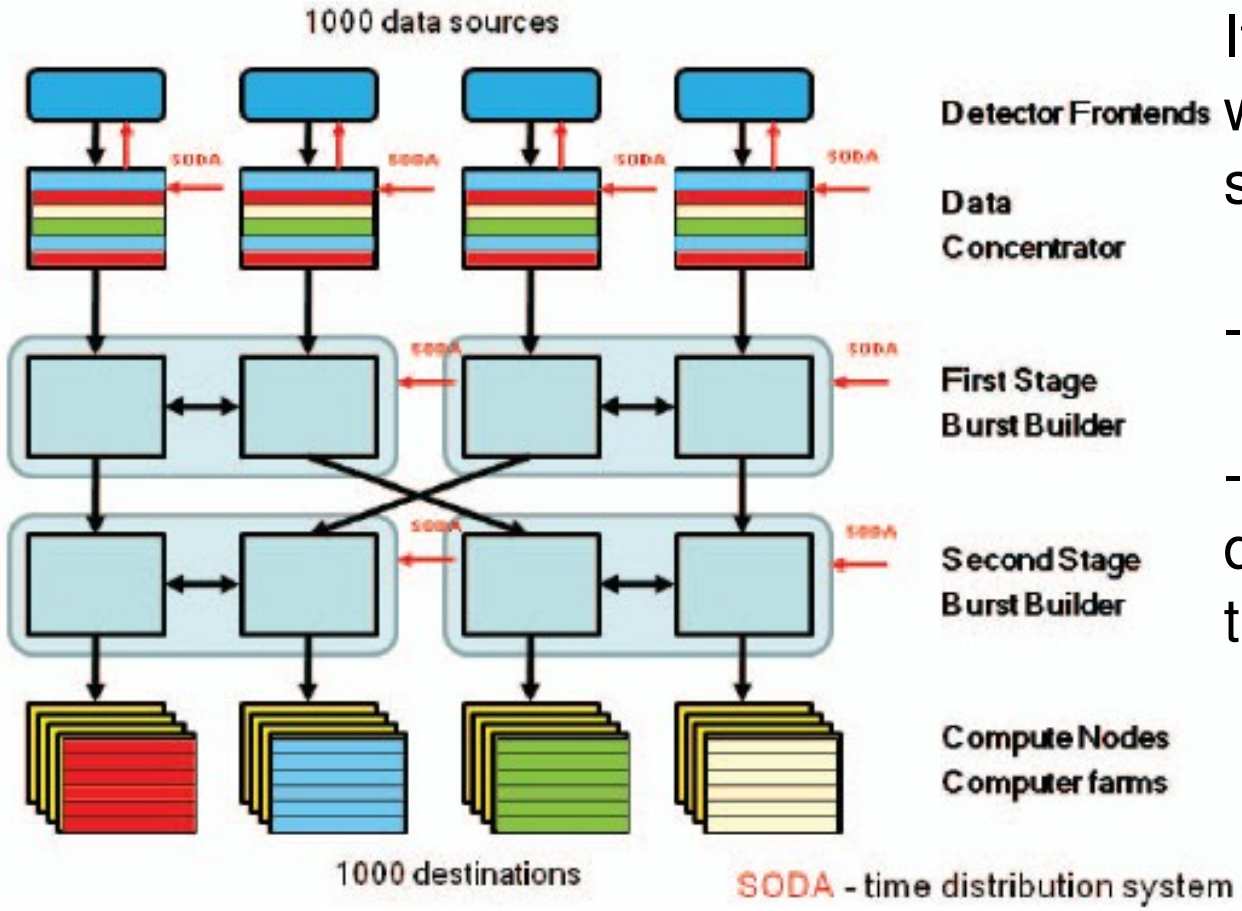
TRB – status of the development

Marek Palka

Requirements of the STT readout

- Central tracker : 4636 straws
- Forward tracker : ~13500 straws
- **Time measurement**: req. electronic resolution < 1 ns
- sensitivity (threshold) ~ 2 fC
- Hit rates up to 800 kHz/channel

Requirements of the STT readout

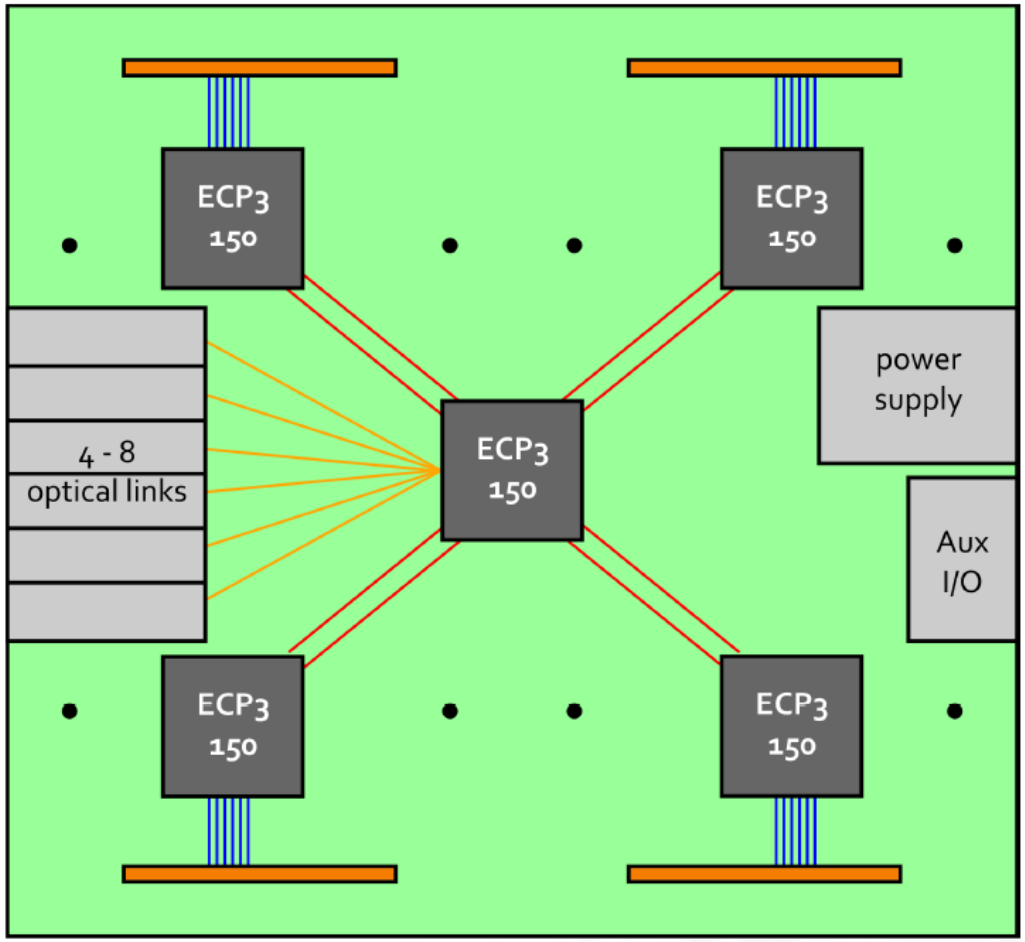


It has to be compatible with PANDA readout scheme:

- SODA

- Compute Node (send data from the given time intervals)

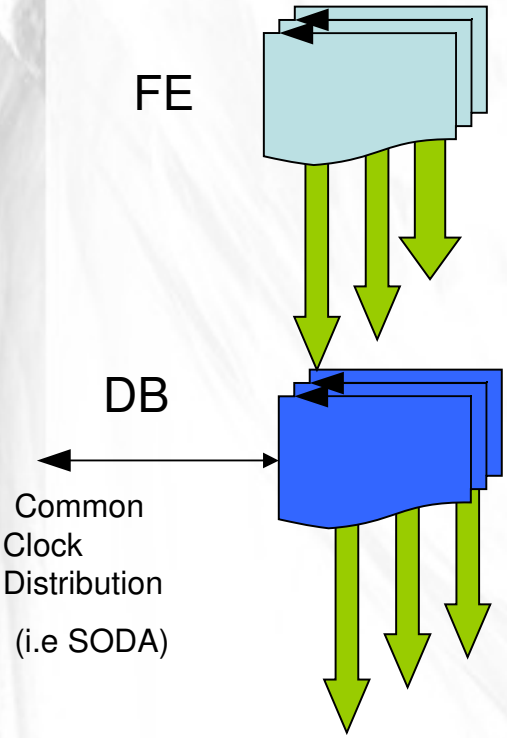
Concept of the STT readout

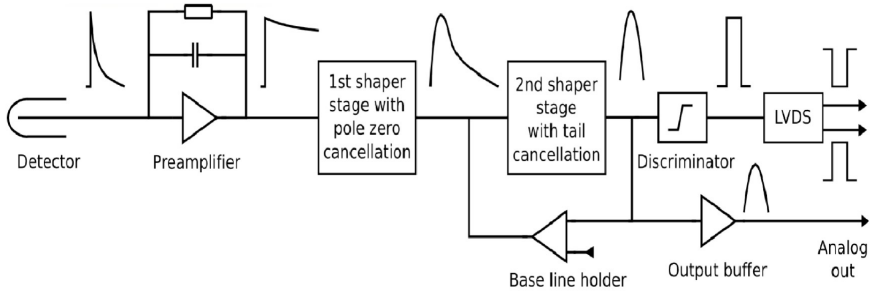


- 4 TDC in FPGA (Lattice ECP3M) up to 48 TDC channels per FPGA
- 1 FPGA for control (Run, Data, Slow-control)
- 8 x 3.2Gbit/s 8/10b serial links for data transmission
- interface for Add-On connectors : i.e ADC
- ~ 20 W power

TRB

FEE: M.Idzik
D. Przyborowski
AGH UST Cracow





196 TDC channels (and more...)

30 ps binning

< 20 ps TDC RMS

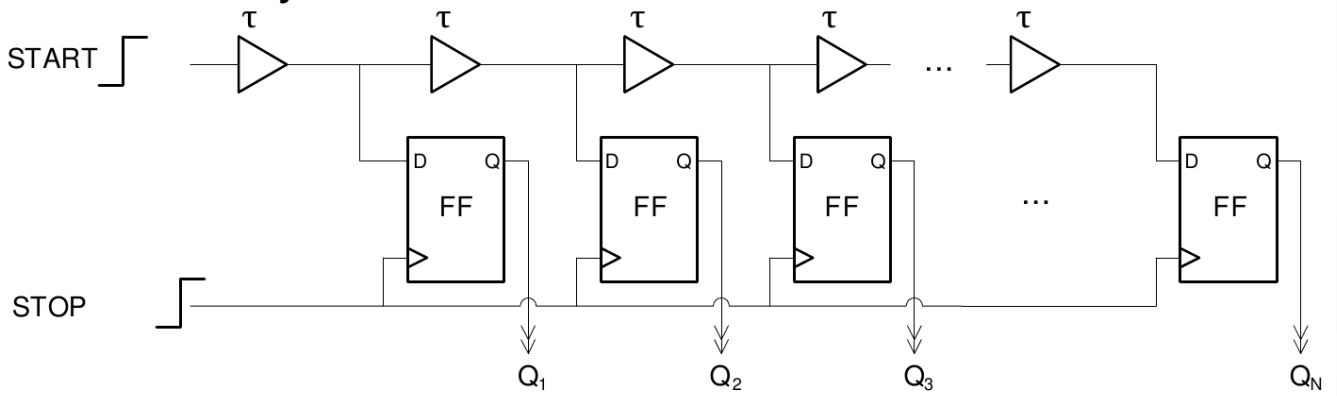
8 x 3.2 Gbit/s more than required Bandwith:

~5Gbit = 800kHz×
32Bits×
192ch.

TDC in the FPGA

Carry chain

TDC RMS < 20 ps



The transition from 0 to 1 (START signal) is saved in the FF array on the rising edge of the system clock (STOP signal)*

C.Ugur:
Already developed for “Exploder” board for the same FPGA family
Implementation started for the TRB

*E.Bayer, M.Traxler, A High Resolution (RMS) 48 Channel Time-to-Digital Converter (TDC) Implemented in a Field Programmable Gate Array (FPGA) , IEEE 17th Real Time Conference, IEEE Transactions on Nuclear Science, August 2011, Volume: 58, Issue:4, p.1547 - 1552

Gbit connections

G.Korcyl :

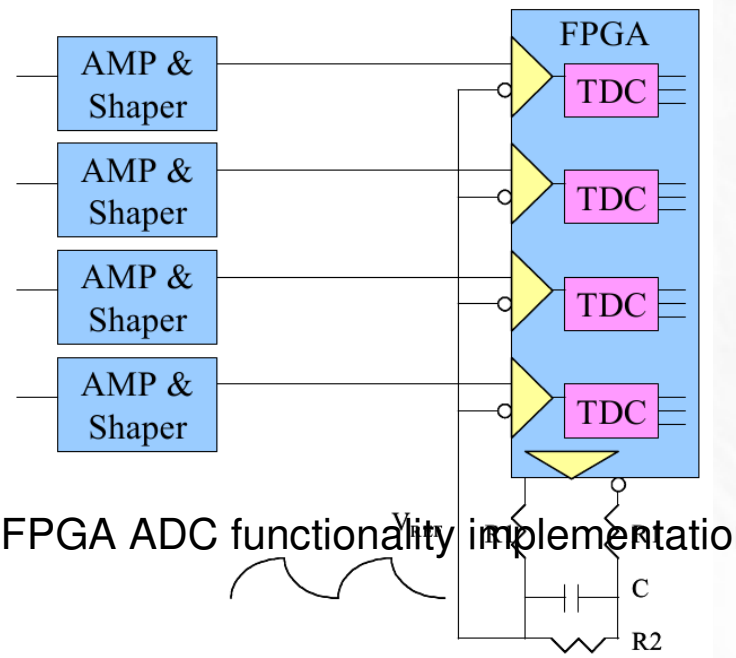
- Sending and receiving Ethernet packets is working,
- Implemented: DHCP, UDP, IP, ARP, ICMP,
- Slow control interface vi optical link,
- Established connection with Compute Node

Problems:

- Stability,
- Joining UDP packets in a larger one.

ADC functionality

1.



Scheme of FPGA ADC functionality implementation*

2. Plus current source to actively discharge capacitor

3. With discrimination, integration, base line restoring...

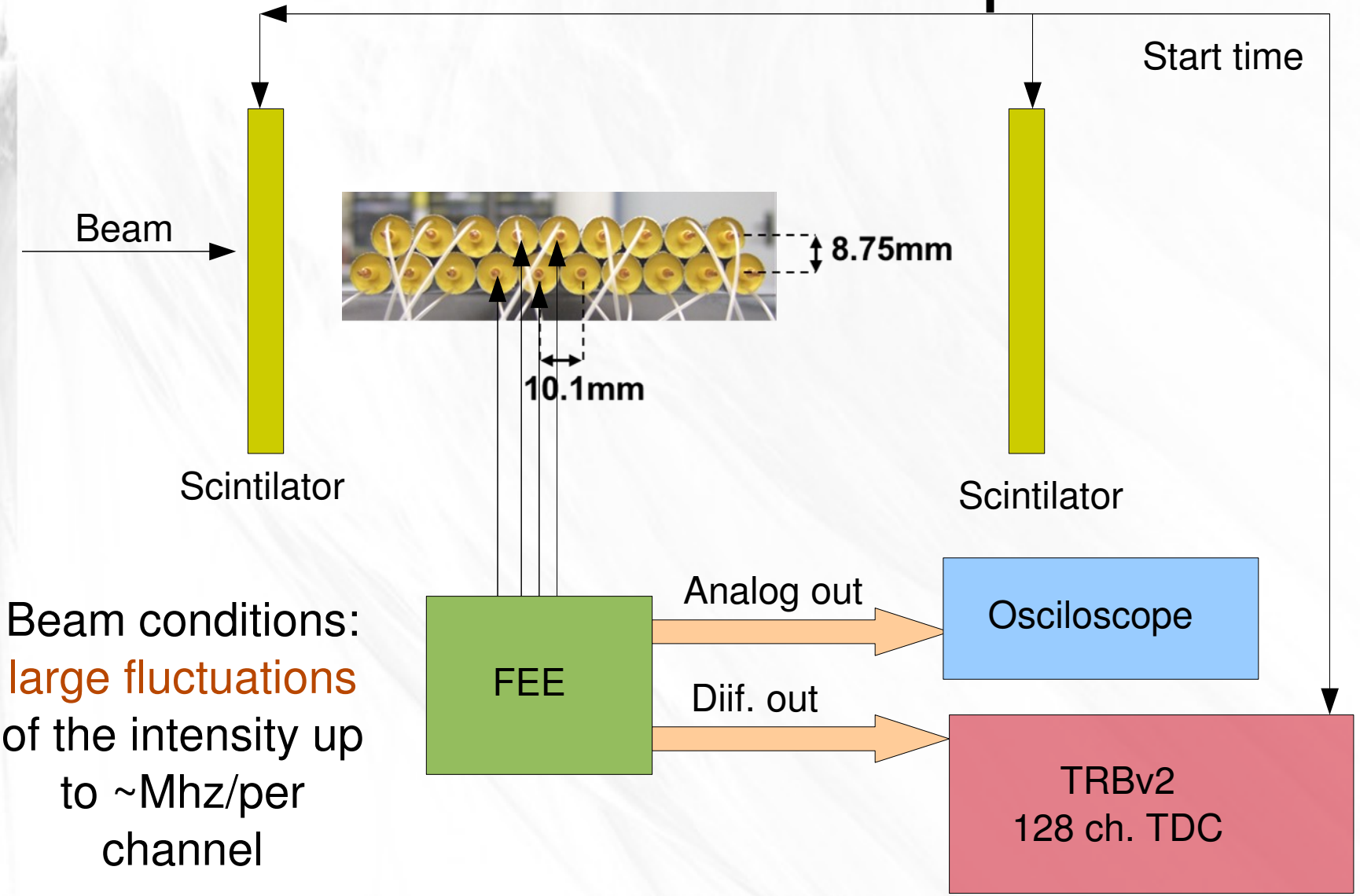
4. “Standard” ASIC AD ...

Four different ideas of ADC implementation will be tested on already developed board

*Jinyuan Wu; Hansen, S.; Zonghan Shi:ADC and TDC implemented using FPGA, Nuclear Science Symposium Conference Record, 2007. NSS '07. IEEE, Oct. 26 2007-Nov. 3 2007,

In beam STT test in Jülich FZ
28.11.2011-04.12.2011

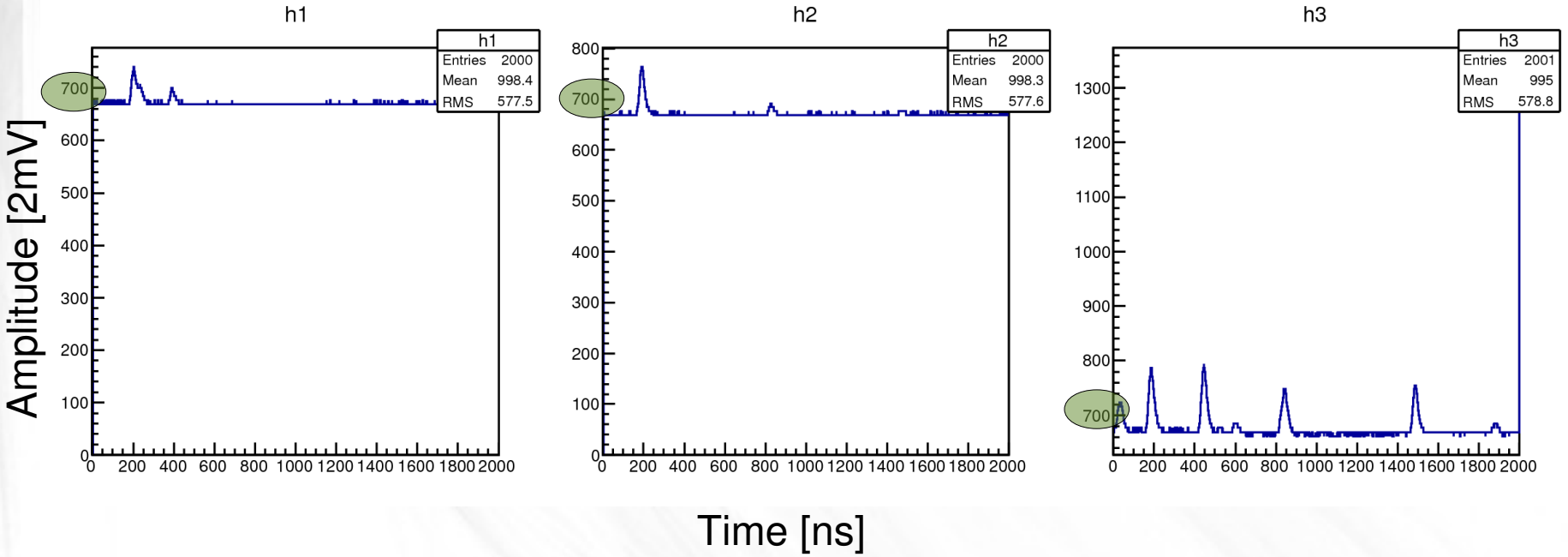
STT test setup



Beam conditions:
large fluctuations
of the intensity up
to ~Mhz/per
channel

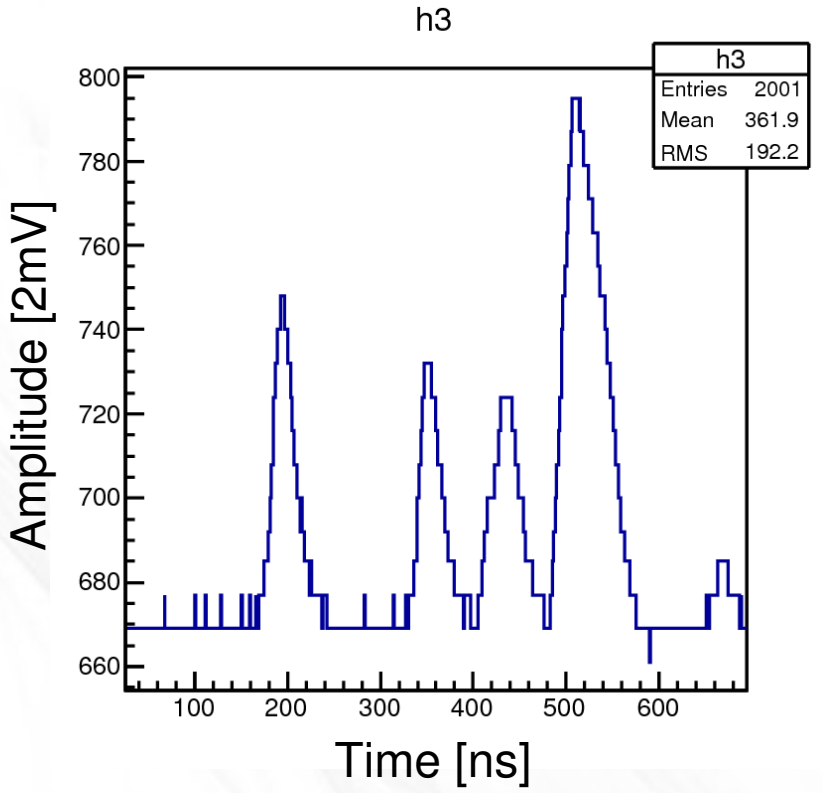
Oscilloscope measurements

The base line is stable

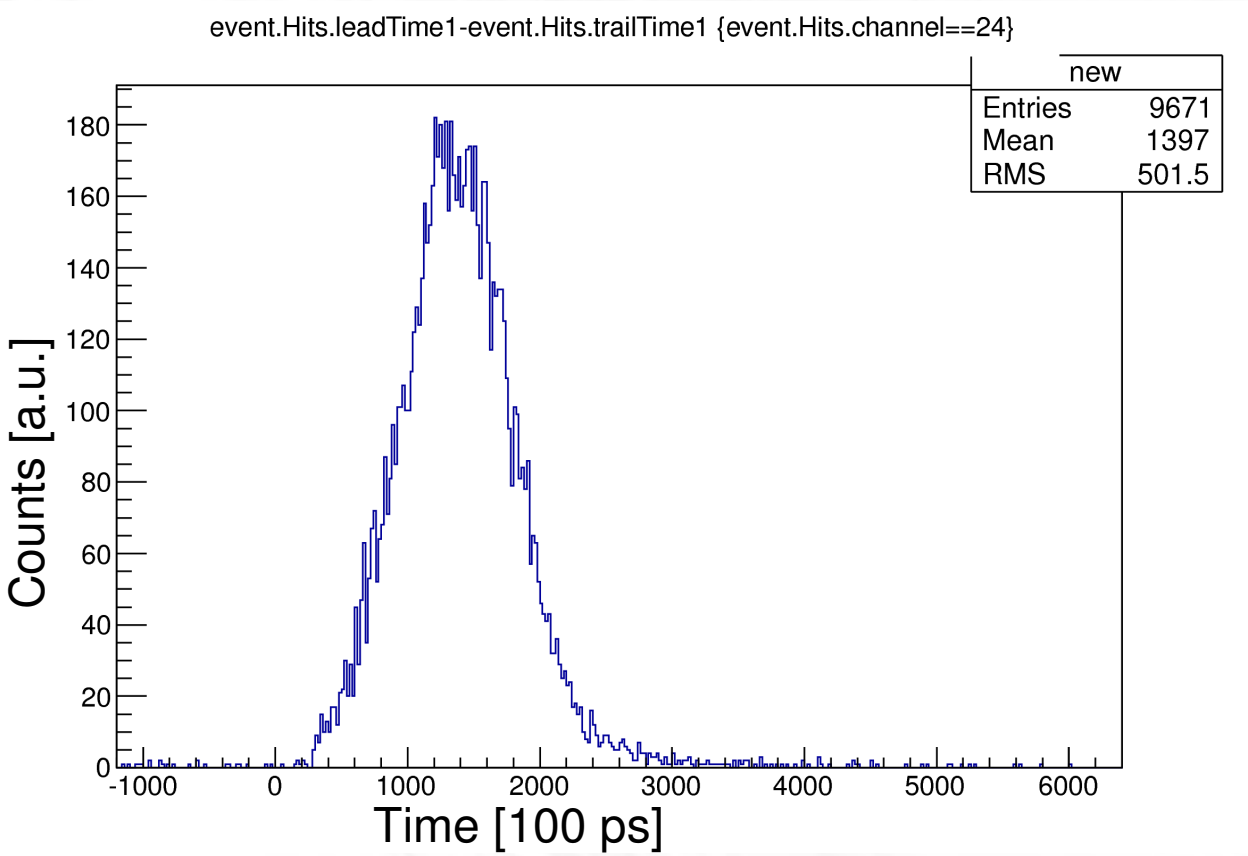


Oscilloscope measurements

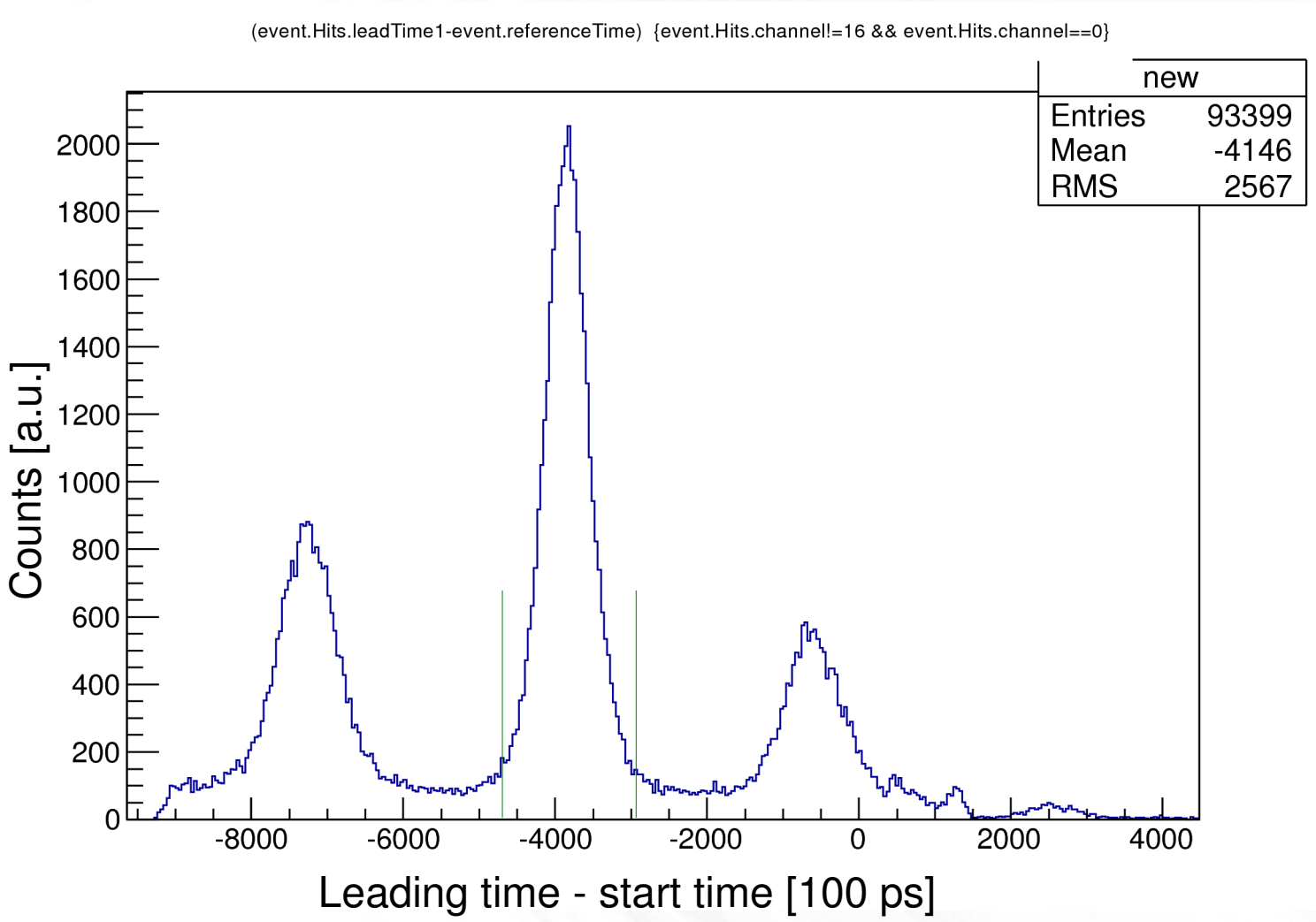
Tail cancellation works &
base line is stable



Time over Threshold



TRB measurements



TOT vs leading time