



PANDA Collaboration Meeting



Sezione di Torino

Pixel readout status report

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on behalf of the MVD Torino group



Pixel specs



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<i>Pixel size</i>	$100 \times 100 \mu\text{m}^2$
<i>Chip active area</i>	$11.4 \times 11.6 \text{ mm}^2$ (116 rows, 110 cols)
<i>dE/dx measurement</i>	ToT, 12 bits dynamic range
<i>Max input charge</i>	50 fC
<i>Noise floor</i>	$< 32 \text{ aC}$ (200 e^-)
<i>Clock frequency</i>	155.52 MHz
<i>Time resolution</i>	6.45 ns (1.9 ns r.m.s.)
<i>Power consumption</i>	$< 750 \text{ mW/cm}^2$
<i>Max event rate</i>	$6 \cdot 10^6$
<i>Total ionizing dose</i>	$< 100 \text{ kGy}$



ToPiX v3



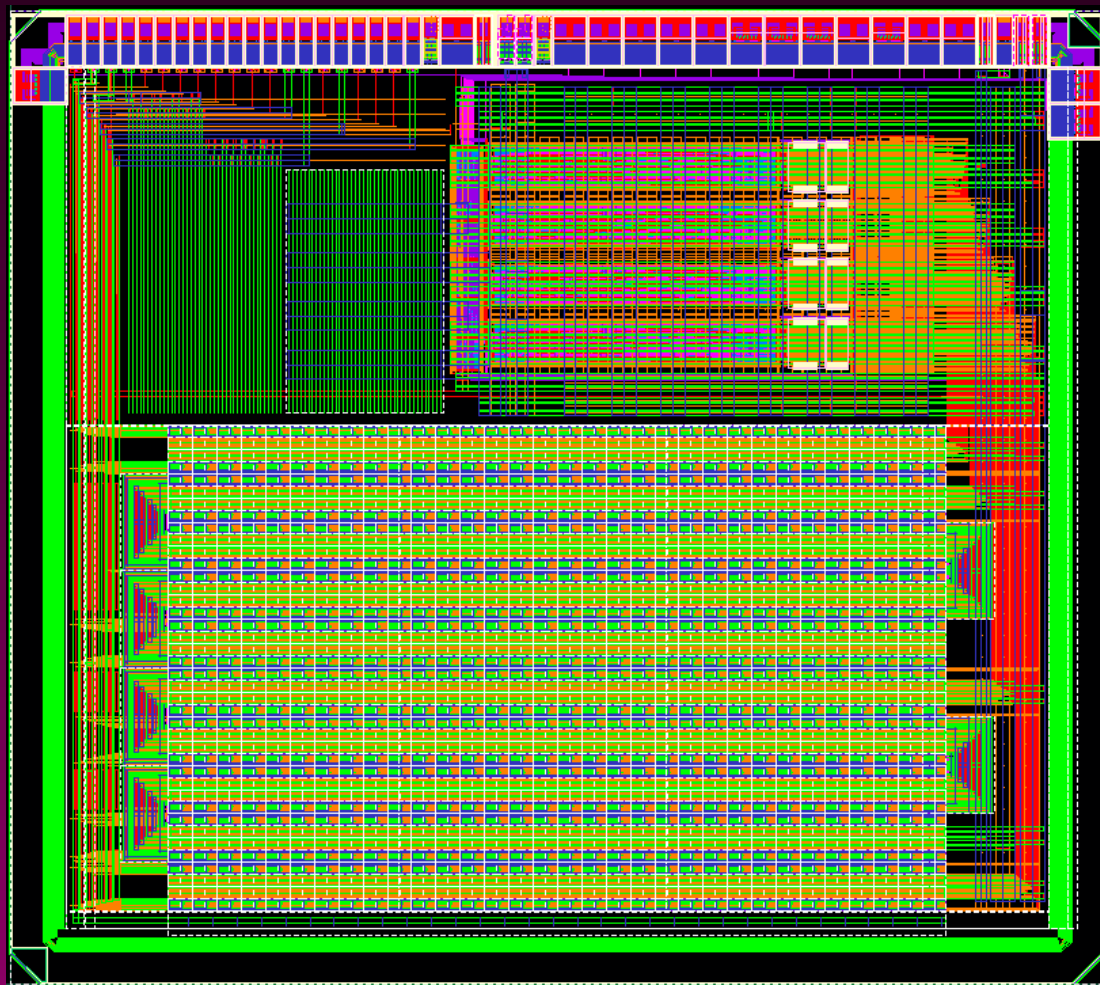
- Layout submitted on February 7th – received May 16th
- 4.5x4 mm² die area
- CMOS 0.13 μm DM technology
- Triple redundancy-based SEU protection
- End of column logic
- 160 Mb/s SLVS serial output
- Pads for bump bonding



ToPiX v3 layout



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- * 4.5 mm × 4 mm
- * CMOS 130 nm
- * Clock frequency 160 MHz
- * bump bonding pads
- * 2×2×128 columns
- * 2×2×32 columns
- * 32 cells EoC FIFO
- * SEU protected EoC
- * Serial data output
- * SLVS I/O

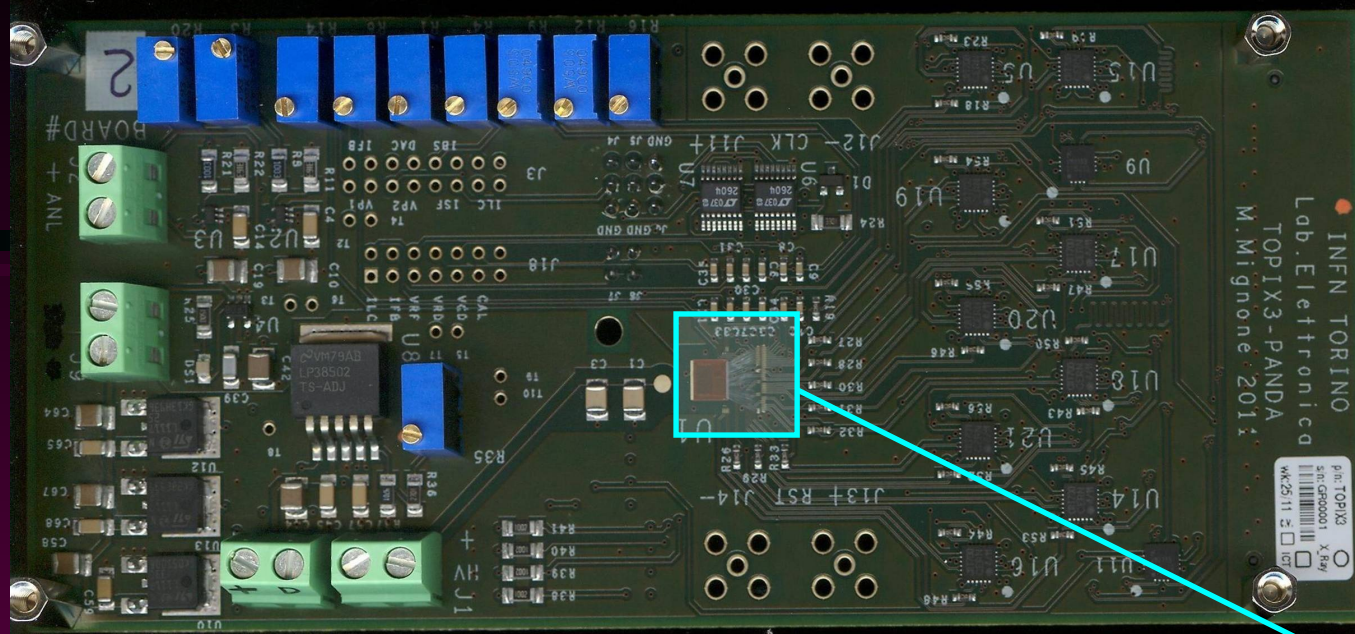


ToPiX v3 test status

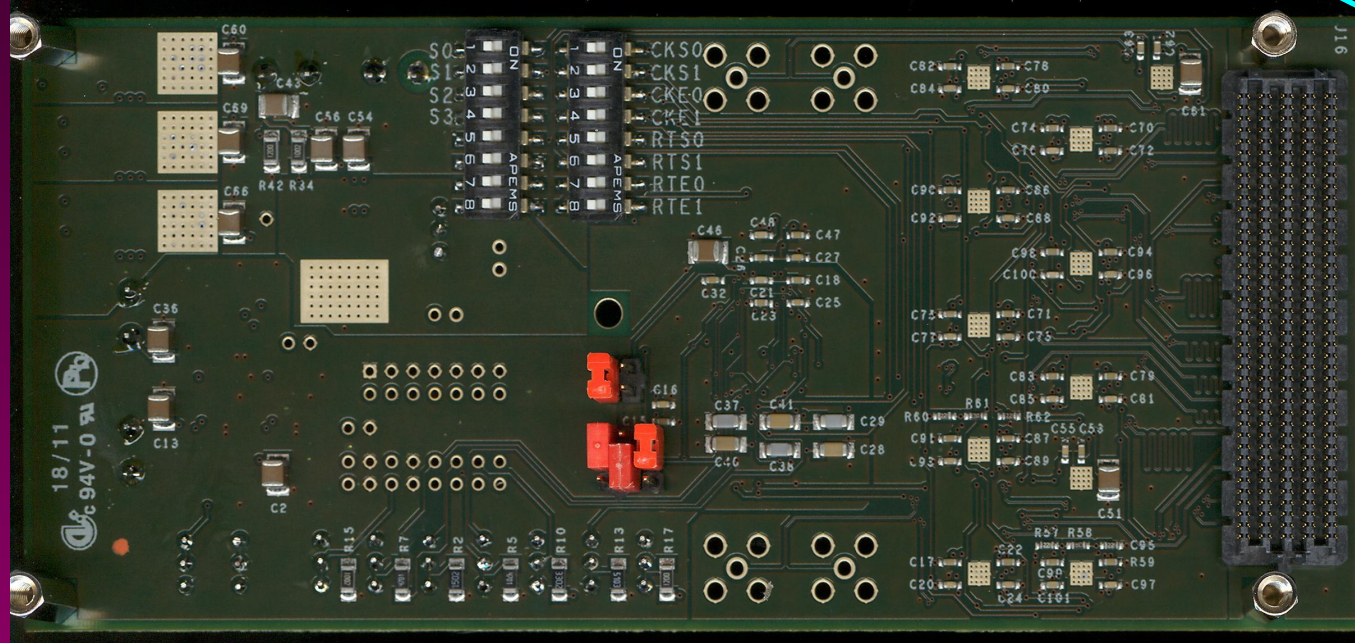
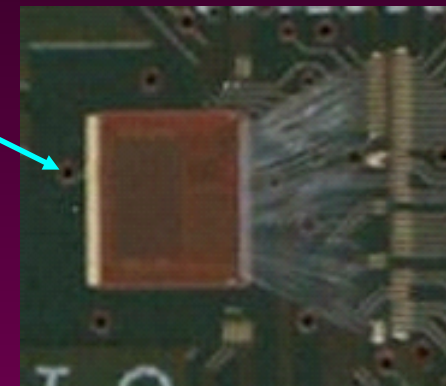


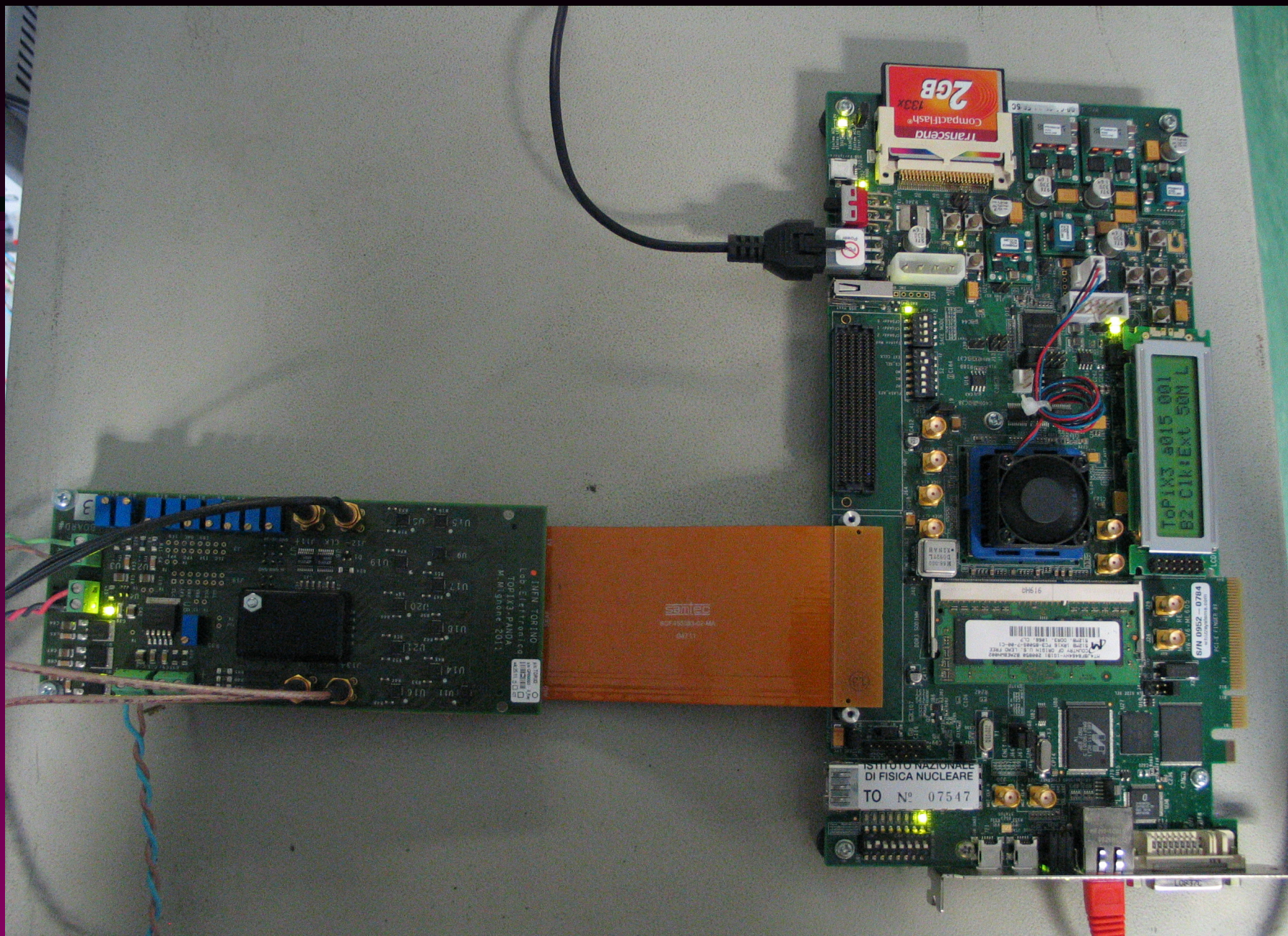
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- * At 160MHz can only read and program first ~32 pixels of each column
- * At 50MHz (with pre-emphasis disabled) full operation
- * S-curve working well (programmable internal test pulse)
- * Baseline measurements ok
- * On-pixel DACs characterised and correction applied
- * Transfer function measurements in good agreement with simulations
- * Acquisition system is working (4 boards)
- * Test beam results under analysis



ToPiX v3







Functional tests @ 50 MHz

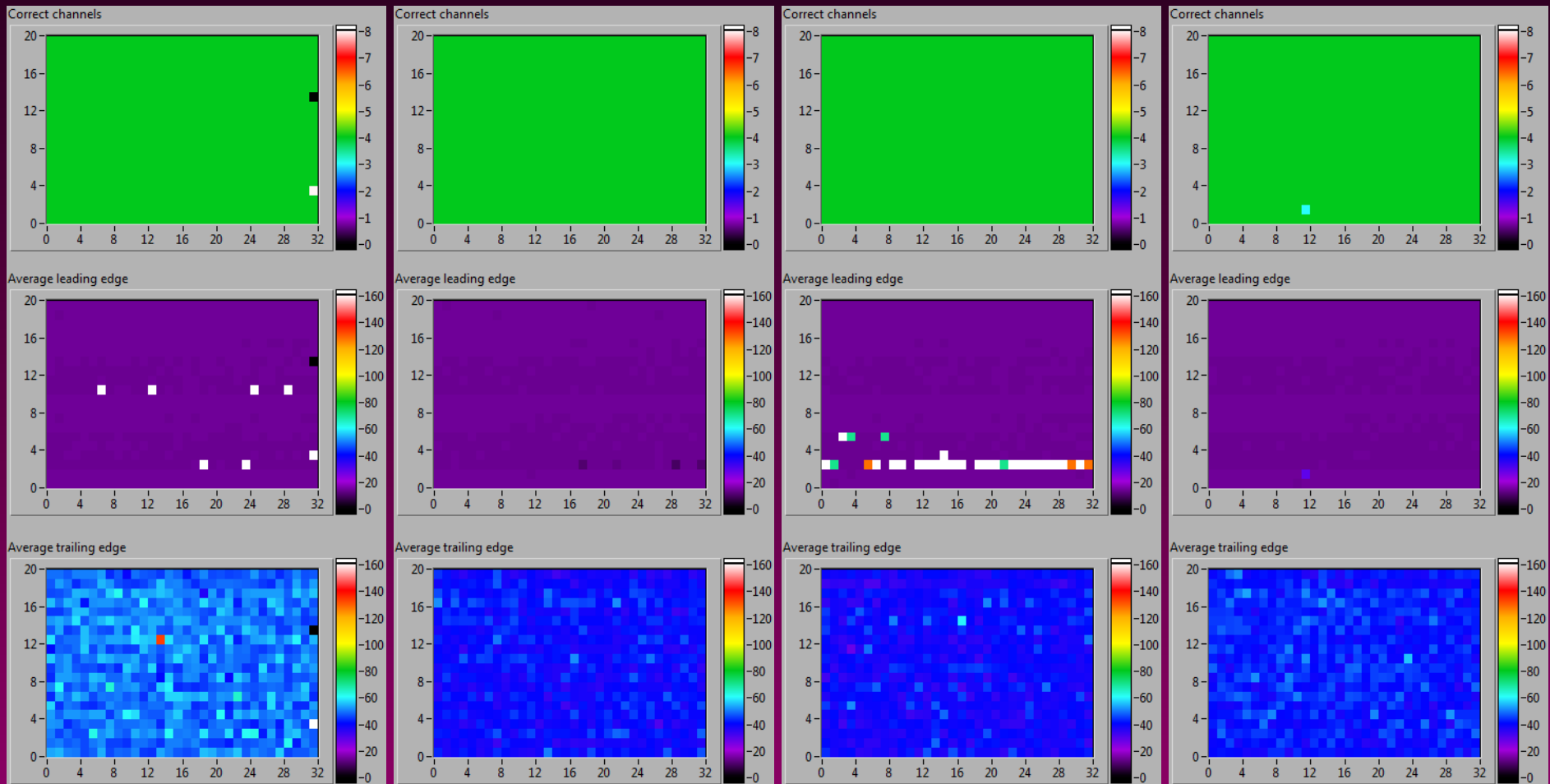


Chip 1

Chip 2

Chip 3

Chip 4

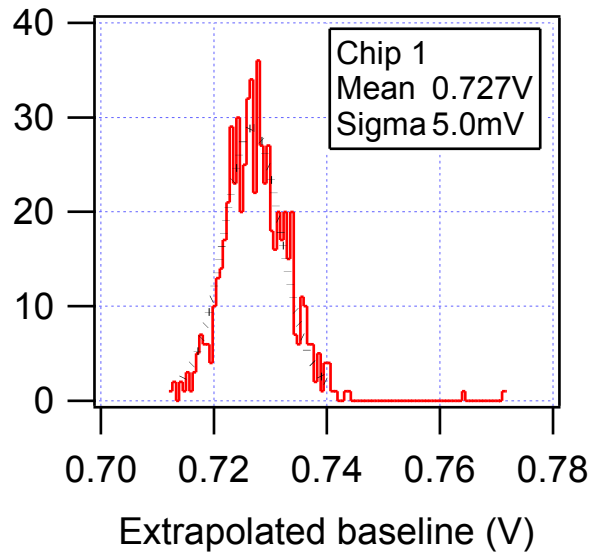
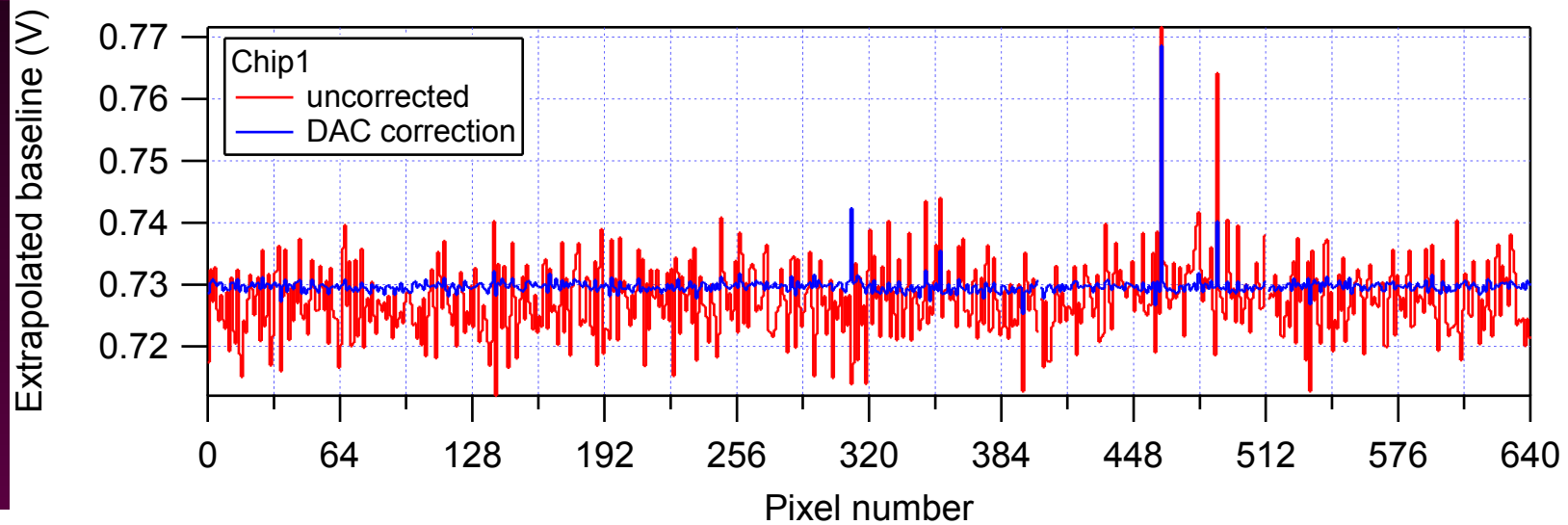




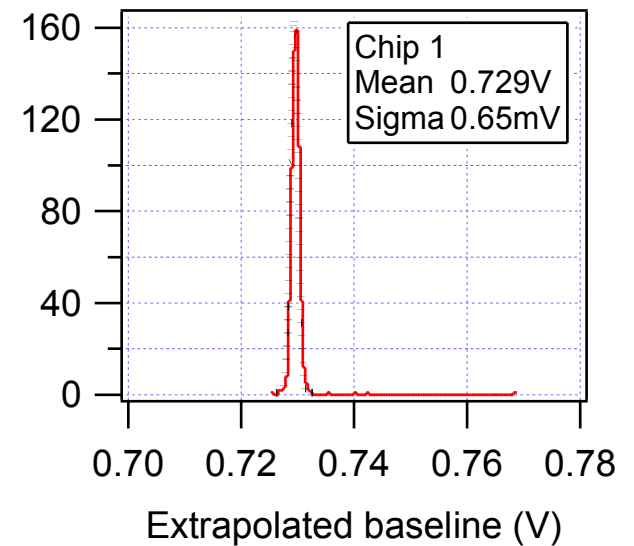
Baseline correction



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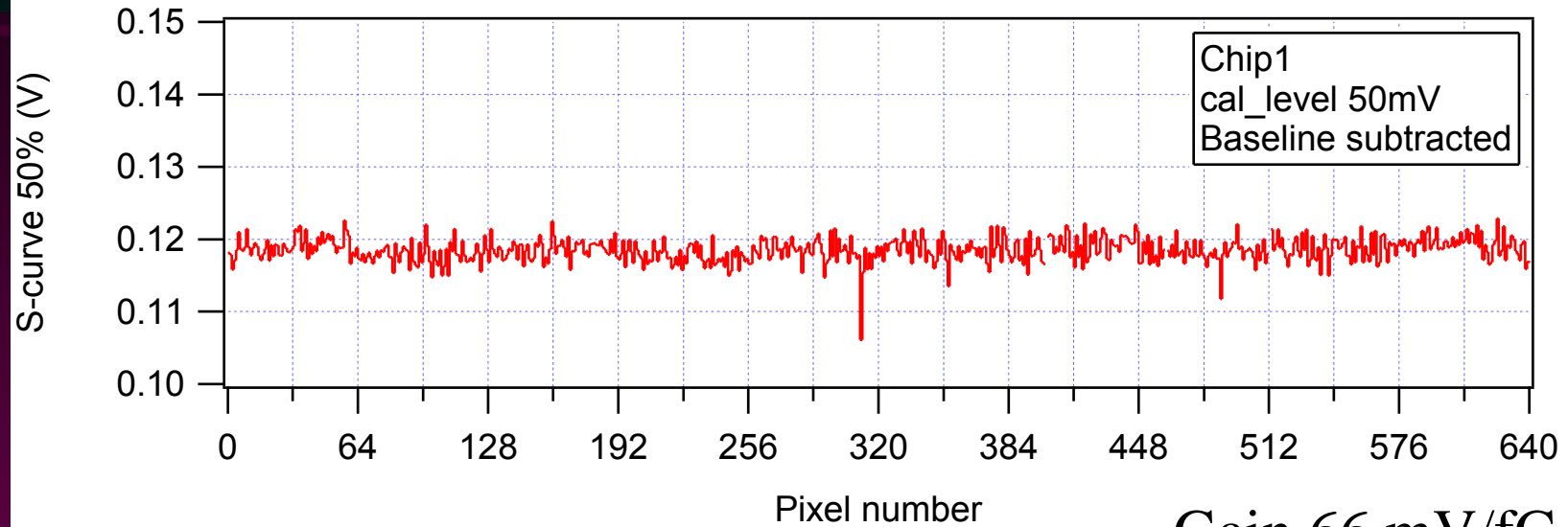


*DAC
correction*

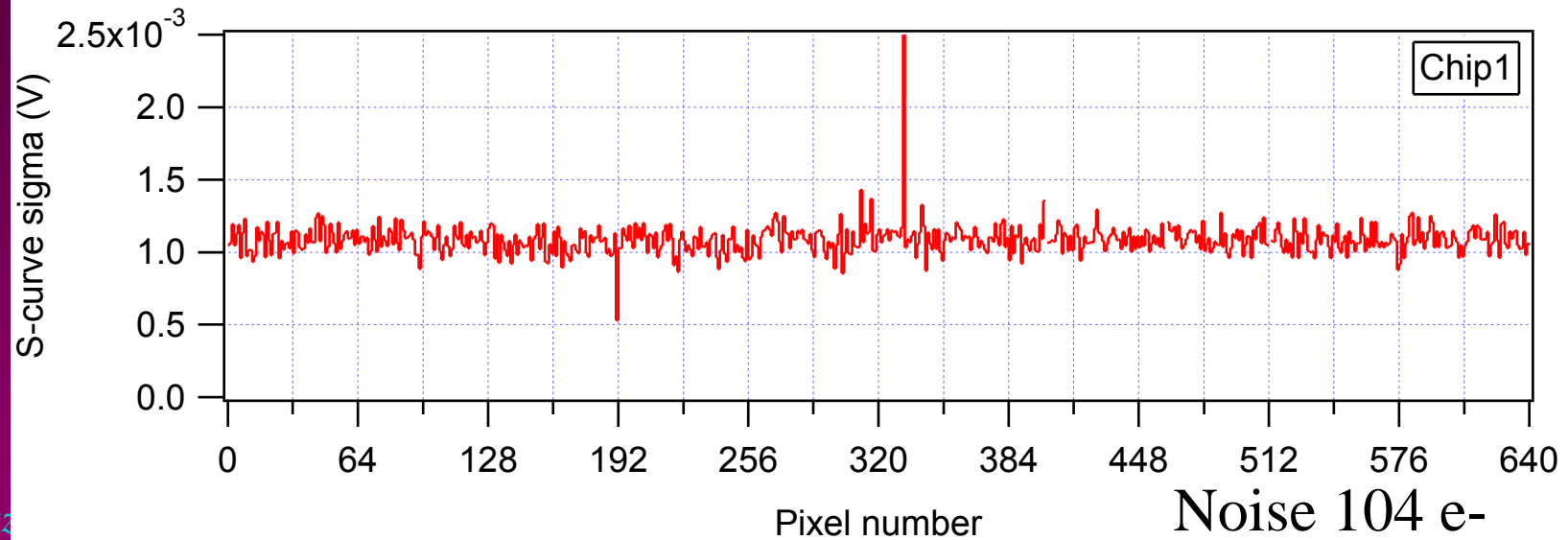




Gain & Noise



Gain 66 mV/fC



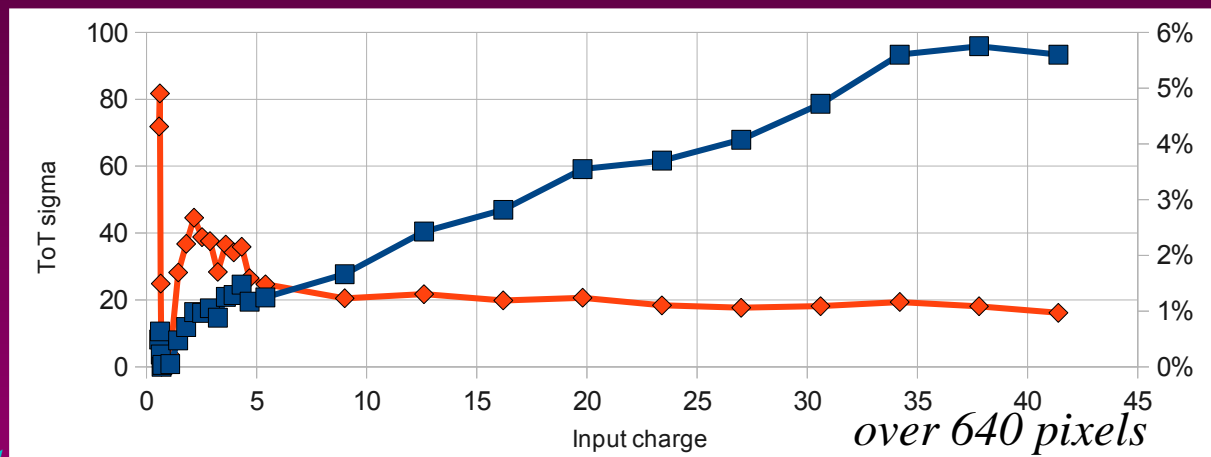
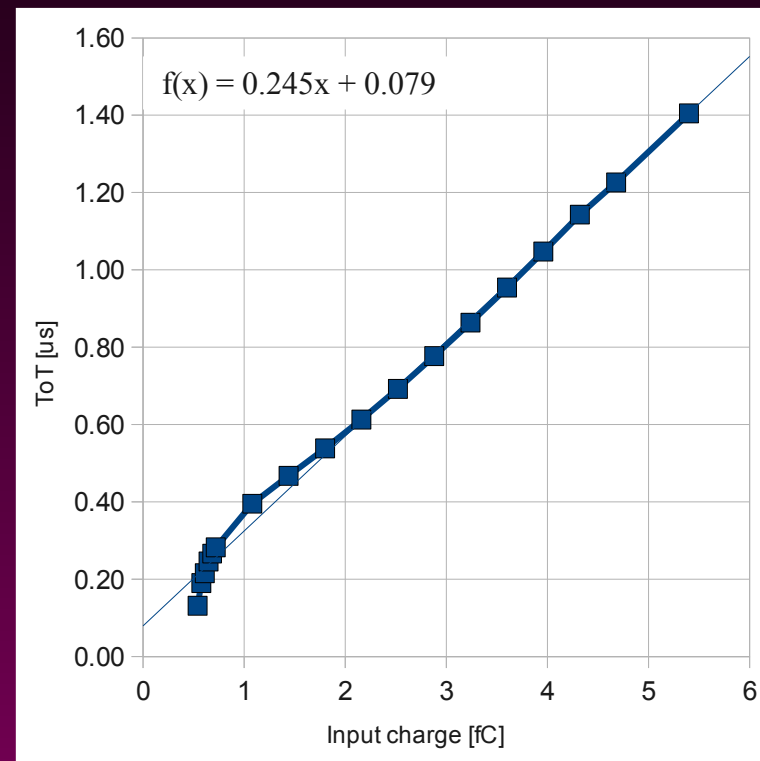
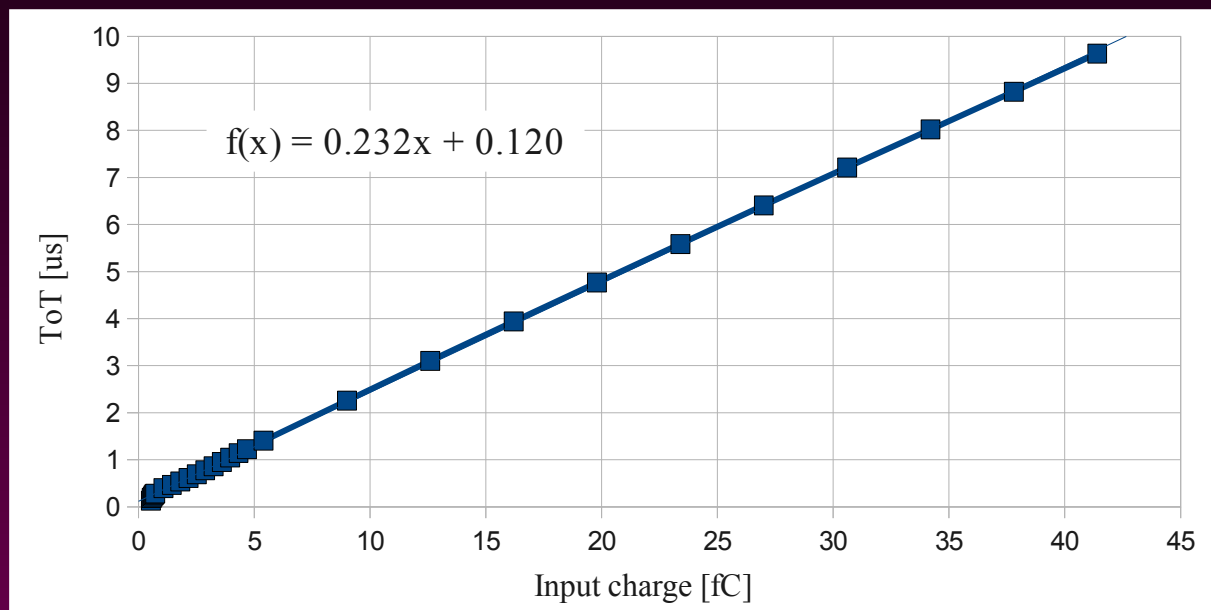
Noise 104 e-



ToT @ 5 nA



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$$I_{FB} = 5 \text{ nA}$$

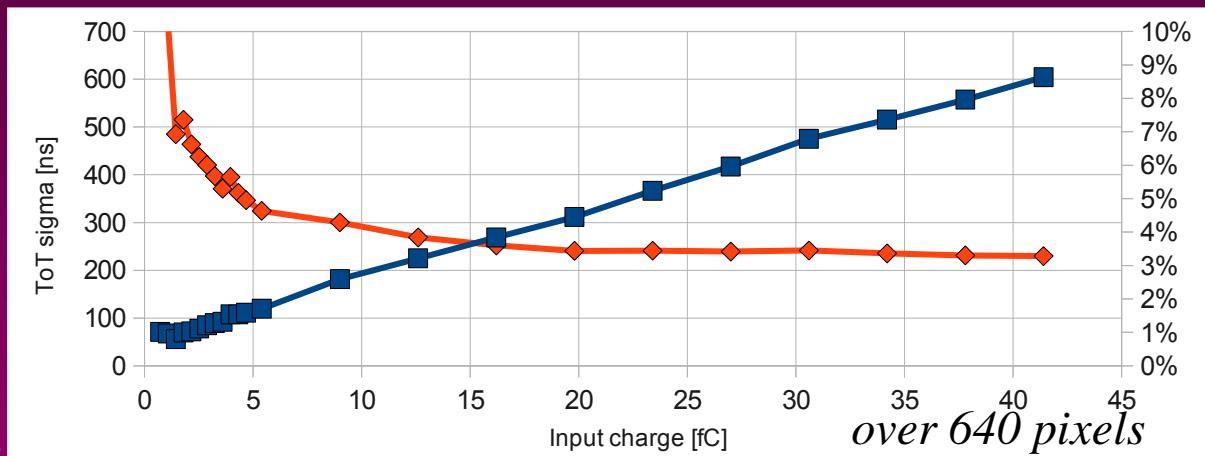
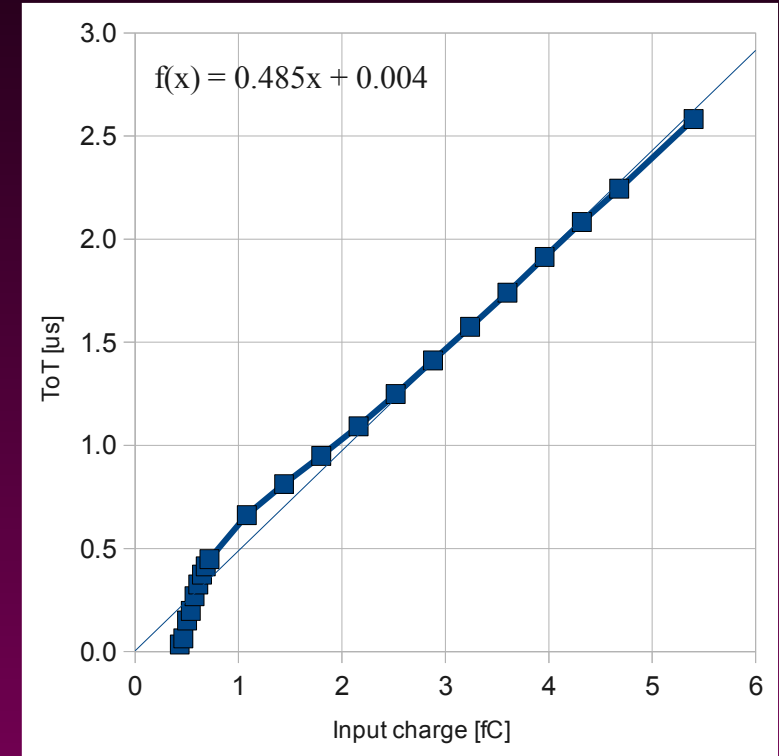
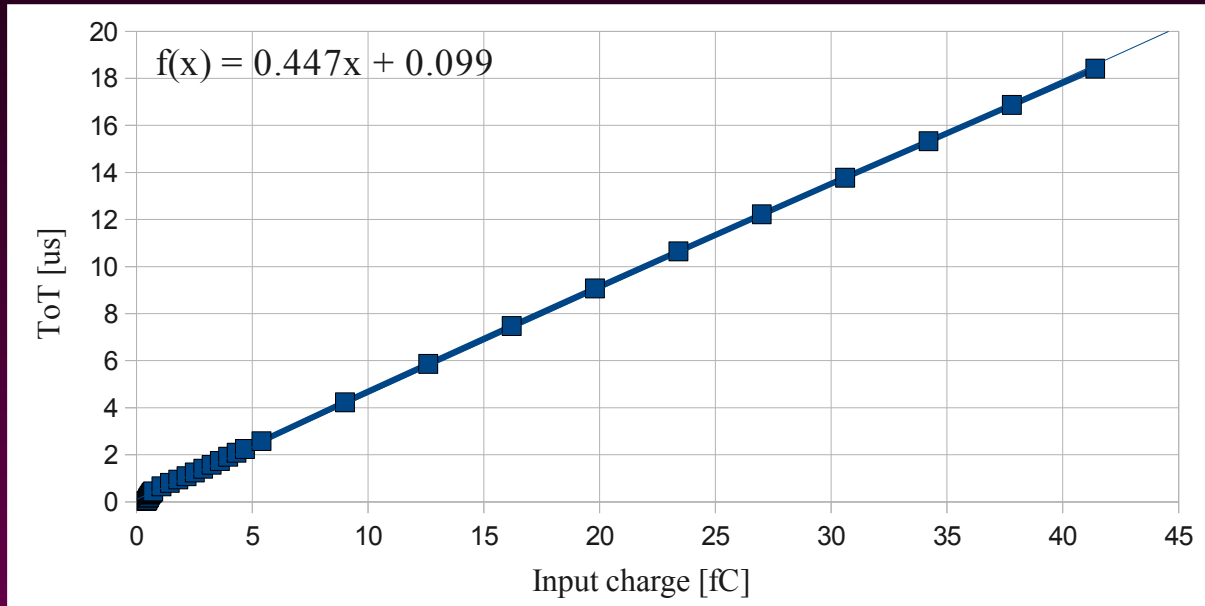
Simulated gain : 202 ns/fC



ToT @ 2.5 nA



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$$I_{FB} = 2.5 \text{ nA}$$

Simulated gain : 400 ns/fC



Clock frequency problem



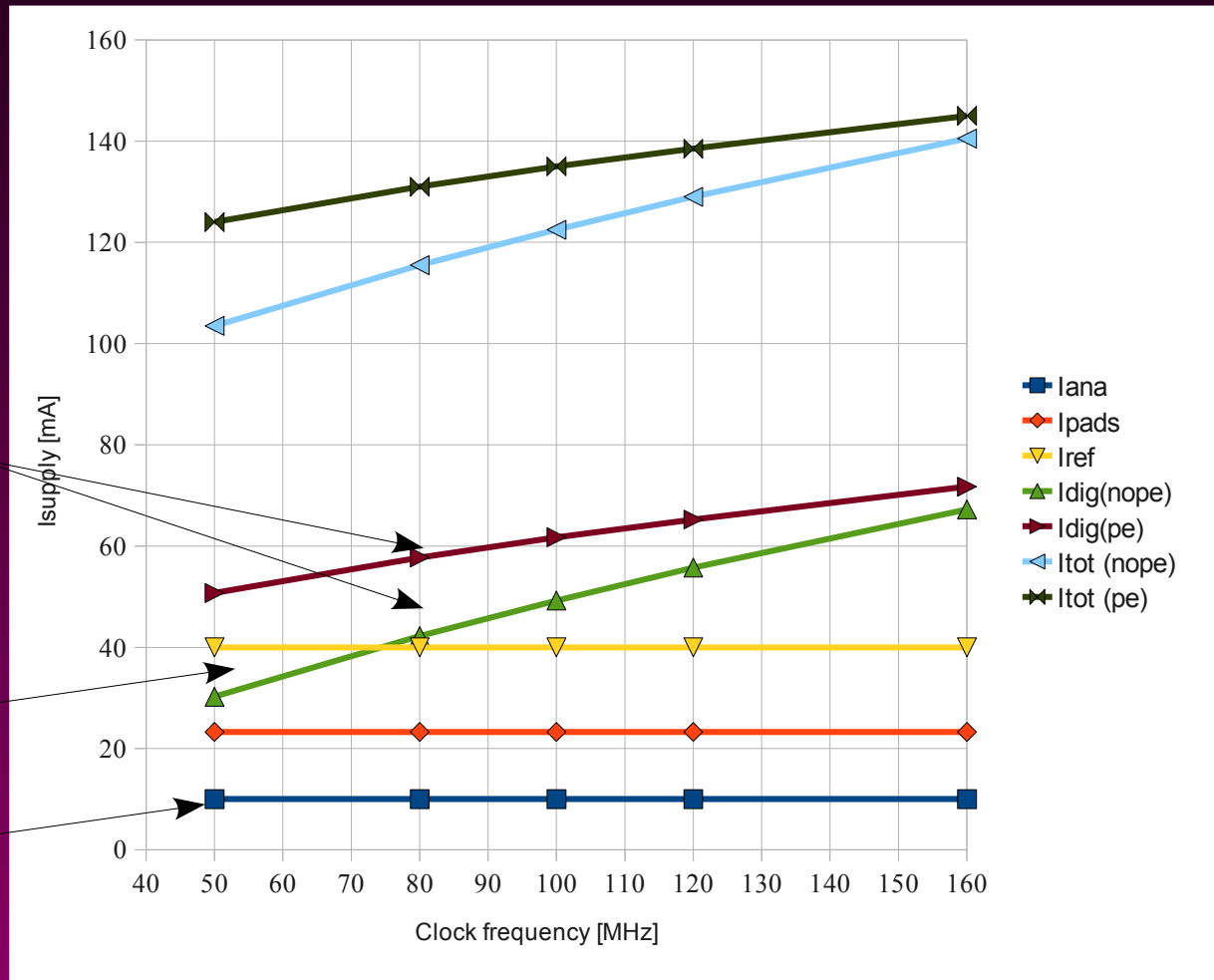
- * At 160 MHz only the first 32 pixels of the 128 cells columns work correctly
- * Response improves when the frequency is decreased
- * “Easy” corrections :
 - * *Prototype full column has 30% longer bus and 10% more cells than the final chip*
 - * *Triple redundancy latches have been connected without buffers*
- * Bus estimated capacitance : 47.35 fF/cell (55% due to the cell, 45% due to interconnection capacitance)
- * Total bus capacitance per line : 6.88 pF (now), 3.48 pF (est.)



Power supply



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55% from the time stamp counter

Can be made almost negligible (<50 μ A/double column in theory)

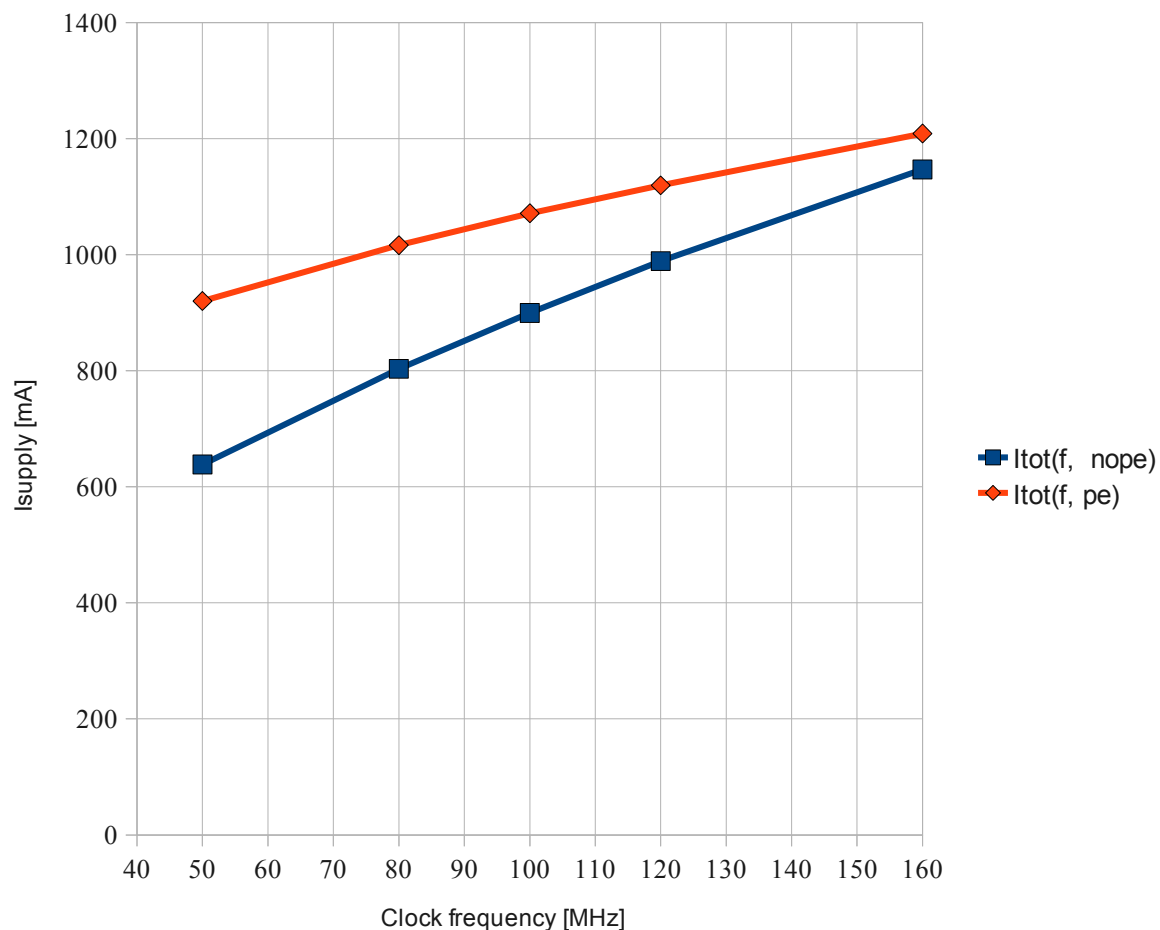
15 μ A/pixel



Full chip estimate



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- * Very rough estimate
- * Still room for improvements (ToPiX v3 not really designed having low power in mind...)
- * However, power consumption seems to be an issue
- * *Do we really need 1.9 ns time resolution ?*



ToPiX v3.1



- * Activity on the new ToPiX version started – main target is power reduction. Still margin for improvements - *ToPiX v3 was definitely not designed for low power...*
- * Custom standard cell library from MediPix collaboration has been analyzed – modifications started to be compatible with the ToPiX requirements.
- * Time stamp bus re-design is required. Targets are capacitance and voltage swing reduction
- * Review of the time resolution requirement is suggested – *speed does not come for free...*



New library



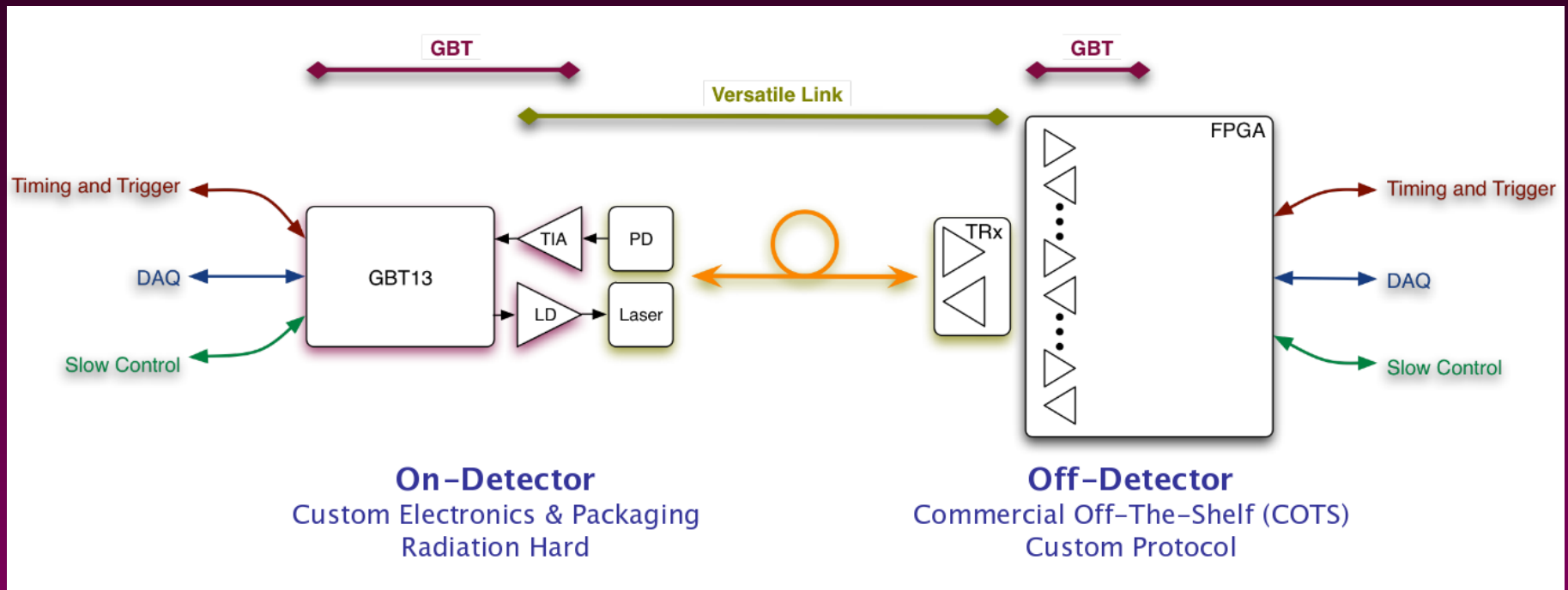
- * Developed at CERN by the MediPix group
- * Cells height : 2.4 μm (IBM library : 4.8 μm)
- * N. of cells : 43 (IBM library : 361)
- * Based on low power transistors for low leakage
- * Characterization with the Cadence Encounter Library Characterization (ELC) tool
- * Requirements for PANDA :
 - * move to normal transistors
 - * add more cells



GBT



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Conclusions



- * Electrical tests of the ToPiX v3 almost completed – chip is functionally ok, but a time stamp distribution problem limits the maximum speed
- * Irradiation tests performed, results under analysis
- * Beam test performed, results under analysis
- * Preliminary work for the new ToPiX prototype has started – the target is to reduce the on-pixel digital part size and the time stamp bus capacitance
- * Power consumption is an issue. The time stamp distribution is a dominant contribution



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Backup slides



GBT chipset



Radiation tolerant chipset :

- * GBTIA : Transimpedance optical receiver
- * GBLD : Laser driver
- * GBTx : Data and Timing Transceiver
- * GBT-SCA : Slow control ASIC

Target Applications :

- * Data readout
- * TTC
- * Slow control and monitoring links

Supports :

- * Bidirectional data transmission
- * Bandwidth :
 - Line rate : 4.8 Gb/s
 - Effective : 3.36 Gb/s

Radiation Tolerance :

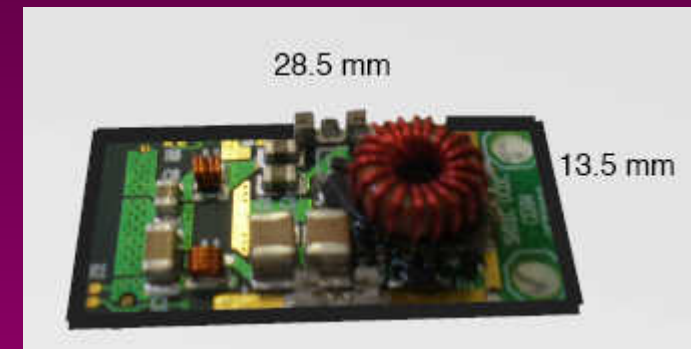
- * Total dose
- * Single Event Upset



Power regulator



- * ToPiX power supply $1.2 \text{ V} - I_{\text{DC}} \sim 1 \text{ A}$ (estimated)
→ voltage drop on cables is not negligible
- * A DC-DC converter solution compatible with the radiation levels and the magnetic field of a silicon tracker is under development @ CERN for sLHC
- * Current CERN version : $V_{\text{IN}} 10 \div 12 \text{ V}$, $V_{\text{OUT}} = 1.8 \div 3.3 \text{ V}$, $I_{\text{OUT}} < 3 \text{ A}$
- * $V_{\text{OUT}} = 1.5 \text{ V}$, $I_{\text{OUT}} < 3-4 \text{ A}$ now avail.
- * Board position t.b.d.
→ *ToPiX internal regulator t.b.d.*



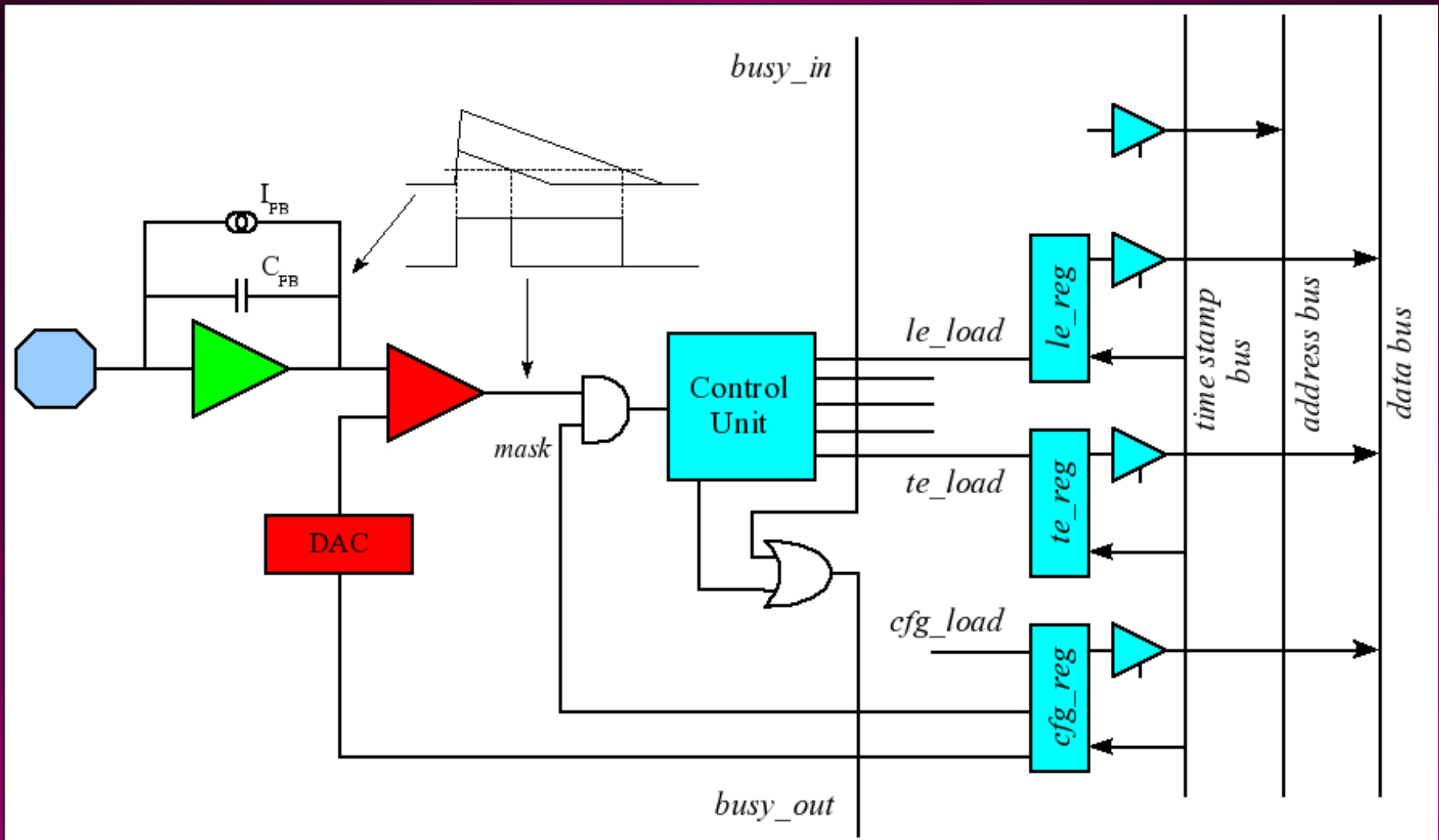


ToPiX ASIC



- * Custom development for the PANDA MVD
- * Provides spatial and time coordinates plus energy resolution measurement (via ToT)
- * Compatible either with p-type or n-type detectors
- * Self triggered architecture
- * Each event has a 12 bits time reference
- * Double rate serial readout
- * Radiation tolerant
- * Data corresponding to a 12 bits counter cycle (26.21 μ s) are packed in a frame, with an 8 bits frame counter (6.71 ms cycle)

Pixel cell

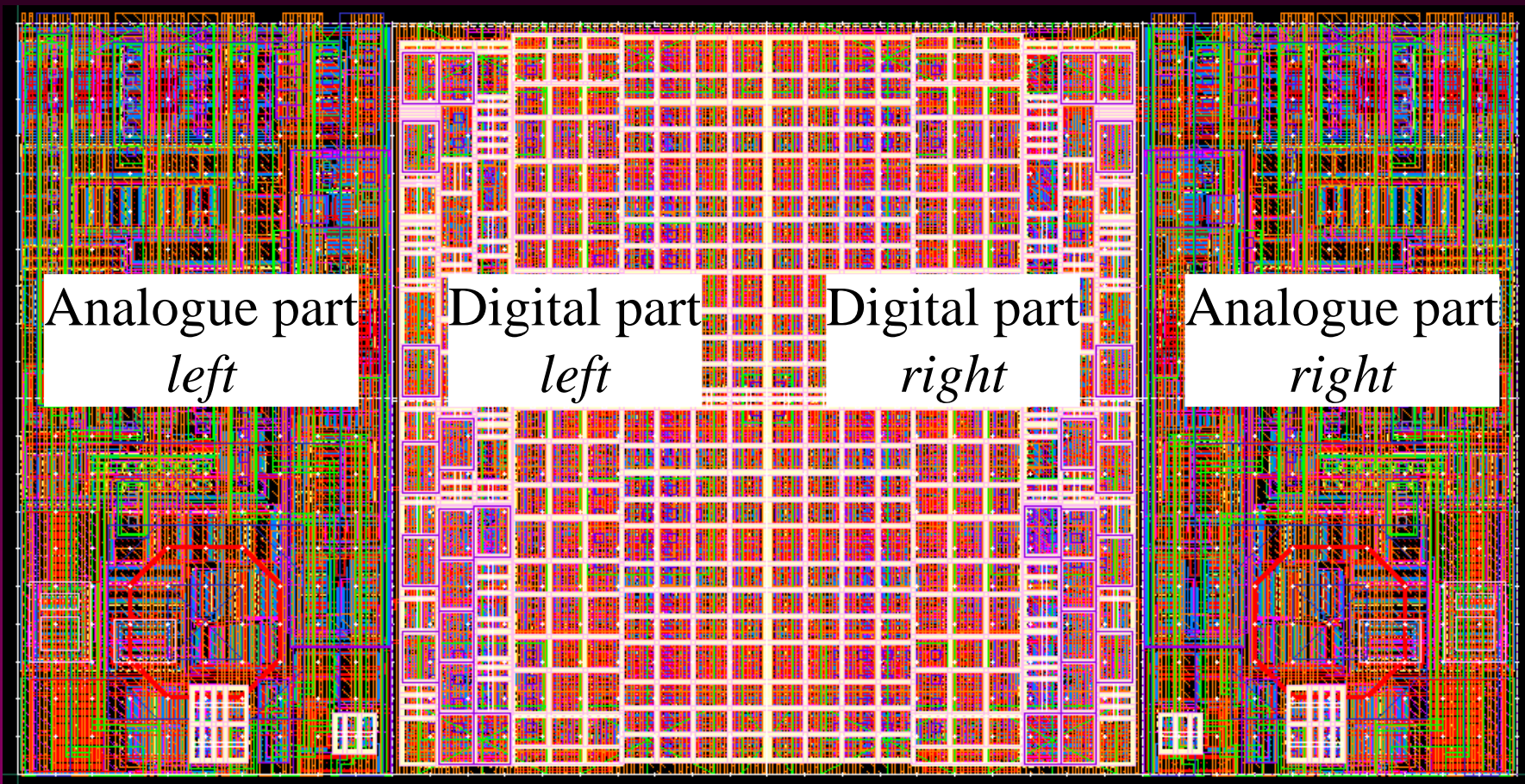




Double cell



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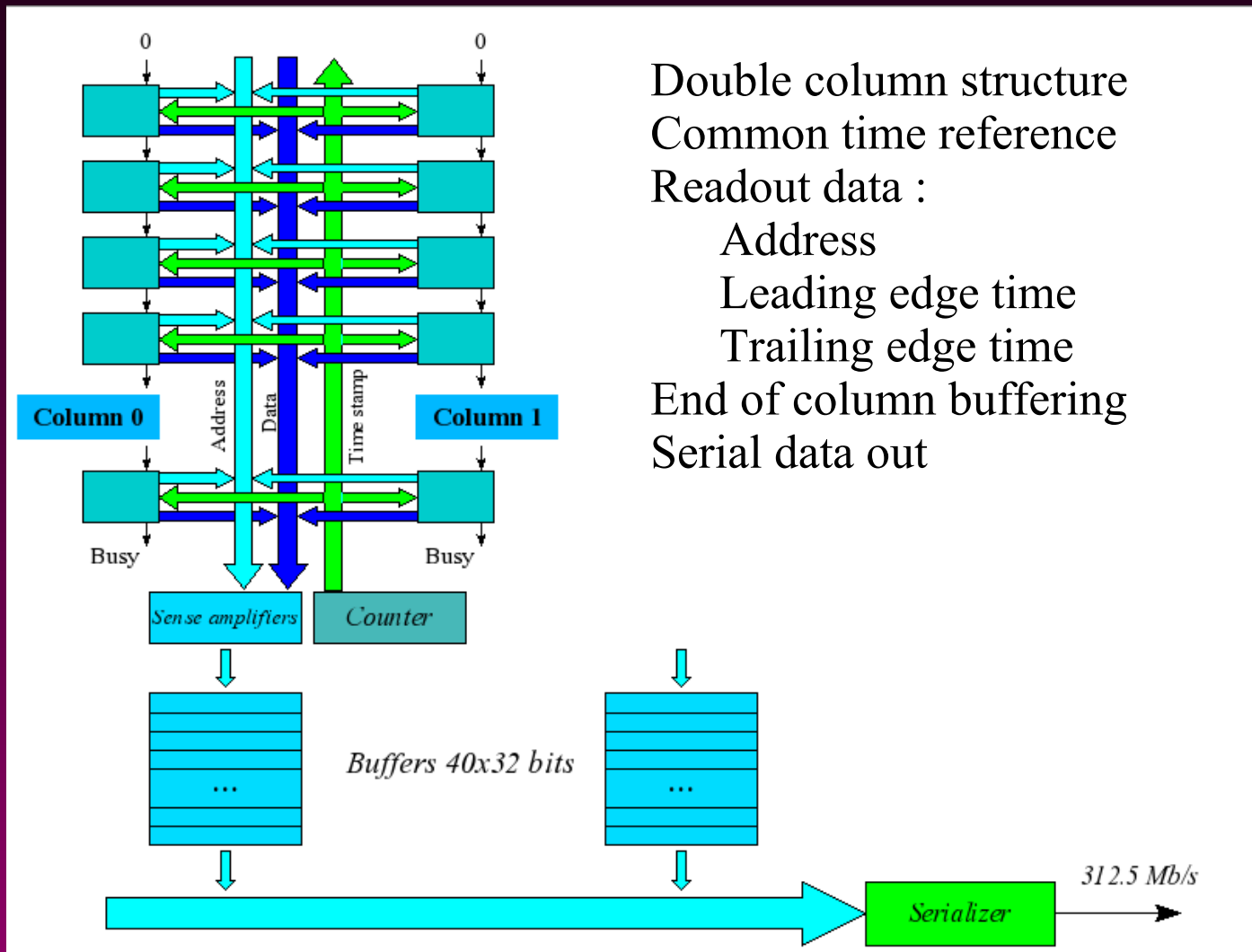
Analogue part
left

Digital part
left

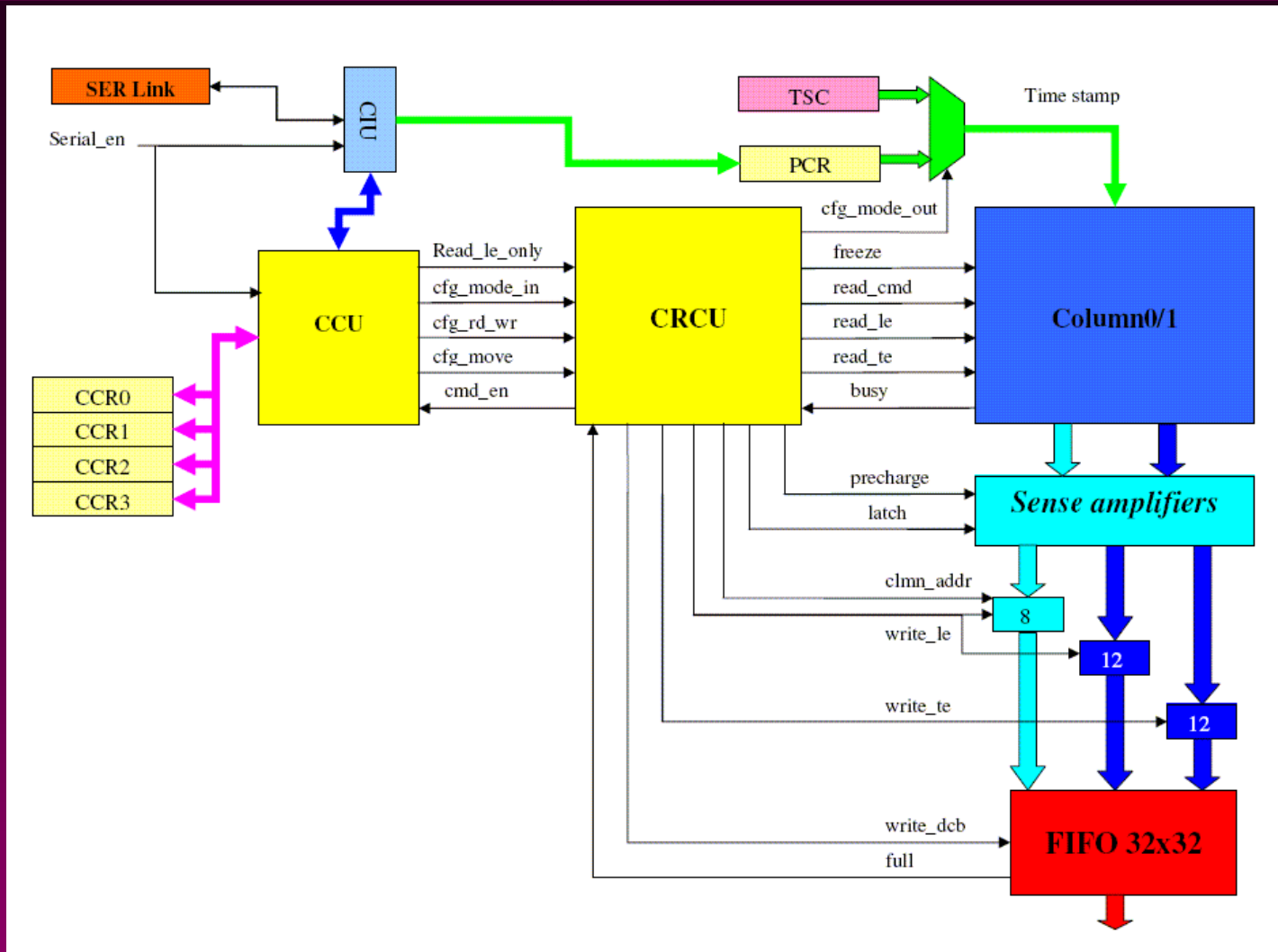
Digital part
right

Analogue part
right

Common bus



Double column structure
 Common time reference
 Readout data :
 Address
 Leading edge time
 Trailing edge time
 End of column buffering
 Serial data out

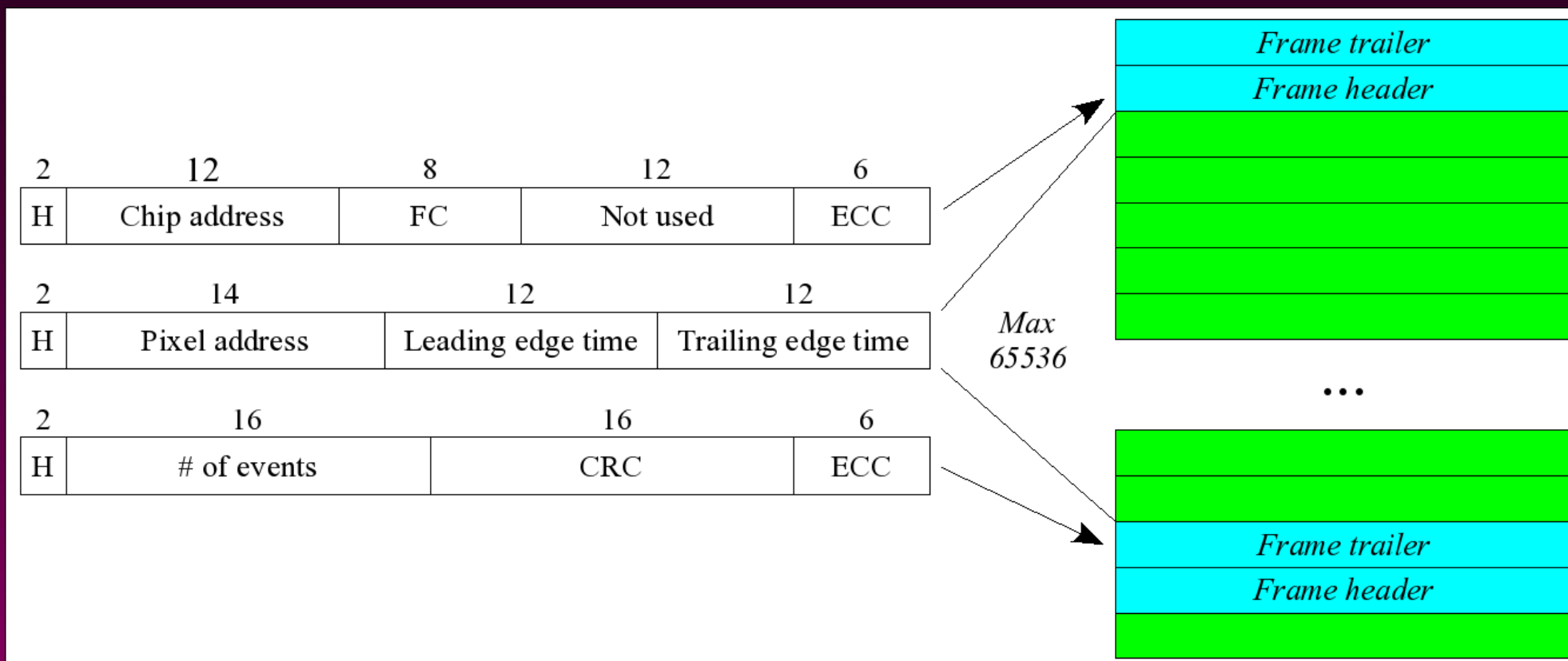




Data format



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