STT read-out

- Detectors requirements and layout
- Read-out concept
- Developments of Analog FEE and Digital Boards
- Tests (next presentation)

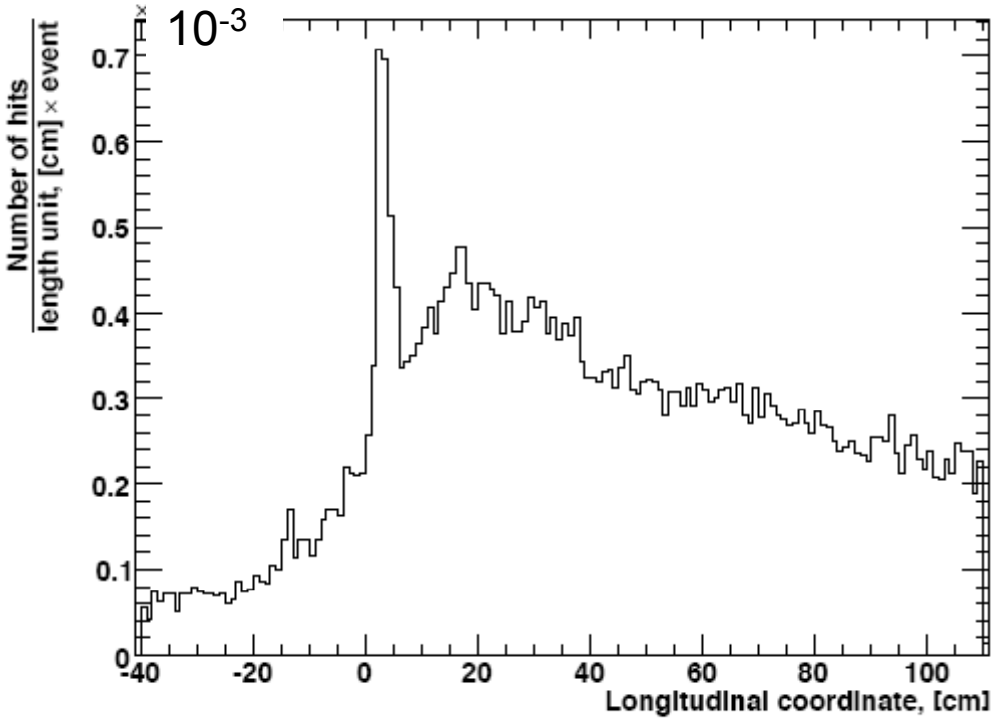
PANDA STT

- Central tracker : 4636 straws
- Forward tracker : ~13500 straws
- Drift time ~ 200 ns
- **Time measurement**: req. electronic resolution < 1 ns
- sensitivity (threshold) ~ 2 fC
- **dE/dx, Q for PID :** MIP: $5*10^6$ e^- , signal charge $10^{6-}10^8$ e^-
  PID (Central tracker): 10% resolution in 24 layers
- detector capacitance: ~ 10-15 pF (9 pF/m)
- Hit rates up to 800 kHz/channel

Expected rates

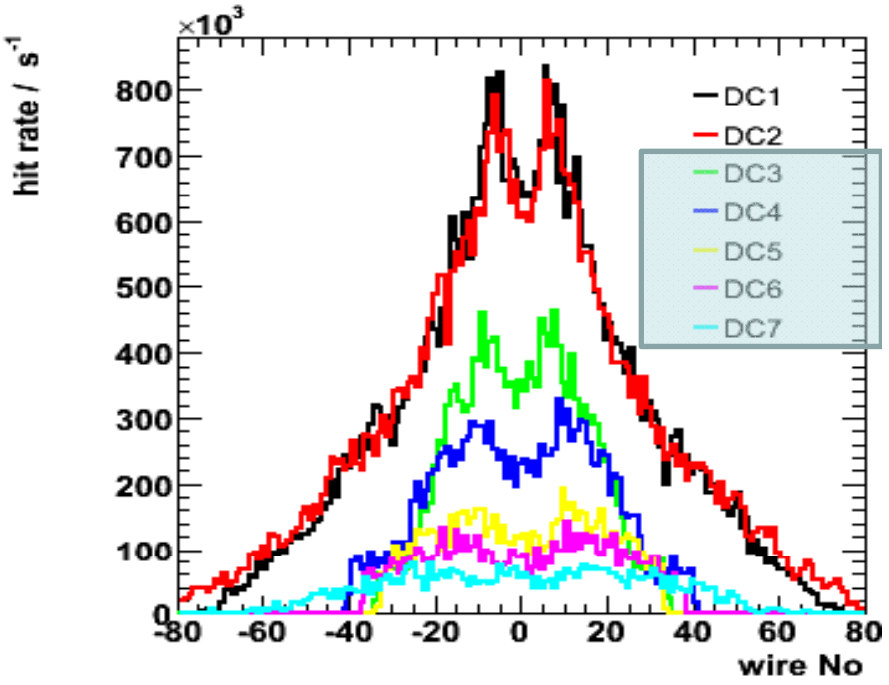
p_{beam} = 15 GeV/c, N_{Int}=2x10^{7} s^{-1}

Hit rate/cm/event in Central STS



Max rate: ~ 5kHz/cm -> ~800 kHz
for 150cm long tube

Hit rate per wire in Forward STS



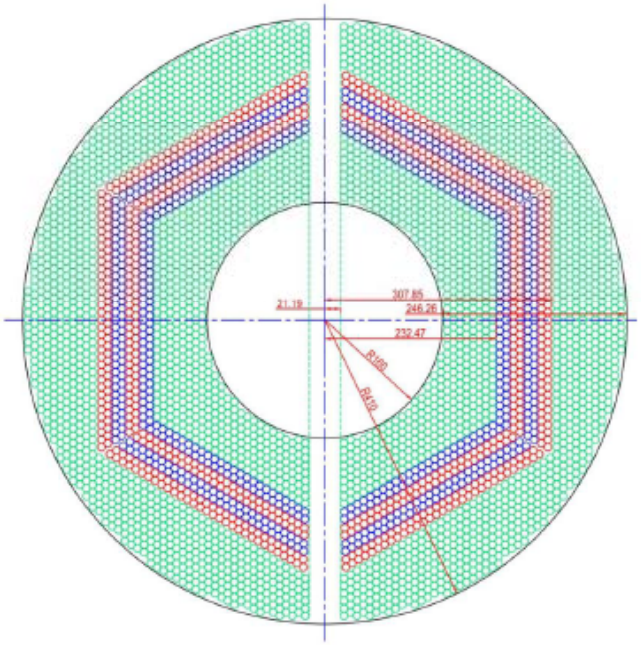
Max rate: ~400 kHz for STS3

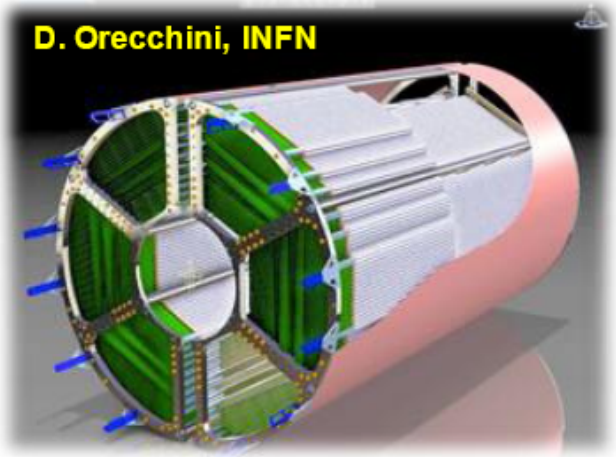
Central Tracker

STT Layout

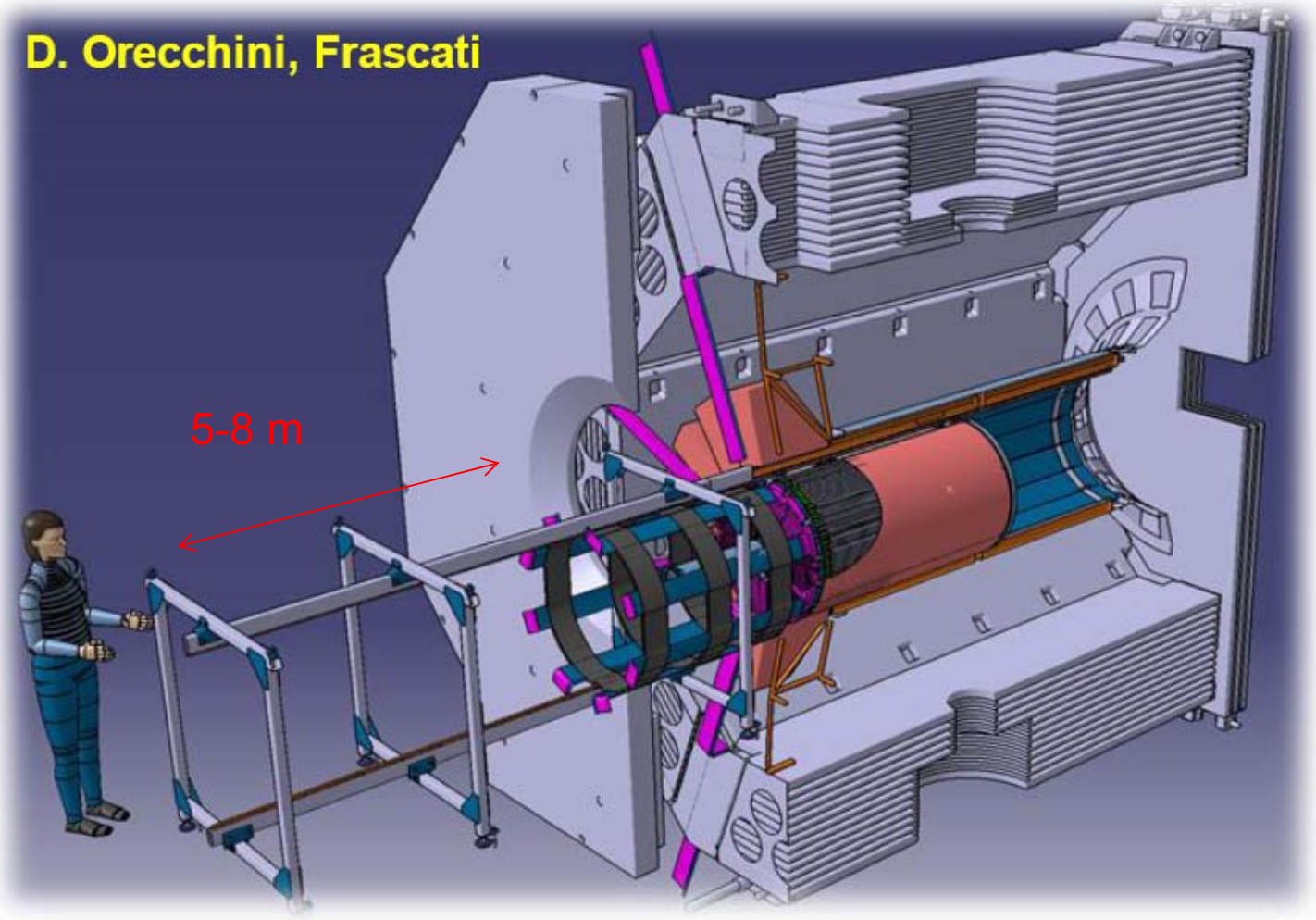
- 4636 Straw tubes in 2 semi-barrels
- 23-27 planar layers in 6 hexagonal sectors
  - 15-19 axial layers (green)
  - 4 stereo double-layers for 3D reconstr., with ±2.89° skew angle (blue / red)
- Time readout (isochrone radius)
- Amplitude readout (energy loss)
- $\sigma_{r\Phi} \sim 150\ \mu m$, $\sigma_z \sim 3.0$ mm (single hit)
- $\sigma_E / E < 10\%$ for π/K identification
- $\sigma_p / p \sim 1 - 2\%$ at B=2 Tesla
- $X/X_0 \sim 1.2\%$ ($^2/_3$ tube wall + $^1/_3$ gas)

- R_{in}/R_{out}: 150 / 418 mm
- Length: 1500mm + 150mm (RO upstream)

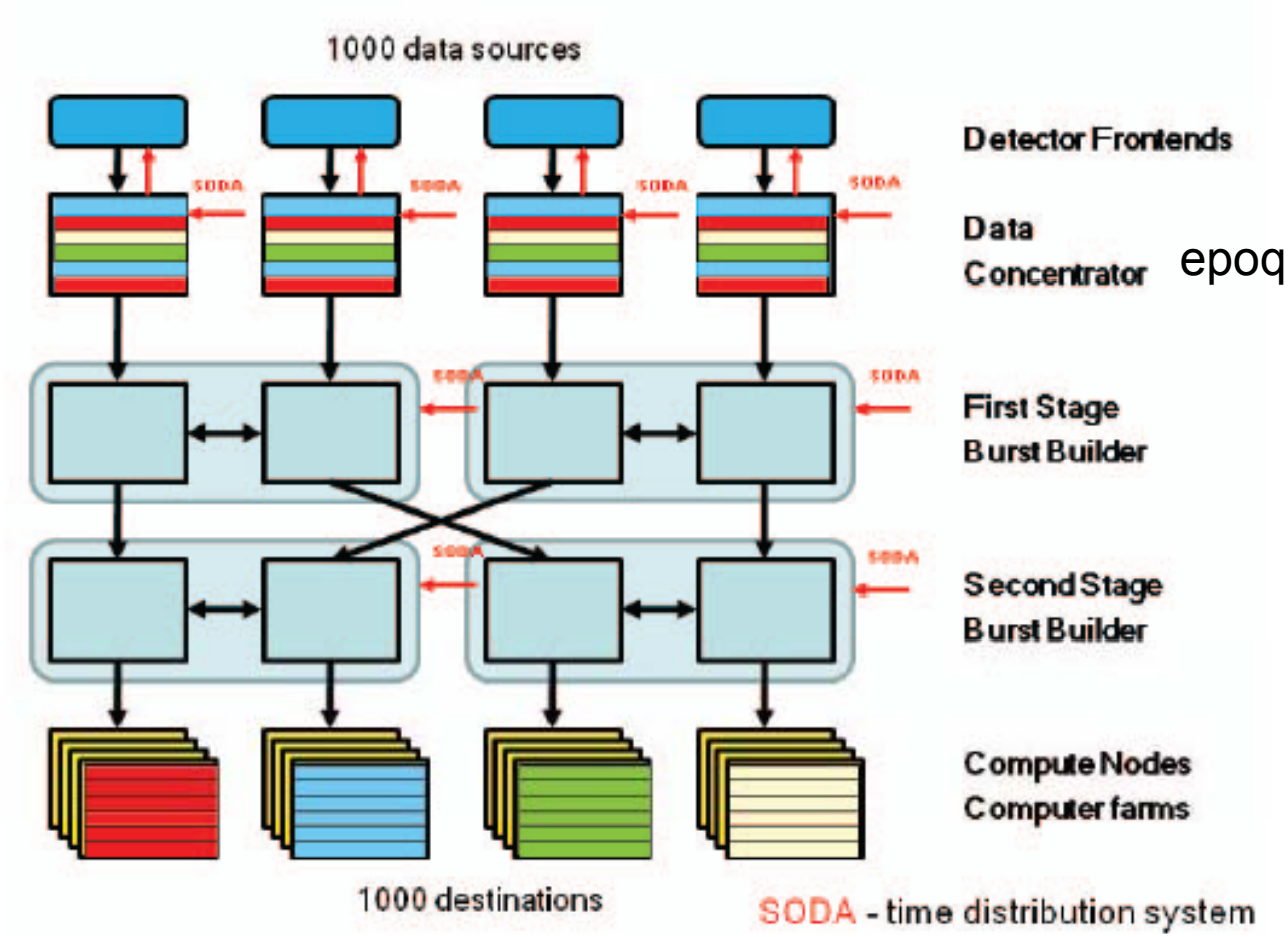




Final Assembly Scheme



PANDA DAQ



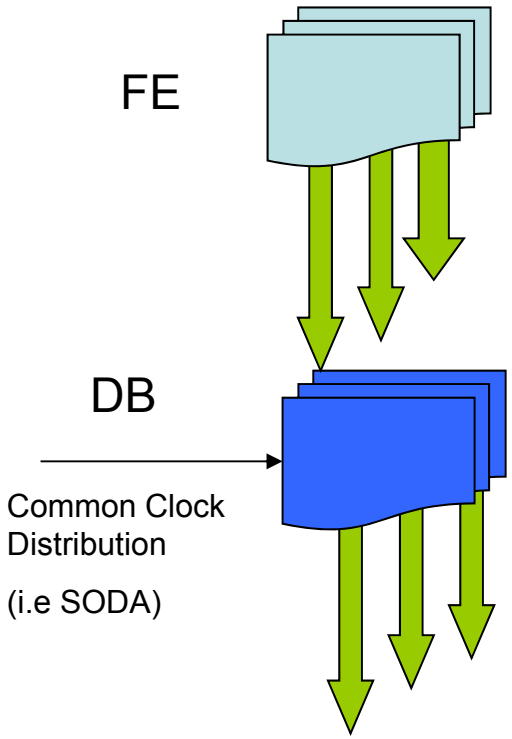
epoques (i.e 500μs)

Read-out concepts

- Complete read-out on detector
- avaliable space ΔL <15 cm A<4000 cm^2
- rad. hardness (FPGA's in digital part ?!)
- cooling system needed

- Compact analog part on detector (ASIC)
  (available space ~40 cm^2 for 16 channels)
- digital part (TDC/ADC) 5-8 m away outside detector
- nGbit/s links to Panda network

Straw tubes read-out chain



Panda DAQ - network

FE cards : Preamp+ Shaper+ BLR + Discriminator

- Dynamic Range ~ 5fC - 1pC, noise <1 fC
- Peaking time ~10-15 ns,
- Signal duration < 100 ns (pile-up < 10% @ 800 kHz)
- Gain 10-15 mV/fC

Digital Boards

- Multihit TDC : Time measurement + TimeOverThreshold (TOT)

for charge measurement OR/AND signal after shaper as input to FADC

- binning 0.5-0.8 ns
- Zero suppression & Hit detection.. Slow /Run/Data flow control

Data Concentration :

- gathering and sorting of hits marked by time stamps in epoques (i.e 500 μs bunch)
- nGbit/s Optical serial link

Developments

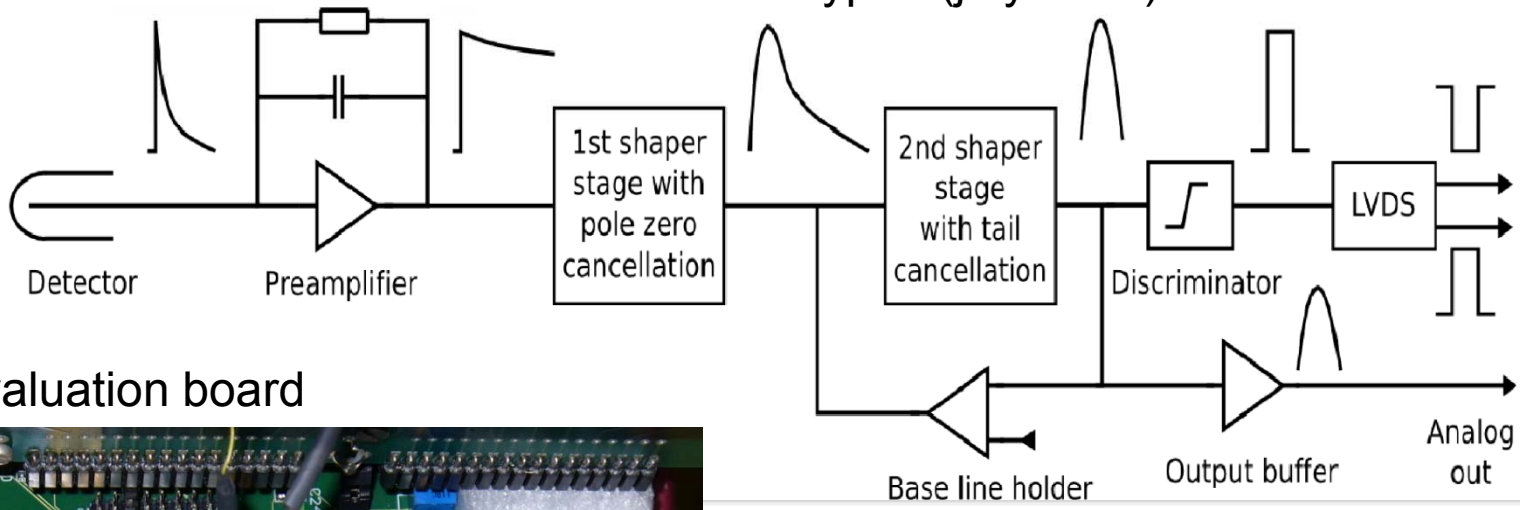
- Concept based on TDC +(ADC?)-Kraków (AGH, JU/GSI)
- New dedicated analog ASIC (preamp+shaper+discriminator) Dominik Przyborowski/Marek Idzik (AGH)
- TRBv2: TDC : HPTDC (CERN) TRBv2 – existing: can be used for detector tests with trigger rates up to 50 kHz
- TRBv3: TDC in in FPGA (new)- TRB v3 – designed to fit also Panda spec. (M.Traxler/J.Michel/M.Pałka/M.Kajetanowicz/G. Korcyl)
- TOT: amplitude measurement via width of signal above threshold (TDC)

or

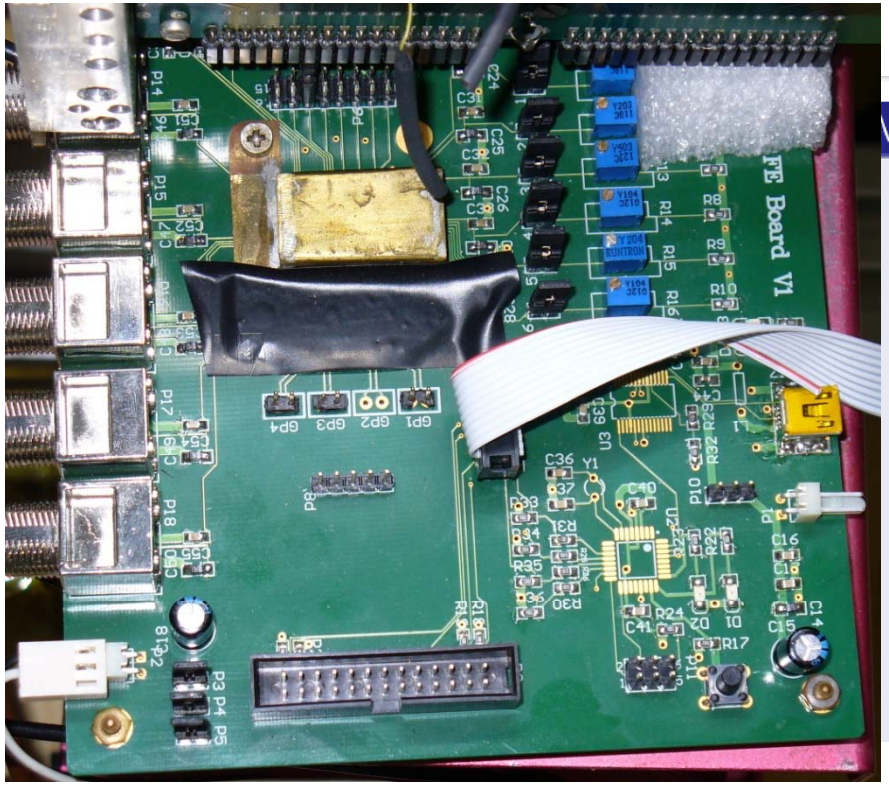
- ADC: charge measurement in FADC (~100 MHz) – as Addon card on TRBv3 –discussion is on-going

New ASIC for Panda STS

Prototype I (july 2011) : in tests



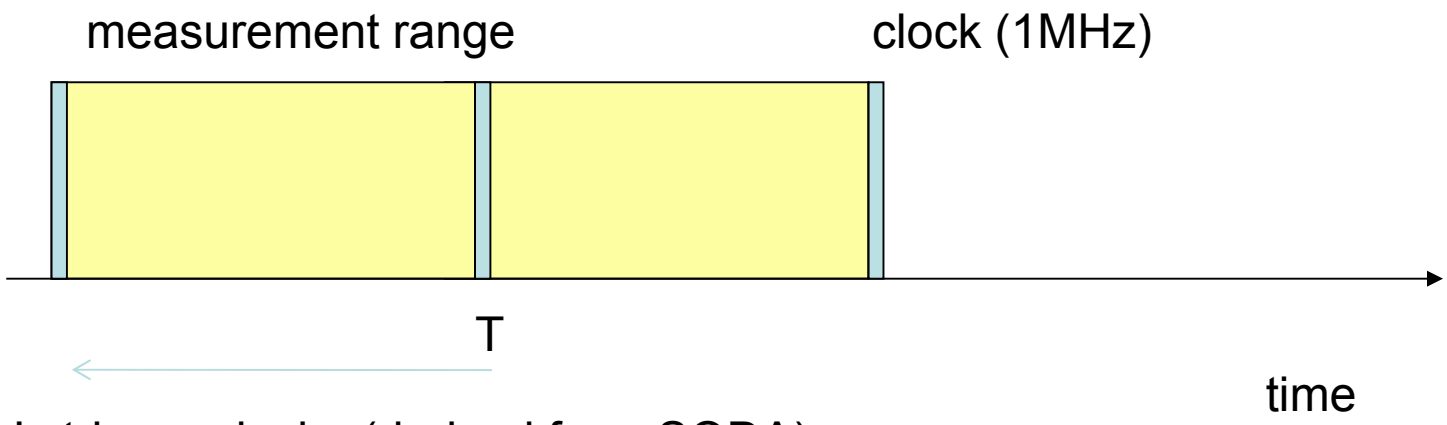
Evaluation board



More detailed specification

Parameter	Range/Value
Charge gain [mV/fC]	3 – 20
Peaking time (for delta) [ns]	15–40
Power consumption [mW]	$\approx$ 16
ENC [fC]	$<$ 0.4
1^{st} TC time constant [ns]	20 – 500
2^{nd} TC time constant [ns]	3 – 40
Input transistor parameters	
Dimensions W/L	$2000\mu/0.35\mu$
Transconductance [mS]	$\approx$ 26
Drain current [mA]	2

TDC operation mode & data volume



- 1 MHz trigger clock (derived from SODA)
- •: TDC with 0.5 ns binning: time 1 μs range: 11 bits

  TOT 200 ns : 8 bits

  channel number(1-32): 5bits

  time stamp (i.e 1-500); 8 bits

  TDC id, +trailer/header ~ 5 bytes/hit
- Data volume: 32 channels TDC @ max 800 kHz hit rate/channel -> ~128 MB/s
- Data buffer : 32 channels TDC (i.e for 500 μs epoque): 64-80 kB

step I (done): Trigger and Read-out Board

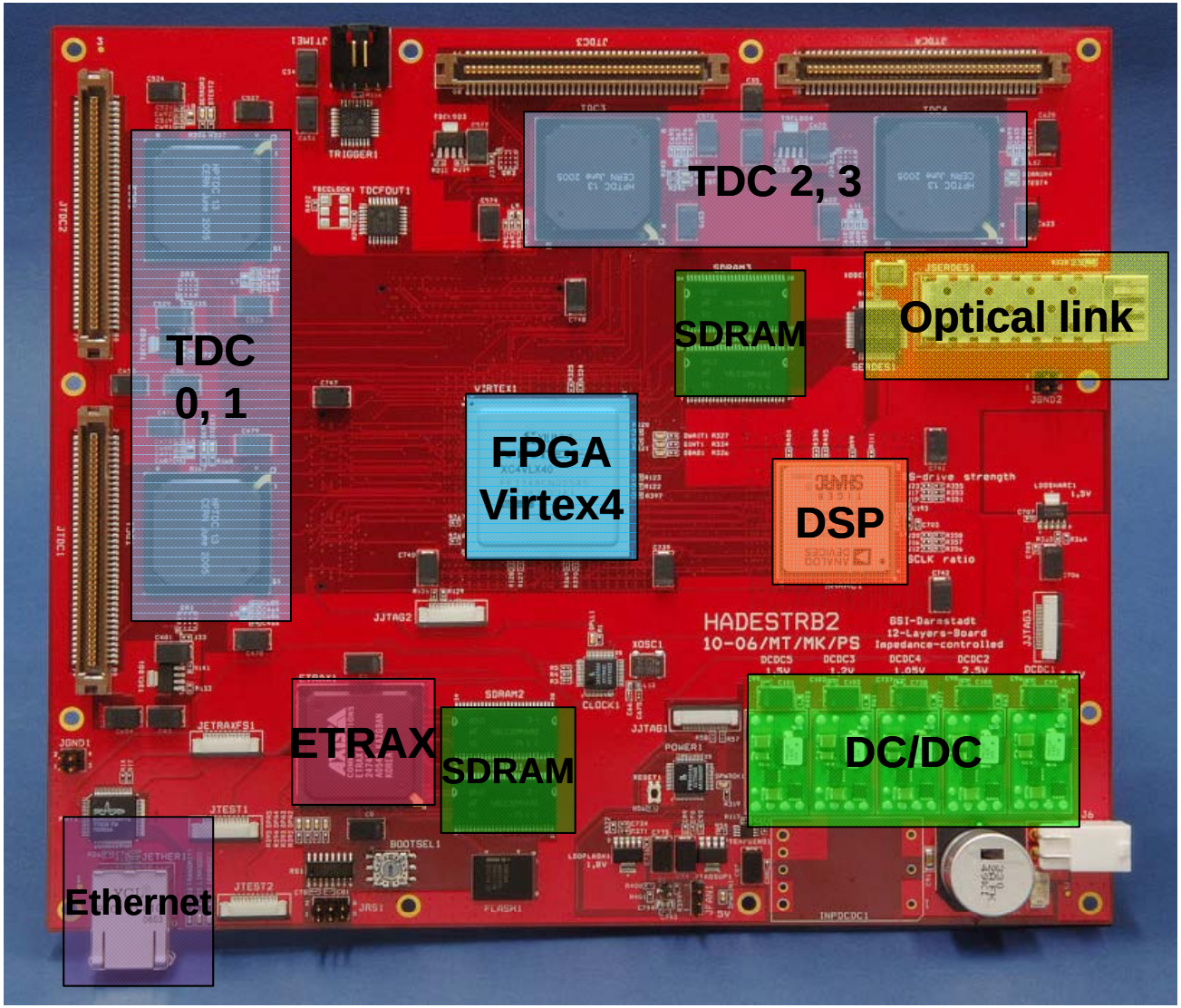
- TRBv2 board developed by HADES DAQ group
- many boards TRB v2 installed and used in the HADES DAQ

✓128 TDC channels (HPTDC)

✓130 MB/s data throughput achieved via optical links with TRBnet (8/10B in 2 Gbit/s)

✓TRBnet protocol (FPGA): 3 logical channels; data transport, slow control, run control

TRBv2



- 128 TDC channels (100ps, 192ps, 780 ps)
- 2.5 Gb/s serial 8/10b link

FPGA: TDC control + TrbNet
- Data flow control
- Slow control
- Run control

more powerfull: TRBv3

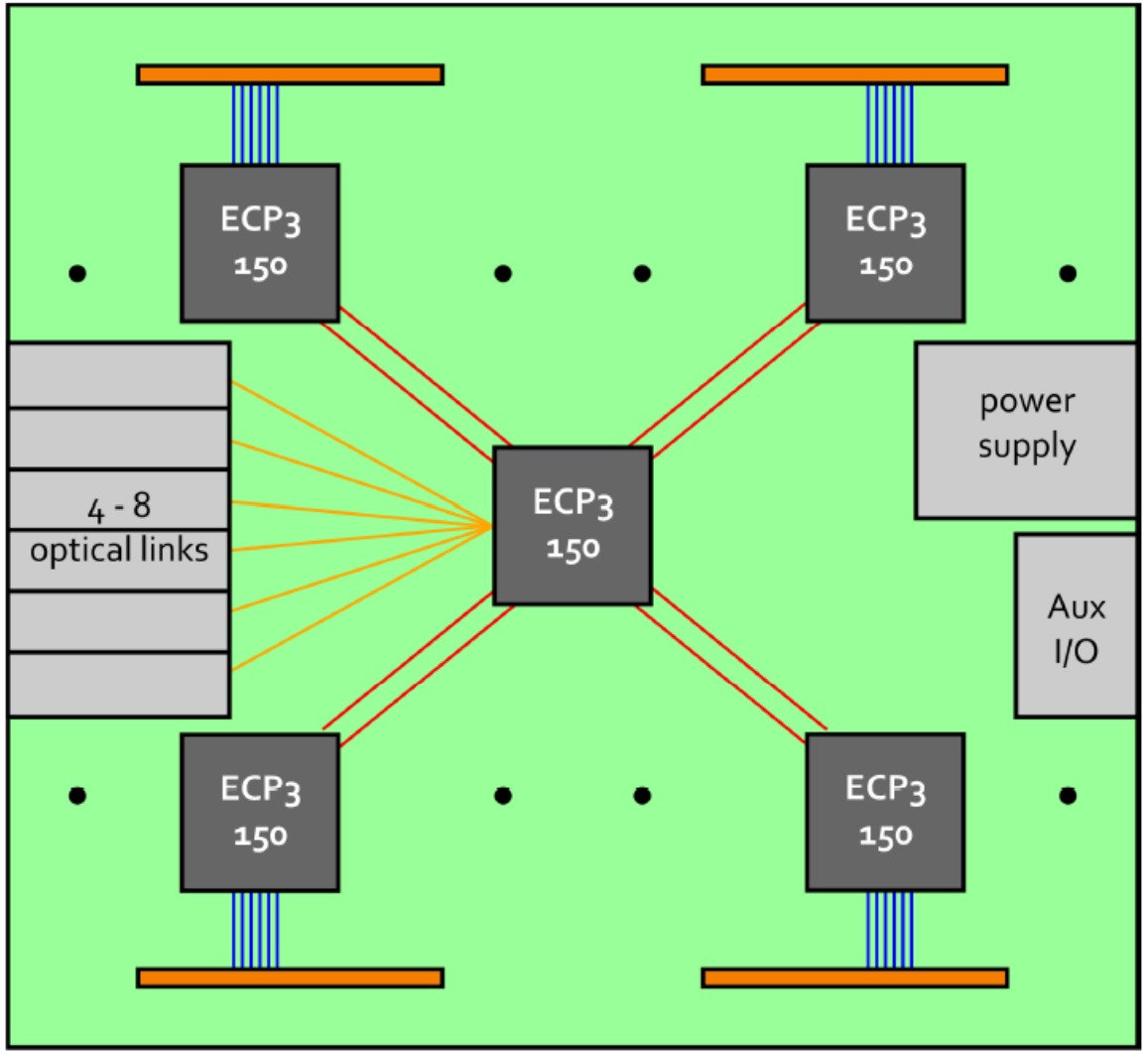
- 4 TDC in FPGA (Lattice ECP3M) up to 256 TDC channels
  4Mbit memory (enough to store one 0.5 ms bunch)

- 1 FPGA for control (Run, Data, Slow-control)

- up to 8 x 3.2Gbit/s (8/10b) serial links for data transmission
(enough to send data from 256 channels with 0.8 MHz hit rate)

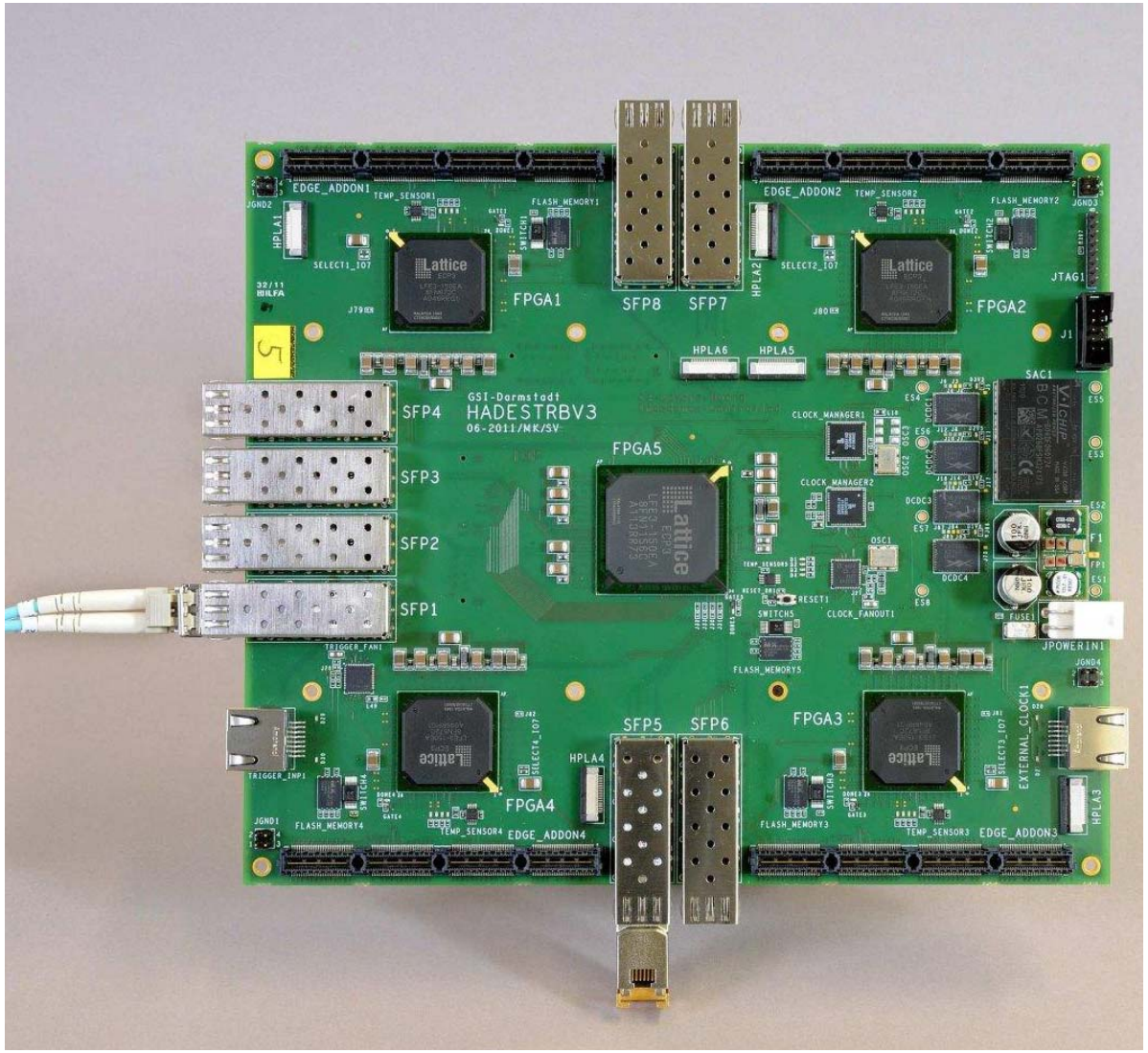
- interface for Add-on connectors : i.e ADC

- ~ 20 W power



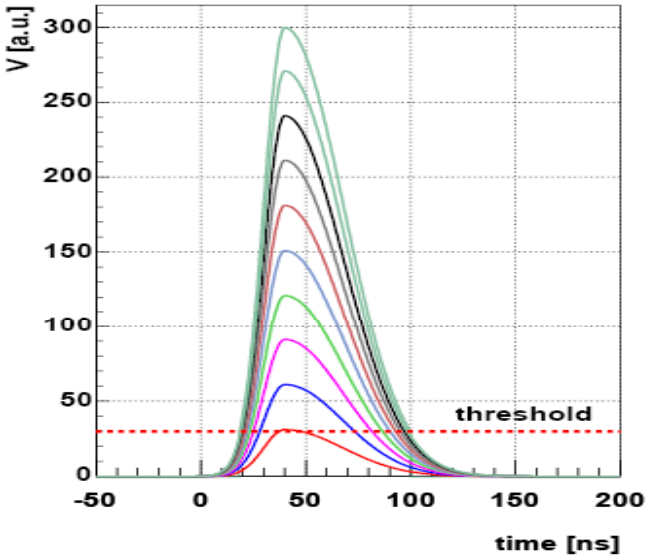
Status TRB v3

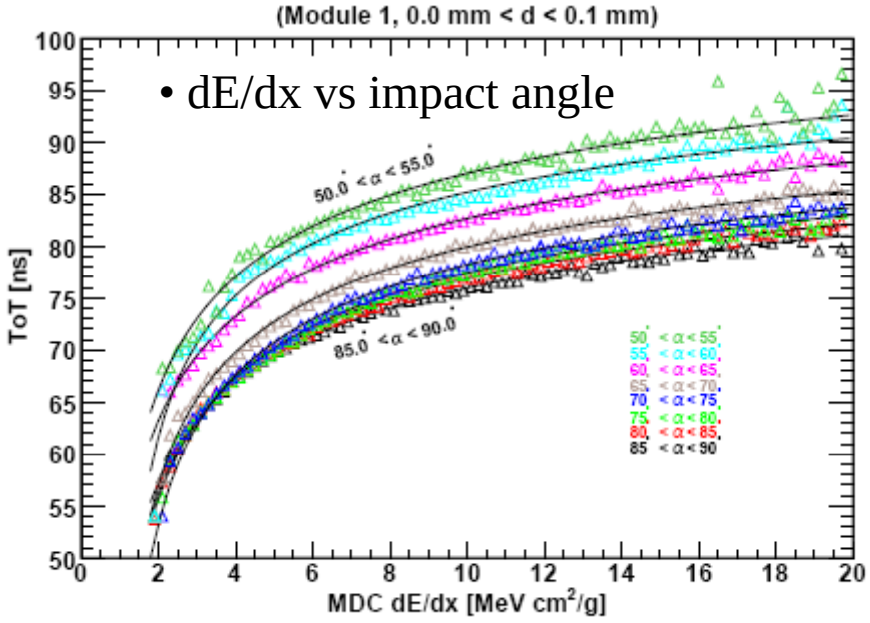
- Board produced and has all basic functionality (FPGA programming etc.)
- GbEth alreay implemented and connection to Compute Node established (G.Korcyl)
- TDC firmware is ongoing (GSI/M.Pałka (UJ))
- TRBnet in progress (J.Michel/U.Frankfurt)



back-up slides

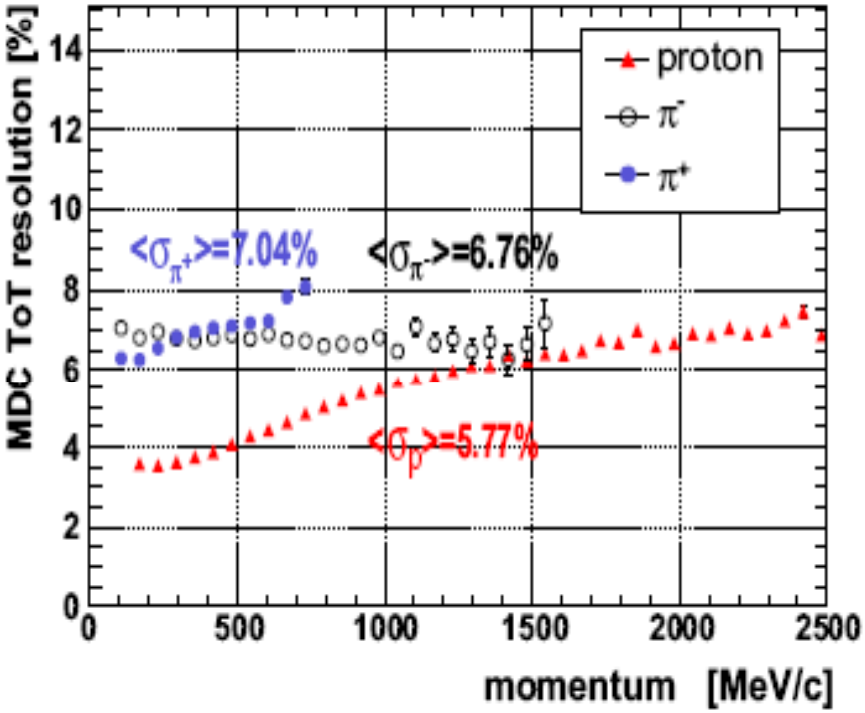
TOT– energy loss : HADES MDC





measured:

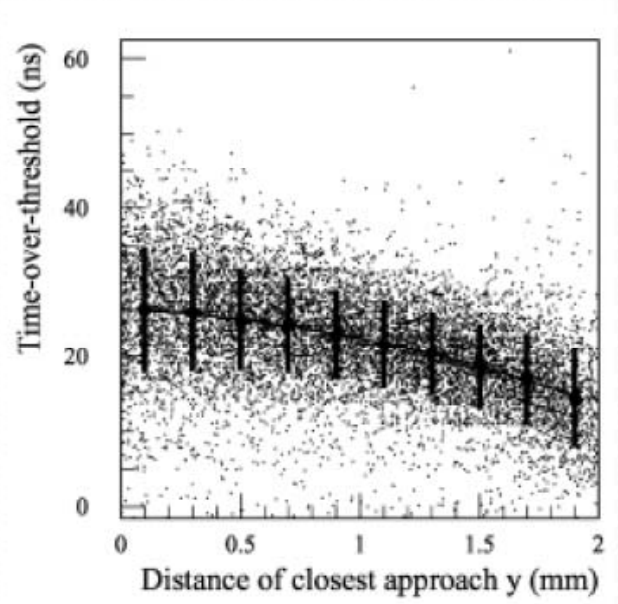
(J. Markert/ A.Schmah –U. Frankfurt)

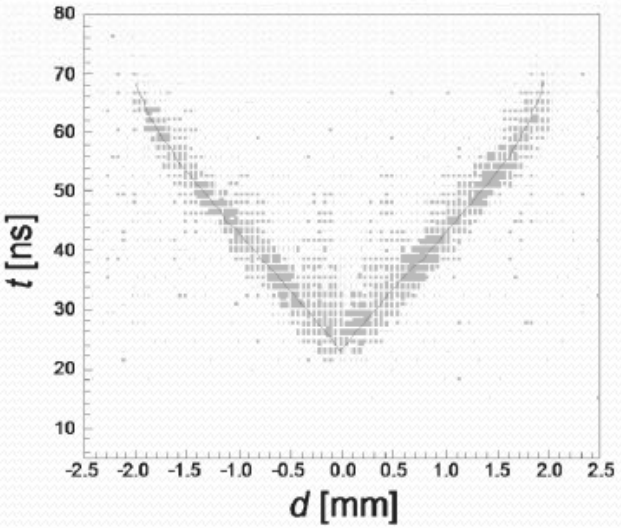


24 * ~7 mm gaps He:Iso (2:1)
FEE based on ASD8 chip

ToT correction – single straw

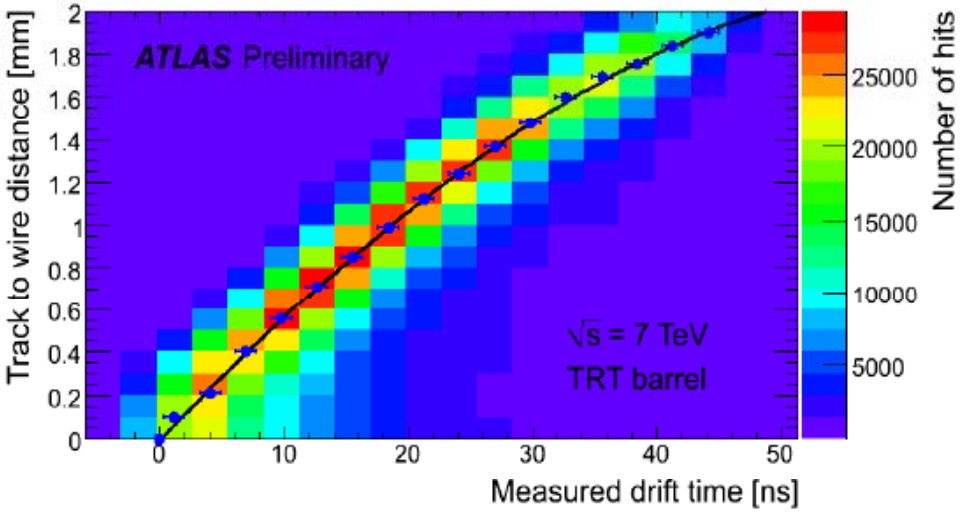
- Parameterization done for 5 GeV pions
  - Straw divided into 200 um bins
  - Polynomial fit
  - $\Delta_{ToT}=ToT_{meas.}(y)-ToT_{fit}(y)$
  - This residual dose not depend on the distance form wire
- Distance extracted from R(t) dependence





Results with 7TeV beam

- R(t) relation for TRT barrel



- Particle identification