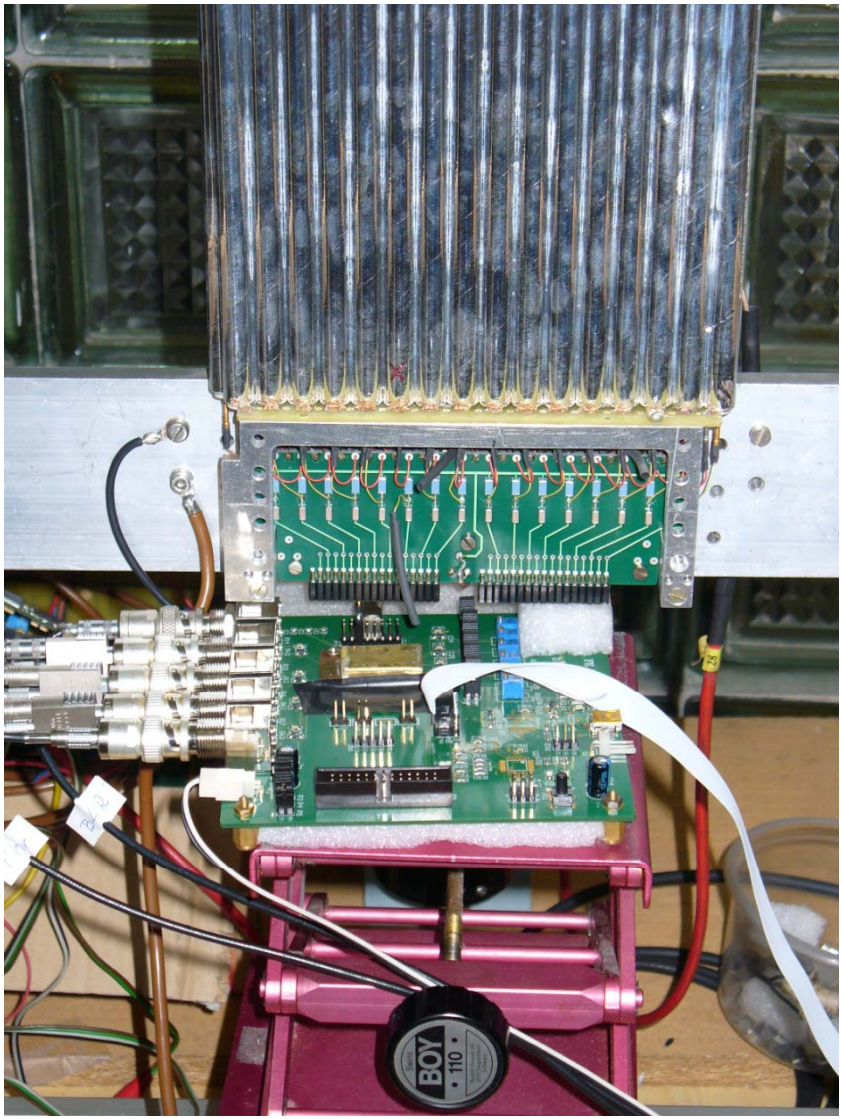
FEE test' october 2011

ASIC settings for test with pulser (voltage step on 0.25pF input capacitor - „delta" current pulse):

- Threshold 1.28 V, base line 1.20 V
- Threshold corresponds to ~ 10 fC and is limited by the pick-up noise
- Tail cancellation Rt_1 = 31 kOhm; Rt_2=11kOhm Ct_1 = 6 pF; Ct2 1.2 pF

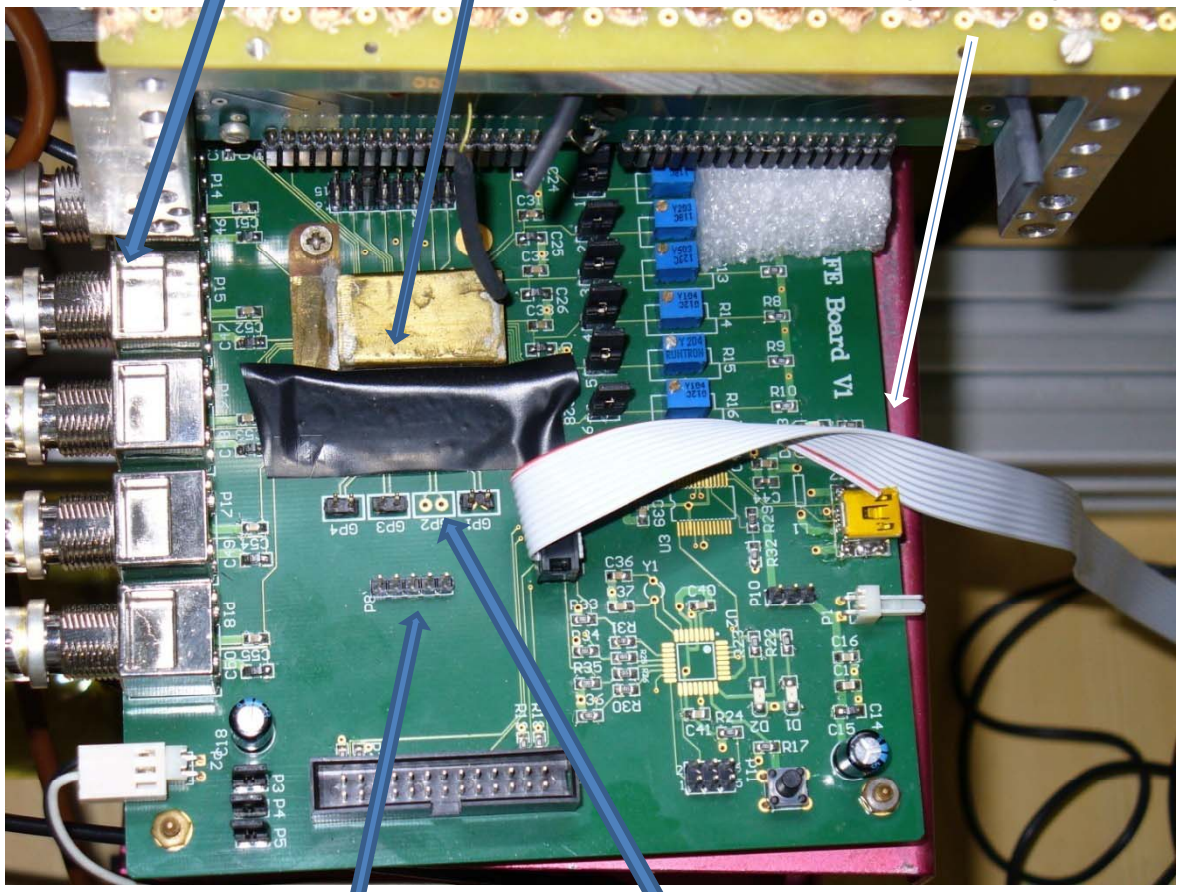
FEE-Straws connection



Connectors for base line & 4 threshold settings

ASIC

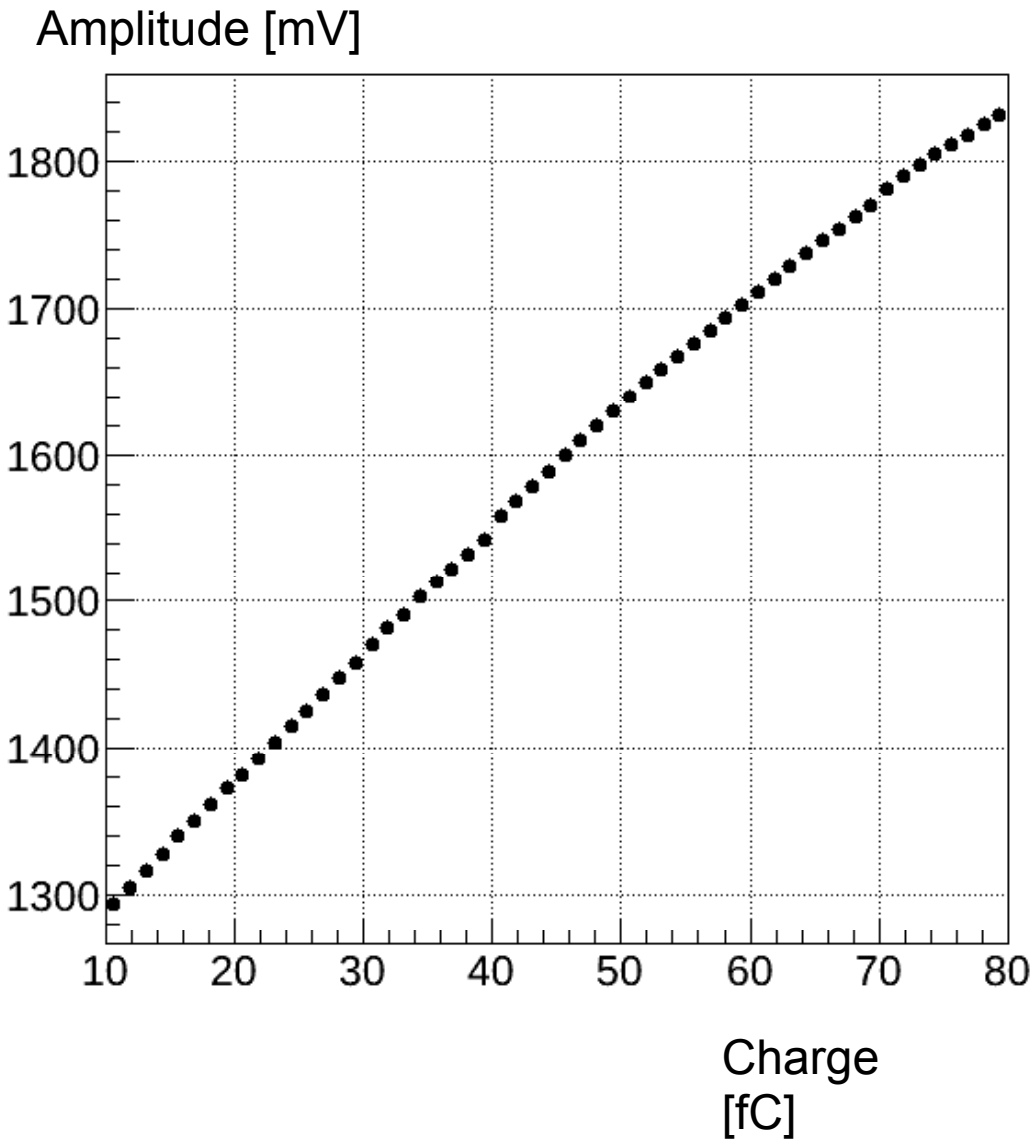
bus for ASIC programming



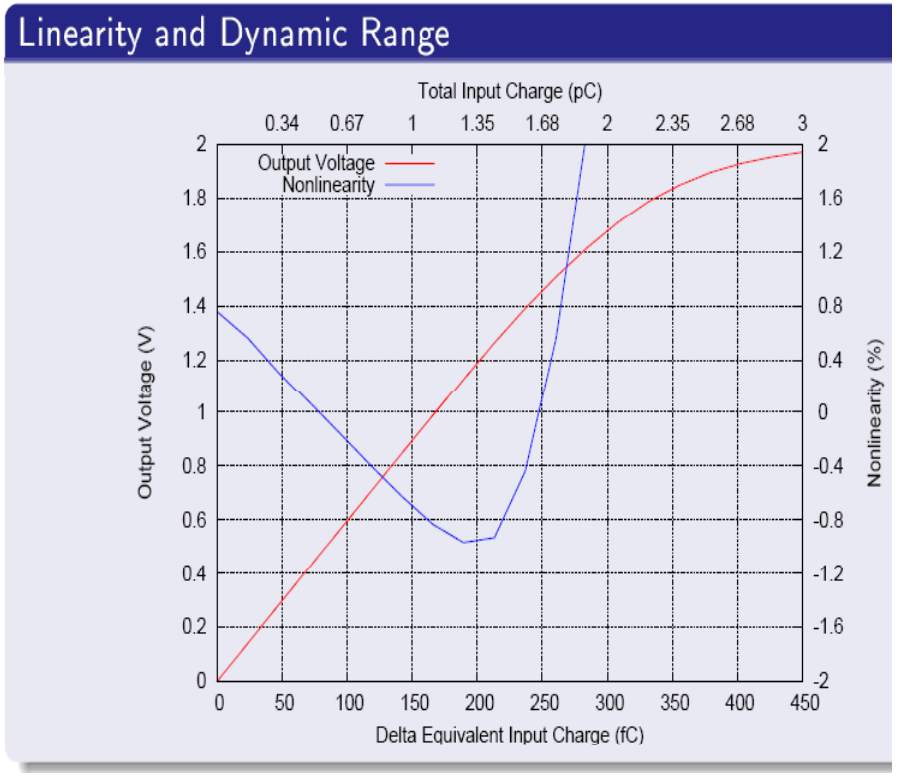
analog output

LVDS: (T, ΔT)

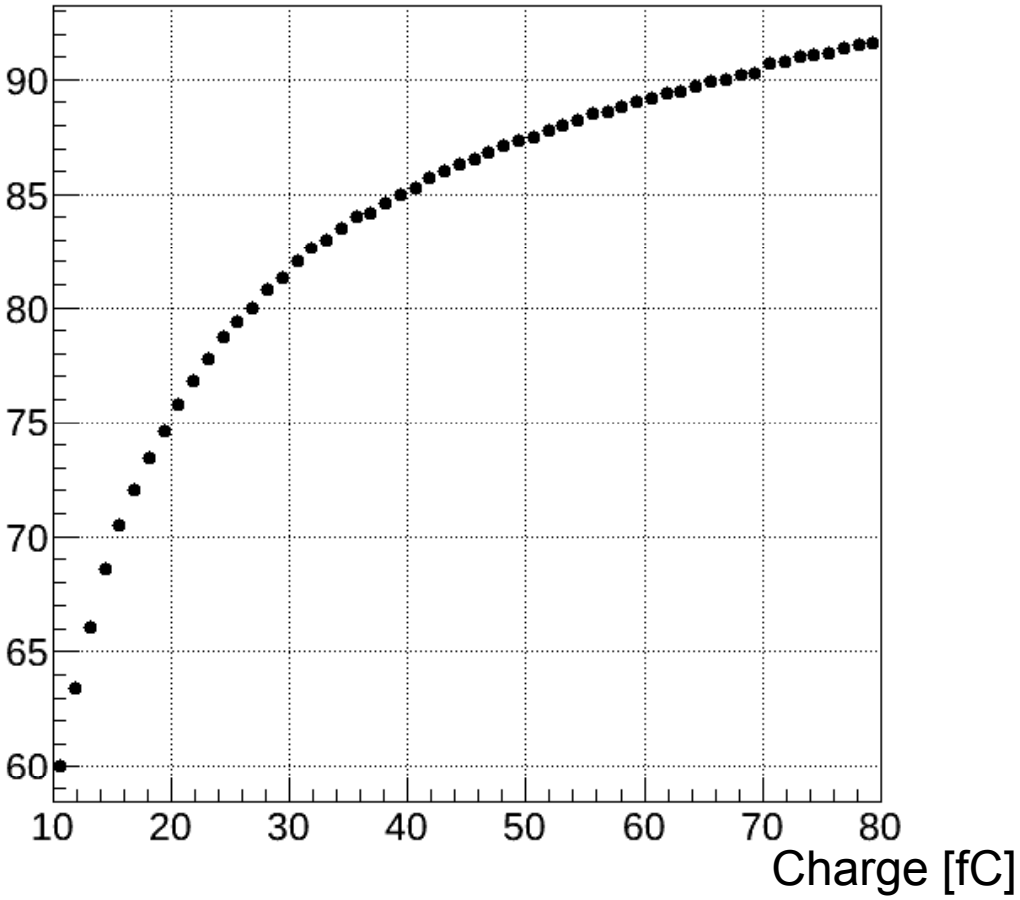
Amplitude vs charge with straw connected to input



Simulation: from STS TDR

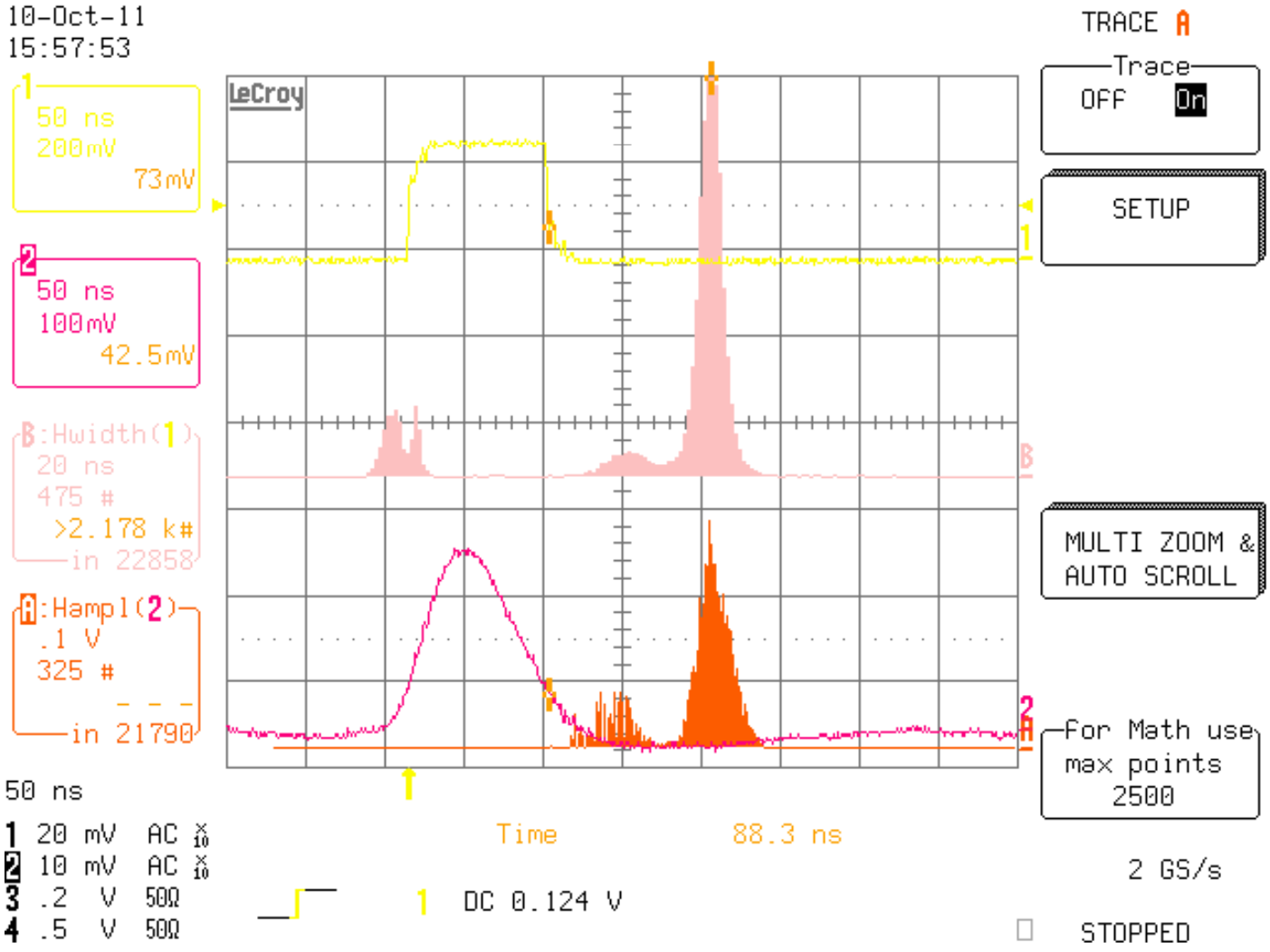


TOT vs charge with straw connected



10 fC is a minium charge we could measure (minium threshold above noise)

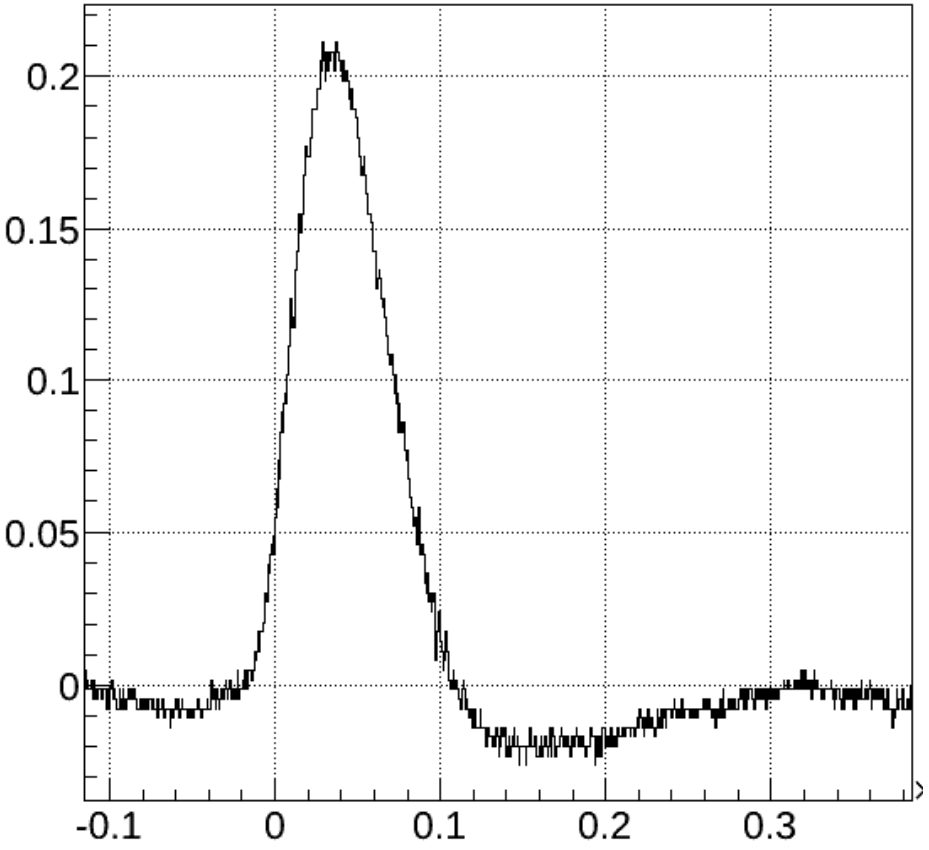
Amplitude and TOT histograms with iron ^{55}Fe source (2.9 and 5.8 keV)



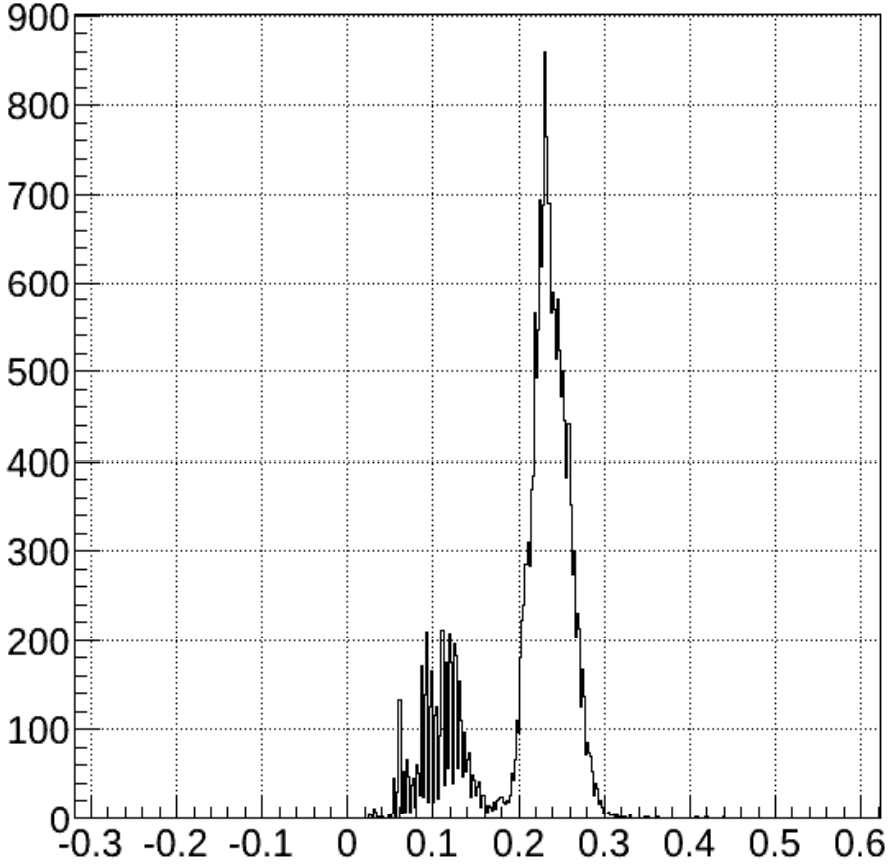
HV – straw 1650 V

histograms taken on digitial scope

Amplitude spectrum-scope

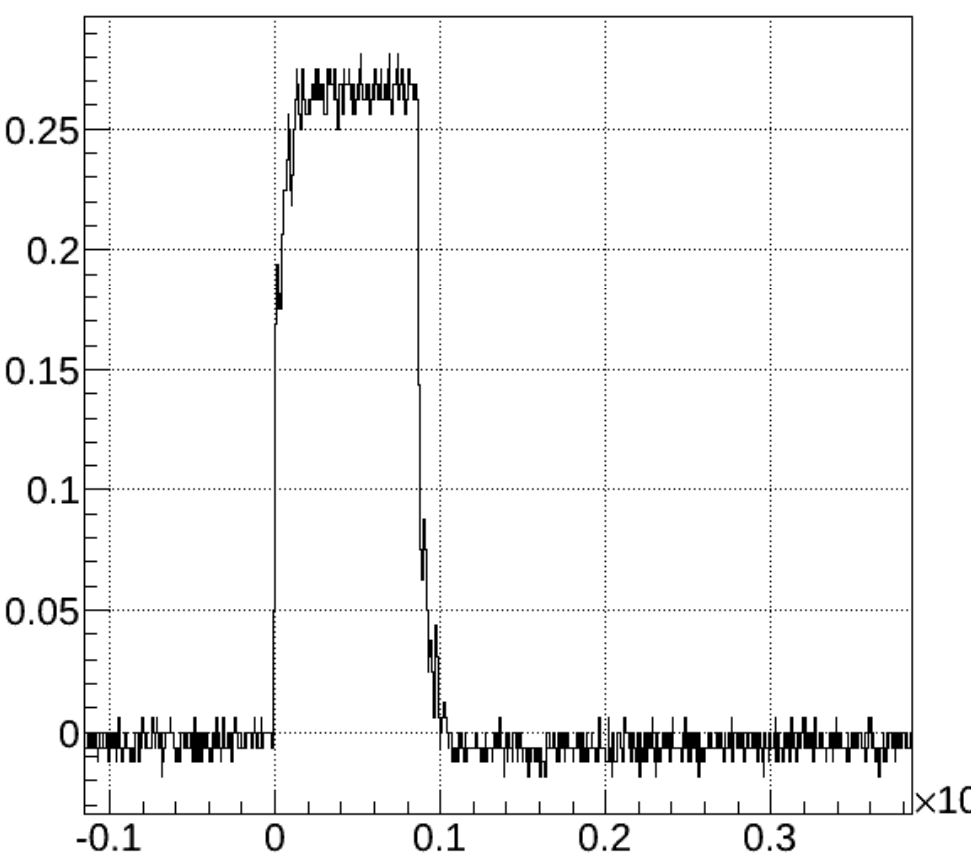


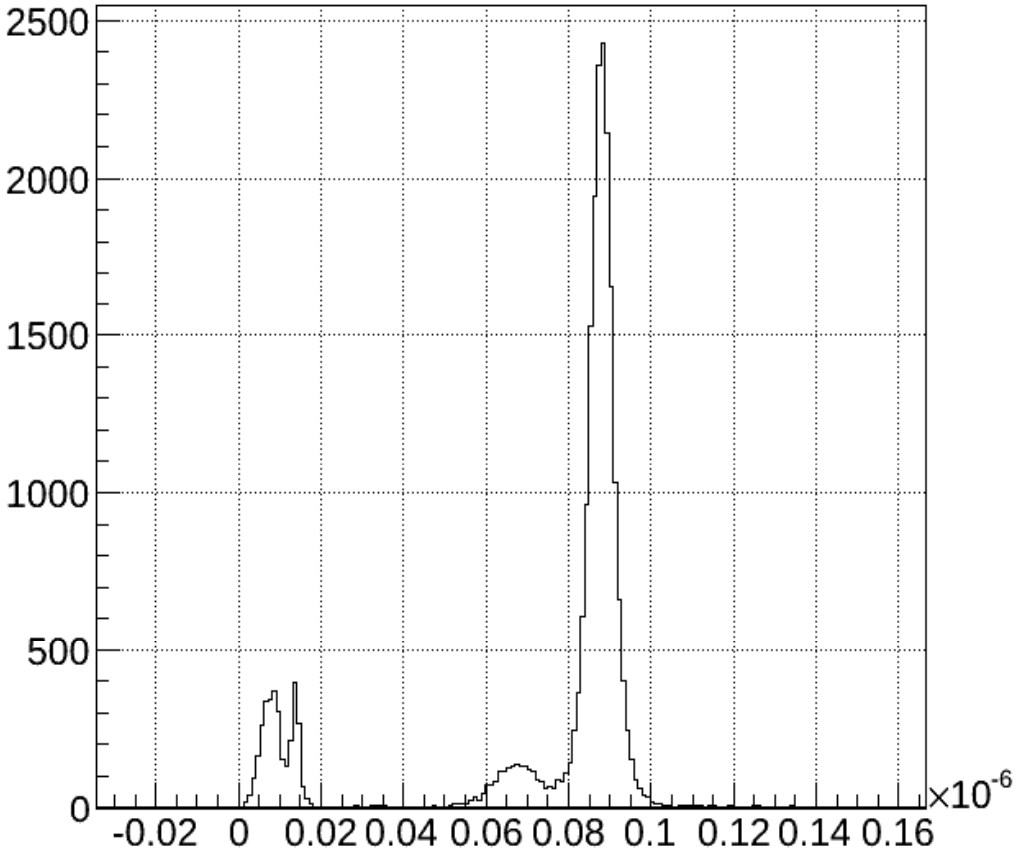
time [μs]



Amplitde [V]

TOT spectrum-scope



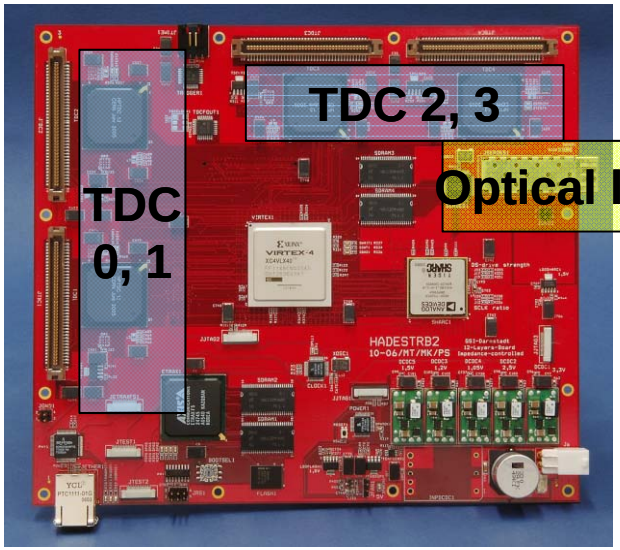


TOT [μs]

Full Read-out scheme for source tests

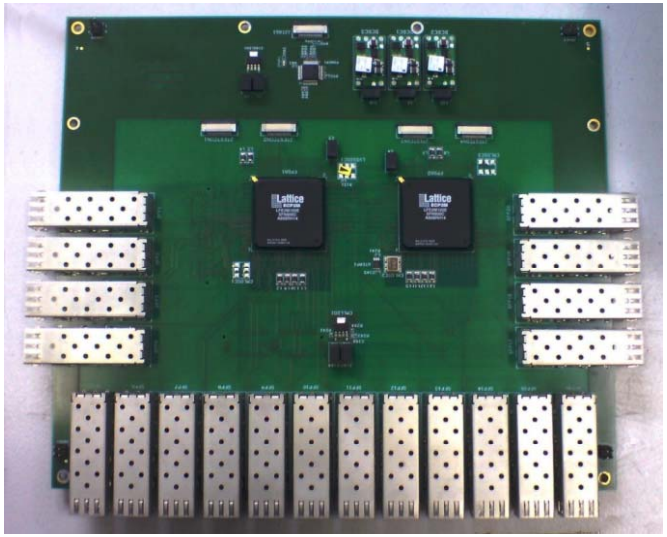
FEE-ASIC (channels)
4x LVDS output (T, TOT)

TRB



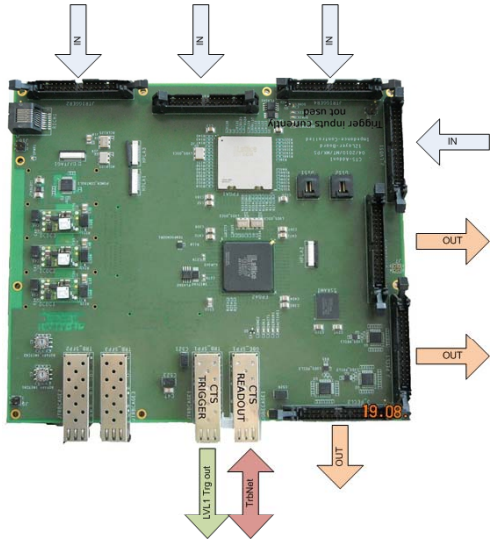
128 TDC channel
100 ps binning

HUB



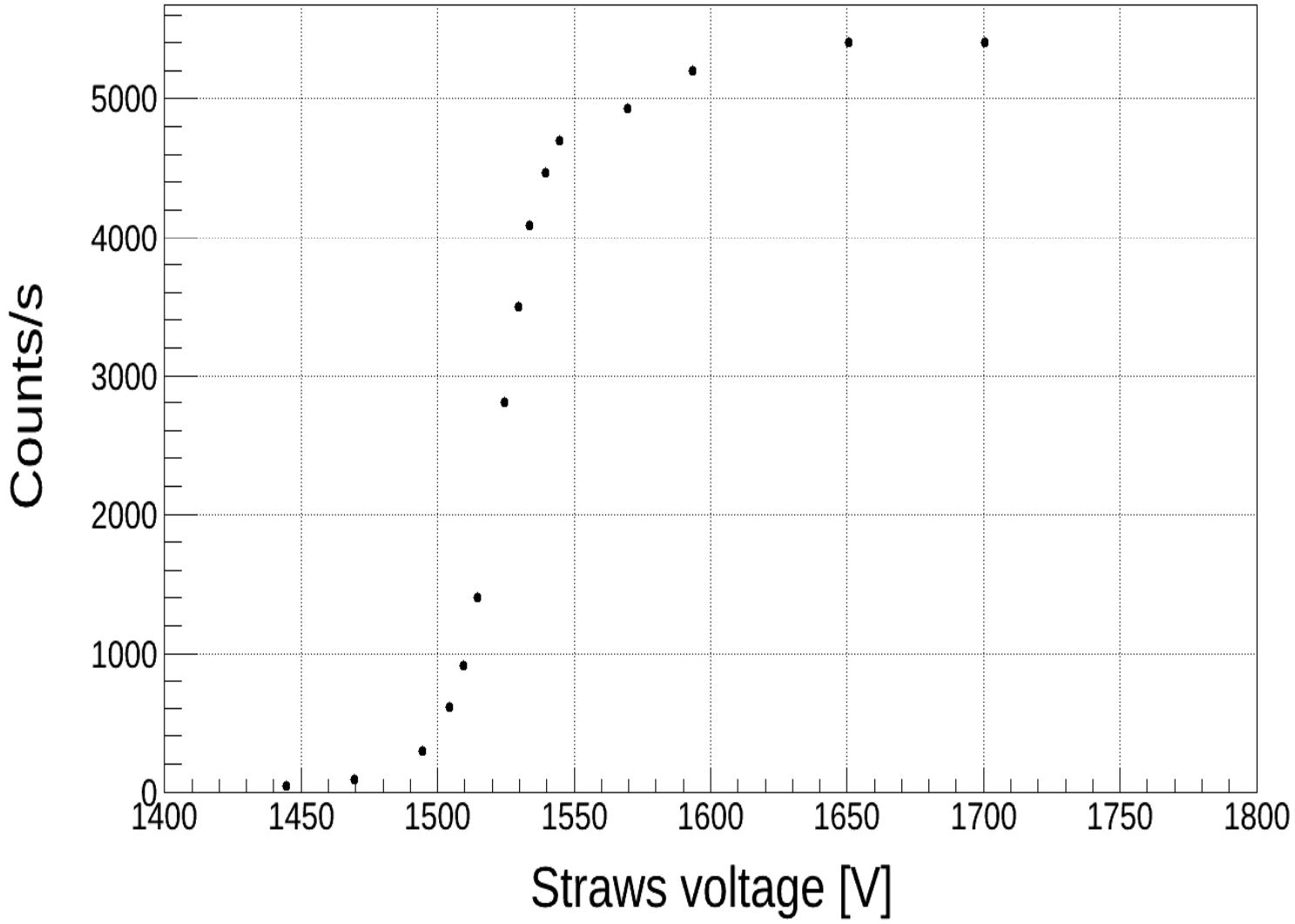
✓can connect up 16 TRB's
✓conversion to Gbit Ethernet
✓-event building on PC

Central Trigger



•free running clock
or
• reference trigger
from detector

Platou measurement with ^{55}Fe



Threshold ~10 fC

TOT : HV 1600-1750 in 50 V steps